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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	84MHz
Connectivity	I²C, IrDA, LINbus, SDIO, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	81
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f401vbt6

3.11 Clocks and startup

On reset the 16 MHz internal RC oscillator is selected as the default CPU clock. The 16 MHz internal RC oscillator is factory-trimmed to offer 1% accuracy at 25 °C. The application can then select as system clock either the RC oscillator or an external 4-26 MHz clock source. This clock can be monitored for failure. If a failure is detected, the system automatically switches back to the internal RC oscillator and a software interrupt is generated (if enabled). This clock source is input to a PLL thus allowing to increase the frequency up to 84 MHz. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example if an indirectly used external oscillator fails).

Several prescalers allow the configuration of the two AHB buses, the high-speed APB (APB2) and the low-speed APB (APB1) domains. The maximum frequency of the two AHB buses is 84 MHz while the maximum frequency of the high-speed APB domains is 84 MHz. The maximum allowed frequency of the low-speed APB domain is 42 MHz.

The devices embed a dedicated PLL (PLLI2S) which allows to achieve audio class performance. In this case, the I^2S master clock can generate all standard sampling frequencies from 8 kHz to 192 kHz.

3.12 Boot modes

At startup, boot pins are used to select one out of three boot options:

- Boot from user Flash
- Boot from system memory
- Boot from embedded SRAM

The bootloader is located in system memory. It is used to reprogram the Flash memory by using either USART1(PA9/10), USART2(PD5/6), USB OTG FS in device mode (PA11/12) through DFU (device firmware upgrade), I2C1(PB6/7), I2C2(PB10/3), I2C3(PA8/PB4), SPI1(PA4/5/6/7), SPI2(PB12/13/14/15) or SPI3(PA15, PC10/11/12).

For more detailed information on the bootloader, refer to Application Note: AN2606, *STM32™ microcontroller system memory boot mode*.

3.13 Power supply schemes

- V_{DD} = 1.7 to 3.6 V: external power supply for I/Os with the internal supervisor (POR/PDR) disabled, provided externally through V_{DD} pins. Requires the use of an external power supply supervisor connected to the VDD and PDR_ON pins.
- V_{DD} = 1.8 to 3.6 V: external power supply for I/Os and the internal regulator (when enabled), provided externally through V_{DD} pins.
- V_{SSA}, V_{DDA} = 1.7 to 3.6 V: external analog power supplies for ADC, Reset blocks, RCs and PLL. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively, with decoupling technique.
- V_{BAT} = 1.65 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

Refer to *Figure 18: Power supply scheme* for more details.

3.14 Power supply supervisor

3.14.1 Internal reset ON

This feature is available for V_{DD} operating voltage range 1.8 V to 3.6 V.

The internal power supply supervisor is enabled by holding PDR_ON high.

The devices have an integrated power-on reset (POR) / power-down reset (PDR) circuitry coupled with a Brownout reset (BOR) circuitry. At power-on, POR is always active, and ensures proper operation starting from 1.8 V. After the 1.8 V POR threshold level is reached, the option byte loading process starts, either to confirm or modify default thresholds, or to disable BOR permanently. Three BOR thresholds are available through option bytes.

The devices remain in reset mode when V_{DD} is below a specified threshold, $V_{POR/PDR}$ or V_{BOR}, without the need for an external reset circuit.

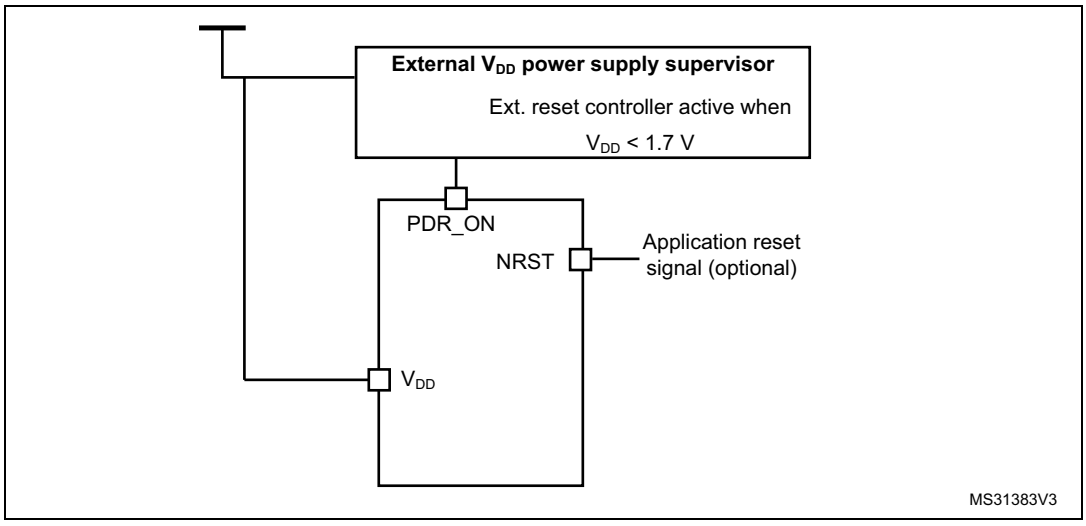
The devices also feature an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when V_{DD}/V_{DDA} drops below the V_{PVD} threshold and/or when V_{DD}/V_{DDA} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

3.14.2 Internal reset OFF

This feature is available only on packages featuring the PDR_ON pin. The internal power-on reset (POR) / power-down reset (PDR) circuitry is disabled by setting the PDR_ON pin to low.

An external power supply supervisor should monitor V_{DD} and should maintain the device in reset mode as long as V_{DD} is below a specified threshold. PDR_ON should be connected to this external power supply supervisor. Refer to *Figure 5: Power supply supervisor interconnection with internal reset OFF*.

Figure 5. Power supply supervisor interconnection with internal reset OFF(1)



1. The PRD_ON pin is only available on the WLCSP49 and UFBGA100 packages.

3.15.1 Regulator ON

On packages embedding the BYPASS_REG pin, the regulator is enabled by holding BYPASS_REG low. On all other packages, the regulator is always enabled.

There are three power modes configured by software when the regulator is ON:

- MR is used in the nominal regulation mode (With different voltage scaling in Run)

  In Main regulator mode (MR mode), different voltage scaling are provided to reach the best compromise between maximum frequency and dynamic power consumption.
- LPR is used in the Stop modes

  The LP regulator mode is configured by software when entering Stop mode.
- Power-down is used in Standby mode.

  The Power-down mode is activated only when entering in Standby mode. The regulator output is in high impedance and the kernel circuitry is powered down, inducing zero consumption. The contents of the registers and SRAM are lost.

Depending on the package, one or two external ceramic capacitors should be connected on the V_{CAP_1} and V_{CAP_2} pins. The V_{CAP_2} pin is only available for the LQFP100 and UFBGA100 packages.

All packages have the regulator ON feature.

3.15.2 Regulator OFF

The Regulator OFF is available only on the UFBGA100, which features the BYPASS_REG pin. The regulator is disabled by holding BYPASS_REG high. The regulator OFF mode allows to supply externally a V12 voltage source through V_{CAP_1} and V_{CAP_2} pins.

Since the internal voltage scaling is not managed internally, the external voltage value must be aligned with the targeted maximum frequency. Refer to *Table 14: General operating conditions*.

The two 2.2 µF V_{CAP} ceramic capacitors should be replaced by two 100 nF decoupling capacitors. Refer to *Figure 18: Power supply scheme*.

When the regulator is OFF, there is no more internal monitoring on V12. An external power supply supervisor should be used to monitor the V12 of the logic power domain. PA0 pin should be used for this purpose, and act as power-on reset on V12 power domain.

In regulator OFF mode, the following features are no more supported:

- PA0 cannot be used as a GPIO pin since it allows to reset a part of the V12 logic power domain which is not reset by the NRST pin.
- As long as PA0 is kept low, the debug mode cannot be used under power-on reset. As a consequence, PA0 and NRST pins must be managed separately if the debug connection under reset or pre-reset is required.

3.19.5 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard downcounter. It features:

- A 24-bit downcounter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source.

3.20 Inter-integrated circuit interface (I^2C)

Up to three I^2C bus interfaces can operate in multimaster and slave modes. They can support the standard (up to 100 kHz) and fast (up to 400 kHz) modes. The I2C bus frequency can be increased up to 1 MHz. For more details about the complete solution, please contact your local ST sales representative.They also support the 7/10-bit addressing mode and the 7-bit dual addressing mode (as slave). A hardware CRC generation/verification is embedded.

They can be served by DMA and they support SMBus 2.0/PMBus.

The devices also include programmable analog and digital noise filters (see *Table 5*).

Table 5. Comparison of I2C analog and digital filters

	Analog filter	Digital filter
Pulse width of suppressed spikes	≥ 50 ns	Programmable length from 1 to 15 I2C peripheral clocks

3.21 Universal synchronous/asynchronous receiver transmitters (USART)

The devices embed three universal synchronous/asynchronous receiver transmitters (USART1, USART2 and USART6).

These three interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode and have LIN Master/Slave capability. The USART1 and USART6 interfaces are able to communicate at speeds of up to 10.5 Mbit/s. The USART2 interface communicates at up to 5.25 bit/s.

USART1 and USART2 also provide hardware management of the CTS and RTS signals, Smart Card mode (ISO 7816 compliant) and SPI-like communication capability. All interfaces can be served by the DMA controller.

3.25 Secure digital input/output interface (SDIO)

An SD/SDIO/MMC host interface is available, that supports MultiMediaCard System Specification Version 4.2 in three different databus modes: 1-bit (default), 4-bit and 8-bit.

The interface allows data transfer at up to 48 MHz, and is compliant with the SD Memory Card Specification Version 2.0.

The SDIO Card Specification Version 2.0 is also supported with two different databus modes: 1-bit (default) and 4-bit.

The current version supports only one SD/SDIO/MMC4.2 card at any one time and a stack of MMC4.1 or previous.

In addition to SD/SDIO/MMC, this interface is fully compliant with the CE-ATA digital protocol Rev1.1.

3.26 Universal serial bus on-the-go full-speed (OTG_FS)

The devices embed an USB OTG full-speed device/host/OTG peripheral with integrated transceivers. The USB OTG FS peripheral is compliant with the USB 2.0 specification and with the OTG 1.0 specification. It has software-configurable endpoint setting and supports suspend/resume. The USB OTG full-speed controller requires a dedicated 48 MHz clock that is generated by a PLL connected to the HSE oscillator. The major features are:

- Combined Rx and Tx FIFO size of 320 × 35 bits with dynamic FIFO sizing
- Supports the session request protocol (SRP) and host negotiation protocol (HNP)
- 4 bidirectional endpoints
- 8 host channels with periodic OUT support
- HNP/SNP/IP inside (no need for any external resistor)
- For OTG/Host modes, a power switch is needed in case bus-powered devices are connected

3.27 General-purpose input/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain, with or without pull-up or pull-down), as input (floating, with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high-current-capable and have speed selection to better manage internal noise, power consumption and electromagnetic emission.

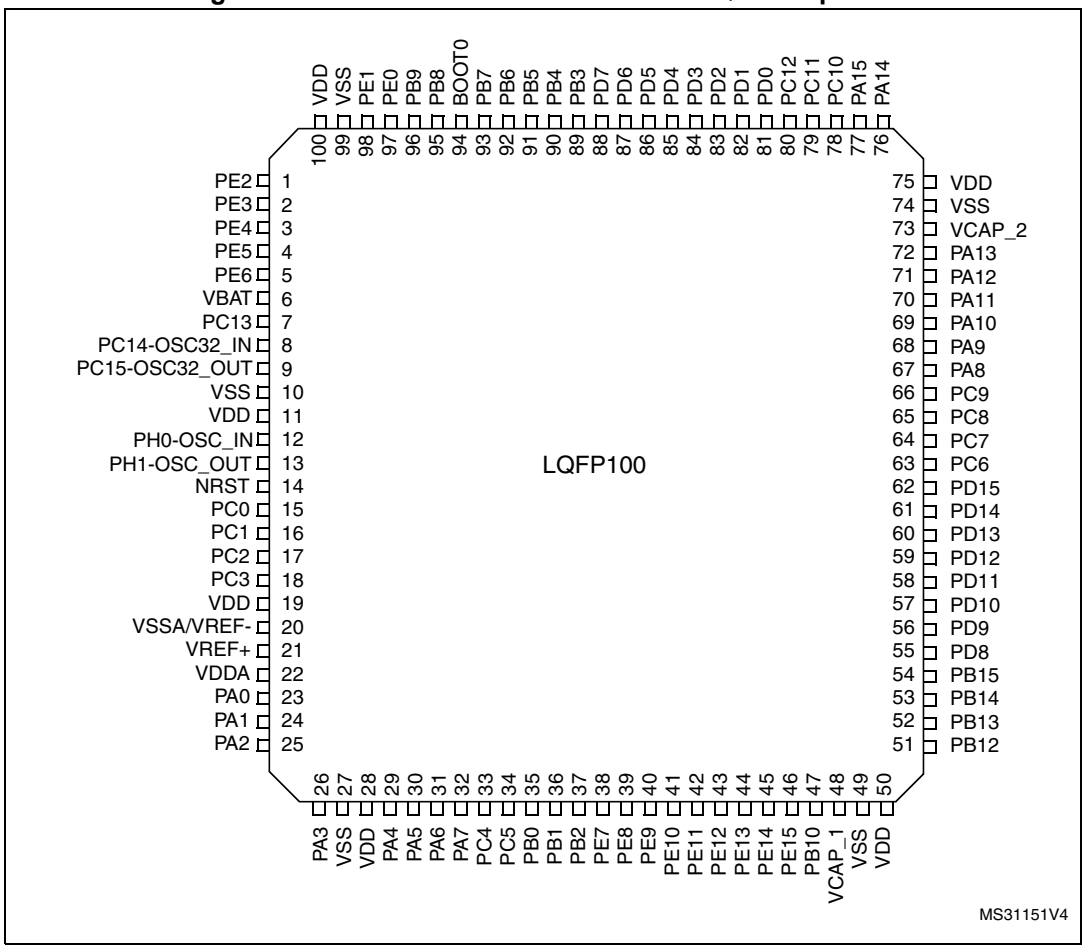
The I/O configuration can be locked if needed by following a specific sequence in order to avoid spurious writing to the I/Os registers.

Fast I/O handling allowing maximum I/O toggling up to 84 MHz.

3.28 Analog-to-digital converter (ADC)

One 12-bit analog-to-digital converter is embedded and shares up to 16 external channels, performing conversions in the single-shot or scan mode. In scan mode, automatic conversion is performed on a selected group of analog inputs.

Figure 13. STM32F401xB/STM32F401xC LQFP100 pinout



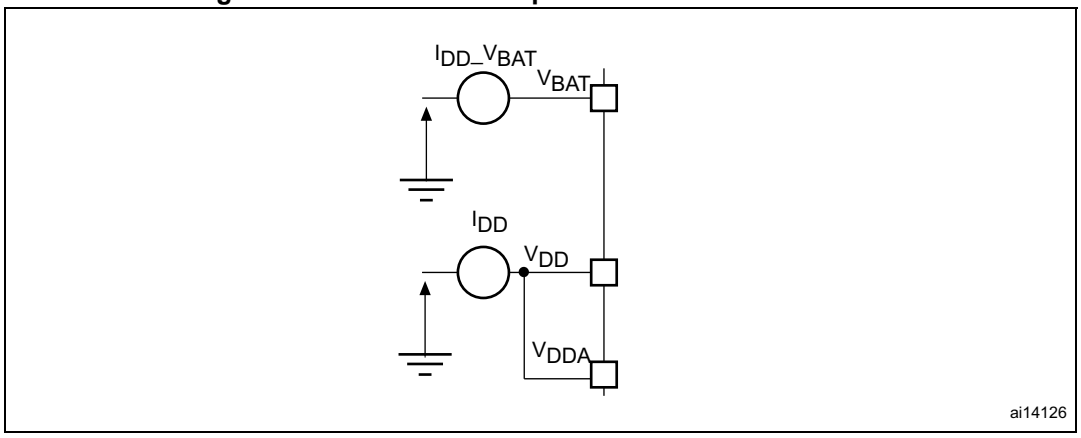
1. The above figure shows the package top view.

Table 8. STM32F401xB/STM32F401xC pin definitions (continued)

Pin Number					Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UQFN48	WLCSP49	LQFP64	LQFP100	UFBGA100						
13	E4	17	26	L3	PA3	I/O	FT	-	USART2_RX, TIM2_CH4, TIM5_CH4, TIM9_CH2, EVENTOUT	ADC1_IN3
-	-	18	27	-	VSS	S	-	-	-	-
-	-	19	28	-	VDD	S	-	-	-	-
-	-	-	-	E3	BYPASS_ REG	I	FT	-	-	-
14	G6	20	29	M3	PA4	I/O	FT	-	SPI1_NSS, SPI3_NSS/I2S3_WS, USART2_CK, EVENTOUT	ADC1_IN4
15	F5	21	30	K4	PA5	I/O	FT	-	SPI1_SCK, TIM2_CH1/TIM2_ETR, EVENTOUT	ADC1_IN5
16	F4	22	31	L4	PA6	I/O	FT	-	SPI1_MISO, TIM1_BKIN, TIM3_CH1, EVENTOUT	ADC1_IN6
17	F3	23	32	M4	PA7	I/O	FT	-	SPI1_MOSI, TIM1_CH1N, TIM3_CH2, EVENTOUT	ADC1_IN7
-	-	24	33	K5	PC4	I/O	FT	-	EVENTOUT	ADC1_IN14
-	-	25	34	L5	PC5	I/O	FT	-	EVENTOUT	ADC1_IN15
18	G5	26	35	M5	PB0	I/O	FT	-	TIM1_CH2N, TIM3_CH3, EVENTOUT	ADC1_IN8
19	G4	27	36	M6	PB1	I/O	FT	-	TIM1_CH3N, TIM3_CH4, EVENTOUT	ADC1_IN9
20	G3	28	37	L6	PB2	I/O	FT	-	EVENTOUT	BOOT1
-	-	-	38	M7	PE7	I/O	FT	-	TIM1_ETR, EVENTOUT	-
-	-	-	39	L7	PE8	I/O	FT	-	TIM1_CH1N, EVENTOUT	-
-	-	-	40	M8	PE9	I/O	FT	-	TIM1_CH1, EVENTOUT	-
-	-	-	41	L8	PE10	I/O	FT	-	TIM1_CH2N, EVENTOUT	-
-	-	-	42	M9	PE11	I/O	FT	-	SPI4_NSS, TIM1_CH2, EVENTOUT	-
-	-	-	43	L9	PE12	I/O	FT	-	SPI4_SCK, TIM1_CH3N, EVENTOUT	-
-	-	-	44	M10	PE13	I/O	FT	-	SPI4_MISO, TIM1_CH3, EVENTOUT	-

6.1.7 Current consumption measurement

Figure 19. Current consumption measurement scheme



6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 11: Voltage characteristics*, *Table 12: Current characteristics*, and *Table 13: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. Device mission profile (application conditions) is compliant with JEDEC JESD47 Qualification Standard. Extended mission profiles are available on demand.

Table 11. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DD}–V_{SS}	External main supply voltage (including V_{DDA}, V_{DD} and V_{BAT})(1)	–0.3	4.0	V
V_{IN}	Input voltage on FT pins(2)	V_{SS}–0.3	V_{DD}+4.0	
	Input voltage on any other pin	V_{SS}–0.3	4.0	
	Input voltage for BOOT0	V_{SS}	9.0	
$\lvert\Delta V_{DDx}\rvert$	Variations between different V_{DD} power pins	-	50	mV
$\lvert V_{SSX} - V_{SS}\rvert$	Variations between all the different ground pins including V_{REF-}	-	50	
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see *Section 6.3.14: Absolute maximum ratings (electrical sensitivity)*		

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum value must always be respected. Refer to *Table 12* for the values of the maximum allowed injected current.

Table 12. Current characteristics

Symbol	Ratings	Max.	Unit
ΣI_{VDD}	Total current into sum of all V_{DD_x} power lines (source)(1)	160	mA
ΣI_{VSS}	Total current out of sum of all V_{SS_x} ground lines (sink)(1)	-160	
I_{VDD}	Maximum current into each V_{DD_x} power line (source)(1)	100	
I_{VSS}	Maximum current out of each V_{SS_x} ground line (sink)(1)	-100	
I_{IO}	Output current sunk by any I/O and control pin	25	
	Output current sourced by any I/O and control pin	-25	
ΣI_{IO}	Total output current sunk by sum of all I/O and control pins (2)	120	
	Total output current sourced by sum of all I/Os and control pins(2)	-120	
$I_{INJ(PIN)}$ (3)	Injected current on FT pins (4)	–5/+0	
	Injected current on NRST and B pins (4)		
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins)(5)	±25	

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count LQFP packages.
3. Negative injection disturbs the analog performance of the device. See note in *Section 6.3.20: 12-bit ADC characteristics*.
4. Positive injection is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
5. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 13. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	125	
T_{LEAD}	Maximum lead temperature during soldering (WLCSP49, LQFP64/100, UFQFPN48, UFBGA100)	see note (1)	

1. Compliant with JEDEC Std J-STD-020D (for small body, Sn-Pb or Pb assembly), the ST ECOPACK® 7191395 specification, and the European directive on Restrictions on Hazardous Substances (ROHS directive 2011/65/EU, July 2011).

Table 19. Embedded reset and power control block characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{PDRhyst}$(2)	PDR hysteresis		-	40	-	mV
V_{BOR1}	Brownout level 1 threshold	Falling edge	2.13	2.19	2.24	V
		Rising edge	2.23	2.29	2.33	
V_{BOR2}	Brownout level 2 threshold	Falling edge	2.44	2.50	2.56	
		Rising edge	2.53	2.59	2.63	
V_{BOR3}	Brownout level 3 threshold	Falling edge	2.75	2.83	2.88	
		Rising edge	2.85	2.92	2.97	
$V_{BORhyst}$(2)	BOR hysteresis		-	100	-	mV
$T_{RSTTEMPO}$(2)(3)	POR reset timing		0.5	1.5	3.0	ms
I_{RUSH}(2)	InRush current on voltage regulator power-on (POR or wakeup from Standby)		-	160	200	mA
E_{RUSH}(2)	InRush energy on voltage regulator power-on (POR or wakeup from Standby)	V_{DD} = 1.7 V, T_A = 105 °C, I_{RUSH} = 171 mA for 31 µs	-	-	5.4	µC

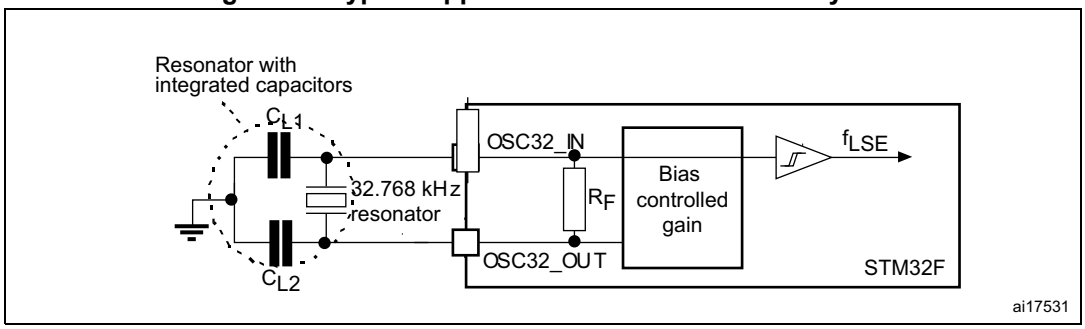
1. The product behavior is guaranteed by design down to the minimum $V_{POR/PDR}$ value.
2. Guaranteed by design.
3. The reset timing is measured from the power-on (POR reset or wakeup from V_{BAT}) to the instant when first instruction is fetched by the user application code.

6.3.6 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.
The current consumption is measured as described in *Figure 19: Current consumption measurement scheme*.

All the run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to CoreMark code.

Figure 25. Typical application with a 32.768 kHz crystal



6.3.9 Internal clock source characteristics

The parameters given in *Table 39* and *Table 40* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 14*.

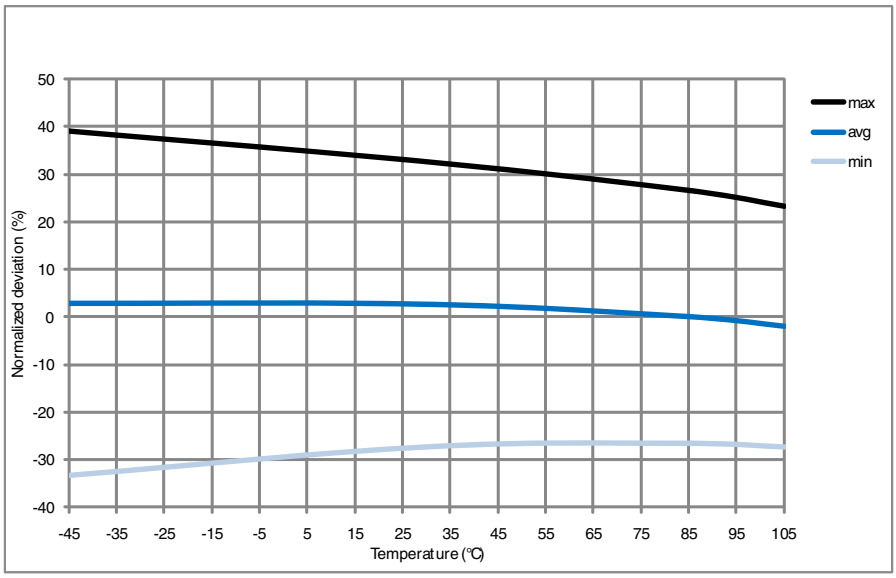
High-speed internal (HSI) RC oscillator

Table 39. HSI oscillator characteristics (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency	-	-	16	-	MHz
ACC_{HSI}	HSI user trimming step(2)	-	-	-	1	%
	Accuracy of the HSI oscillator	T_A = –40 to 105 °C(3)	–8	-	4.5	%
		T_A = –10 to 85 °C(3)	–4	-	4	%
		T_A = 25 °C(4)	–1	-	1	%
$t_{su(HSI)}$(2)	HSI oscillator startup time	-	-	2.2	4	µs
$I_{DD(HSI)}$(2)	HSI oscillator power consumption	-	-	60	80	µA

1. V_{DD} = 3.3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Guaranteed by design.
3. Guaranteed by characterization.
4. Factory calibrated, parts not soldered.

Figure 27. ACC_{LSI} versus temperature



6.3.10 PLL characteristics

The parameters given in *Table 41* and *Table 42* are derived from tests performed under temperature and V_{DD} supply voltage conditions summarized in *Table 14*.

Table 41. Main PLL characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock(1)			0.95(2)	1	2.10	MHz
f_{PLL_OUT}	PLL multiplier output clock			24	-	84	MHz
f_{PLL48_OUT}	48 MHz PLL multiplier output clock			-	48	75	MHz
f_{VCO_OUT}	PLL VCO output			192	-	432	MHz
t_{LOCK}	PLL lock time	VCO freq = 192 MHz		75	-	200	µs
		VCO freq = 432 MHz		100	-	300	
Jitter(3)	Cycle-to-cycle jitter	System clock 84 MHz	RMS	-	25	-	ps
			peak to peak	-	±150	-	
	Period Jitter		RMS	-	15	-	
			peak to peak	-	±200	-	

Table 46. Flash memory programming with V_{PP} voltage (continued)

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
V_{prog}	Programming voltage		2.7	-	3.6	V
V_{PP}	V_{PP} voltage range		7	-	9	V
I_{PP}	Minimum current sunk on the V_{PP} pin		10	-	-	mA
t_{VPP}(3)	Cumulative time during which V_{PP} is applied		-	-	1	hour

1. Guaranteed by design.
2. The maximum programming time is measured after 100K erase operations.
3. V_{PP} should only be connected during programming/erasing.

Table 47. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Value	Unit
			Min(1)	
N_{END}	Endurance	T_A = –40 to +85 °C (6 suffix versions) T_A = –40 to +105 °C (7 suffix versions)	10	kcycles
t_{RET}	Data retention	1 kcycle(2) at T_A = 85 °C	30	Years
		1 kcycle(2) at T_A = 105 °C	10	
		10 kcycles(2) at T_A = 55 °C	20	

1. Guaranteed by characterization.
2. Cycling performed over the whole temperature range.

6.3.13 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 48*. They are based on the EMS levels and classes defined in application note AN1709.

Table 48. EMS characteristics for LQFP100 package

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, LQFP100, WLCSP49, T_A = +25 °C, f_{HCLK} = 84 MHz, conforms to IEC 61000-4-2	2B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, LQFP100, WLCSP49, T_A = +25 °C, f_{HCLK} = 84 MHz, conforms to IEC 61000-4-4	4A

When the application is exposed to a noisy environment, it is recommended to avoid pin exposition to disturbances. The pins showing a middle range robustness are: PA0, PA1, PA2, on LQFP100 packages and PDR_ON on WLCSP49.

As a consequence, it is recommended to add a serial resistor (1 kΩ maximum) located as close as possible to the MCU to the pins exposed to noise (connected to tracks longer than 50 mm on PCB).

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

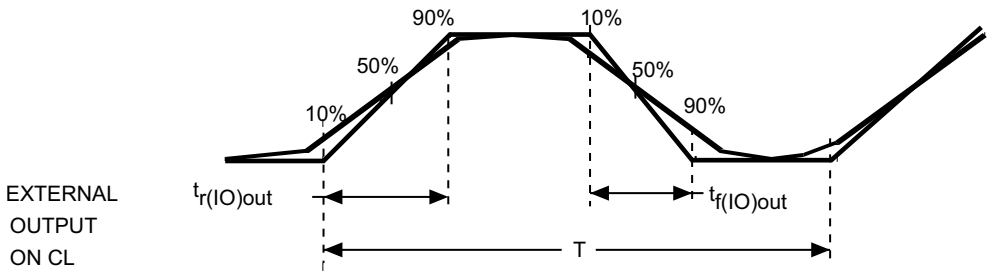
Table 54. I/O static characteristics (continued)

Symbol	Parameter		Conditions	Min	Typ	Max	Unit
V_{HYS}	FT and NRST I/O input hysteresis		1.7 V≤V_{DD}≤3.6 V	-	10% V_{DD} (3)	-	V
	BOOT0 I/O input hysteresis		1.75 V≤V_{DD} ≤3.6 V, -40 °C≤T_A ≤105 °C	-	100	-	mV
			1.7 V≤V_{DD} ≤3.6 V, 0 °C≤T_A ≤105 °C				
I_{lkg}	I/O input leakage current (4)		V_{SS} ≤V_{IN} ≤V_{DD}	-	-	±1	µA
	I/O FT input leakage current (5)		V_{IN} = 5 V	-	-	3	
R_{PU}	Weak pull-up equivalent resistor(6)	All pins except for PA10 (OTG_FS_ID)	V_{IN} = V_{SS}	30	40	50	kΩ
		PA10 (OTG_FS_ID)		7	10	14	
R_{PD}	Weak pull-down equivalent resistor(7)	All pins except for PA10 (OTG_FS_ID)	V_{IN} = V_{DD}	30	40	50	
		PA10 (OTG_FS_ID)		7	10	14	
C_{IO} (8)	I/O pin capacitance		-	-	5	-	pF

1. Guaranteed by design.
2. Guaranteed by test in production.
3. With a minimum of 200 mV.
4. Leakage could be higher than the maximum value, if negative current is injected on adjacent pins, Refer to *Table 53: I/O current injection susceptibility*
5. To sustain a voltage higher than VDD +0.3 V, the internal pull-up/pull-down resistors must be disabled. Leakage could be higher than the maximum value, if negative current is injected on adjacent pins.Refer to *Table 53: I/O current injection susceptibility*
6. Pull-up resistors are designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimum (~10% order).
7. Pull-down resistors are designed with a true resistance in series with a switchable NMOS. This NMOS contribution to the series resistance is minimum (~10% order).
8. Hysteresis voltage between Schmitt trigger switching levels. Guaranteed by characterization.

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements for FT I/Os is shown in *Figure 30*.

Figure 31. I/O AC characteristics definition



Maximum frequency is achieved if (t_r + t_f) ≤ (2/3)T and if the duty cycle is (45-55%) when loaded by CL specified in the table " *I/O AC characteristics*".

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6.3.17 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see *Table 54*).

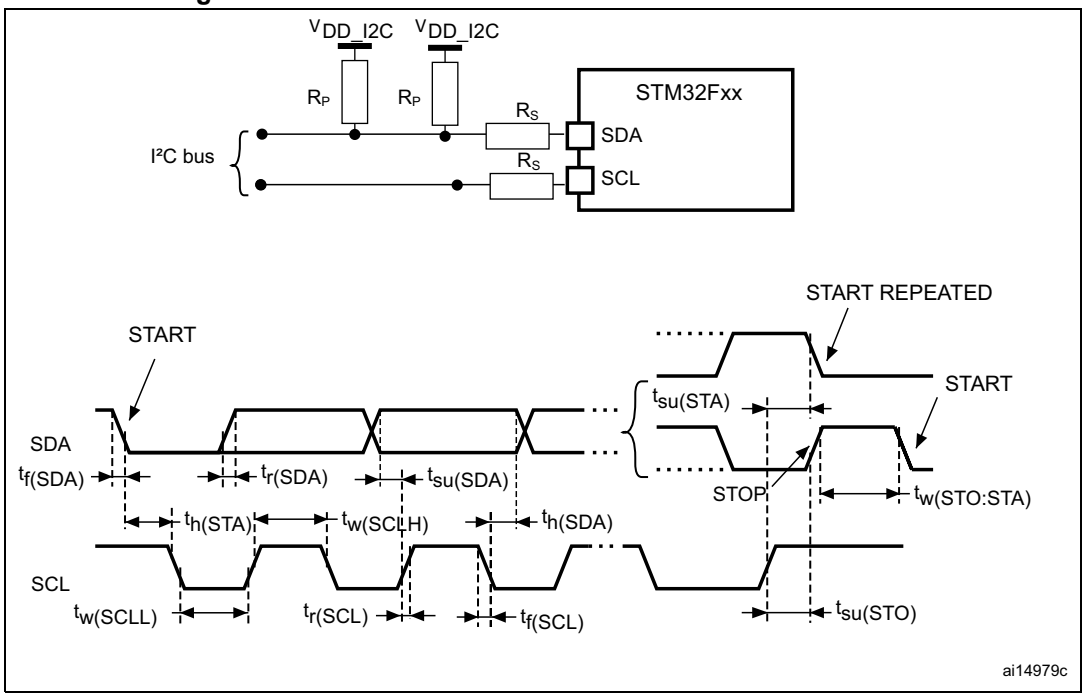
Unless otherwise specified, the parameters given in *Table 57* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 14*. Refer to *Table 54: I/O static characteristics* for the values of VIH and VIL for NRST pin.

Table 57. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{PU}	Weak pull-up equivalent resistor(1)	$V_{IN} = V_{SS}$	30	40	50	kΩ
$V_{F(NRST)}$(2)	NRST Input filtered pulse		-	-	100	ns
$V_{NF(NRST)}$(2)	NRST Input not filtered pulse	V_{DD} > 2.7 V	300	-	-	ns
T_{NRST_OUT}	Generated reset pulse duration	Internal Reset source	20	-	-	µs

1. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).
2. Guaranteed by design.

Figure 33. I²C bus AC waveforms and measurement circuit



1. R_S = series protection resistor.
2. R_P = external pull-up resistor.
3. V_{DD_I2C} is the I2C bus power supply.

Table 60. SCL frequency (f_{PCLK1}= 42 MHz, V_{DD} = V_{DD_I2C} = 3.3 V)(1)(2)

f_{SCL} (kHz)	I2C_CCR value
	R_P = 4.7 kΩ
400	0x8019
300	0x8021
200	0x8032
100	0x0096
50	0x012C
20	0x02EE

1. R_P = External pull-up resistance, f_{SCL} = I²C speed
2. For speeds around 200 kHz, the tolerance on the achieved speed is of ±5%. For other speed ranges, the tolerance on the achieved speed is ±2%. These variations depend on the accuracy of the external components used to design the application.

USB OTG full speed (FS) characteristics

This interface is present in USB OTG FS controller.

Table 63. USB OTG FS startup time

Symbol	Parameter	Max	Unit
$t_{STARTUP}$(1)	USB OTG FS transceiver startup time	1	µs

1. Guaranteed by design.

Table 64. USB OTG FS DC electrical characteristics

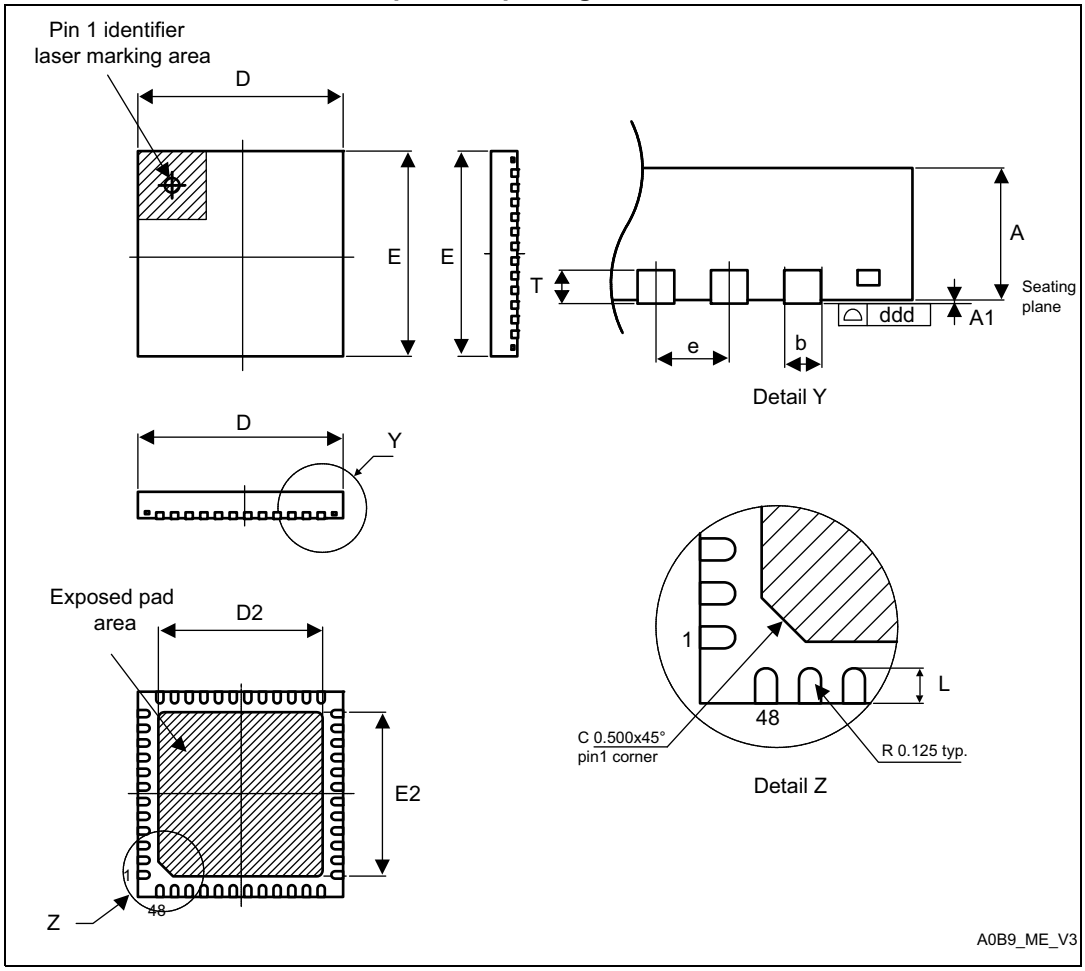
Symbol		Parameter	Conditions	Min.(1)	Typ.	Max.(1)	Unit
Input levels	V_{DD}	USB OTG FS operating voltage		3.0(2)	-	3.6	V
	V_{DI}(3)	Differential input sensitivity	I(USB_FS_DP/DM)	0.2	-	-	V
	V_{CM}(3)	Differential common mode range	Includes V_{DI} range	0.8	-	2.5	
	V_{SE}(3)	Single ended receiver threshold		1.3	-	2.0	
Output levels	V_{OL}	Static output level low	R_L of 1.5 kΩ to 3.6 V(4)	-	-	0.3	V
	V_{OH}	Static output level high	R_L of 15 kΩ to V_{SS}(4)	2.8	-	3.6	
R_{PD}		PA11, PA12 (USB_FS_DM/DP)	V_{IN} = V_{DD}	17	21	24	kΩ
		PA9 (OTG_FS_VBUS)		0.65	1.1	2.0	
R_{PU}		PA11, PA12 (USB_FS_DM/DP)	V_{IN} = V_{SS}	1.5	1.8	2.1	
		PA9 (OTG_FS_VBUS)	V_{IN} = V_{SS}	0.25	0.37	0.55	

1. All the voltages are measured from the local ground potential.
2. The USB OTG FS functionality is ensured down to 2.7 V but not the full USB full speed electrical characteristics which are degraded in the 2.7-to-3.0 V V_{DD} voltage range.
3. Guaranteed by design.
4. R_L is the load connected on the USB OTG FS drivers.

Note: When VBUS sensing feature is enabled, PA9 should be left at their default state (floating input), not as alternate function. A typical 200 µA current consumption of the embedded sensing block (current to voltage conversion to determine the different sessions) can be observed on PA9 when the feature is enabled.

7.2 UFQFPN48 package information

Figure 49. UFQFPN48 - 48-lead, 7 x 7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package outline



1. Drawing is not to scale.
2. All leads/pads should also be soldered to the PCB to improve the lead/pad solder joint life.
3. There is an exposed die pad on the underside of the UFQFPN package. It is recommended to connect and solder this back-side pad to PCB ground.

Table 81. UFQFPN48 - 48-lead, 7 x 7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package mechanical data

Symbol	millimeters			inches(1)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
D	6.900	7.000	7.100	0.2717	0.2756	0.2795
E	6.900	7.000	7.100	0.2717	0.2756	0.2795
D2	5.500	5.600	5.700	0.2165	0.2205	0.2244