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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	66MHz
Co-Processors/DSP	Communications; CPM
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (1)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 110°C (TC)
Security Features	-
Package / Case	357-BBGA
Supplier Device Package	357-PBGA (25x25)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/tsxpc860srvzqu66d

Screening/Quality

This product will be manufactured in full compliance with:

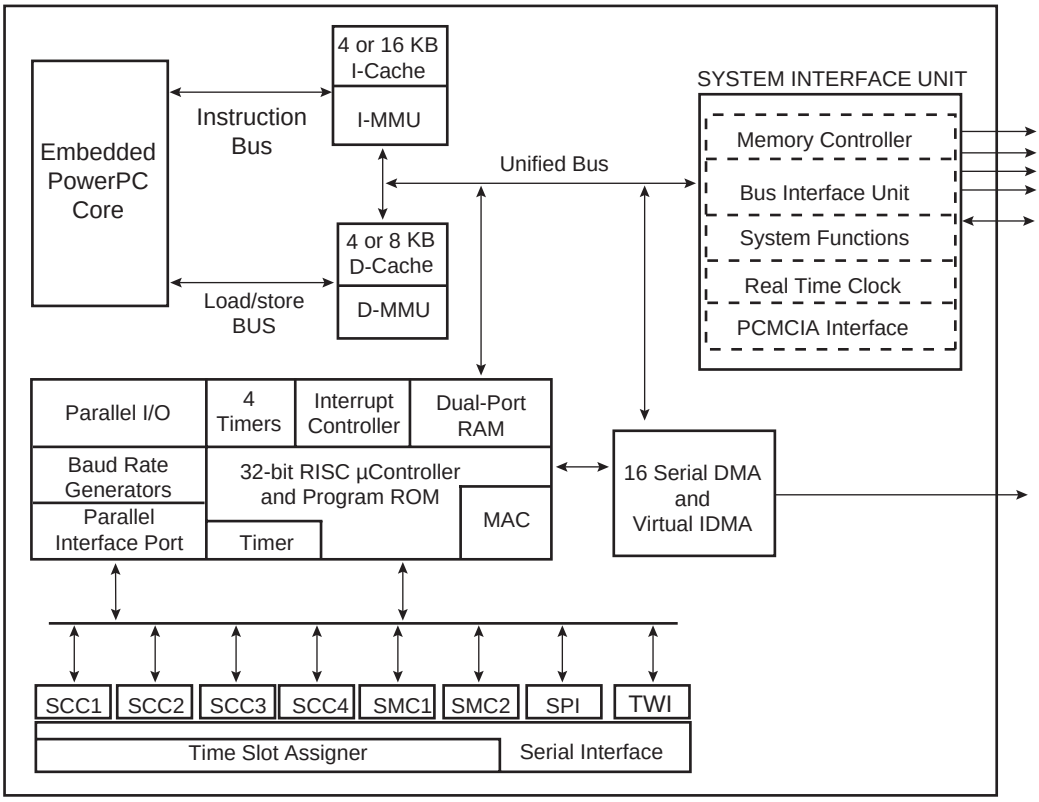
- According to Atmel Standards

General Description

The TSPC860 is functionally composed of three major blocks:

- A 32-bit PowerPC Core with MMUs and Caches
- A System Interface Unit
- A Communications Processor Module

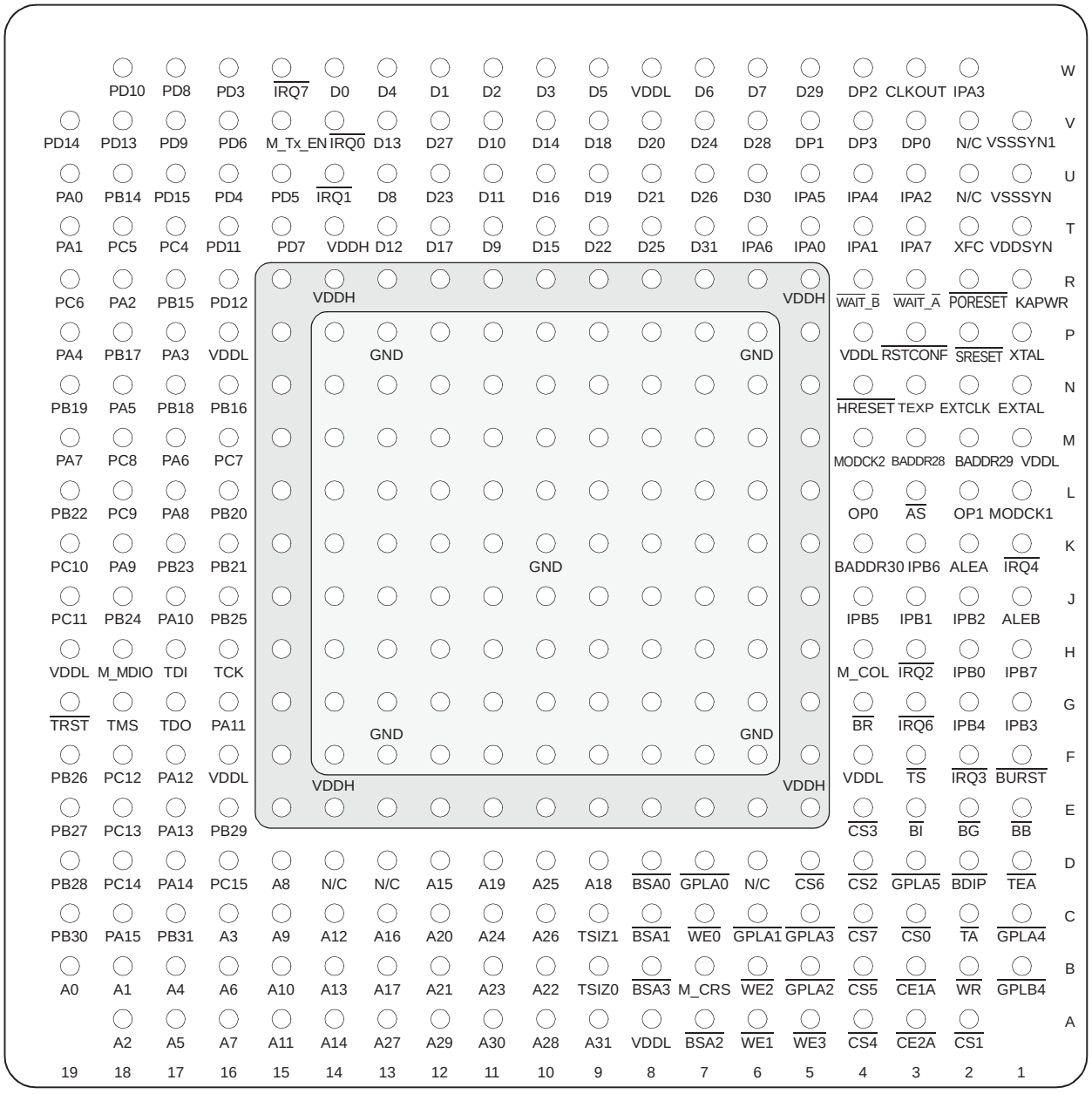
Figure 1. Block Diagram View of the TSPC860



Pin Assignment

Plastic Ball Grid Array

Figure 2. Pin Assignment: Top View



Signal Descriptions

This section describes the signals on the TSPC860.

Figure 3. TSPC860 External Signals

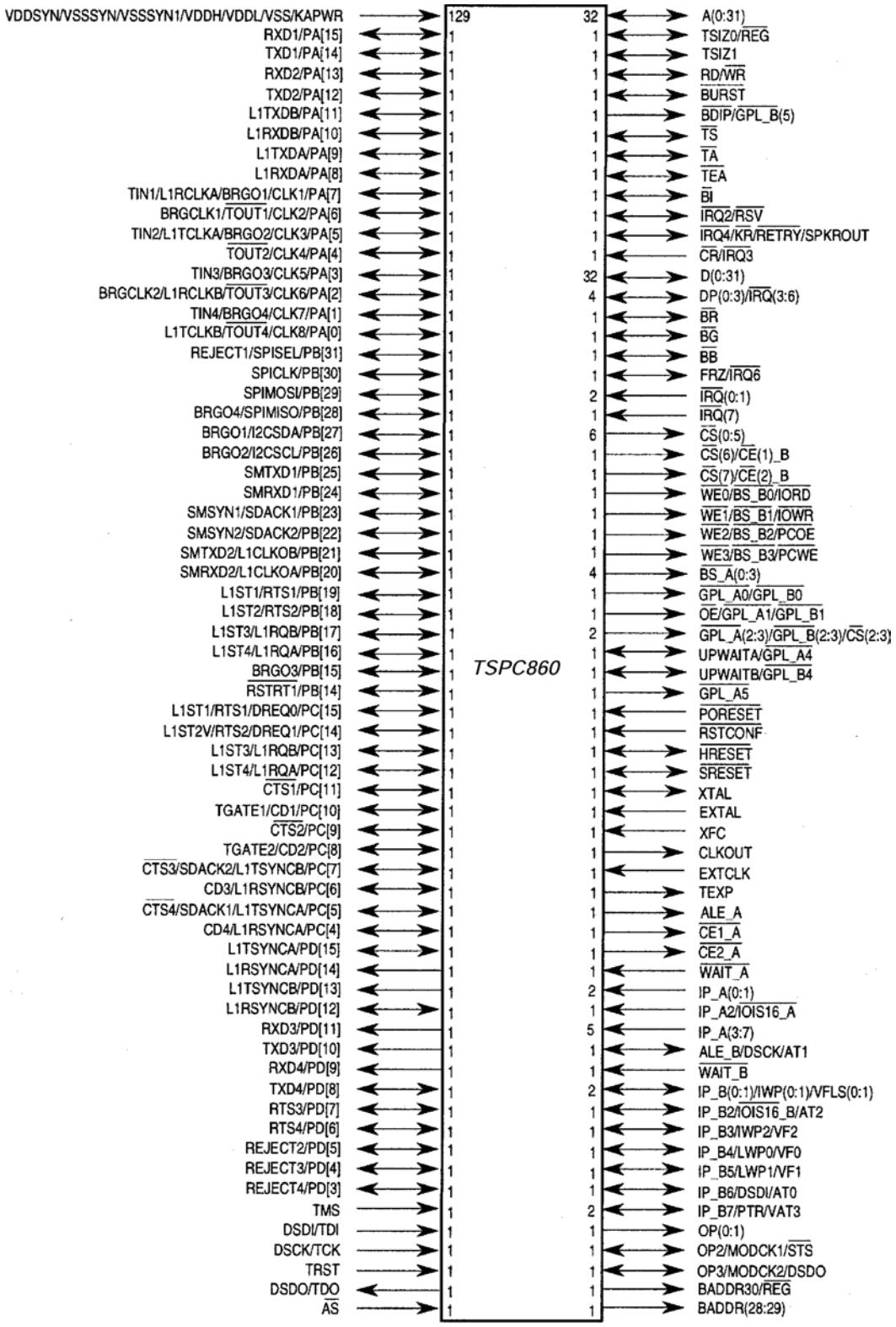


Table 1. Signal Descriptions (Continued)

Name	Reset	Number	Type	Description
$\overline{TA}$	Hi-Z	C2	Bidirectional Active Pull-up	Transfer Acknowledge — Indicates that the slave device addressed in the current transaction accepted data sent by the master (write) or has driven the data bus with valid data (read). This is an output when the PCMCIA interface or memory controller controls the transaction. The only exception occurs when the memory controller controls the slave access by means of the GPCM and the corresponding option register is instructed to wait for an external assertion of $\overline{TA}$. Every slave device should negate $\overline{TA}$ after a transaction ends and immediately three-state it to avoid bus contention if a new transfer is initiated addressing other slave devices. $\overline{TA}$ requires the use of an external pull-up resistor.
$\overline{TEA}$	Hi-Z	D1	Open-drain	Transfer Error Acknowledge — Indicates that a bus error occurred in the current transaction. The TSPC860 asserts $\overline{TEA}$ when the bus monitor does not detect a bus cycle termination within a reasonable amount of time. Asserting $\overline{TEA}$ terminates the bus cycle, thus ignoring the state of $\overline{TA}$. $\overline{TEA}$ requires the use of an external pull-up resistor.
$\overline{BI}$	Hi-Z	E3	Bidirectional Active Pull-up	Burst Inhibit — Indicates that the slave device addressed in the current burst transaction cannot support burst transfers. It acts as an output when the PCMCIA interface or the memory controller takes control of the transaction. $\overline{BI}$ requires the use of an external pull-up resistor.
$\overline{RSV}$ $\overline{IRQ2}$	See Section "Signal States During Hardware Reset" on page 28	H3	Bidirectional Three-state	Reservation — The TSPC860 outputs this three-state signal in conjunction with the address bus to indicate that the core initiated a transfer as a result of a **stwcx.** or **lwarx.** Interrupt Request 2 — One of eight external inputs that can request (by means of the internal interrupt controller) a service routine from the core.
$\overline{KR}$/$\overline{RETRY}$ $\overline{IRQ4}$ SPKROUT	See Section "Signal States During Hardware Reset" on page 28	K1	Bidirectional Three-state	Kill Reservation — This input is used as a part of the memory reservation protocol, when the TSPC860 initiated a transaction as the result of a **stwcx.** instruction. Retry — This input is used by a slave device to indicate it cannot accept the transaction. The TSPC860 must relinquish mastership and reinitiate the transaction after winning in the bus arbitration. Interrupt Request 4 – One of eight external inputs that can request (by means of the internal interrupt controller) a service routine from the core. Note that the interrupt request signal that is sent to the interrupt controller is the logical AND of this line (if defined as $\overline{IRQ4}$) and DP1/$\overline{IRQ4}$ (if defined as $\overline{IRQ4}$). SPKROUT — Digital audio wave form output to be driven to the system speaker.
$\overline{CR}$ $\overline{IRQ3}$	Hi-Z	F2	Input	Cancel Reservation — This input is used as a part of the storage reservation protocol. Interrupt Request 3 — One of eight external inputs that can request (by means of the internal interrupt controller) a service routine from the core. Note that the interrupt request signal sent to the interrupt controller is the logical AND of $\overline{CR}$/$\overline{IRQ3}$ (if defined as $\overline{IRQ3}$) and DP0/$\overline{IRQ3}$ if defined as $\overline{IRQ3}$.

Table 1. Signal Descriptions (Continued)

Name	Reset	Number	Type	Description
IP_B5 LWP1 VF1	Hi-Z	J4	Bidirectional	Input Port B 5 — The TSPC860 monitors this input; its value and changes are reported in the PIPR and PSCR of the PCMCIA interface. Load/Store Watchpoint 1 — This output reports the detection of a data watchpoint in the program flow executed by the core. Visible Instruction Queue Flushes Status — The TSPC860 outputs VF1 with VF0 and VF2 when instruction flow tracking is required. VFn reports the number of instructions flushed from the instruction queue in the core.
IP_B6 DSDI AT0	Hi-Z	K3	Bidirectional Three-state	Input Port B 6 — The TSPC860 senses this input and its value and changes are reported in the PIPR and PSCR of the PCMCIA interface. Development Serial Data Input — Data input for the debug port interface. Address Type 0 — The TSPC860 drives this bidirectional three-state line when it initiates a transaction on the external bus. If high (1), the transaction is the CPM. If low (0), the transaction initiator is the CPU. This signal is not used for transactions initiated by external masters.
IP_B7 $\overline{\text{PTR}}$ AT3	Hi-Z	H1	Bidirectional Three-state	Input Port B 7 — The TSPC860 monitors this input; its value and changes are reported in the PIPR and PSCR of the PCMCIA interface. Program Trace — To allow program flow tracking, the TSPC860 asserts this output to indicate an instruction fetch is taking place. Address Type 3 — The TSPC860 drives the bidirectional three-state signal when it starts a transaction on the external bus. When the core initiates a transfer, AT3 indicates whether it is a reservation for a data transfer or a program trace indication for an instruction fetch. This signal is not used for transactions initiated by external masters.
OP(0-1)	Low	L4, L2	Output	Output Port 0-1 — The TSPC860 generates these outputs as a result of a write to the PGCRA register in the PCMCIA interface.
OP2 MODCK1 $\overline{\text{STS}}$	Hi-Z	L1	Bidirectional	Output Port 2 — This output is generated by the TSPC860 as a result of a write to the PGCRB register in the PCMCIA interface. Mode Clock 1 — Input sampled when $\overline{\text{PORESET}}$ is negated to configure PLL/clock mode. Special Transfer Start — The TSPC860 drives this output to indicate the start of an external bus transfer or of an internal transaction in show-cycle mode.
OP3 MODCK2 DSDO	Hi-Z	M4	Bidirectional	Output Port 3 — This output is generated by the TSPC860 as a result of a write to the PGCRB register in the PCMCIA interface. Mode Clock 2 — This input is sampled at the $\overline{\text{PORESET}}$ negation to configure the PLL/clock mode of operation. Development Serial Data Output — Output data from the debug port interface.

Table 1. Signal Descriptions (Continued)

Name	Reset	Number	Type	Description
PA[1] CLK7 TIN4 BRGO4		T19	Bidirectional	General-Purpose I/O Port A Bit 1 — Bit 1 of the general-purpose I/O port A. CLK7 — One of eight clock inputs that can be used to clock SCCs and SMCs. TIN4 — Timer 4 external clock input. BRGO4 — BRG4 output clock.
PA[0] CLK8 $\overline{\text{TOUT4}}$ L1TCLKB		U19	Bidirectional	General-Purpose I/O Port A Bit 0 — Bit 0 of the general-purpose I/O port A. CLK8 — One of eight clock inputs that can be used to clock SCCs and SMCs. $\overline{\text{TOUT4}}$ — Timer 4 output. L1TCLKB — Transmit clock for the serial interface TDM port B.
PB[31] $\overline{\text{SPISEL}}$ $\overline{\text{REJECT1}}$		C17	Bidirectional (Optional: Open-drain)	General-Purpose I/O Port B Bit 31 — Bit 31 of the general-purpose I/O port B. $\overline{\text{SPISEL}}$ — SPI slave select input. $\overline{\text{REJECT1}}$ — SCC1 CAM interface reject pin.
PB[30] SPICLK $\overline{\text{RSTRT2}}$		C19	Bidirectional (Optional: Open-drain)	General-Purpose I/O Port B Bit 30 — Bit 30 of the general-purpose I/O port B. SPICLK — SPI output clock when it is configured as a master or SPI input clock when it is configured as a slave. $\overline{\text{RSTRT2}}$ — SCC2 serial CAM interface output signal that marks the start of a frame.
PB[29] SPIMOSI		E16	Bidirectional (Optional: Open-drain)	General-Purpose I/O Port B Bit 29 — Bit 29 of the general-purpose I/O port B. SPIMOSI — SPI output data when it is configured as a master or SPI input data when it is configured as a slave.
PB[28] SPIMISO BRGO4		D19	Bidirectional (Optional: Open-drain)	General-Purpose I/O Port B Bit 28 — Bit 29 of the general-purpose I/O port B. SPIMISO — SPI input data when the TSPC860 is a master; SPI output data when it is a slave. BRGO4 — BRG4 output clock.
PB[27] I2CSDA BRGO1	Hi-Z	E19	Bidirectional (Optional: Open-drain)	General-Purpose I/O Port B Bit 27 — Bit 27 of the general-purpose I/O port B. I2CSDA — TWI serial data pin. Bidirectional; should be configured as an open-drain output. BRGO1 — BRG1 output clock.
PB[26] I2CSCL BRGO2		F19	Bidirectional (Optional: Open-drain)	General-Purpose I/O Port B Bit 26 — Bit 26 of the general-purpose I/O port B. I2CSCL — TWI serial clock pin. Bidirectional; should be configured as an open-drain output. BRGO2 — BRG2 output clock.
PB[25] SMTXD1		J16	Bidirectional (Optional: Open-drain)	General-Purpose I/O Port B Bit 25 — Bit 25 of the general-purpose I/O port B. SMTXD1 — SMC1 transmit data output.
PB[24] SMRXD1		J18	Bidirectional (Optional: Open-drain)	General-Purpose I/O Port B Bit 24 — Bit 24 of the general-purpose I/O port B. SMRXD1 — SMC1 receive data input.

Table 1. Signal Descriptions (Continued)

Name	Reset	Number	Type	Description
PB[14] $\overline{\text{RSTRT1}}$		U18	Bidirectional	General-Purpose I/O Port B Bit 14 — Bit 14 of the general-purpose I/O port B. $\overline{\text{RSTRT1}}$ — SCC1 serial CAM interface outputs that marks the start of a frame.
PC[15] $\overline{\text{DREQ0}}$ $\overline{\text{RTS1}}$ L1ST1		D16	Bidirectional	General-Purpose I/O Port C Bit 15 — Bit 15 of the general-purpose I/O port C. $\overline{\text{DREQ0}}$ — IDMA channel 0 request input. $\overline{\text{RTS1}}$ — Request to send modem line for SCC1. L1ST1 — One of four output strobes that can be generated by the serial interface.
PC[14] $\overline{\text{DREQ1}}$ $\overline{\text{RTS2}}$ L1ST2		D18	Bidirectional	General-Purpose I/O Port C Bit 14 — Bit 14 of the general-purpose I/O port C. $\overline{\text{DREQ1}}$ — IDMA channel 1 request input. $\overline{\text{RTS2}}$ — Request to send modem line for SCC2. L1ST2 — One of four output strobes that can be generated by the serial interface.
PC[13] $\overline{\text{L1RQB}}$ L1ST3		E18	Bidirectional	General-Purpose I/O Port C Bit 13 — Bit 13 of the general-purpose I/O port C. $\overline{\text{L1RQB}}$ — D-channel request signal for the serial interface TDM port B. L1ST3 — One of four output strobes that can be generated by the serial interface.
PC[12] $\overline{\text{L1RQA}}$ L1ST4		F18	Bidirectional	General-Purpose I/O Port C Bit 12 — Bit 12 of the general-purpose I/O port C. $\overline{\text{L1RQA}}$ — D-channel request signal for the serial interface TDM port A. L1ST4 — One of four output strobes that can be generated by the serial interface.
PC[11] $\overline{\text{CTS1}}$		J19	Bidirectional	General-Purpose I/O Port C Bit 11 — Bit 11 of the general-purpose I/O port C. $\overline{\text{CTS1}}$ — Clear to send modem line for SCC1.
PC[10] $\overline{\text{CD1}}$ $\overline{\text{TGATE1}}$	Hi-Z	K19	Bidirectional	General-Purpose I/O Port C Bit 10 — Bit 10 of the general-purpose I/O port C. $\overline{\text{CD1}}$ — Carrier detect modem line for SCC1. $\overline{\text{TGATE1}}$ — Timer 1/timer 2 gate signal.
PC[9] $\overline{\text{CTS2}}$		L18	Bidirectional	General-Purpose I/O Port C Bit 9 — Bit 9 of the general-purpose I/O port C. $\overline{\text{CTS2}}$ — Clear to send modem line for SCC2.
PC[8] $\overline{\text{CD2}}$ $\overline{\text{TGATE2}}$		M18	Bidirectional	General-Purpose I/O Port C Bit 8 — Bit 8 of the general-purpose I/O port C. $\overline{\text{CD2}}$ — Carrier detect modem line for SCC2. $\overline{\text{TGATE2}}$ — Timer 3/timer 4 gate signal.

Figure 16. External Bus Read Timing (GPCM Controlled – TRLX = ‘0’ ACS = ‘11’)

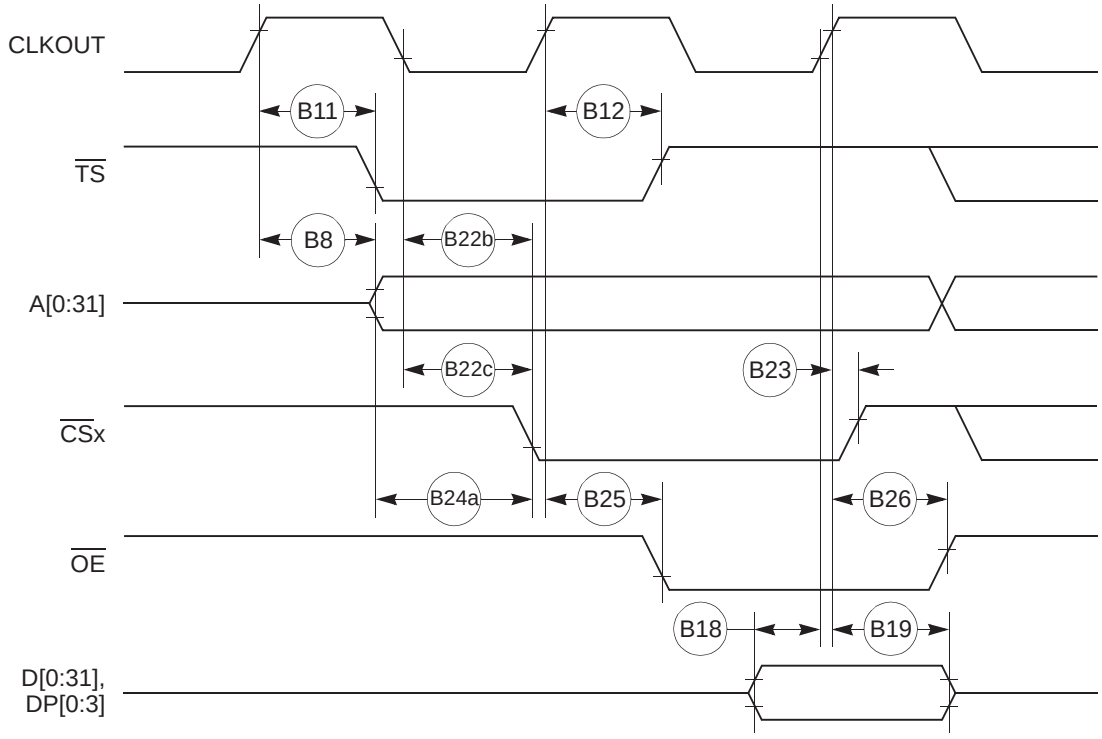


Figure 17. External Bus Read Timing (GPCM Controlled – TRLX = ‘1’, ACS = ‘10’, ACS = ‘11’)

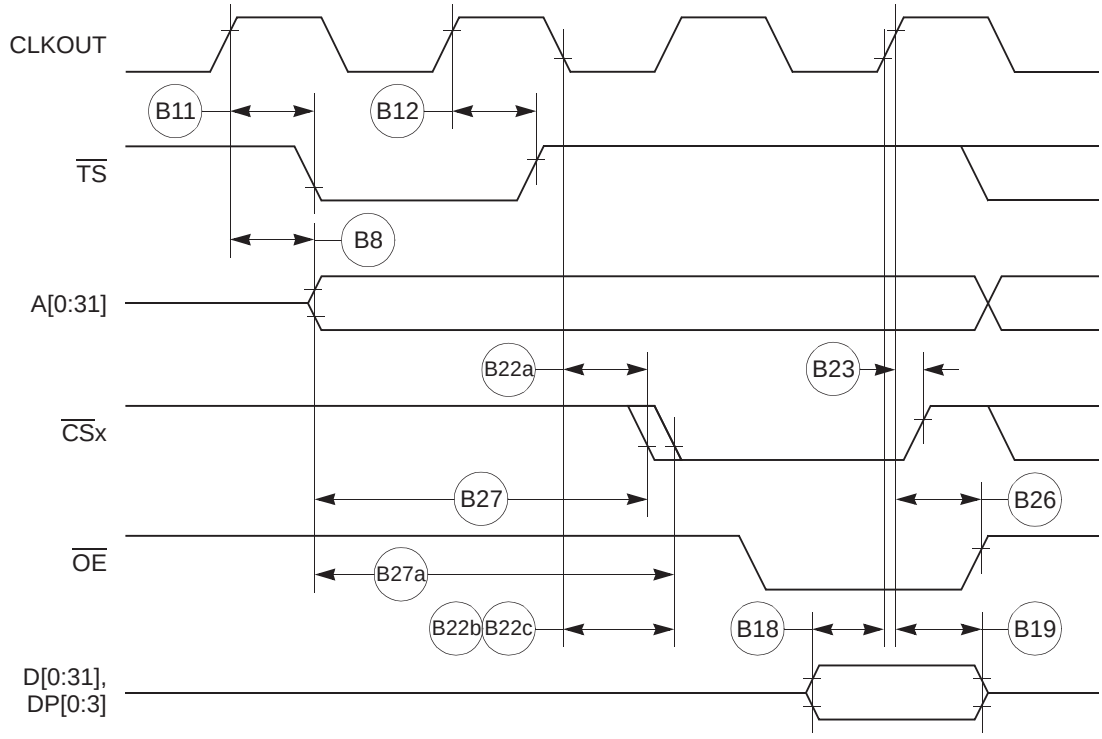


Figure 18. External Bus Write Timing (GPCM controlled – TRLX = ‘0’, CSNT = ‘0’)

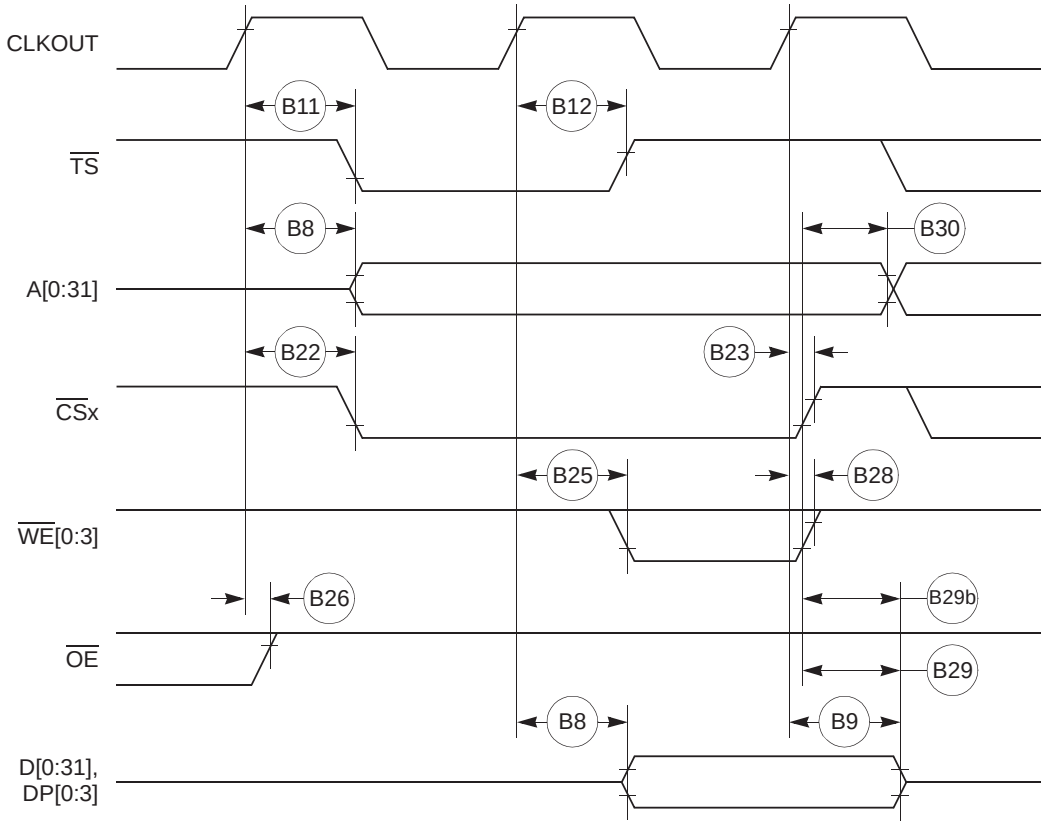


Figure 19. External Bus Write Timing (GPCM controlled – TRLX = ‘0’, CSNT = ‘1’)

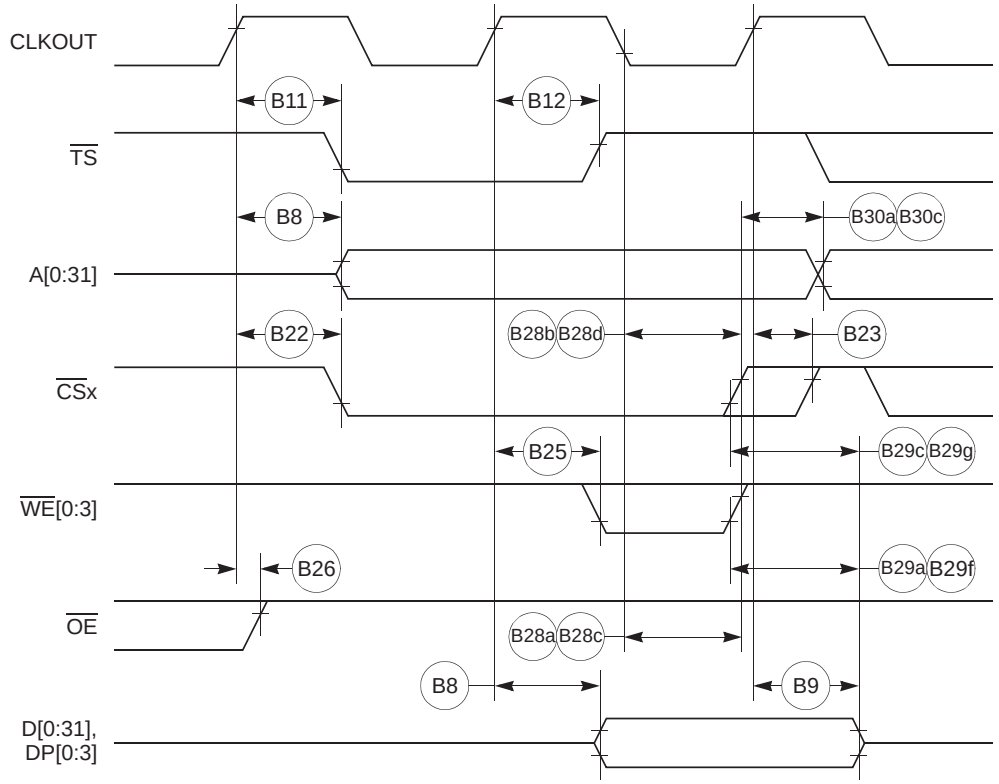


Figure 23. Asynchronous UPWAIT Negated Detection in UPM Handled Cycles Timing

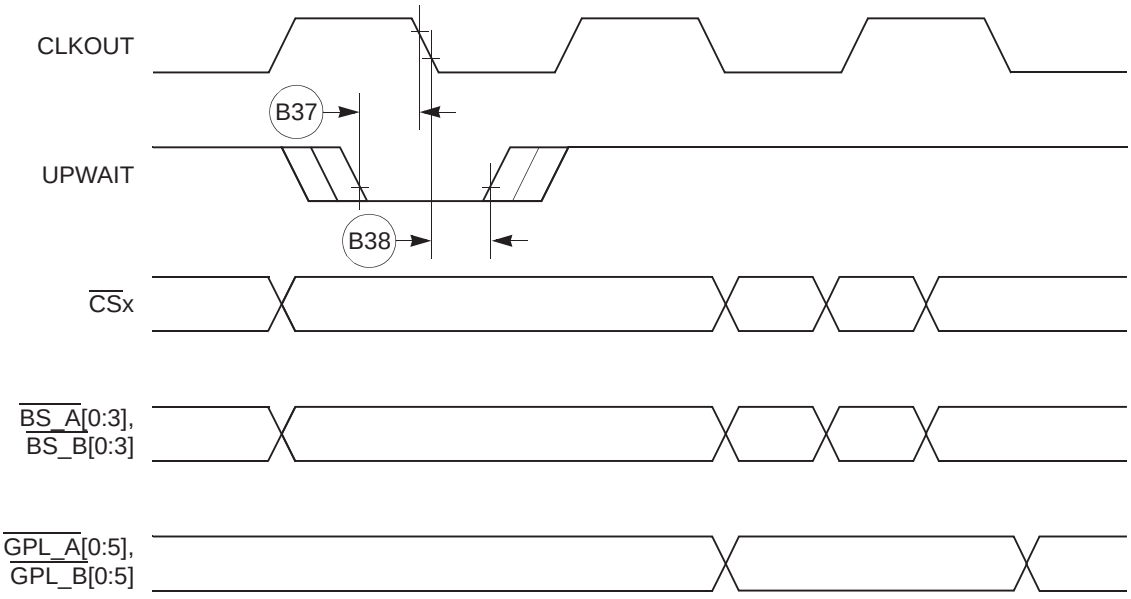


Figure 24. Synchronous External Master Access Timing – GPCM handled ACS = ‘00’

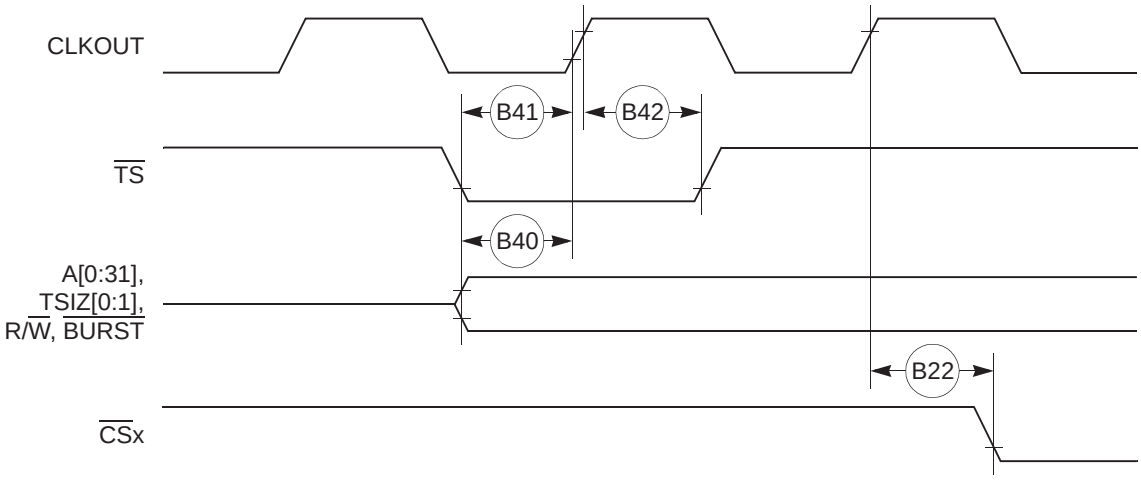


Figure 30. PCMCIA Access Cycles Timing External Bus Write

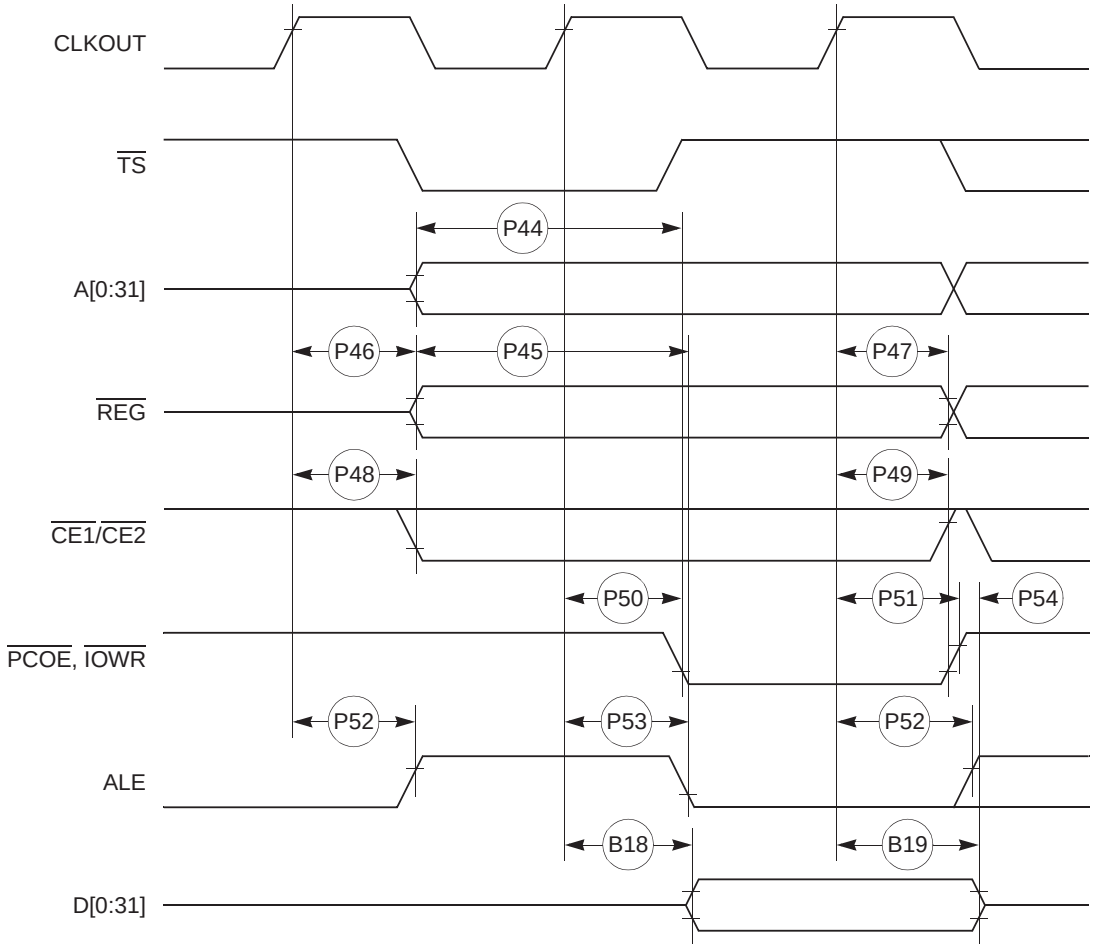


Figure 31. PCMCIA Wait Signals Detection Timing

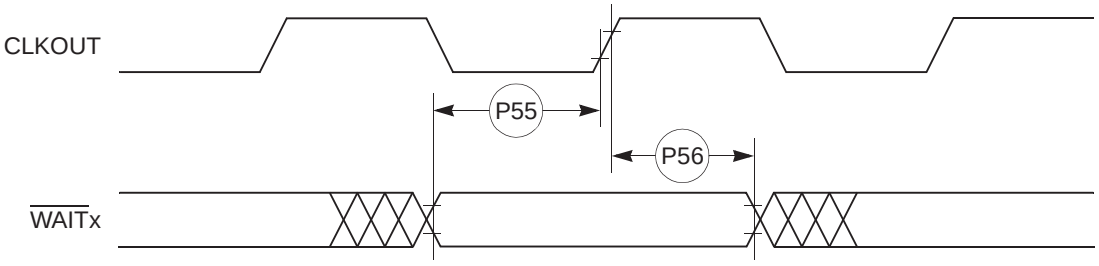


Table 11. PCMCIA Port Timing

Num	Characteristic	33 MHz		40 MHz		50 MHz		66 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
P57	CLKOUT to OPx Valid	–	19	–	19	–	19	–	19	ns
P58	HRESET negated to OPx drive(1)	25.73	–	21.75	–	18	–	14.36	–	ns
P59	IP_Xx valid to CLKOUT Rising Edge	5	–	5	–	5	–	5	–	ns
P60	CLKOUT Rising Edge to IP_Xx invalid	1	–	1	–	1	–	1	–	ns

Note: 1. OP2 and OP3 only.

Figure 32. PCMCIA Output Port Timing

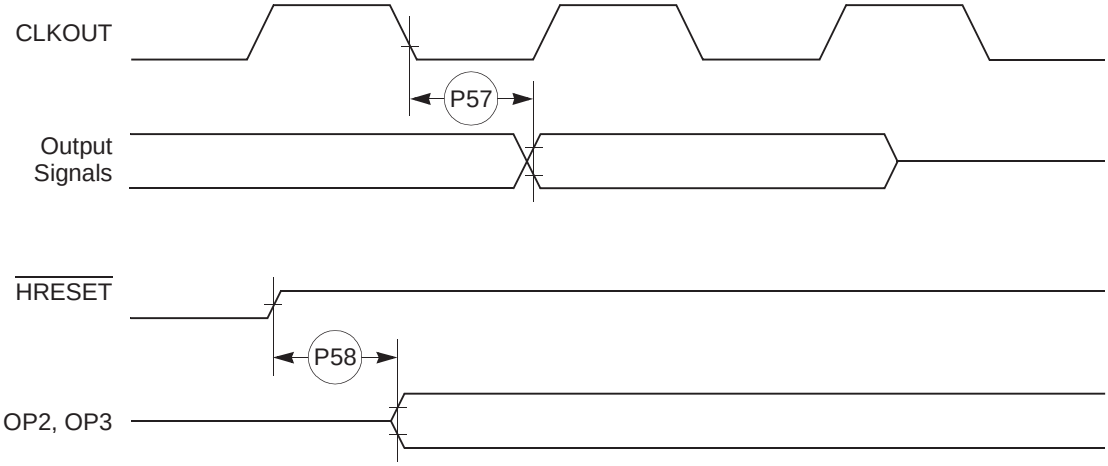


Figure 33. PCMCIA Input Port Timing

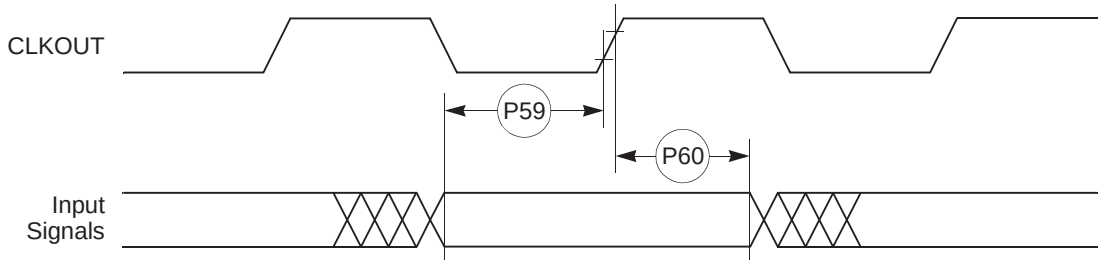


Table 12. Debug Port Timing

Num	Characteristic	All Frequencies		Unit
		Min	Max	
P61	DSCK Cycle Time	$3xT_{CLOCKOUT}$	–	–
P62	DSCK Clock Pulse Width	$1.25xT_{CLOCKOUT}$	–	–
P63	DSCK Rise and Fall Times	0	3	ns
P64	DSDI Input Data Setup Time	8	–	ns
P65	DSDI Data Hold Time	5	–	ns
P66	DSCK Low to DSDO Data Valid	0	15	ns
P67	DSCK Low to DSDO Invalid	0	2	ns

Figure 34. Debug Port Clock Input Timing

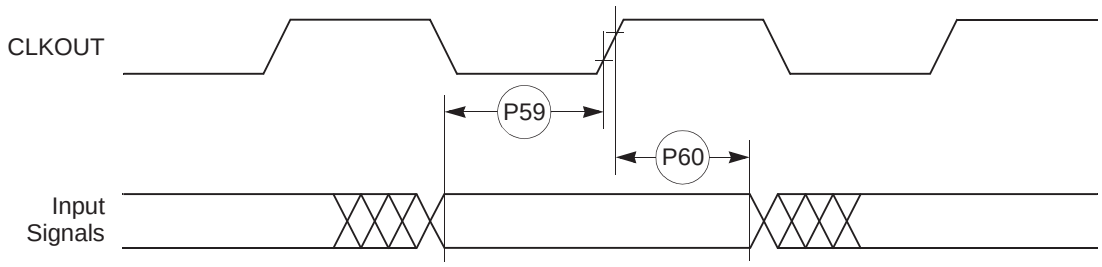


Figure 35. Debug Port Timings

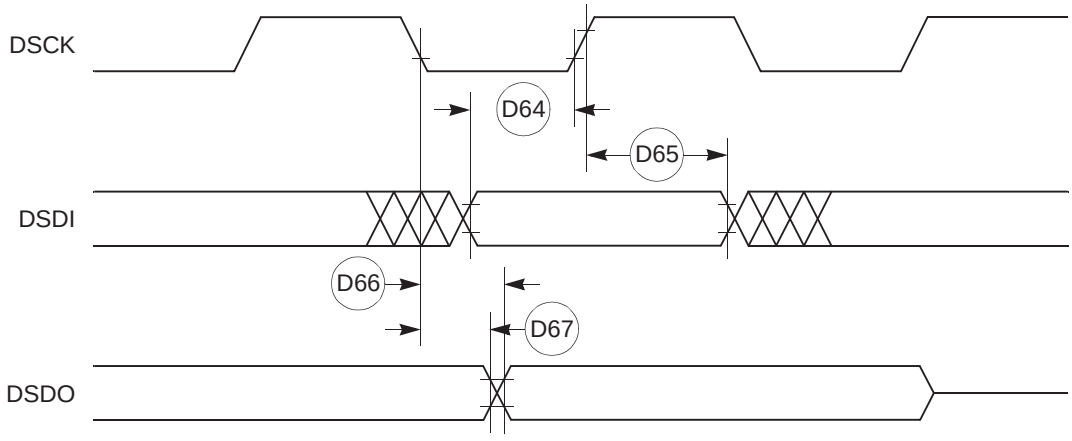


Figure 37. Reset Timing – TSPC860 Data Bus Weak Drive during Configuration

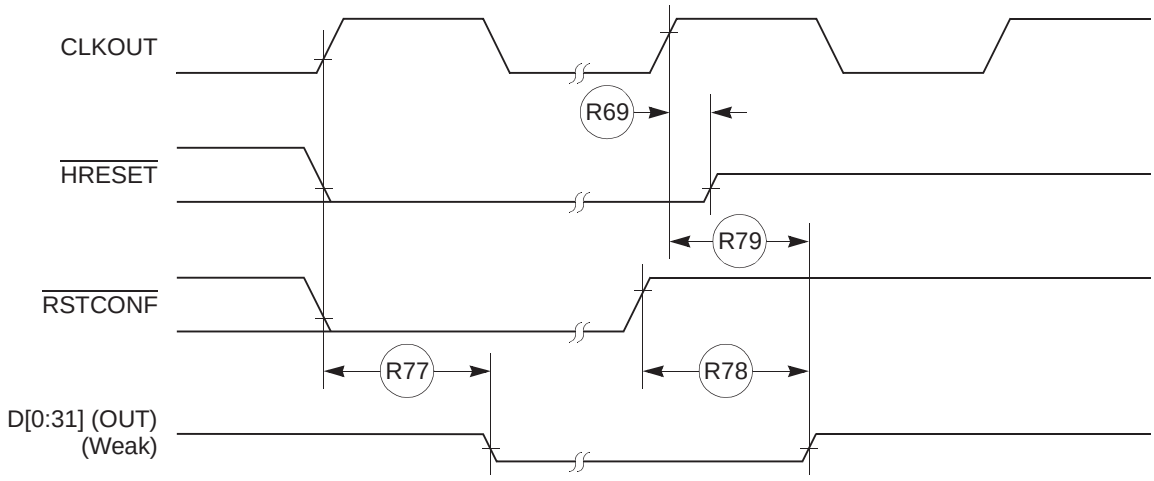


Figure 38. Reset Timing – Debug Port Configuration IEEE 1149.1 Electrical Specifications

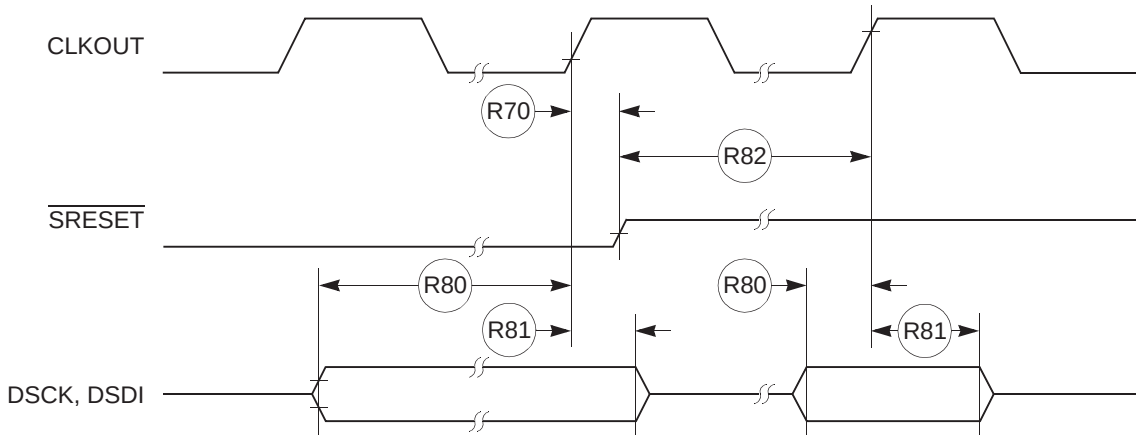


Figure 49. SDACK Timing Diagram – Peripheral Write, TA Sampled Low at the Falling Edge of the Clock

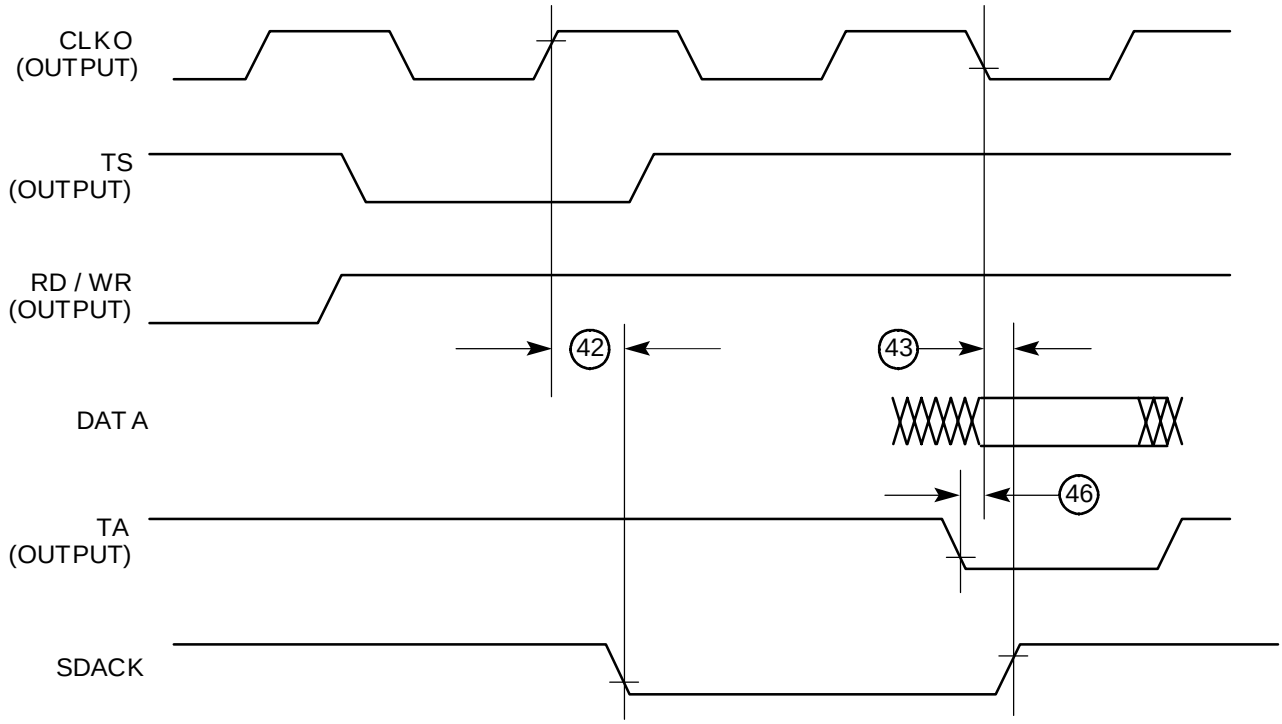


Figure 50. SDACK Timing Diagram – Peripheral Write, TA Sampled High at the Falling Edge of the Clock

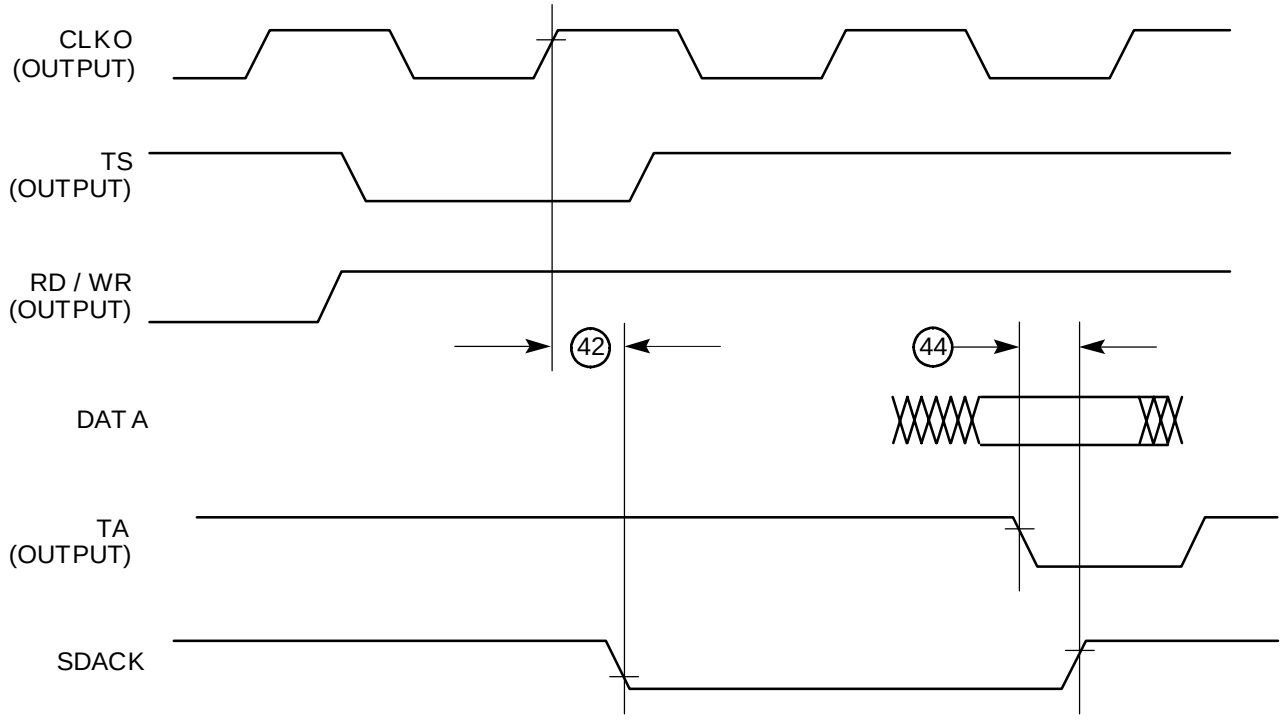


Figure 54. SI Receive Timing Diagram With Normal Clocking (DSC = 0)

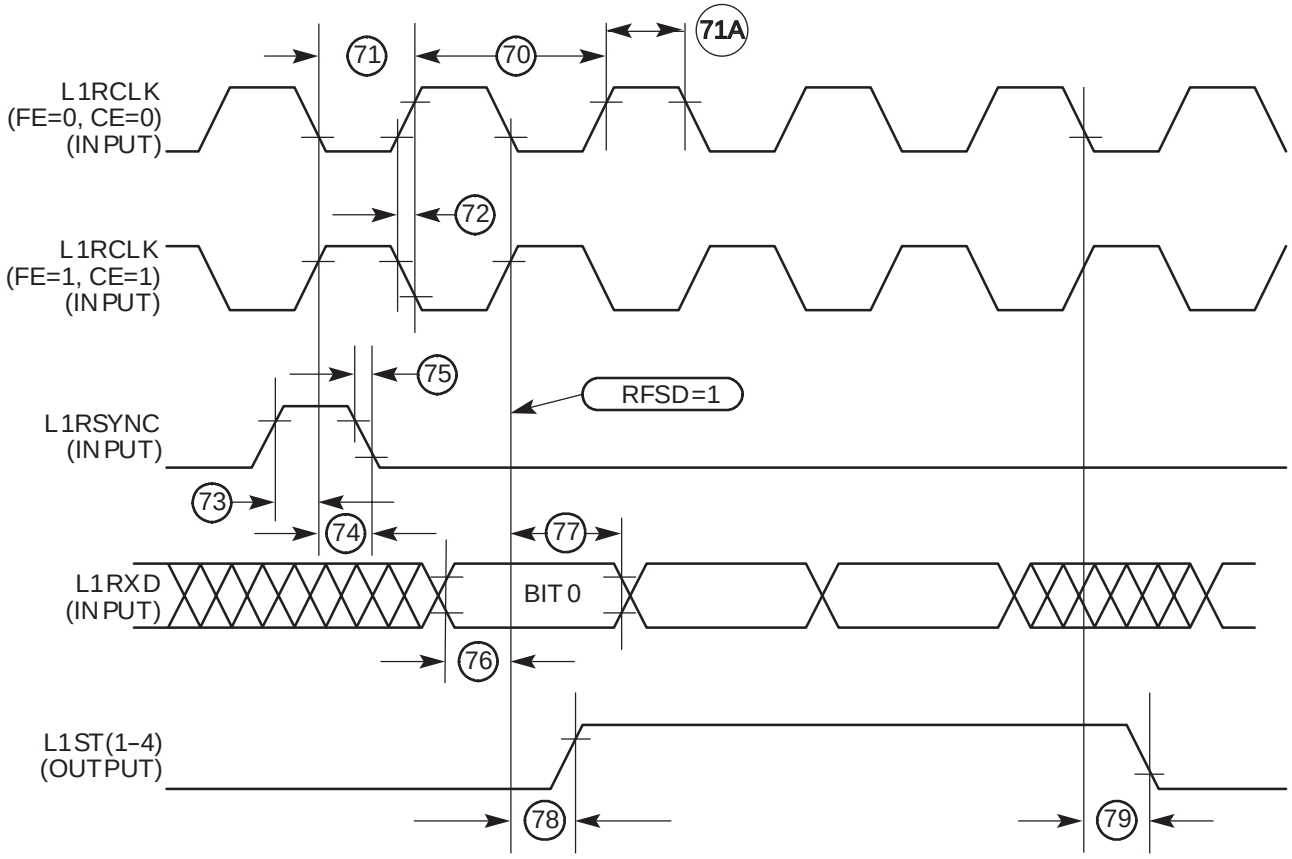


Figure 55. SI Receive Timing with Double-Speed Clocking (DSC = 1)

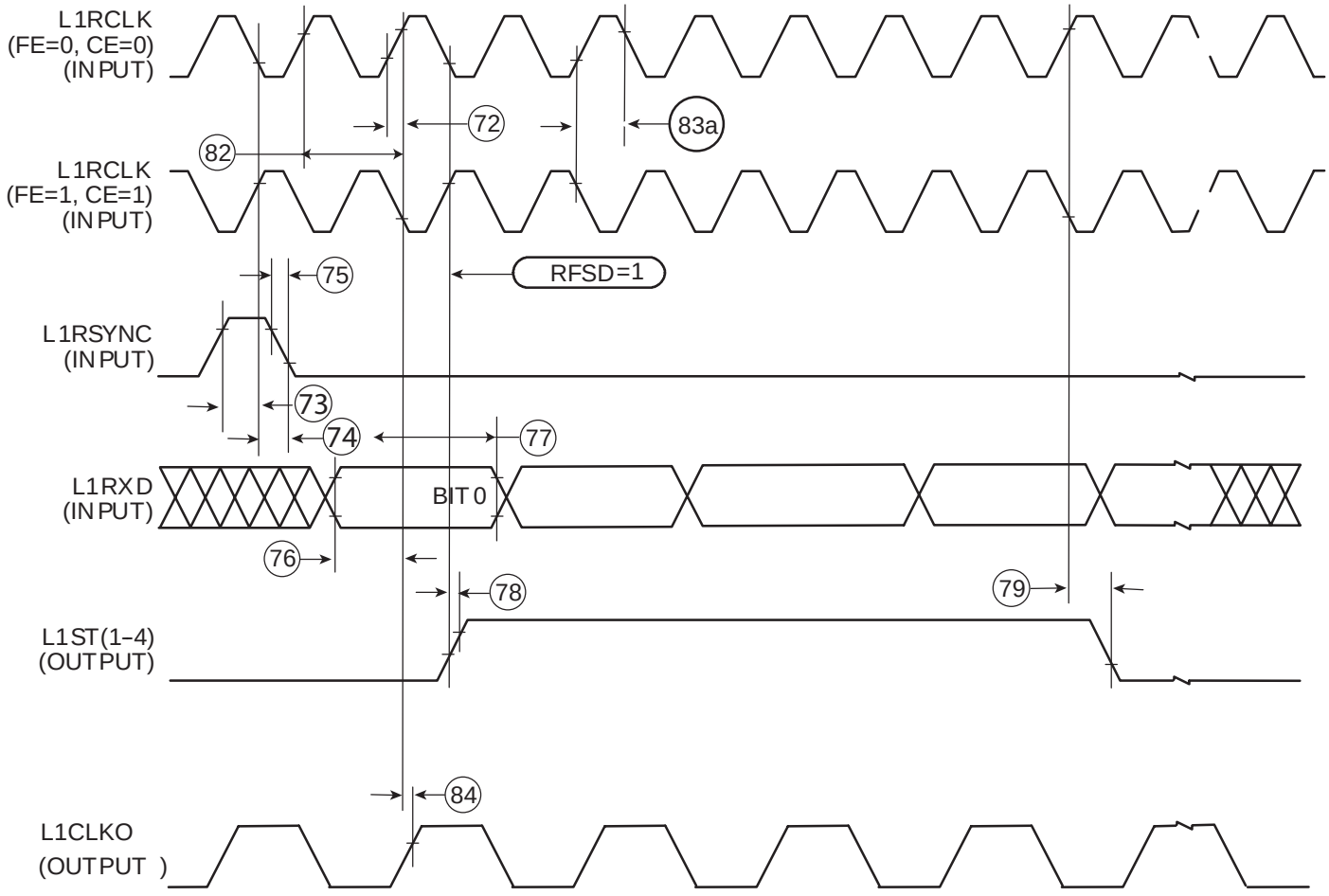
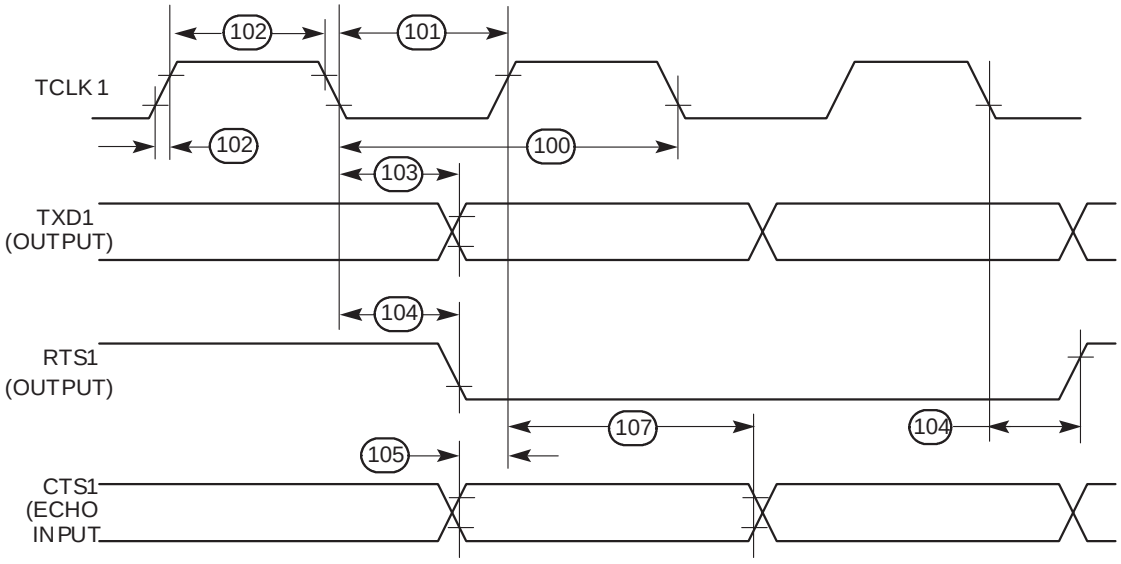


Figure 61. HDLC Bus Timing Diagram



Ethernet Electrical Specifications

Num	Characteristic	All Frequencies		Unit
		Min	Max	
120	CLSN Width High	40	–	ns
121	RCLK1 Rise/Fall Time	–	15	ns
122	RCLK1 Width Low	40	–	ns
123	RCLK1 Clock Period(1)	80	120	ns
124	RXD1 Setup Time	20	–	ns
125	RXD1 Hold Time	5	–	ns
126	RENA Active Delay (From RCLK1 Rising Edge of the Last Data Bit)	10	–	ns
127	RENA Width Low	100	–	ns
128	TCLK1 Rise/Fall Time	–	15	ns
129	TCLK1 Width Low	40	–	ns
130	TCLK1 Clock Period(1)	99	101	ns
131	TXD1 Active Delay (From TCLK1 Rising Edge)	10	50	ns
132	TXD1 Inactive Delay (From TCLK1 Rising Edge)	10	50	ns
133	TENA Active Delay (From TCLK1 Rising Edge)	10	50	ns
134	TENA Inactive Delay (From TCLK1 Rising Edge)	10	50	ns
135	$\overline{\text{RSTRT}}$ Active Delay (From TCLK1 Falling Edge)	10	50	ns
136	$\overline{\text{RSTRT}}$ Inactive Delay (From TCLK1 Falling Edge)	10	50	ns
137	$\overline{\text{REJECT}}$ Width Low	1	–	CLK
138	CLKO1 Low to $\overline{\text{SDACK}}$ Asserted(2)	–	20	ns
139	CLKO1 Low to $\overline{\text{SDACK}}$ Negated(2)	–	20	ns

Notes: 1. The ratio SyncCLK/RCLK1 and SyncCLK/TCLK1 must be greater or equal to 2/1
2. $\overline{\text{SDACK}}$ is asserted whenever the SDMA writes the incoming frame DA into memory.

Preparation For Delivery

Packaging

Microcircuits are prepared for delivery in accordance with MIL-PRF-38535.

Certificate of Compliance

Atmel offers a certificate of compliances with each shipment of parts, affirming the products are in compliance either with MIL-STD-883 and guarantying the parameters not tested at temperature extremes for the entire temperature range.

Power Consideration

The average chip-junction temperature, Tj, in °C can be obtained from the equation:

$$Tj = T_A + (P_D \cdot \Theta_{JA}) \quad (1)$$

where

T_A = Ambient temperature, °C

Θ_{JA} = Package thermal resistance, junction to ambient, °C/W

$P_D = P_{INT} + P_{I/O}$

$P_{INT} = I_{DD} \times V_{DD}$, watts – chip internal power

$P_{I/O}$ = Power dissipation on input and output pins – user determined

For most applications $P_{I/O} < 0.3 \cdot P_{INT}$ and can be neglected. If $P_{I/O}$ is neglected, an approximate relationship between P_D and T_J is:

$$P_D = K \div (T_J + 273°C) \quad (2)$$

Solving equations (1) and (2) for K gives:

$$K = P_D \cdot T\ (T_A + 273°C) + \Theta_{JA} \cdot P_D^2 \quad (3)$$

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

Layout Practices

Each V_{CC} pin on the TSPC860 should be provided with a low-impedance path to the board's supply. Each GND pin should likewise be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on chip. The V_{CC} power supply should be bypassed to ground using at least four 0.1 µF bypass capacitors located as close as possible to the four sides of the package. The capacitor leads and associated printed circuit traces connecting to chip V_{CC} and GND should be kept to less than half an inch per capacitor lead. A four-layer board is recommended, employing two inner layers as V_{CC} and GND planes.

All output pins on the TSPC860 have fast rise and fall times. Printed circuit (PC) trace interconnection length should be minimized in order to minimize undershoot and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data busses. Maximum PC trace lengths of six inches are recommended. Capacitance calculations should consider all device loads as well as parasitic capacitances due to the PC traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient current in the V_{CC} and GND circuits. Pull up all unused inputs or signals that will be inputs during reset. Special care should be taken to minimize the noise levels on the PLL supply pins.

Software Compatibility Issues

The following list summarizes the major software differences between the TS68EN360 QUICC and the TSPC860 PowerQUICC:

- Since the TSPC860 PowerQUICC uses an Embedded PowerPC Core, code written for the TS68EN360 must be recompiled for the PowerPC instruction set. Code which accesses the TS68EN360 peripherals requires only minor modifications for use with the TSPC860. Although the functions performed by the PowerQUICC SIU are similar to those performed by the QUICC SIM, the initialization sequence for the SIU is different and therefore code that accesses the SIU must be rewritten. Many developers of 68K compilers now provide compilers which also support the PowerPC architecture.
- The addition of the MAC function to the TSPC860 CPM block to support the needs of higher performance communication software is the only major difference between the CPM on the TS68EN360 and that on the TSPC860. Therefore the registers used to initialize the QUICC CPM are similar to the TSPC860 CPM, but there are some minor changes necessary for supporting the MAC function.
- When porting code from the TS68EN360 CPM to the TSPC860 CPM, the software writer will find new options for hardware breakpoint on CPU commands, address, and serial request which are useful for software debugging. Support for single step operation with all the registers of the CPM visible makes software development for the CPM on the TSPC860 processor even simpler.

TSPC860 PowerQUICC Glueless System Design

A fundamental design goal of the TSPC860 PowerQUICC was ease of interface to other system components. Figure 72 on page 80 shows a system configuration that offers one EPROM, one flash EPROM, and supports two DRAM SIMMs. Depending on the capacitance on the system bus, external buffers may be required. From a logic standpoint, however, a glueless system is maintained.

Figure 73. TSPC860 System Configuration