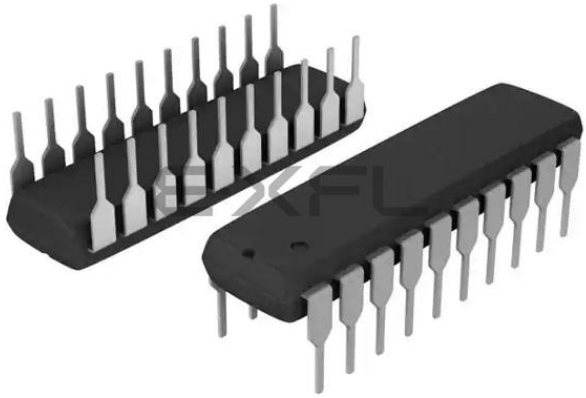

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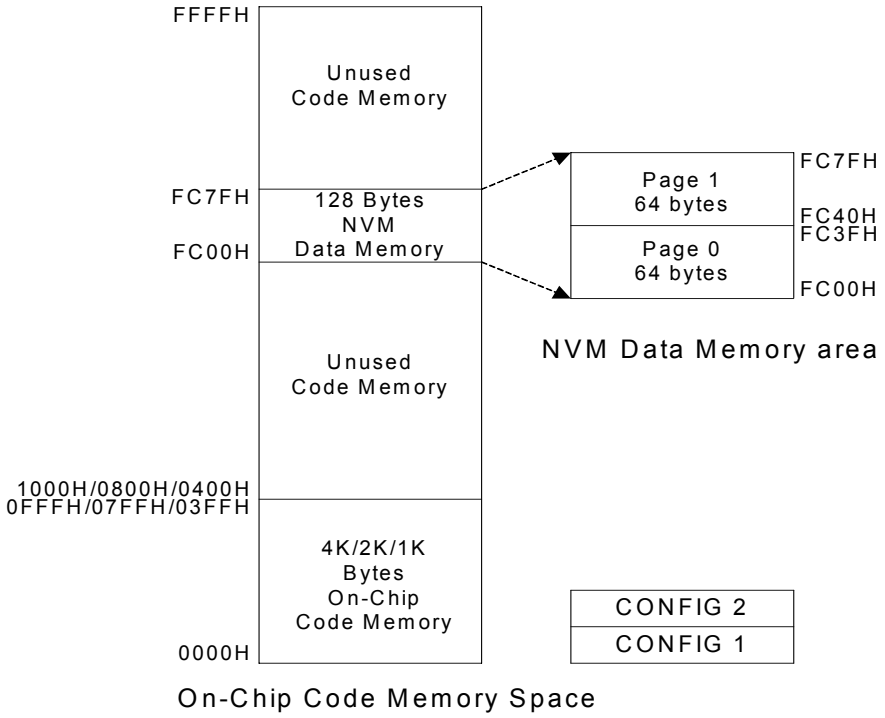
Applications of "Embedded - Microcontrollers"

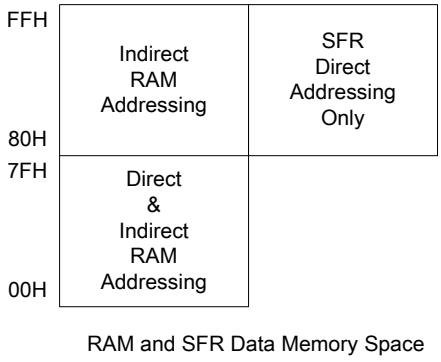
Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, UART/USART
Peripherals	Brown-out Detect/Reset, LED, LVD, POR, PWM, WDT
Number of I/O	18
Program Memory Size	1KB (1K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	20-DIP (0.300", 7.62mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/w79e821adg



W79E823/W79E822/W79E821 Memory Map

Register Map

As mentioned before the W79E82X series have separate Program and Data Memory areas. The on-chip **256/128** bytes scratch pad RAM is in addition to the external memory. There are also several Special Function Registers (SFRs) which can be accessed by software. The SFRs can be accessed only by direct addressing, while the on-chip RAM can be accessed by either direct or indirect addressing.



W79E825/W79E824 RAM and SFR Memory Map

Continued.

BIT	NAME	FUNCTION
3	IE1	Interrupt 1 Edge Detect: Set by hardware when an edge/level is detected on $\overline{INT1}$. This bit is cleared by hardware when the service routine is vectored to only if the interrupt was edge triggered. Otherwise it follows the pin.
2	IT1	Interrupt 1 type control: Set/cleared by software to specify falling edge/ low level triggered external inputs.
1	IE0	Interrupt 0 Edge Detect: Set by hardware when an edge/level is detected on $\overline{INT0}$. This bit is cleared by hardware when the service routine is vectored to only if the interrupt was edge triggered. Otherwise it follows the pin.
0	IT0	Interrupt 0 type control: Set/cleared by software to specify falling edge/ low level triggered external inputs.

TIMER MODE CONTROL

Bit:	7	6	5	4	3	2	1	0
	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0

Mnemonic: TMOD Address: 89h

BIT	NAME	FUNCTION
7	GATE	Gating control: When this bit is set, Timer/counter 1 is enabled only while $\overline{INT1}$ pin is high and TR1 control bit is set. When cleared, Timer 1 is enabled whenever TR1 control bit is set.
6	C/$\overline{T}$	Timer or Counter Select: When cleared, the timer is incremented by internal clocks. When set, the timer counts high-to-low edges of the T1 pin.
5	M1	Timer1 Mode Select bit1: See table below.
4	M0	Timer1 Mode Select bit0: See table below.
3	GATE	Gating control: When this bit is set, Timer/counter 0 is enabled only while $\overline{INT0}$ pin is high and TR0 control bit is set. When cleared, Timer 0 is enabled whenever TR0 control bit is set.
2	C/$\overline{T}$	Timer or Counter Select: When cleared, the timer is incremented by internal clocks. When set, the timer counts high-to-low edges of the T0 pin.
1	M1	Timer0 Mode Select bit1: See table below.
0	M0	Timer0 Mode Select bit0: See table below.

BIT	NAME	FUNCTION
7	SM0/FE	Serial port mode select bit 0 or Framing Error Flag: The SMOD0 bit in PCON SFR determines whether this bit acts as SM0 or as FE. The operation of SM0 is described below. When used as FE, this bit will be set to indicate an invalid stop bit. This bit must be manually cleared in software to clear the FE condition.
6	SM1	Serial port Mode bit 1: **Mode: SM0 SM1 Description Length Baud rate** 0 0 0 Synchronous 8 4/12 Tclk 1 0 1 Asynchronous 10 Variable 2 1 0 Asynchronous 11 64/32 Tclk 3 1 1 Asynchronous 11 Variable
5	SM2	Multiple processors communication. Setting this bit to 1 enables the multiprocessor communication feature in mode 2 and 3. In mode 2 or 3, if SM2 is set to 1, then RI will not be activated if the received 9th data bit (RB8) is 0. In mode 1, if SM2 = 1, then RI will not be activated if a valid stop bit was not received. In mode 0, the SM2 bit controls the serial port clock. If set to 0, then the serial port runs at a divide by 12 clock of the oscillator. This gives compatibility with the standard 8052. When set to 1, the serial clock become divide by 4 of the oscillator clock. This results in faster synchronous serial communication.
4	REN	Receive enable: When set to 1 serial reception is enabled, otherwise reception is disabled.
3	TB8	This is the 9th bit to be transmitted in modes 2 and 3. This bit is set and cleared by software as desired.
2	RB8	In modes 2 and 3 this is the received 9th data bit. In mode 1, if SM2 = 0, RB8 is the stop bit that was received. In mode 0 it has no function.
1	TI	Transmit interrupt flag: This flag is set by hardware at the end of the 8th bit time in mode 0, or at the beginning of the stop bit in all other modes during serial transmission. This bit must be cleared by software.
0	RI	Receive interrupt flag: This flag is set by hardware at the end of the 8th bit time in mode 0, or halfway through the stop bits time in the other modes during serial reception. However the restrictions of SM2 apply to this bit. This bit can be cleared only by software.

SERIAL DATA BUFFER

Bit:	7	6	5	4	3	2	1	0
	SBUF.7	SBUF.6	SBUF.5	SBUF.4	SBUF.3	SBUF.2	SBUF.1	SBUF.0

Mnemonic: SBUF Address: 99h

BIT	NAME	FUNCTION
7~0	SBUF	Serial data on the serial port is read from or written to this location. It actually consists of two separate internal 8-bit registers. One is the receive resister, and the other is the transmit buffer. Any read access gets data from the receive data buffer, while write access is to the transmit data buffer.

PORT 2

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	P2.1	P2.0

Mnemonic: P2 Address: A0h

BIT	NAME	FUNCTION
7~2	-	Reserved
1	P2.1	XTAL2 or CLKOUT pin by alternative.
0	P2.0	XTAL1 clock input pin.

Keyboard Interrupt

Bit:	7	6	5	4	3	2	1	0
	KBI.7	KBI.6	KBI.5	KBI.4	KBI.3	KBI.2	KBI.1	KBI.0

Mnemonic: KBI Address: A1h

Keyboard interrupt enable.

BIT	NAME	FUNCTION
7	KBI.7	1: Enable P0.7 as a cause of a Keyboard interrupt.
6	KBI.6	1: Enable P0.6 as a cause of a Keyboard interrupt.
5	KBI.5	1: Enable P0.5 as a cause of a Keyboard interrupt.
4	KBI.4	1: Enable P0.4 as a cause of a Keyboard interrupt.
3	KBI.3	1: Enable P0.3 as a cause of a Keyboard interrupt.
2	KBI.2	1: Enable P0.2 as a cause of a Keyboard interrupt.
1	KBI.1	1: Enable P0.1 as a cause of a Keyboard interrupt.
0	KBI.0	1: Enable P0.0 as a cause of a Keyboard interrupt.

AUX Function Register 1

Bit:	7	6	5	4	3	2	1	0
	KBF	BOD	BOI	LPBOV	SRST	ADCEN	0	DPS

Mnemonic: AUXR1 Address: A2h

BIT	NAME	FUNCTION
7	KBF	Keyboard Interrupt Flag: 1: When any pin of port 0 that is enabled for the Keyboard Interrupt function goes low. Must be cleared by software.
6	BOD	Brown Out Disable: 0: Enable Brownout Detect function. 1: Disable Brownout Detect function and save power.

Continued.

BIT	NAME	FUNCTION
5	BOI	Brown Out Interrupt: 0: Disable Brownout Detect Interrupt function and it will cause chip reset when BOF is set. 1: This prevents Brownout Detection from causing a chip reset and allows the Brownout Detect function to be used as an interrupt.
4	LPBOV	Low Power Brown Out Detect control: 0: When BOD is enable, the Brown Out detect is always turned on by normal run or Power Down mode. 1: When BOD is enable, the 1/16 time will be turned on Brown Out detect circuit by Power Down mode. When uC is in Power Down mode, the BOD will enable internal RC OSC(2MHz~0.5MHZ)
3	SRST	Software reset: 1: reset the chip as if a hardware reset occurred.
2	ADCEN	0: Disable ADC circuit. 1: Enable ADC circuit.
1	0	Reserved
0	DPS	Dual Data Pointer Select 0: To select DPTR of standard 8051. 1: To select DPTR1

INTERRUPT ENABLE

Bit:	7	6	5	4	3	2	1	0
	EA	EADC	EBO	ES	ET1	EX1	ET0	EX0

Mnemonic: IE Address: A8h

BIT	NAME	FUNCTION
7	EA	Global enable. Enable/Disable all interrupts.
6	EADC	Enable ADC interrupt.
5	EBO	Enable Brown Out interrupt.
4	ES	Enable Serial Port interrupt.
3	ET1	Enable Timer 1 interrupt.
2	EX1	Enable external interrupt 1.
1	ET0	Enable Timer 0 interrupt.
0	EX0	Enable external interrupt 0.

SLAVE ADDRESS

Bit:	7	6	5	4	3	2	1	0
	SADDR.7	SADDR.6	SADDR.5	SADDR.4	SADDR.3	SADDR.2	SADDR.1	SADDR.0

Mnemonic: SADDR Address: A9h

Port 1 Output Mode 2

Bit:	7	6	5	4	3	2	1	0
	P1M2.7	P1M2.6	-	P1M2.4	-	-	P1M2.1	P1M2.0

Mnemonic: P1M2 Address: B4h

Port 2 Output Mode 1

Bit:	7	6	5	4	3	2	1	0
	P2S	P1S	P0S	ENCLK	T1OE	T0OE	P2M1.1	P2M1.0

Mnemonic: P2M1 Address: B5h

BIT	NAME	FUNCTION
7	P2S	1: Enables Schmitt trigger inputs on Port 2.
6	P1S	1: Enables Schmitt trigger inputs on Port 1.
5	P0S	1: Enables Schmitt trigger inputs on Port 0.
4	ENCLK	1: To use the on-chip RC oscillator, a clock output is enabled on the XTAL2 pin (P2.0).
3	T1OE	1: The P0.7 pin is toggled whenever Timer 1 overflows. The output frequency is therefore one half of the Timer 1 overflow rate.
2	T0OE	1: The P1.2 pin is toggled whenever Timer 1 overflows. The output frequency is therefore one half of the Timer 1 overflow rate.
1	P2M1.1	To control the output configuration of P2.1.
0	P2M1.0	To control the output configuration of P2.0.

Port 2 Output Mode 2

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	P2M2.1	P2M2.0

Mnemonic: P2M2 Address: B6h

Port Output Configuration Settings:

PXM1.Y	PXM2.Y	PORT INPUT/OUTPUT MODE
0	0	Quasi-bidirectional
0	1	Push-Pull
1	0	Input Only (High Impedance) P2M1.PxS=0, TTL input P2M1.PxS=1, Schmitt input
1	1	Open Drain

Interrupt High Priority

Bit:	7	6	5	4	3	2	1	0
	-	PADCH	PBOH	PSH	PT1H	PX1H	PT0H	PX0H

Mnemonic: IP0H Address: B7h

BIT	NAME	FUNCTION
7	ADC.1	The ADC conversion result.
6	ADC.0	The ADC conversion result.
5	ADCEX	Enable STADC-triggered conversion 0: Conversion can only be started by software (i.e., by setting ADCS). 1: Conversion can be started by software or by a rising edge on STADC (pin P1.4).
4	ADCI	ADC Interrupt flag: This flag is set when the result of an A/D conversion is ready. This generates an ADC interrupt, if it is enabled. The flag may be cleared by the ISR. While this flag is 1, the ADC cannot start a new conversion. ADCI can not be set by software.
3	ADCS	ADC Start and Status: Set this bit to start an A/D conversion. It may also be set by STADC if ADCEX is 1. This signal remains high while the ADC is busy and is reset right after ADCI is set. ADCS can not be reset by software, and the ADC cannot start a new conversion while ADCS is high. **ADCI / ADCS / ADC Status** 0 / 0 / ADC not busy; a conversion can be started 0 / 1 / ADC busy; start of a new conversion is blocked 1 / 0 / Conversion completed; start of a new conversion requires ADCI=0 1 / 1 / Conversion completed; start of a new conversion requires ADCI=0 It is recommended to clear ADCI ***before*** ADCS is set. However, if ADCI is cleared and ADCS is set at the same time, a new A/D conversion may start on the same channel.
2	RCCLK	0: The CPU clock is used as ADC clock. 1: The internal RC clock is used as ADC clock.
1	AADR1	The ADC input select. See table below.
0	AADR0	The ADC input select. See table below.

AADR1, AADR0: ADC Analog Input Channel select bits:

These bits can only be changed when ADCI and ADCS are both zero.

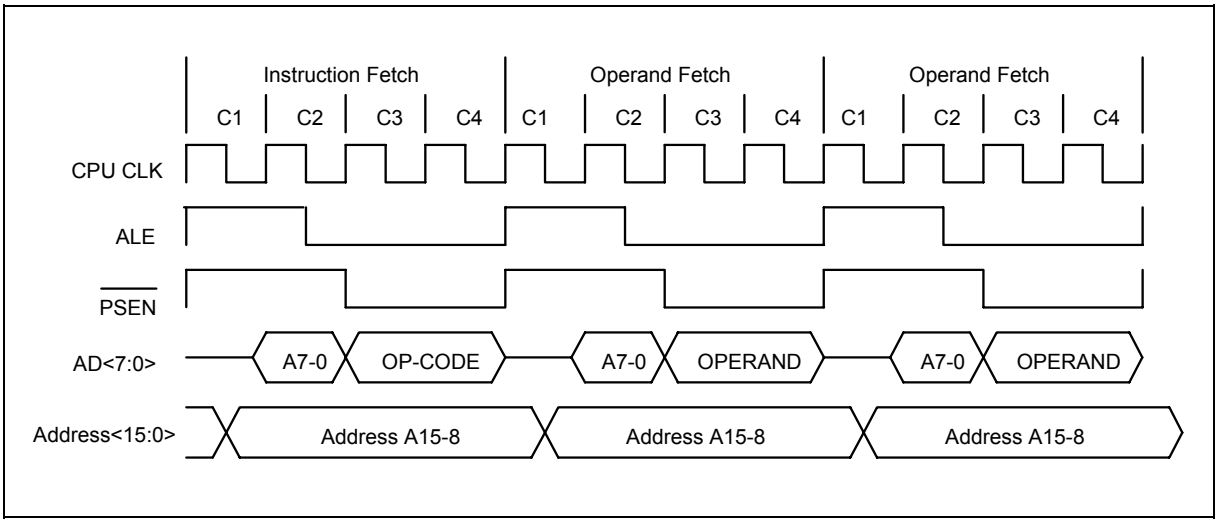
AADR1	AADR0	SELECTED ANALOG INPUT CHANNEL
0	0	AD0 (P0.3)
0	1	AD1 (P0.4)
1	0	AD2 (P0.5)
1	1	AD3 (P0.6)

ADC CONVERTER RESULT REGISTER

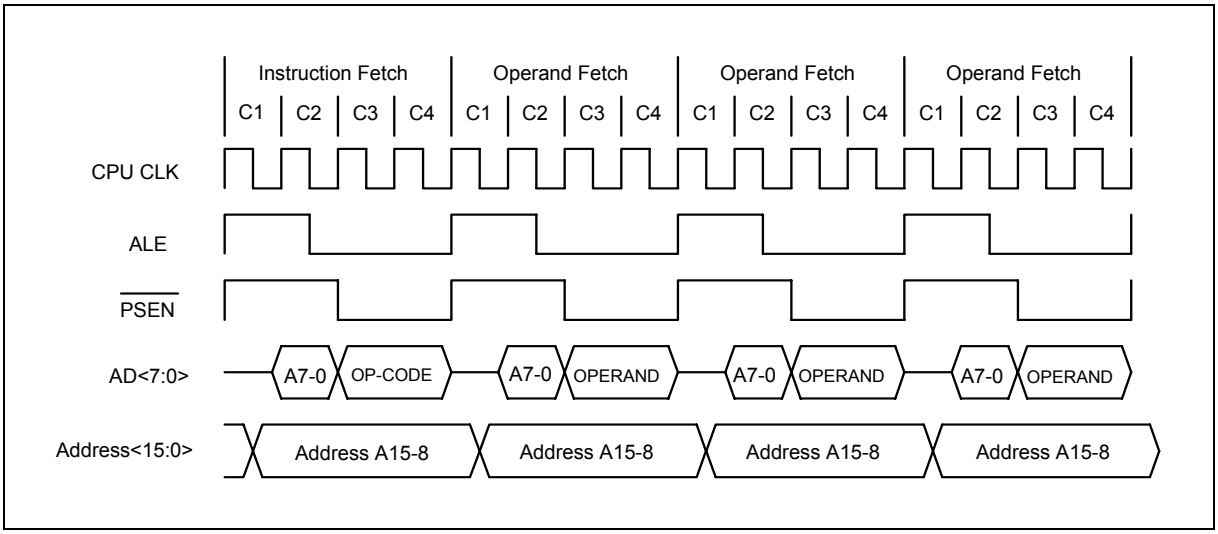
Bit:	7	6	5	4	3	2	1	0
	ADC.9	ADC.8	ADC.7	ADC.6	ADC.5	ADC.4	ADC.3	ADC.2

Mnemonic: ADCH Address: E2h

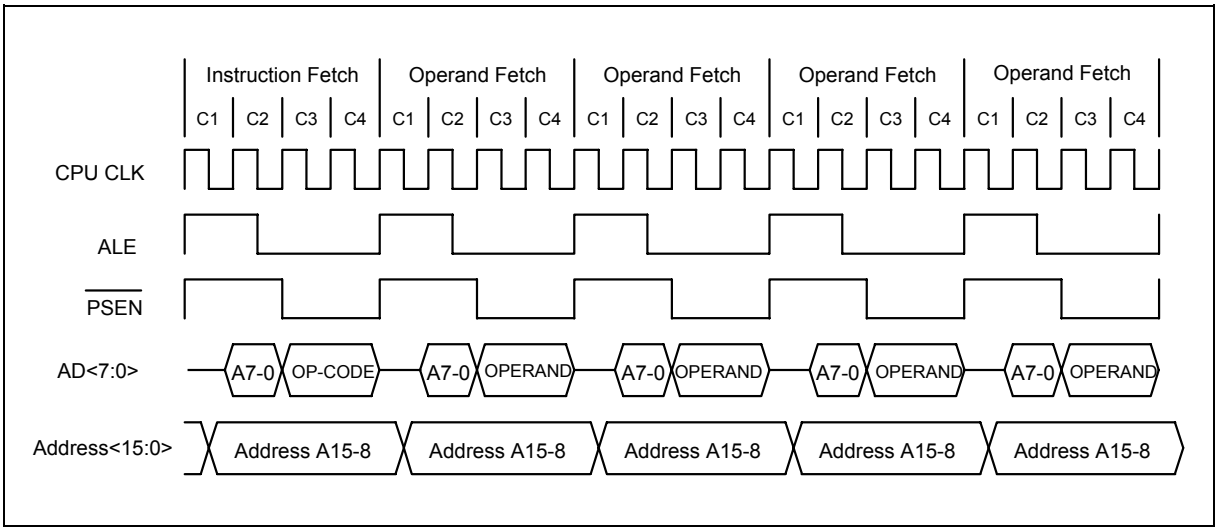
BIT	NAME	FUNCTION
7~0	ADC.9 ~ADC.2	The ADC conversion result.



Three Cycle Instruction Timing



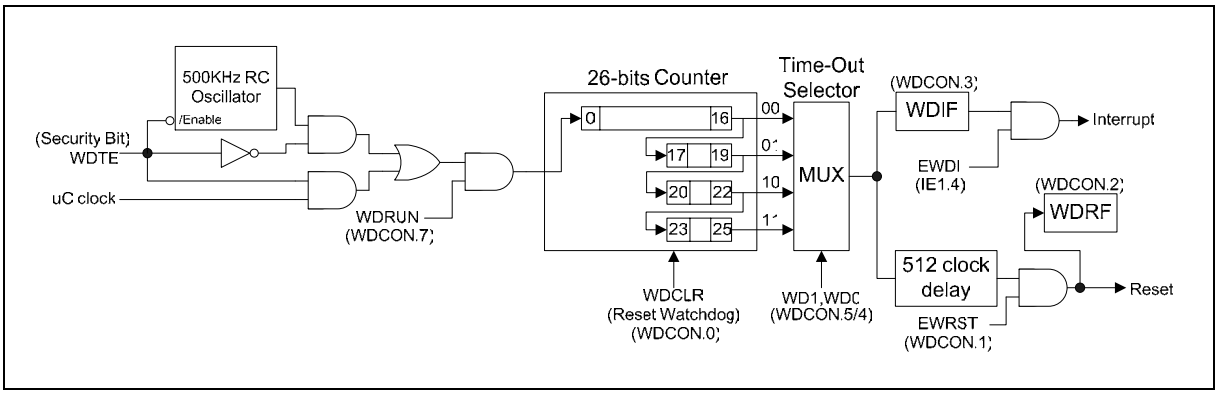
Four Cycle Instruction Timing



Five Cycle Instruction Timing

15. WATCHDOG TIMER

The Watchdog Timer is a free-running Timer which can be programmed by the user to serve as a system monitor, a time-base generator or an event timer. It is basically a set of dividers that divide the system clock. The divider output is selectable and determines the time-out interval. When the time-out occurs a flag is set, which can cause an interrupt if enabled, and a system reset can also be caused if it is enabled. The interrupt will occur if the individual interrupt enable and the global enable are set. The interrupt and reset functions are independent of each other and may be used separately or together depending on the users software.



Watchdog Timer

The Watchdog Timer should first be restarted by using WDCLR. This ensures that the timer starts from a known state. The WDCLR bit is used to restart the Watchdog Timer. This bit is self clearing, i.e. after writing a 1 to this bit the software will automatically clear it. The Watchdog Timer will now count clock cycles. The time-out interval is selected by the two bits WD1 and WD0 (WDCON.5 and WDCON.4). When the selected time-out occurs, the Watchdog interrupt flag WDIF (WDCON.3) is set. After the time-out has occurred, the Watchdog Timer waits for an additional 512 clock cycles. If the Watchdog Reset EWRST (WDCON.1) is enabled, then 512 clocks after the time-out, if there is no WDCLR, a system reset due to Watchdog Timer will occur. This will last for two machine cycles, and the Watchdog Timer reset flag WDRF (WDCON.2) will be set. This indicates to the software that the Watchdog was the cause of the reset.

When used as a simple timer, the reset and interrupt functions are disabled. The timer will set the WDIF flag each time the timer completes the selected time interval. The WDIF flag is polled to detect a time-out and the WDCLR allows software to restart the timer. The Watchdog Timer can also be used as a very long timer. The interrupt feature is enabled in this case. Every time the time-out occurs an interrupt will occur if the global interrupt enable EA is set.

The main use of the Watchdog Timer is as a system monitor. This is important in real-time control applications. In case of some power glitches or electro-magnetic interference, the processor may begin to execute errant code. If this is left unchecked the entire system may crash. Using the watchdog timer interrupt during software development will allow the user to select ideal watchdog reset locations. The code is first written without the watchdog interrupt or reset. Then the Watchdog interrupt is enabled to identify code locations where interrupt occurs. The user can now insert instructions to reset the Watchdog Timer, which will allow the code to run without any Watchdog Timer

16. SERIAL PORT (UART)

Serial port in the W79E82X series is a full duplex port. The W79E82X series provide the user with additional features such as the Frame Error Detection and the Automatic Address Recognition. The serial ports are capable of synchronous as well as asynchronous communication. In Synchronous mode the W79E82X series generate the clock and operates in a half duplex mode. In the asynchronous mode, full duplex operation is available. This means that it can simultaneously transmit and receive data. The transmit register and the receive buffer are both addressed as SBUF Special Function Register. However any write to SBUF will be to the transmit register, while a read from SBUF will be from the receiver buffer register. The serial port can operate in four different modes as described below.

16.1 MODE 0

This mode provides synchronous communication with external devices. In this mode serial data is transmitted and received on the RXD line. TXD is used to transmit the shift clock. The TxD clock is provided by the W79E82X series whether the device is transmitting or receiving. This mode is therefore a half duplex mode of serial communication. In this mode, 8 bits are transmitted or received per frame. The LSB is Transmitted/Received first. The baud rate is fixed at 1/12 or 1/4 of the oscillator frequency. This Baud Rate is determined by the SM2 bit (SCON.5). When this bit is set to 0, then the serial port runs at 1/12 of the clock. When set to 1, the serial port runs at 1/4 of the clock. This additional facility of programmable baud rate in mode 0 is the only difference between the standard 8051 and the W79E82X series.

The functional block diagram is shown below. Data enters and leaves the Serial port on the RxD line. The TxD line is used to output the shift clock. The shift clock is used to shift data into and out of the W79E82X series and the device at the other end of the line. Any instruction that causes a write to SBUF will start the transmission. The shift clock will be activated and data will be shifted out on the RxD pin till all 8 bits are transmitted. If SM2 = 1, then the data on RxD will appear 1 clock period before the falling edge of shift clock on TxD. The clock on TxD then remains low for 2 clock periods, and then goes high again. If SM2 = 0, the data on RxD will appear 3 clock periods before the falling edge of shift clock on TxD. The clock on TxD then remains low for 6 clock periods, and then goes high again. This ensures that at the receiving end the data on RxD line can either be clocked on the rising edge of the shift clock on TxD or latched when the TxD clock is low.

If the first bit detected after the falling edge of RxD pin, is not 0, then this indicates an invalid start bit, and the reception is immediately aborted. The serial port again looks for a falling edge in the RxD line. If a valid start bit is detected, then the rest of the bits are also detected and shifted into the SBUF. After shifting in 9 data bits, there is one more shift to do, after which the SBUF and RB8 are loaded and RI is set. However certain conditions must be met before the loading and setting of RI can be done.

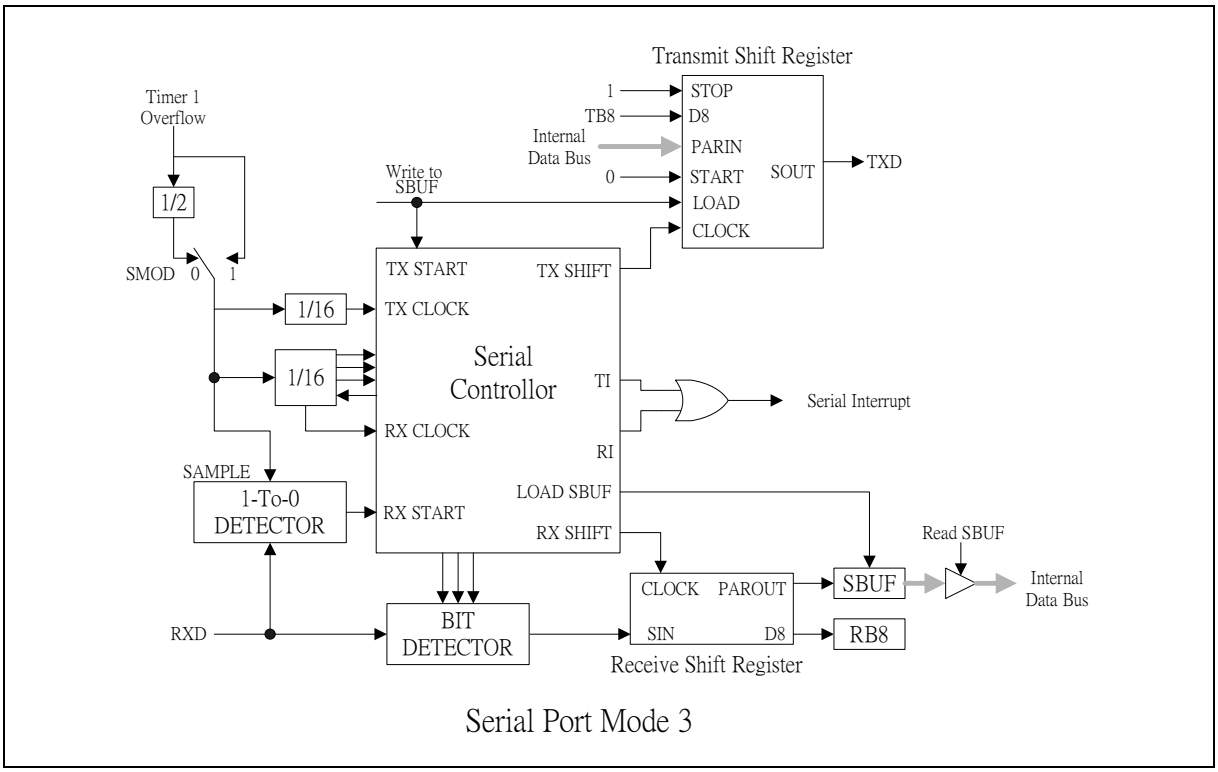
1. RI must be 0 and

2. Either SM2 = 0, or the received stop bit = 1.

If these conditions are met, then the stop bit goes to RB8, the 8 data bits go into SBUF and RI is set. Otherwise the received frame may be lost. After the middle of the stop bit, the receiver goes back to looking for a 1-to-0 transition on the RxD pin.

16.4 MODE 3

This mode is similar to Mode 2 in all respects, except that the baud rate is programmable. The user must first initialize the Serial related SFR SCON before any communication can take place. This involves selection of the Mode and baud rate. The Timer 1 should also be initialized if modes 1 and 3 are used. In all four modes, transmission is started by any instruction that uses SBUF as a destination register. Reception is initiated in Mode 0 by the condition RI = 0 and REN = 1. This will generate a clock on the TxD pin and shift in 8 bits on the RxD pin. Reception is initiated in the other modes by the incoming start bit if REN = 1. The external device will start the communication by transmitting the start bit.



Serial Port Mode 3

20. I/O PORT CONFIGURATION

The W79E82X series have three I/O ports, port 0, port 1 and port 2. All pins of I/O ports can be configured to one of four types by software except P1.5 is only input pin. When P1.5 is configured reset pin by RPD=0 in the CONFIG 1 register, the W79E82X series can support 15 pins by use Crystal. If used on-chip RC oscillator the P1.5 is configured input pin, the W79E82X series can be supported up to 18 pins. The I/O ports configuration setting as below table.

I/O port configuration table

PXM1.Y	PXM2.Y	PORT INPUT/OUTPUT MODE
0	0	Quasi-bidirectional
0	1	Push-Pull
1	0	Input Only (High Impedance) P2M1.PxS=0, TTL input P2M1.PxS=1, Schmitt input
1	1	Open Drain

All port pins can be determined to high or low after reset by configure PRHI bit in the CONFIG1 register. After reset, these pins are in quasi-bidirectional mode. The port pin of P1.5 only is a Schmitt trigger input.

Enabled toggle outputs from Timer 0 and Timer 1 by ENT0 and ENT1 on P2M1 register, the output frequency of Timer 0 or Timer 1 is by Timer overflow.

Each I/O port of the W79E82X series may be selected to use TTL level inputs or Schmitt inputs by P(n)S bit on P2M1 register, where n is 0, 1 or 2. When P(n)S is set to 1, Ports are selected Schmitt trigger inputs on Port(n). The P2.0(XTAL2) can be configured clock output when used on-chip RC or external Oscillator is clock source, and the frequency of clock output is divided by 4 on on-chip RC clock or external Oscillator.

20.1 Quasi-Bidirectional Output Configuration

After chip was power on or reset, the all ports output are this mode, and output is common with the 8051. This mode can be used as both an input and output without the need to reconfigure the port.

When the pin is pulled low, it is driven strongly and able to sink a fairly large current. These features are somewhat similar to an open drain output except that there are three pull-up transistors in the quasi-bidirectional output that serve different purposes.

This mode has three pull-up resisters that are “strong” pull-up, “weak” pull-up and “very weak” pull-up. The “strong” pull-up is used fast transition from logic “0” change to logic “1”, and it is fast latch and transition. When port pins is occur from logic “0” to logic “1”, the strong pull-up will quickly turn on two CPU clocks to pull high then turn off.

21.3 CPU Clock Rate select

The CPU clock of W79E82X series may be selected by the DIVM register. If DIVM = 00H, the CPU clock is running at 4 CPU clock pre machine cycle, and without any division from source clock (Fosc). When the DIVM register is set to N value, the CPU clock is divided by 2(DVIM+1), so CPU clock frequency division is from 4 to 512. The user may use this feature to set CPU at a lower speed rate for reducing power consumption. This is very similar to the situation when CPU has entered Idle mode. In addition this frequency division function affect all peripheral timings as they are all sourcing from the CPU clock(Fcpu).

22. POWER MONITORING FUNCTION

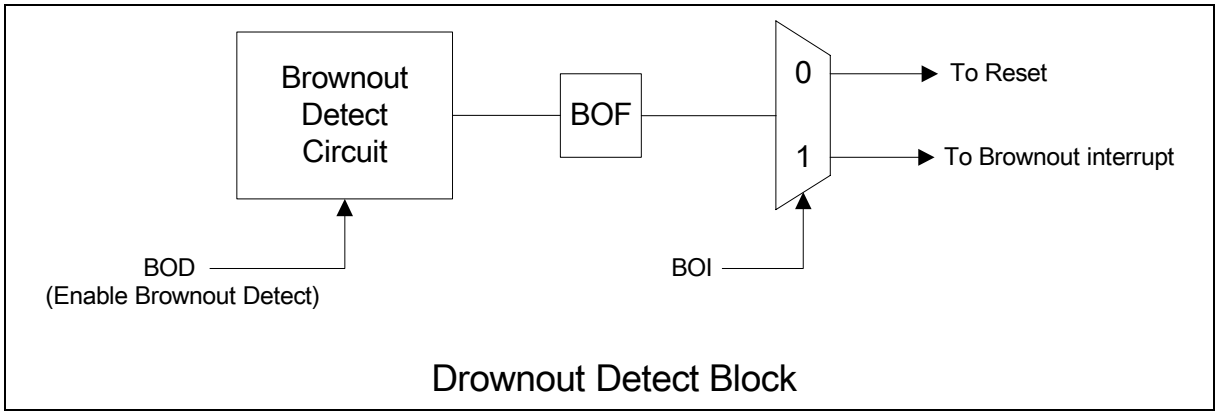
Power-On Detect and Brownout are two additional power monitoring functions implemented in W79E82X to prevent incorrect operation during power up and power drop or loss.

22.1 Power On Detect

The Power–On Detect function is a designed to detect power up after power voltage reaches to a level where Brownout Detect can work. After power on detect, the POR (PCON.4) will be set to “1” to indicate an initial power up condition. The POR flag will be cleared by software.

22.2 Brownout Detect

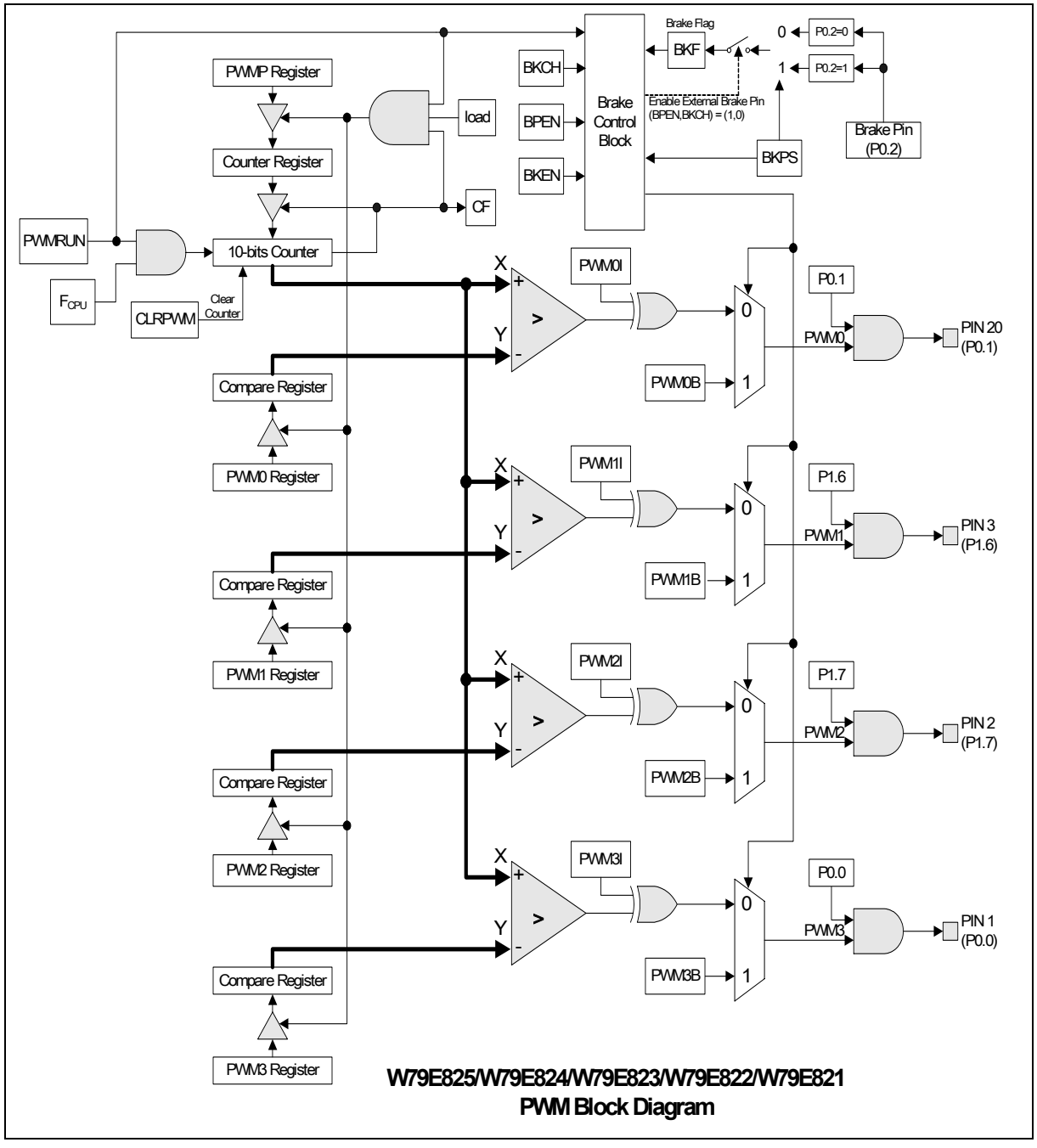
The Brownout Detect function is detect power voltage is drops to brownout voltage level, and allows preventing some process work or indicate power warming. The W79E82X series have two brownout voltage levels to select by BOV (CONFIG1.4). If BOV =0 that brownout voltage level is 3.8V, If BOV = 1 that brownout voltage level is 2.5V. When the Brownout voltage is drop to select level, the brownout detector will detect and keeps this active until VDD is returns to above brownout Detect voltage. The Brownout Detect block is as follow.



Drownout Detect Block

When Brownout Detect is enabled by BOD (AUXR1.6), the BOF (PCON.5) flag will be set that it cause brownout reset or interrupt, and BOF will be cleared by software. If BOI (AUXR1.5) is set to “1”, the brownout detect will cause interrupt via the EA (IE.7) and EBO (IE.5) bits is set.

In order to guarantee a correct detection of Brownout, The VDD fail time must be slower than 50mV/us, and rise time is slower than 2mV/us to ensure a proper reset.



W79E825/W79E824/W79E823/W79E822/W79E821
PWM Block Diagram

The all PWM control registers are PWMCON1, PWMCON2, and PWMCON3 register, and function description as below.

PWM Counter Low Bits Register PWMPL(D9H)

BIT	NAME	FUNCTION
7~0	PWMP.7 ~PWMP.0	PWM Counter low bit 7~0 register

PWM Counter High Bits Register PWMPH(D1H)

BIT	NAME	FUNCTION
7~2	-	Reserved
1~0	PWMP.9 ~PWMP.8	PWM Counter high bit 9~8 register

PWM 0 Low Bits Register PWM0L(DAH)

BIT	NAME	FUNCTION
7~0	PWM0.7 ~PWM0.0	PWM 0 low bit 7~0 register

PWM 1 Low Bits Register PWM1L(DBH)

BIT	NAME	FUNCTION
7~0	PWM1.7 ~PWM1.0	PWM 1 low bit 7~0 register

PWM 2 Low Bits Register PWM2L(DDH)

BIT	NAME	FUNCTION
7~0	PWM2.7 ~PWM2.0	PWM 2 low bit 7~0 register

PWM 3 Low Bits Register PWM3L(DEH)

BIT	NAME	FUNCTION
7~0	PWM3.7 ~PWM3.0	PWM3 low bit 7~0 register

PWM Control Register 3 PWMCON3(D7H)

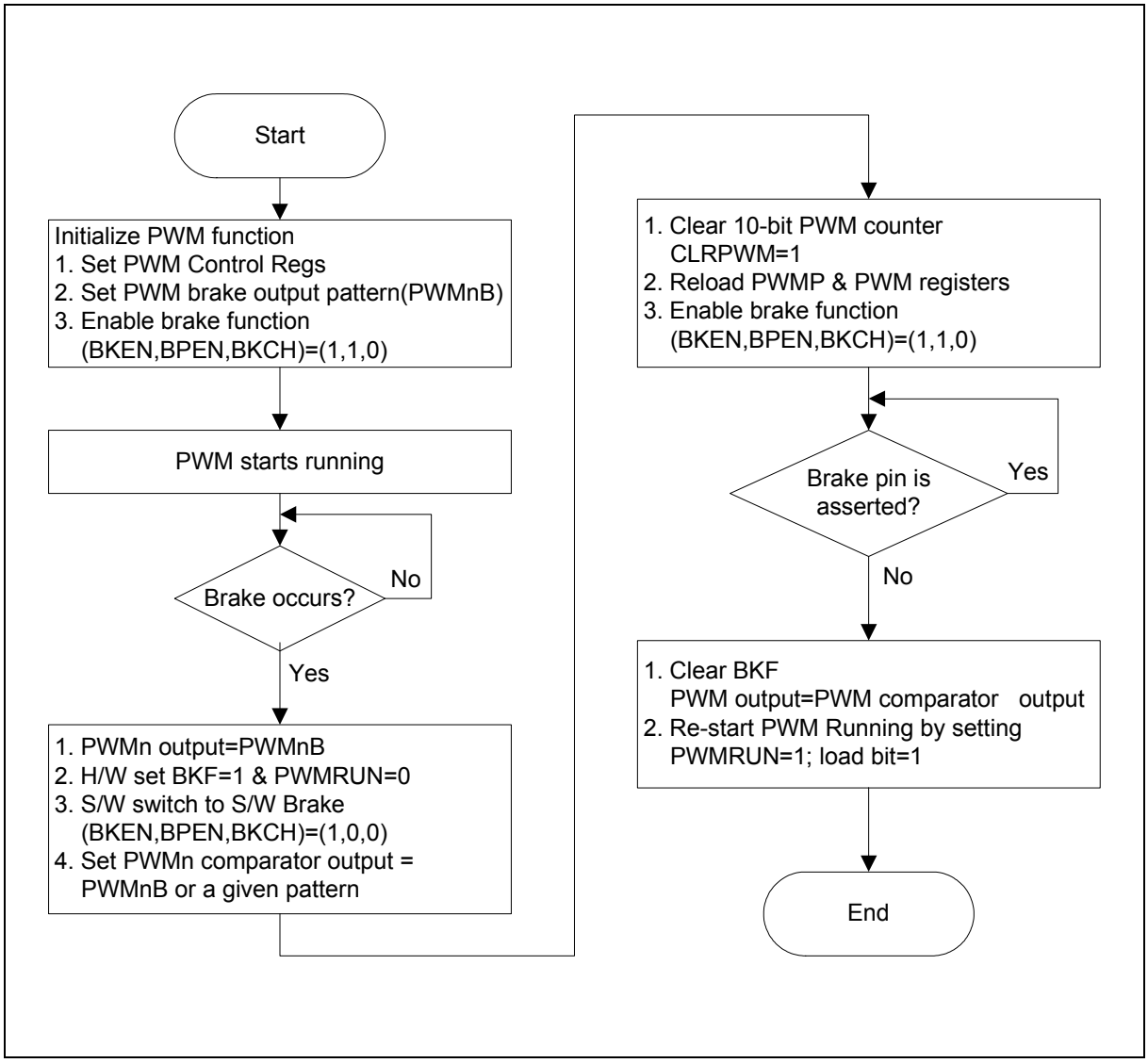
BIT	NAME	FUNCTION
7~1	-	Reserved
0	BKF	The external brake pin flag. 0: The PWM is not brake. 1: The PWM is brake by external brake pin. It will be cleared by software. If this bit is set, PWMRUN can't be set.

The W79E82X series chips have support brake function by software or external pin(P0.2). That brake control is by PWMCON2 register. The software brake and external pin brake setting as refer brake condition table. When brake is asserted, the PWM outputs are by PWMnB setting. By the software brake, the BKEN is set to "1" that will enable brake function and determined by BPEN and BKCH bits. The (BPEN, BKCH) = (0,0), brake is asserted. The (BPEN, BKCH) = (0,1), the PWM outputs are follow PWMRUN bit; When PWM is not running that mean is PWMRUN = 0, the PWM outputs are asserted by PWMnB setting; When PWM is running, the PWMRUN = 1, and keeping PWM outputs.

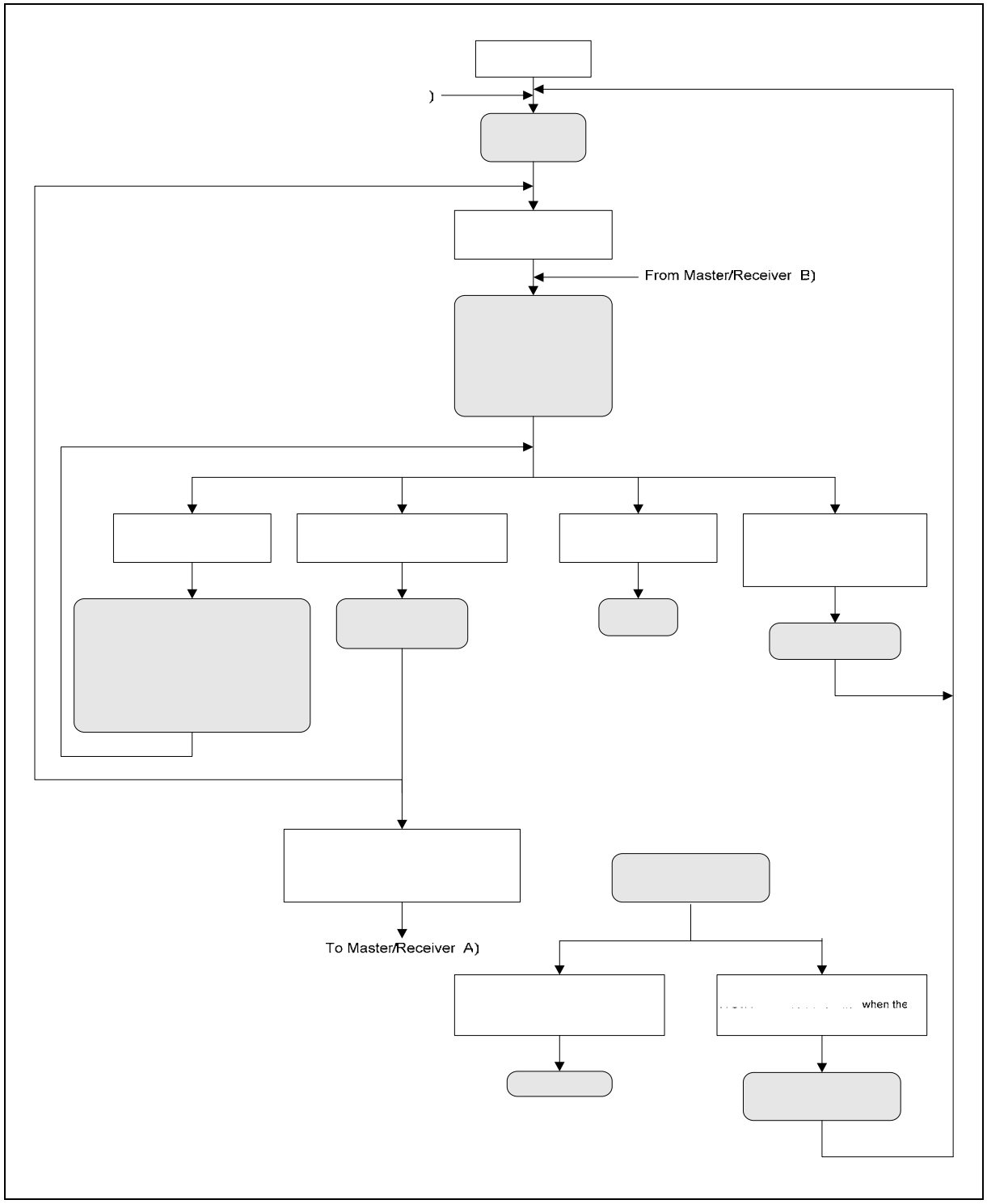
By the external brake pin(P0.2) brake, W79E82X series chips have brake interrupt service or polling brake flag (BKF) if external pin is asserted. If to decide P0.2 is low is asserted by BKPS = 0, the BKF(PWMCON3.0) will be set to "1" and PWNRUN will be cleared to stop PWM run, the PWM outputs condition are by PWMnB setting. After brake pin is release,

Since the Brake Pin being asserted will automatically clear the Run bit and BKF(PWMCON3.0) flag will be set, PWMCON1.7, the user program can poll this bit or enable PWM's brake interrupt to determine when the Brake Pin causes a brake to occur. The other method for detecting a brake caused by the Brake Pin would be to tie the Brake Pin to one of the external interrupt pins. This latter approach is needed if the Brake signal can be of insufficient length to ensure that it can be captured by a polling routine. When, after being asserted, the condition causing the brake is removed, the PWM outputs go to whatever state that had immediately prior to the brake. This means that in order to go from brake being asserted to having the PWM run without going through an indeterminate state care must be taken. If the

In order to smoothly release brake by external brake pin is asserted then PWM is going to run, the step interval as refer below figure.


Start
Initialize PWM function
1. Set PWM Control Regs
2. Set PWM brake output pattern(PWMnB)
3. Enable brake function
(BKEN,BPEN,BKCH)=(1,1,0)
PWM starts running
Brake occurs?
No
Yes
1. PWMn output=PWMnB
2. H/W set BKF=1 & PWMRUN=0
3. S/W switch to S/W Brake
(BKEN,BPEN,BKCH)=(1,0,0)
4. Set PWMn comparator output =
PWMnB or a given pattern
1. Clear 10-bit PWM counter
CLRPWM=1
2. Reload PWMP & PWM registers
3. Enable brake function
(BKEN,BPEN,BKCH)=(1,1,0)
Brake pin is asserted?
Yes
No
1. Clear BKF
PWM output=PWM comparator output
2. Re-start PWM Running by setting
PWMRUN=1; load bit=1
End

Master Transmitter Mode



27. CONFIG BITS

The W79E82X series have two CONFIG bits(CONFIG1, CONFIG2) that must be define at power up and can not be set after the program start of execution. Those features are configured through the use of two flash EPROM bytes, and the flash EPROM can be programmed and verified repeatedly. Until the code inside the Flash EPROM is confirmed OK, the code can be protected. The protection of flash EPROM (CONFIG2) and those operations on it are described below. The data of these bytes may be read by the MOVC instruction at the addresses.

27.1 CONFIG1

CONFIG 1 :

7	6	5	4	3	2	1	0	
WDTE	RPD	PRHI	BOV	-	-	Fosc1	Fosc0	CONFIG Bit

WDTE: Watchdog Timer clock source Bit.
RPD: Reset Pin Disable Bit.
PRHI: Port Reset High or Low Bit.
BOV: Brownout voltage select Bit.
Fosc1: CPU oscillator type select Bit 1.
Fosc0: CPU oscillator type select Bit 0.

CONFIG Register 1

BIT	NAME	FUNCTION
7	WDTE	Clock source of Watchdog Timer select bit: 0: The internal RC oscillator clock is for Watchdog Timer clock used. 1: The uC clock is for Watchdog Timer clock used.
6	RPD	Reset Pin Disable bit: 0: Enable Reset function of Pin 1.5. 1: Disable Reset function of Pin 1.5, and it to be used as an input port pin.
5	PRHI	Port Reset High or Low bit: 0: Port reset to low state. 1: Port reset to high state.
4	BOV	Brownout Voltage Select bit: 0: Brownout detect voltage is 3.8V. 1: Brownout detect voltage is 2.5V.