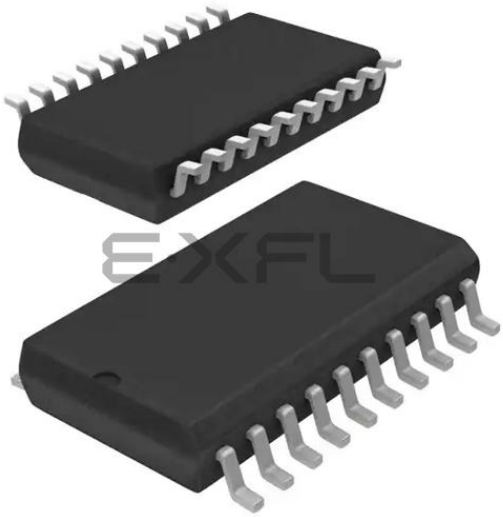

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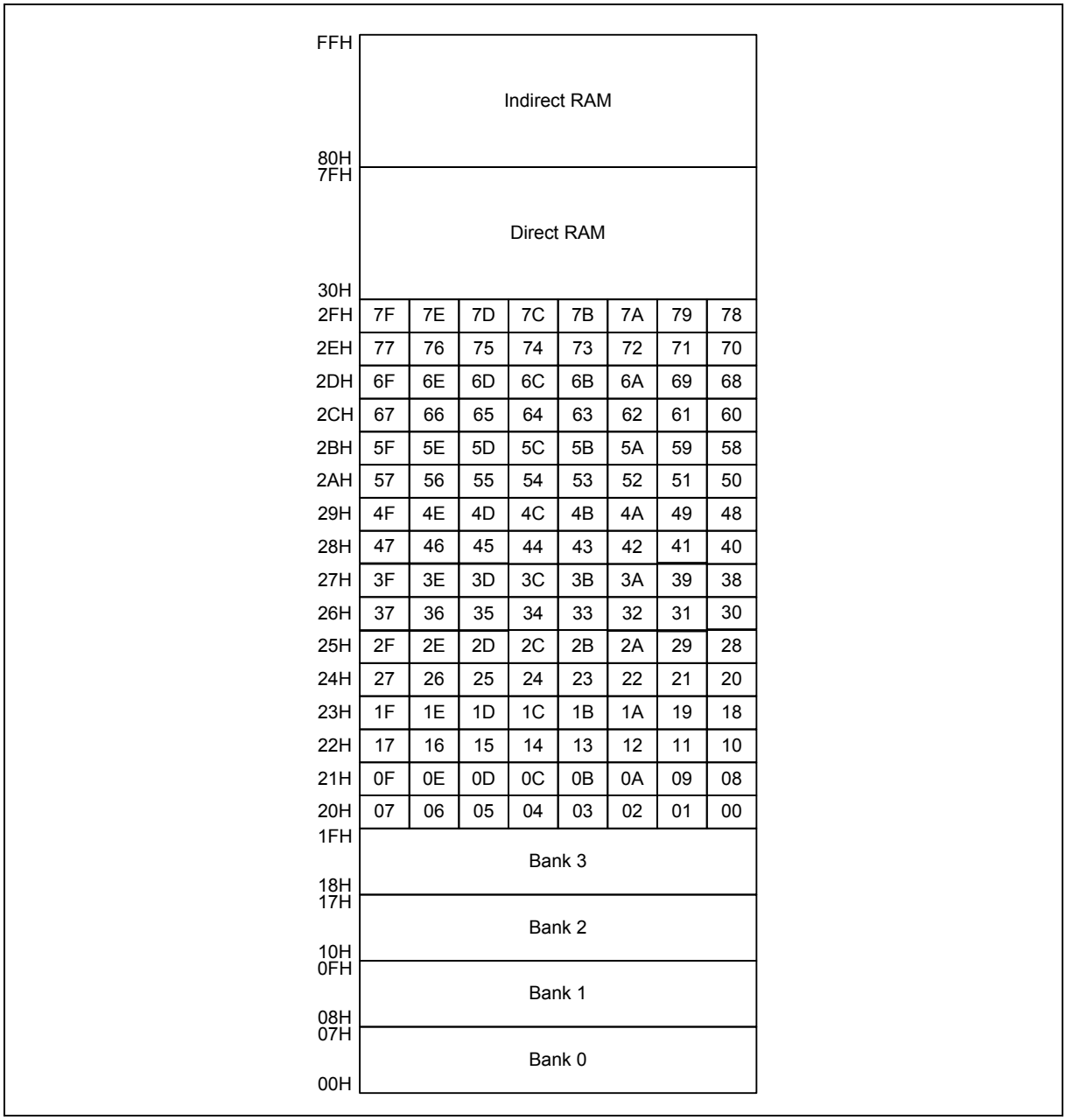
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, UART/USART
Peripherals	Brown-out Detect/Reset, LED, LVD, POR, PWM, WDT
Number of I/O	18
Program Memory Size	1KB (1K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/w79e821asg



Working Registers

There are four sets of working registers, each consisting of eight 8-bit registers. These are termed ads Banks 0, 1, 2, and 3. Individual registers within these banks can be directly accessed by separate instructions. These individual registers are named as R0, R1, R2, R3, R4, R5, R6 and R7. However, at one time the W79E82X series can work with only one particular bank. The bank selection is done by setting RS1-RS0 bits in the PSW. The R0 and R1 registers are used to store the address for indirect accessing.

8. SPECIAL FUNCTION REGISTERS

The W79E82X series uses Special Function Registers (SFRs) to control and monitor peripherals and their Modes. The SFRs reside in the register locations 80-FFh and are accessed by direct addressing only. Some of the SFRs are bit addressable. This is very useful in cases where we wish to modify a particular bit without changing the others. The SFRs that are bit addressable are those whose addresses end in 0 or 8. The W79E82X series contain all the SFRs present in the standard 8052. However some additional SFRs are added. In some cases the unused bits in the original 8052, have been given new functions. The list of the SFRs is as follows.

Table 1 Special Function Register Location Table

F8	IP1							
F0	B						P0ID	IP1H
E8	IE1							
E0	ACC	ADCCON	ADCH					
D8	WDCON	PWMPL	PWM0L	PWM1L	PWMCON1	PWM2L	PWM3L	PWMCON2
D0	PSW	PWMPH	PWM0H	PWM1H		PWM2H	PWM3H	PWMCON3
C8							NVMCON	NVMDAT
C0	I2CON	I2ADDR					NVMADDR	TA
B8	IP0	SADEN			I2DAT	I2STATUS	I2CLK	I2TIMER
B0		P0M1	P0M2	P1M1	P1M2	P2M1	P2M2	IP0H
A8	IE	SADDR			CMP1	CMP2		
A0	P2	KBI	AUXR1					
98	SCON	SBUF						
90	P1					DIVM		
88	TCON	TMOD	TL0	TL1	TH0	TH1	CKCON	
80	P0	SP	DPL	DPH				PCON

Note: 1. The SFRs in the column with dark borders are bit-addressable

2. The table is condensed with eight locations per row. Empty locations indicate that these are no registers at these addresses. When a bit or register is not implemented, it will read high.

PWM 1 High Bits Register

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	PWM1.9	PWM1.8

Mnemonic: PWM1H Address: D3h

BIT	NAME	FUNCTION
7~2	-	Reserved
1~0	PWM1.9 ~PWM1.8	The PWM1 High Bits Register bit 9~8.

PWM 2 High Bits Register

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	PWM2.9	PWM2.8

Mnemonic: PWM2H Address: D5h

BIT	NAME	FUNCTION
7~2	-	Reserved
1~0	PWM2.9 ~PWM2.8	The PWM2 High Bits Register bit 9~8.

PWM 3 High Bits Register

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	PWM3.9	PWM3.8

Mnemonic: PWM3H Address: D6h

BIT	NAME	FUNCTION
7~2	-	Reserved
1~0	PWM3.9 ~PWM3.8	The PWM3 High Bits Register bit 9~8.

PWM Control Register 3

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	BKF

Mnemonic: PWMCON3 Address: D7h

BIT	NAME	FUNCTION
7~1	-	Reserved
0	BKF	The external brake pin Flag. 0: The PWM is not brake. 1: The PWM is brake by external brake pin. It will be cleared by software.

BIT	NAME	FUNCTION
7	PWMRUN	0: The PWM is not running. 1: The PWM counter is running.
6	Load	0: The registers value of PWMP and Comparators are never loaded to counter and Comparator registers. 1: The PWMP register will be load value to counter register after counter underflow, and hardware will clear by next clock cycle.
5	CF	0: The 10-bit counter down count is not underflow. 1: The 10-bit counter down count is underflow. It will be cleared by software.
4	CLRPWM	1: Clear 10-bit PWM counter to 000H.
3	PWM3I	0: PWM3 out is non-inverted. 1: PWM3 output is inverted.
2	PWM2I	0: PWM2 out is non-inverted. 1: PWM2 output is inverted.
1	PWM1I	0: PWM1 out is non-inverted. 1: PWM1 output is inverted.
0	PWM0I	0: PWM0 out is non-inverted. 1: PWM0 output is inverted.

PWM 2 Low Bits Register

Bit:	7	6	5	4	3	2	1	0
	PWM2.7	PWM2.6	PWM2.5	PWM2.4	PWM2.3	PWM2.2	PWM2.1	PWM2.0

Mnemonic: PWM2L Address: DDh

BIT	NAME	FUNCTION
7~0	PWM2.7 ~PWM2.0	PWM 2 Low Bits Register.

PWM 3 Low Bits Register

Bit:	7	6	5	4	3	2	1	0
	PWM3.7	PWM3.6	PWM3.5	PWM3.4	PWM3.3	PWM3.2	PWM3.1	PWM3.0

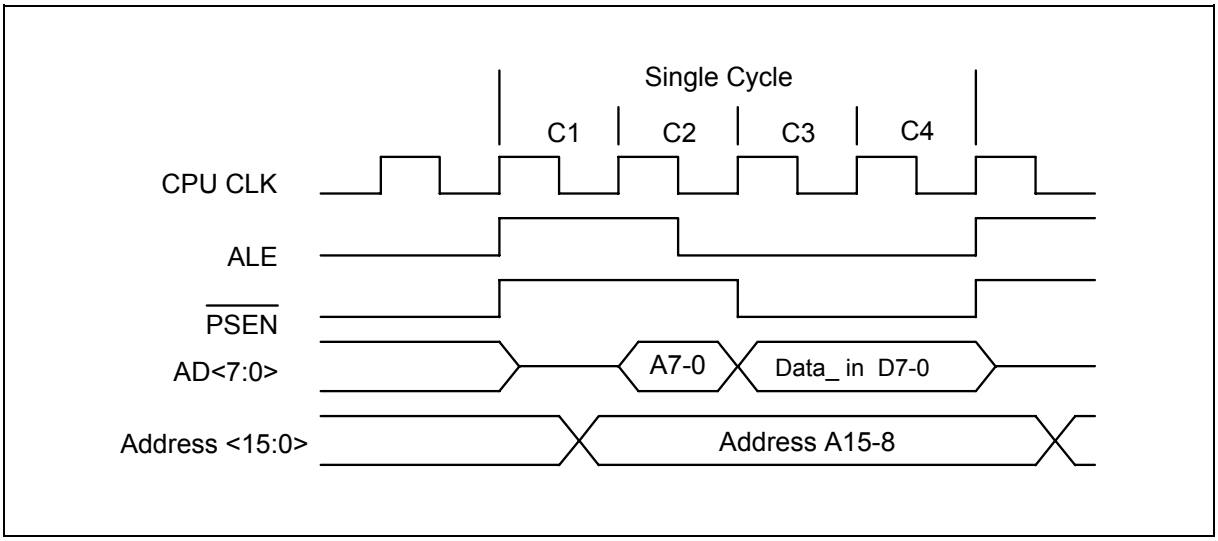
Mnemonic: PWM3L Address: DEh

BIT	NAME	FUNCTION
7~0	PWM3.7 ~PWM3.0	PWM 3 Low Bits Register.

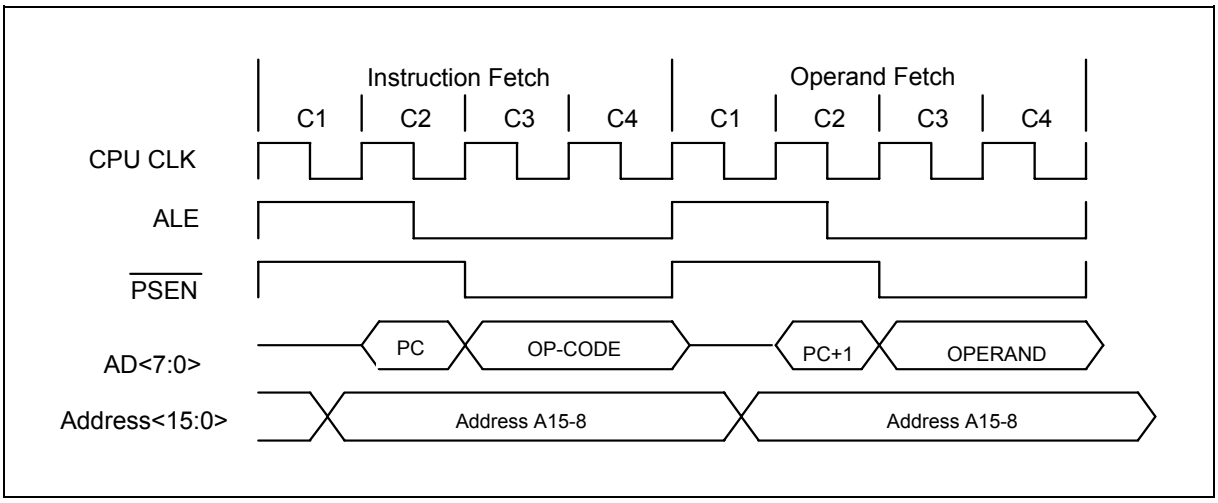
PWM Control Register 2

Bit:	7	6	5	4	3	2	1	0
	BKCH	BKPS	BPEN	BKEN	PWM3B	PWM2B	PWM1B	PWM0B

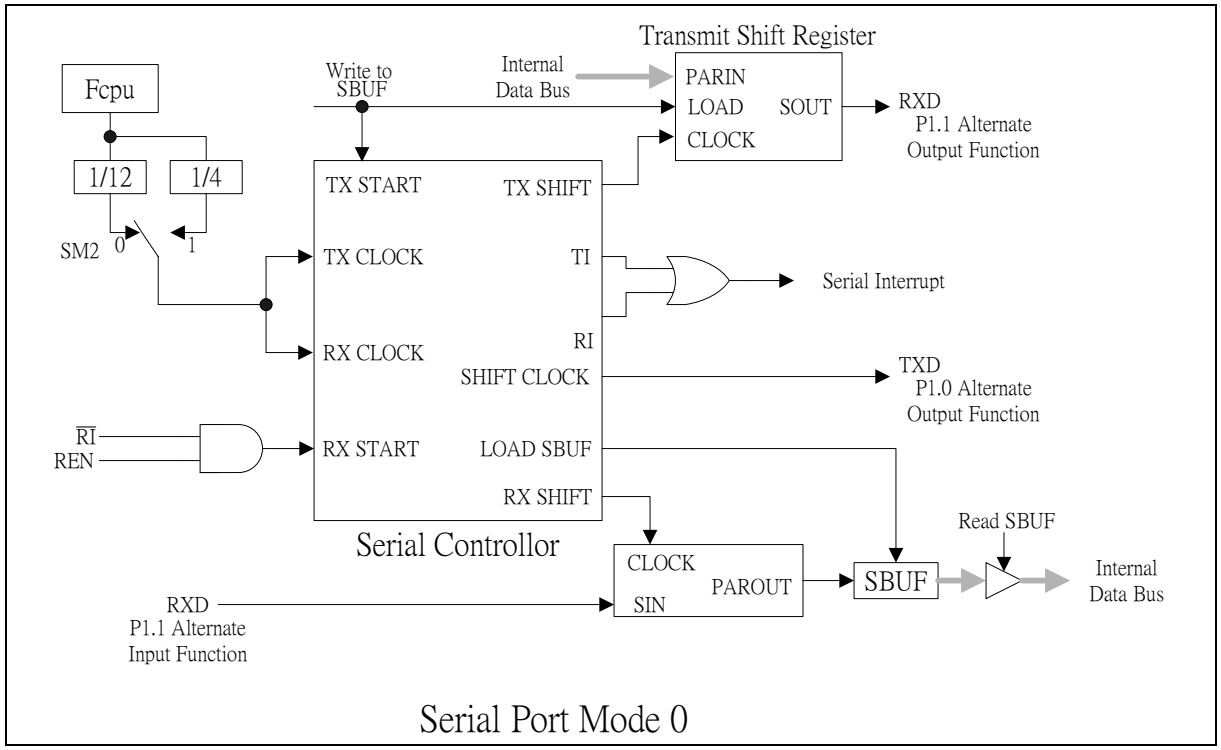
Mnemonic: PWMCON2 Address: DFh



Single Cycle Instruction Timing



Two Cycle Instruction Timing



Serial Port Mode 0

The TI flag is set high in C1 following the end of transmission of the last bit. The serial port will receive data when REN is 1 and RI is zero. The shift clock (TxD) will be activated and the serial port will latch data on the rising edge of shift clock. The external device should therefore present data on the falling edge on the shift clock. This process continues till all the 8 bits have been received. The RI flag is set in C1 following the last rising edge of the shift clock on TxD. This will stop reception, till the RI is cleared by software.

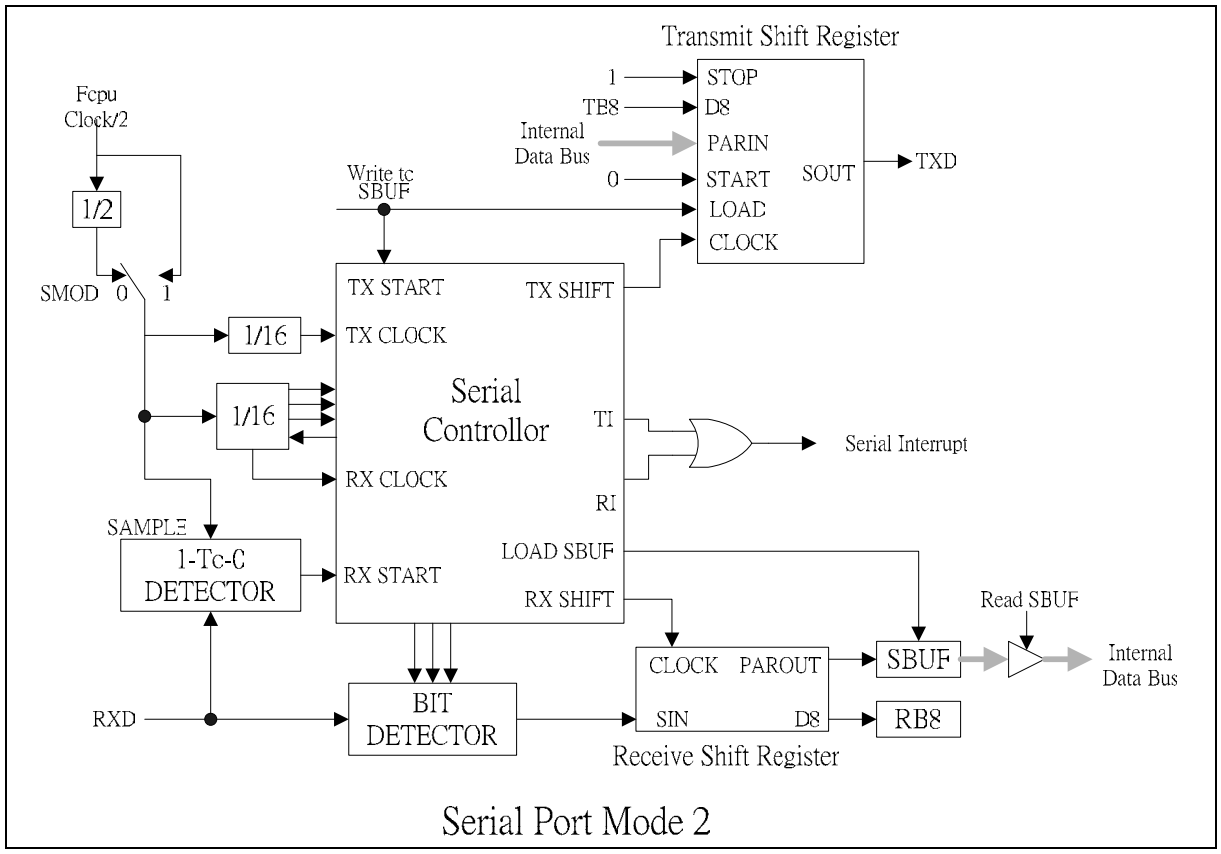
16.2 MODE 1

In Mode 1, the full duplex asynchronous mode is used. Serial communication frames are made up of 10 bits transmitted on TXD and received on RXD. The 10 bits consist of a start bit (0), 8 data bits (LSB first), and a stop bit (1). On received, the stop bit goes into RB8 in the SFR SCON. The baud rate in this mode is variable. The serial baud can be programmed to be 1/16 or 1/32 of the Timer 1 overflow. Since the Timer 1 can be set to different reload values, a wide variation in baud rates is possible.

Transmission begins with a write to SBUF. The serial data is brought out on to TxD pin at C1 following the first roll-over of divide by 16 counter. The next bit is placed on TxD pin at C1 following the next rollover of the divide by 16 counter. Thus the transmission is synchronized to the divide by 16 counter and not directly to the write to SBUF signal. After all 8 bits of data are transmitted, the stop bit is transmitted. The TI flag is set in the C1 state after the stop bit has been put out on TxD pin. This will be at the 10th rollover of the divide by 16 counter after a write to SBUF.

16.3 MODE 2

This mode uses a total of 11 bits in asynchronous full-duplex communication. The functional description is shown in the figure below. The frame consists of one start bit (0), 8 data bits (LSB first), a programmable 9th bit (TB8) and a stop bit (0). The 9th bit received is put into RB8. The baud rate is programmable to 1/32 or 1/64 of the oscillator frequency, which is determined by the SMOD bit in PCON SFR. Transmission begins with a write to SBUF. The serial data is brought out on to TxD pin at C1 following the first roll-over of the divide by 16 counter. The next bit is placed on TxD pin at C1 following the next rollover of the divide by 16 counter. Thus the transmission is synchronized to the divide by 16 counter, and not directly to the write to SBUF signal. After all 9 bits of data are transmitted, the stop bit is transmitted. The TI flag is set in the C1 state after the stop bit has been put out on TxD pin. This will be at the 11th rollover of the divide by 16 counter after a write to SBUF. Reception is enabled only if REN is high. The serial port actually starts the receiving of serial data, with the detection of a falling edge on the RxD pin. The 1-to-0 detector continuously monitors the RxD line, sampling it at the rate of 16 times the selected baud rate. When a falling edge is detected, the divide by 16 counter is immediately reset. This helps to align the bit boundaries with the rollovers of the divide by 16 counter. The 16 states of the counter effectively divide the bit time into 16 slices. The bit detection is done on a best of three bases. The bit detector samples the RxD pin, at the 8th, 9th and 10th counter states. By using a majority 2 of 3 voting system, the bit value is selected. This is done to improve the noise rejection feature of the serial port.



Serial Port Mode 2

If the first bit detected after the falling edge of RxD pin, is not 0, then this indicates an invalid start bit, and the reception is immediately aborted. The serial port again looks for a falling edge in the RxD line. If a valid start bit is detected, then the rest of the bits are also detected and shifted into the SBUF. After shifting in 9 data bits, there is one more shift to do, after which the SBUF and RB8 are loaded and RI is set. However certain conditions must be met before the loading and setting of RI can be done.

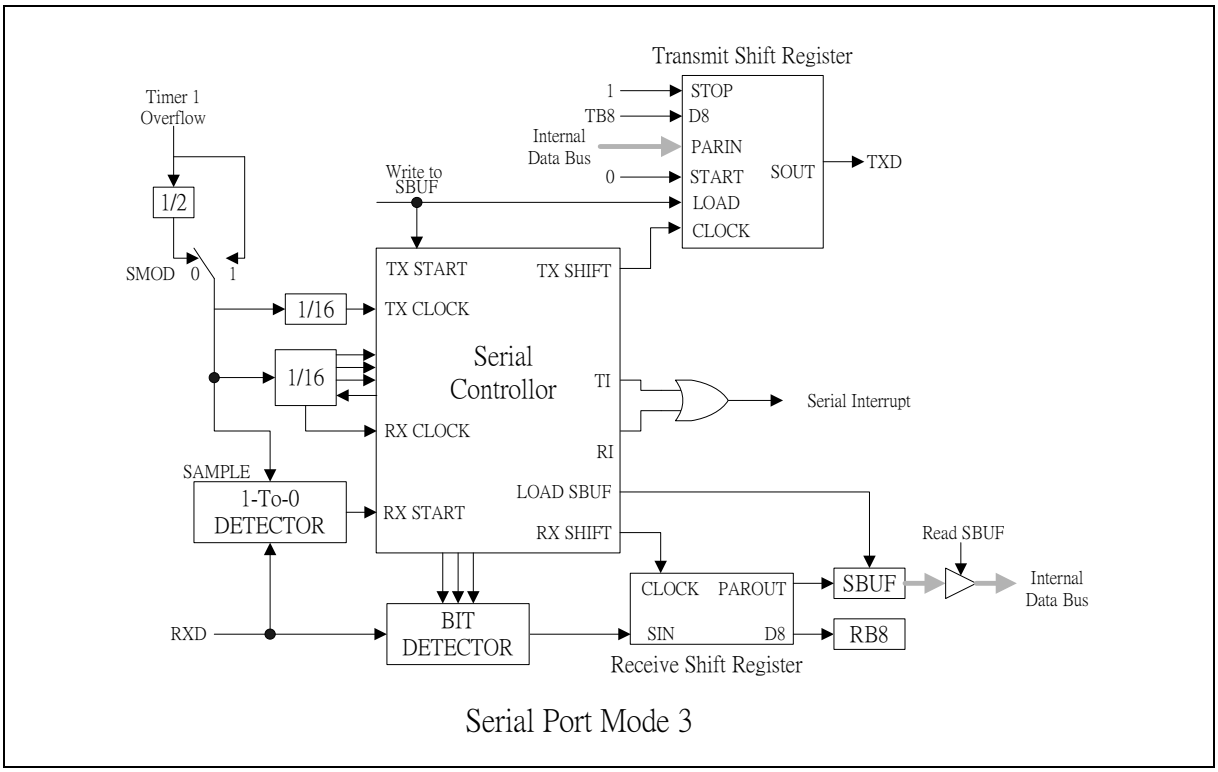
1. RI must be 0 and

2. Either SM2 = 0, or the received stop bit = 1.

If these conditions are met, then the stop bit goes to RB8, the 8 data bits go into SBUF and RI is set. Otherwise the received frame may be lost. After the middle of the stop bit, the receiver goes back to looking for a 1-to-0 transition on the RxD pin.

16.4 MODE 3

This mode is similar to Mode 2 in all respects, except that the baud rate is programmable. The user must first initialize the Serial related SFR SCON before any communication can take place. This involves selection of the Mode and baud rate. The Timer 1 should also be initialized if modes 1 and 3 are used. In all four modes, transmission is started by any instruction that uses SBUF as a destination register. Reception is initiated in Mode 0 by the condition RI = 0 and REN = 1. This will generate a clock on the TxD pin and shift in 8 bits on the RxD pin. Reception is initiated in the other modes by the incoming start bit if REN = 1. The external device will start the communication by transmitting the start bit.



Serial Port Mode 3

20. I/O PORT CONFIGURATION

The W79E82X series have three I/O ports, port 0, port 1 and port 2. All pins of I/O ports can be configured to one of four types by software except P1.5 is only input pin. When P1.5 is configured reset pin by RPD=0 in the CONFIG 1 register, the W79E82X series can support 15 pins by use Crystal. If used on-chip RC oscillator the P1.5 is configured input pin, the W79E82X series can be supported up to 18 pins. The I/O ports configuration setting as below table.

I/O port configuration table

PXM1.Y	PXM2.Y	PORT INPUT/OUTPUT MODE
0	0	Quasi-bidirectional
0	1	Push-Pull
1	0	Input Only (High Impedance) P2M1.PxS=0, TTL input P2M1.PxS=1, Schmitt input
1	1	Open Drain

All port pins can be determined to high or low after reset by configure PRHI bit in the CONFIG1 register. After reset, these pins are in quasi-bidirectional mode. The port pin of P1.5 only is a Schmitt trigger input.

Enabled toggle outputs from Timer 0 and Timer 1 by ENT0 and ENT1 on P2M1 register, the output frequency of Timer 0 or Timer 1 is by Timer overflow.

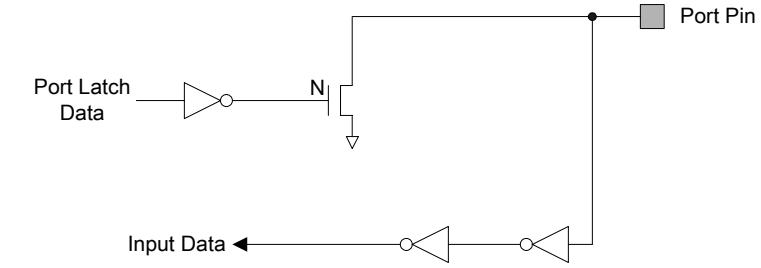
Each I/O port of the W79E82X series may be selected to use TTL level inputs or Schmitt inputs by P(n)S bit on P2M1 register, where n is 0, 1 or 2. When P(n)S is set to 1, Ports are selected Schmitt trigger inputs on Port(n). The P2.0(XTAL2) can be configured clock output when used on-chip RC or external Oscillator is clock source, and the frequency of clock output is divided by 4 on on-chip RC clock or external Oscillator.

20.1 Quasi-Bidirectional Output Configuration

After chip was power on or reset, the all ports output are this mode, and output is common with the 8051. This mode can be used as both an input and output without the need to reconfigure the port.

When the pin is pulled low, it is driven strongly and able to sink a fairly large current. These features are somewhat similar to an open drain output except that there are three pull-up transistors in the quasi-bidirectional output that serve different purposes.

This mode has three pull-up resisters that are “strong” pull-up, “weak” pull-up and “very weak” pull-up. The “strong” pull-up is used fast transition from logic “0” change to logic “1”, and it is fast latch and transition. When port pins is occur from logic “0” to logic “1”, the strong pull-up will quickly turn on two CPU clocks to pull high then turn off.

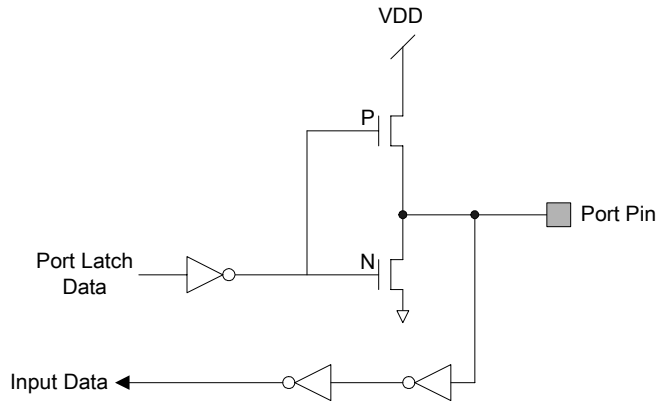


Open Drain Output

20.3 Push-Pull Output Configuration

The push-pull output mode has two strong pull-up and pull-down structure that support large source and sink current output. it remove “weak” pull-up and “very weak” pull-up resister and remain “strong pull-up resister on quasi-bidirectional output mode. The “strong” pull-up is always turns on when port latch is logic “1” to support source current. The push-pull port configuration is shown in below Figure.

The W79E82X series have three port pins that can’t be configured are P1.2, P1.3, and P1.5. The port pins P1.2 and P1.3 are configured to open drain outputs. They may be used as inputs by writing ones to their respective port latches.

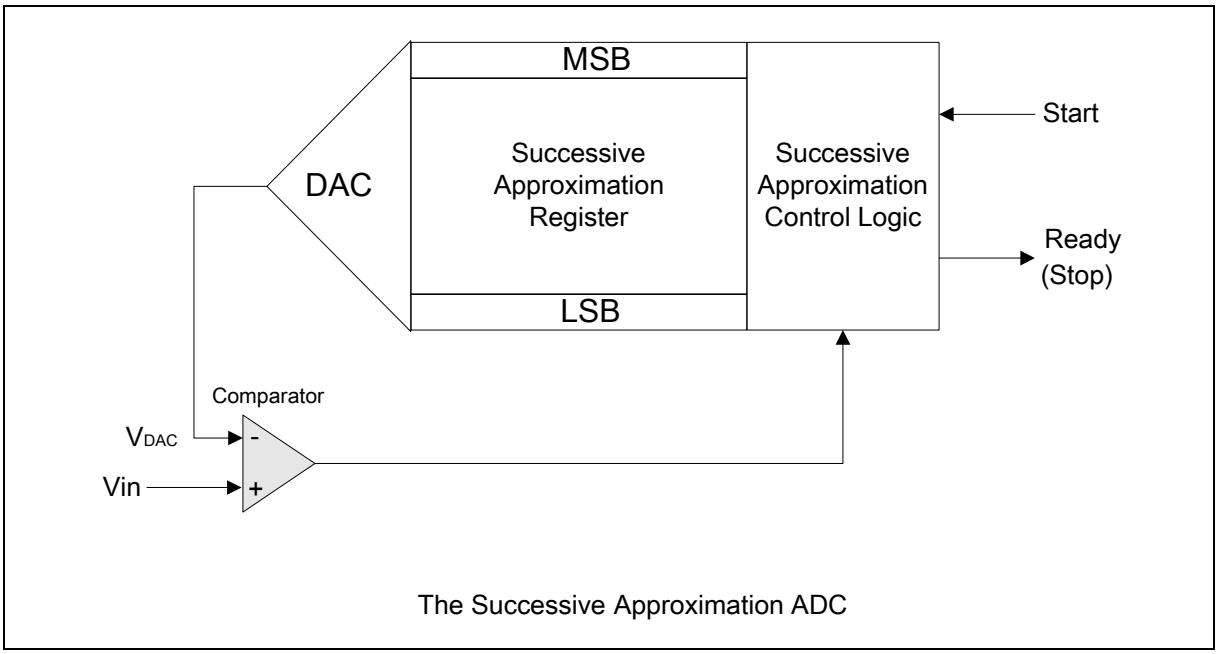


Push-Pull Output

20.4 Input Only Configuration

By configure this mode, the ports are only digital input and disable digital output. The W79E82X series can select input pin to Schmitt trigger or TTL level input by PxM1.y and PxM2.y registers.

selects one of 4 analog channels. An ADC conversion in progress is unaffected by an external or software ADC start. The result of a completed conversion remains unaffected provided ADCI = logic 1; a new ADC conversion already in progress is aborted when the idle or power down mode is entered. The result of a completed conversion (ADCI = logic 1) remains unaffected when entering the idle mode.



Successive Approximation ADC

24.1 ADC Resolution and Analog Supply:

The ADC circuit has its own supply pins (AVDD and AVSS) and one pins (Vref+) connected to each end of the DAC's resistance-ladder that the AVDD and Vref+ are connected to VDD and AVSS is connected to VSS. The ladder has 1023 equally spaced taps, separated by a resistance of "R". The first tap is located 0.5×R above AVSS, and the last tap is located 0.5×R below Vref+. This gives a total ladder resistance of 1024×R. This structure ensures that the DAC is monotonic and results in a symmetrical quantization error.

For input voltages between VSS and [(Vref+) + ½ LSB], the 10-bit result of an A/D conversion will be 0000000000B = 000H. For input voltages between [(Vref+) – 3/2 LSB] and Vref+, the result of a conversion will be 1111111111B = 3FFH. Vref+ and AVSS may be between AVDD + 0.2V and VSS – 0.2 V. Vref+ should be positive with respect to VSS, and the input voltage (Vin) should be between Vref+ and VSS.

The result can always be calculated from the following formula:

$$\text{Result} = 1024 \times \frac{\text{Vin}}{\text{Vref}+} \quad \text{or Result} = 1024 \times \frac{\text{Vin}}{\text{VDD}}$$

25.2.4 The I2C Clock Baud Rate Bits, I2CLK

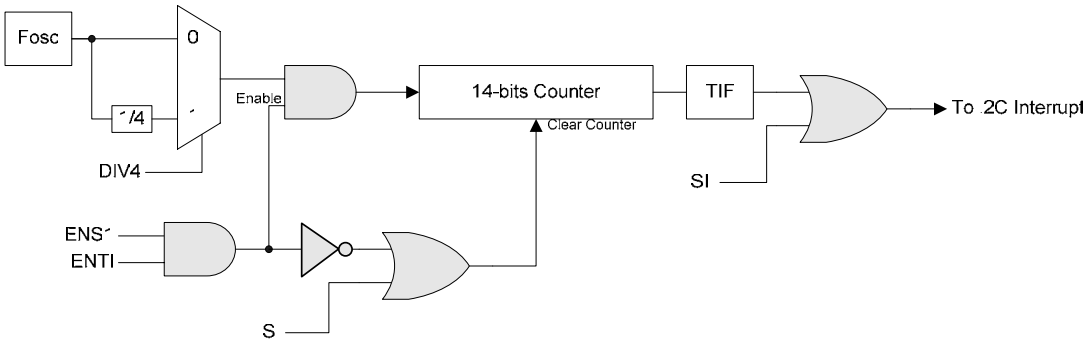
The data baud rate of I2C is determines by I2CLK register when SIO1 is in a master mode. It is not important when SIO1 is in a slave mode. In the slave modes, SIO1 will automatically synchronize with any clock frequency up to 400 KHz from master I2C device.

The data baud rate of I2C setting is Data Baud Rate of I2C = Fcpu / (I2CLK+1). The Fcpu=Fosc/4. If Fosc = 16MHz, the I2CLK = 40(28H), so data baud rate of I2C = 16MHz /(4X (40 +1)) = 97.56Kbits/sec. The block diagram is as below figure.

Bit:	7	6	5	4	3	2	1	0
	I2CLK.7	I2CLK.6	I2CLK.5	I2CLK.4	I2CLK.3	I2CLK.2	I2CLK.1	I2CLK.0

Mnemonic: I2CLK Address: BEh

BIT	NAME	FUNCTION
7 ~ 0	I2CLK	The I2C clock baud rate bits.



I2C Timer Count Block Diagram

25.2.5 The Status Register, I2STATUS

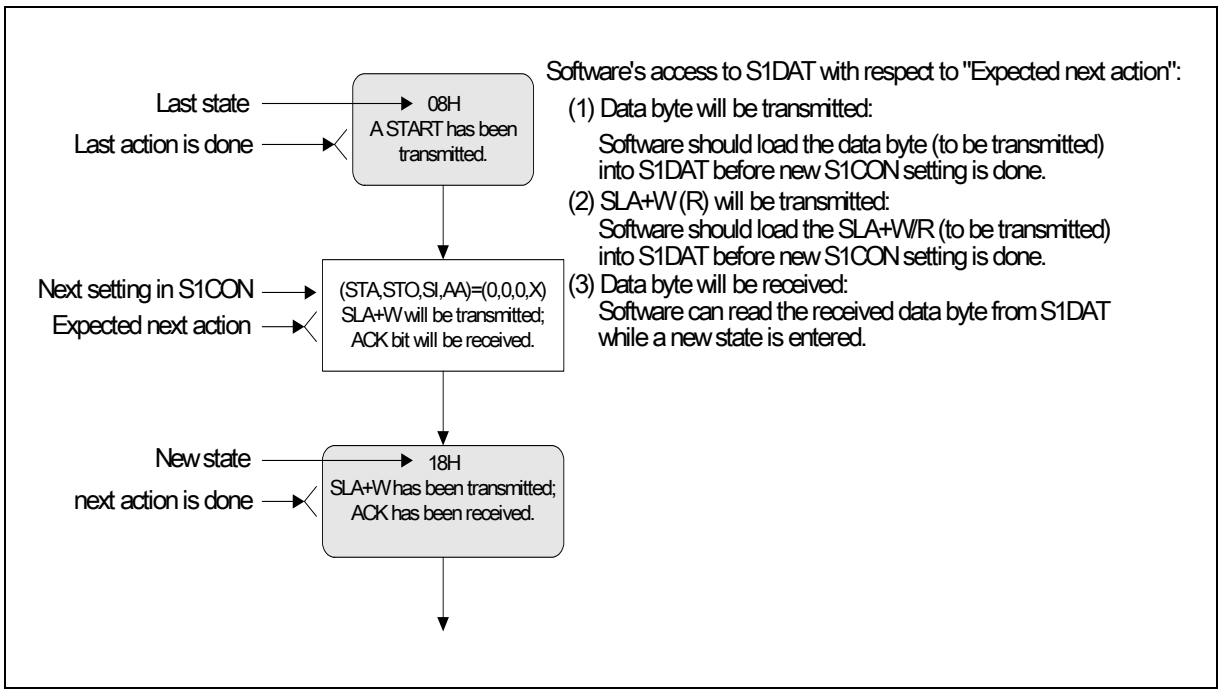
I2STATUS is an 8-bit read-only register. The three least significant bits are always 0. The five most significant bits contain the status code. There are 23 possible status codes. When I2STATUS contains F8H, no serial interrupt is requested. All other I2STATUS values correspond to defined SIO1 states. When each of these states is entered, a status interrupt is requested (SI = 1). A valid status code is present in I2STATUS one machine cycle after SI is set by hardware and is still present one machine cycle after SI has been reset by software.

In addition, state 00H stands for a Bus Error. A Bus Error occurs when a START or STOP condition is present at an illegal position in the format frame. Examples of illegal positions are during the serial transfer of an address byte, a data byte or an acknowledge bit.

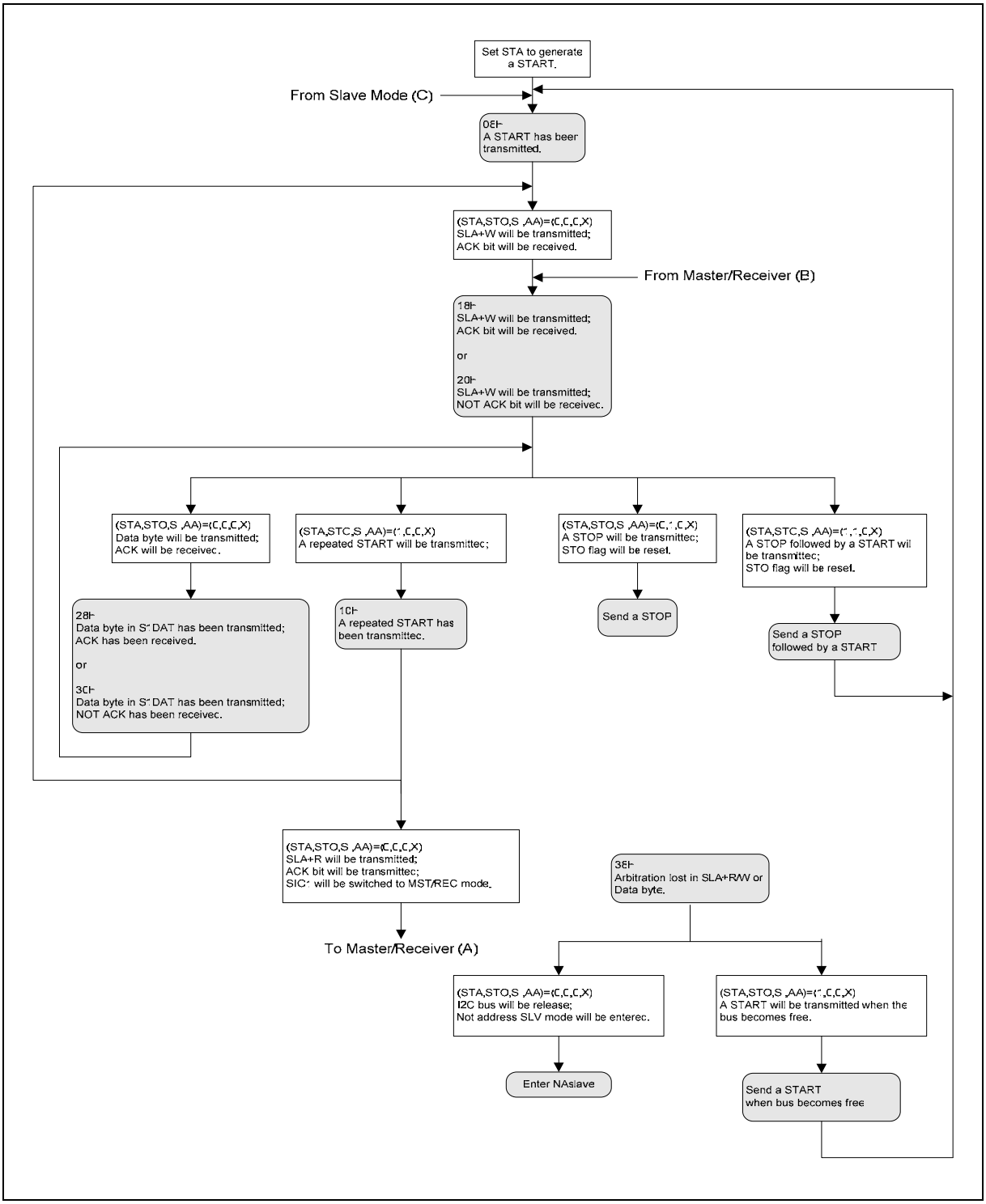
25.3 Operating Modes of I2C

The four operating modes are: Master/Transmitter, Master/Receiver, Slave/Transmitter and Slave/Receiver. Bits STA, STO and AA in I2CON decide the next action the SIO1 hardware will take after SI is cleared. When the next action is completed, a new status code in I2STATUS will be updated and SI will be set by hardware in the same time. Now, the interrupt service routine is entered (if the SI interrupt is enabled), the new status code can be used to decide which appropriate service routine the software is to branch. Data transfers in each mode are shown in the following figures.

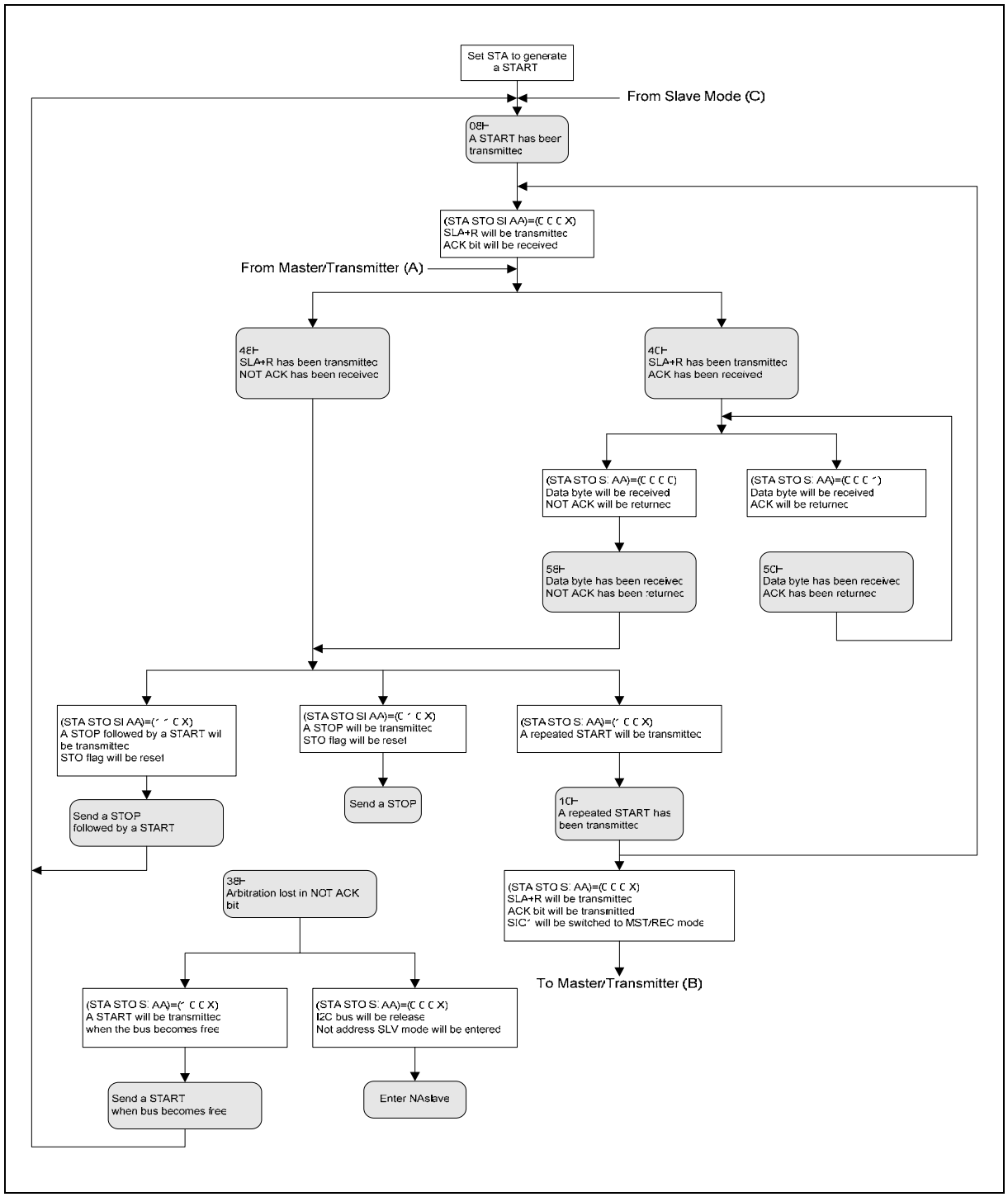
*** Legend for the following four figures:



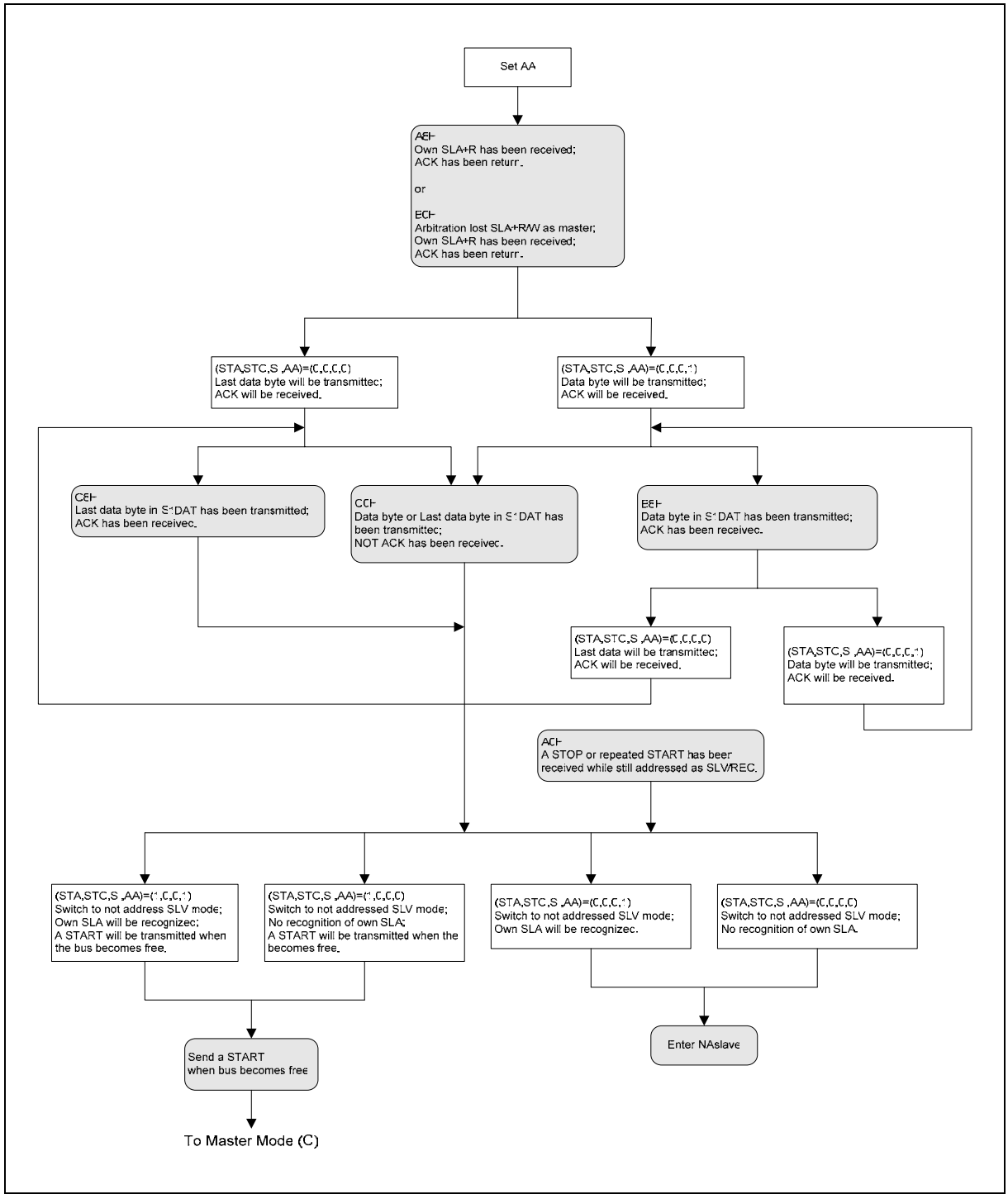
Master Transmitter Mode



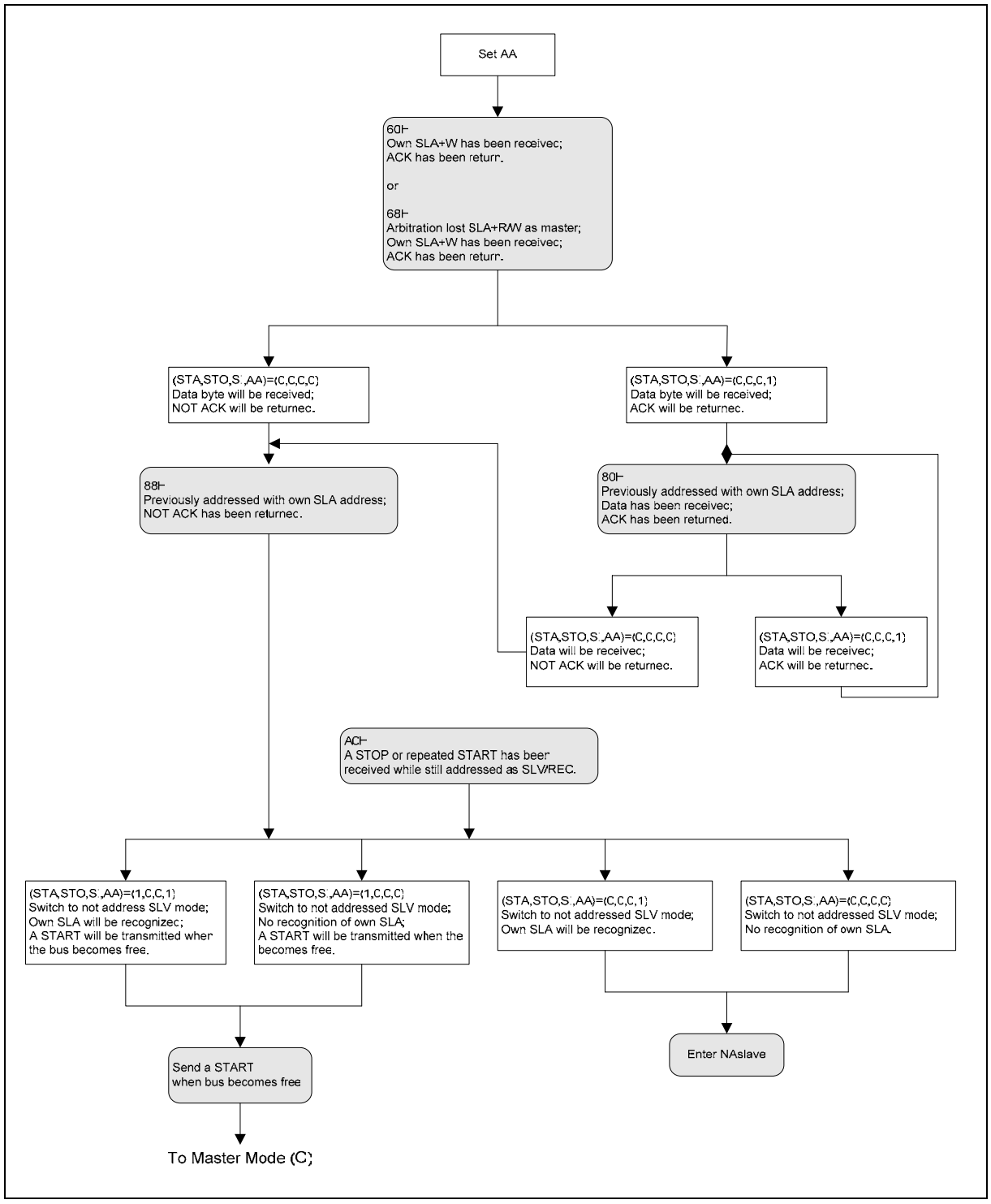
Master Receiver Mode



Slave Transmitter Mode



Slave Receiver Mode



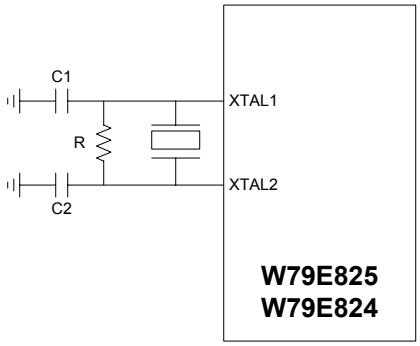
32. AC SPECIFICATION

PARAMETER	SYMBOL	VARIABLE CLOCK MIN.	VARIABLE CLOCK MAX.	UNITS
Oscillator Frequency	$1/t_{CLCL}$	0	20	MHz

33. TYPICAL APPLICATION CIRCUITS

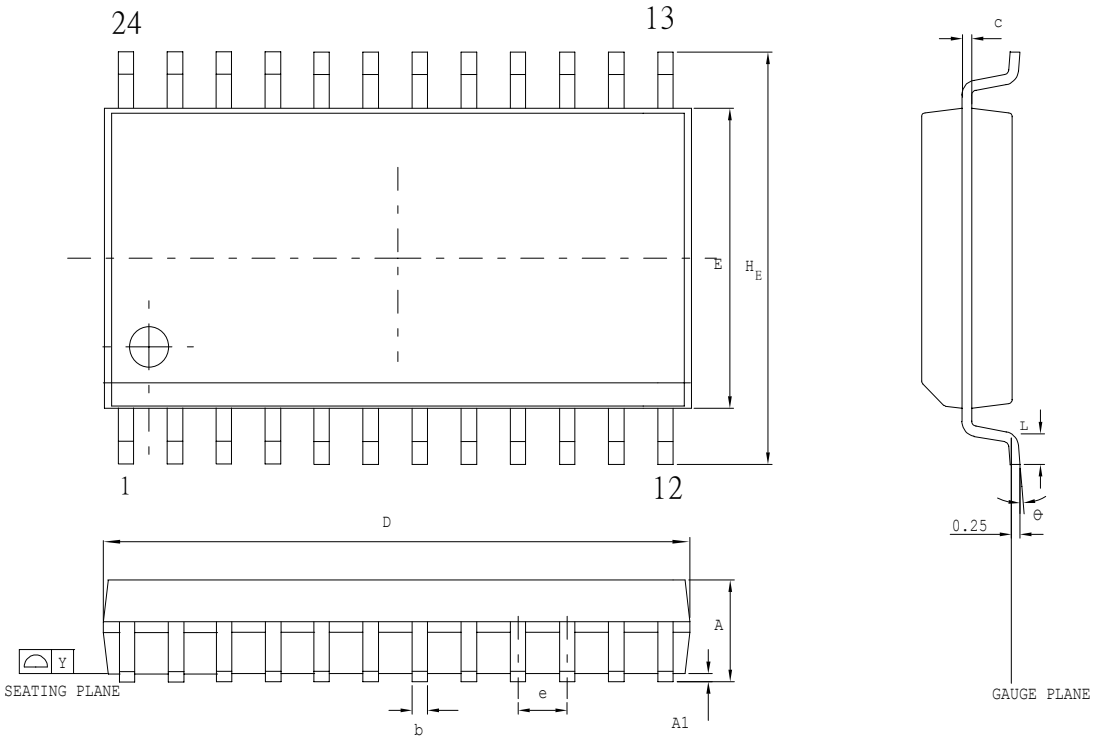
CRYSTAL	C1	C2	R
4MHz ~ 20 MHz	without	without	without

The above table shows the reference values for crystal applications.



34.3 24-pin SO

24L SOP-300mil



Control demensions are in milmeters .

SYMBOL	DIMENSION IN MM		DIMENSION IN INCH	
	MIN.	MAX.	MIN.	MAX.
A	2.35	2.65	0.093	0.104
A1	0.10	0.30	0.004	0.012
b	0.33	0.51	0.013	0.020
c	0.23	0.32	0.009	0.013
E	7.40	7.60	0.291	0.299
D	15.20	15.60	0.598	0.614
e	1.27 BSC		0.050 BSC	
H_E	10.00	10.65	0.394	0.419
Y	—	0.10	—	0.004
L	0.40	1.27	0.016	0.050
θ	0	8	0	8