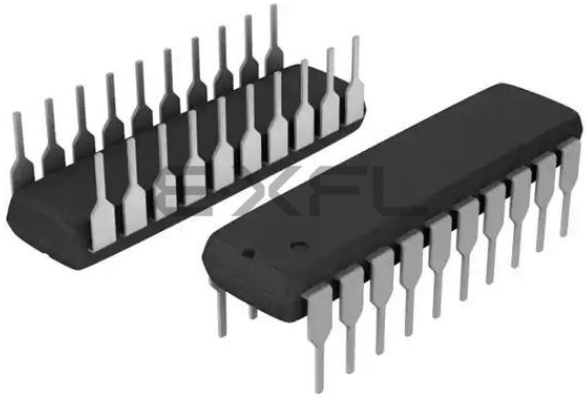

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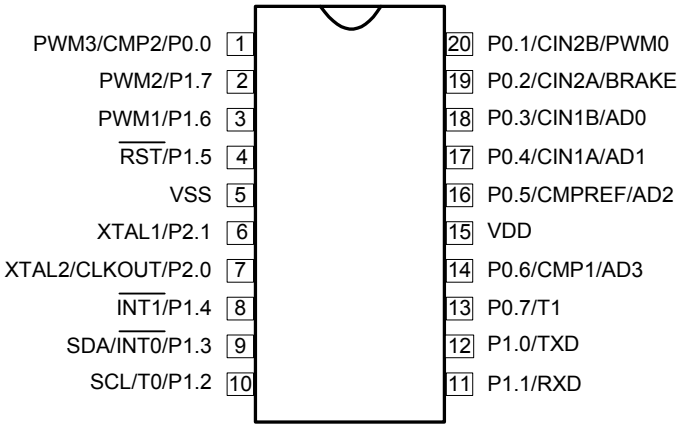
Applications of "Embedded - Microcontrollers"

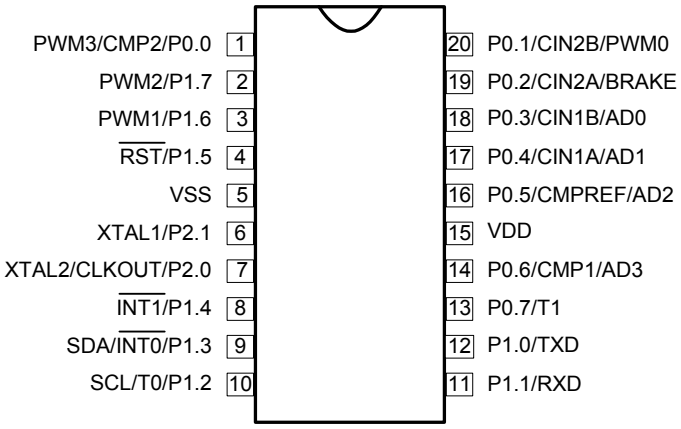
Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, UART/USART
Peripherals	Brown-out Detect/Reset, LED, LVD, POR, PWM, WDT
Number of I/O	18
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	20-DIP (0.300", 7.62mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/w79e823adg

4. PIN CONFIGURATION

20 PIN DIP



20 PIN SOP



6. FUNCTIONAL DESCRIPTION

The W79E82X series architecture consist of a 4T 8051 core controller surrounded by various registers, **16K/8K/4K/2K/1K** bytes Flash EPROM, **256/128** bytes of RAM, **256/128** bytes NVM Data Flash EPROM, three general purpose I/O ports, two timer/counters, one serial port, one I2C serial I/O, 4 channel PWM with 10-bit counter, 4-channel multiplexed with 10-bit ADC analog input, Flash EPROM program by Writer and ICP.

6.1 On-Chip Flash EPROM

The W79E82X series include one **16K/8K/4K/2K/1K** bytes of main Flash EPROM for application program when operating the in-circuit programming features by the Flash EPROM itself which need Writer or ICP program board to program the Flash EPROM. This ICP(In-Circuit Programming) feature makes the job easy and efficient in which the application needs to update firmware frequently. In some applications, the in-circuit programming feature makes it possible that the end-user is able to easily update the system firmware by themselves without opening the chassis.

6.2 I/O Ports

The W79E82X series have two 8-bit and one 2-bit port, up to 18 I/O pins using on-chip oscillator & /RST is input only by reset options. All ports can be used as four outputs mode when it may set by PxM1.y and PxM2.y registers, it has strong pull-ups and pull-downs, and does not need any external pull-ups. Otherwise it can be used as general I/O port as open drain circuit. All ports can be used bi-directional and these are as I/O ports. These ports are not true I/O, but rather are pseudo-I/O ports. This is because these ports have strong pull-downs and weak pull-ups.

6.3 Serial I/O

The W79E82X series have one serial port that is functionally similar to the serial port of the original 8032 family. However the serial port on the W79E82X series can operate in different modes in order to obtain timing similarity as well. The Serial port has the enhanced features of Automatic Address recognition and Frame Error detection.

6.4 Timers

The W79E82X series have two 16-bit timers that are functionally and similar to the timers of the 8052 family. When used as timers, they are set 12 or 4 clocks per count that emulates the timing of the original 8052.

6.5 Interrupts

The Interrupt structure in the W79E82X series is slightly different from that of the standard 8052. Due to the presence of additional features and peripherals, the number of interrupt sources and vectors has been increased.

7. MEMORY ORGANIZATION

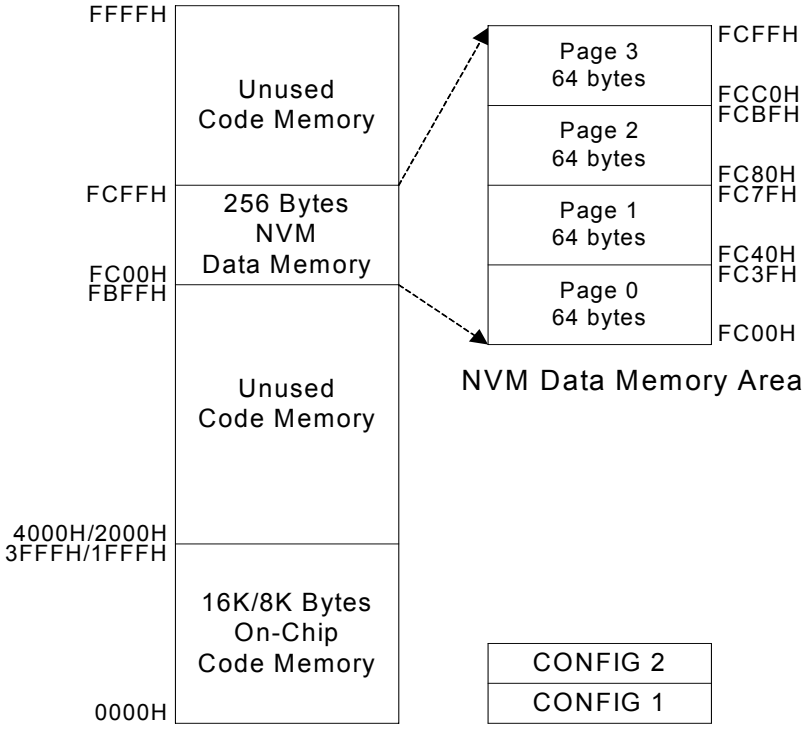
The W79E82X series separate the memory into two separate sections, the Program Memory and the Data Memory. The Program Memory is used to store the instruction op-codes, while the Data Memory is used to store data or for memory mapped devices.

Program Memory

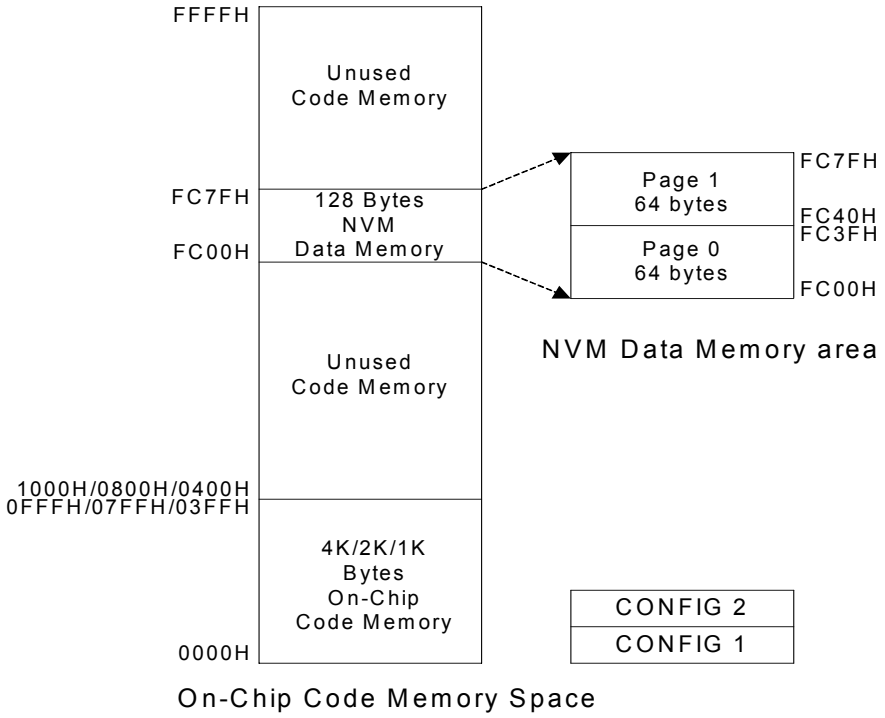
The Program Memory on the W79E82X series can be up to **16K/8K/4K/2K/1K** bytes long. All instructions are fetched for execution from this memory area. The MOVC instruction can also access this memory region.

Data Memory

The NVM Data Memory of Flash EPROM on the W79E82X series can be up to **256/128** bytes long. The W79E82X series read the content of data memory by using "MOVC A,@A+DPTR". To write data is by NVMADDR, NVMDAT and NVMCON SFR's registers.



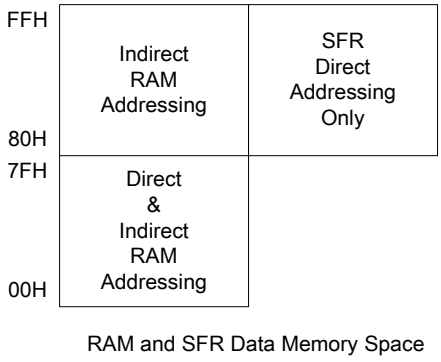
W79E825/W79E824 Memory Map



W79E823/W79E822/W79E821 Memory Map

Register Map

As mentioned before the W79E82X series have separate Program and Data Memory areas. The on-chip **256/128** bytes scratch pad RAM is in addition to the external memory. There are also several Special Function Registers (SFRs) which can be accessed by software. The SFRs can be accessed only by direct addressing, while the on-chip RAM can be accessed by either direct or indirect addressing.



W79E825/W79E824 RAM and SFR Memory Map

Bit addressable Locations

The Scratch-pad RAM area from location 20h to 2Fh is byte as well as bit addressable. This means that a bit in this area can be individually addressed. In addition some of the SFRs are also bit addressable. The instruction decoder is able to distinguish a bit access from a byte access by the type of the instruction itself. In the SFR area, any existing SFR whose address ends in a 0 or 8 is bit addressable.

Stack

The scratch-pad RAM can be used for the stack. This area is selected by the Stack Pointer (SP), which stores the address of the top of the stack. Whenever a jump, call or interrupt is invoked the return address is placed on the stack. There is no restriction as to where the stack can begin in the RAM. By default however, the Stack Pointer contains 07h at reset. The user can then change this to any value desired. The SP will point to the last used value. Therefore, the SP will be incremented and then address saved onto the stack. Conversely, while popping from the stack the contents will be read first, then the SP is decreased.

Continued.

BIT	NAME	FUNCTION
3	IE1	Interrupt 1 Edge Detect: Set by hardware when an edge/level is detected on $\overline{INT1}$. This bit is cleared by hardware when the service routine is vectored to only if the interrupt was edge triggered. Otherwise it follows the pin.
2	IT1	Interrupt 1 type control: Set/cleared by software to specify falling edge/ low level triggered external inputs.
1	IE0	Interrupt 0 Edge Detect: Set by hardware when an edge/level is detected on $\overline{INT0}$. This bit is cleared by hardware when the service routine is vectored to only if the interrupt was edge triggered. Otherwise it follows the pin.
0	IT0	Interrupt 0 type control: Set/cleared by software to specify falling edge/ low level triggered external inputs.

TIMER MODE CONTROL

Bit:	7	6	5	4	3	2	1	0
	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0

Mnemonic: TMOD Address: 89h

BIT	NAME	FUNCTION
7	GATE	Gating control: When this bit is set, Timer/counter 1 is enabled only while $\overline{INT1}$ pin is high and TR1 control bit is set. When cleared, Timer 1 is enabled whenever TR1 control bit is set.
6	C/$\overline{T}$	Timer or Counter Select: When cleared, the timer is incremented by internal clocks. When set, the timer counts high-to-low edges of the T1 pin.
5	M1	Timer1 Mode Select bit1: See table below.
4	M0	Timer1 Mode Select bit0: See table below.
3	GATE	Gating control: When this bit is set, Timer/counter 0 is enabled only while $\overline{INT0}$ pin is high and TR0 control bit is set. When cleared, Timer 0 is enabled whenever TR0 control bit is set.
2	C/$\overline{T}$	Timer or Counter Select: When cleared, the timer is incremented by internal clocks. When set, the timer counts high-to-low edges of the T0 pin.
1	M1	Timer0 Mode Select bit1: See table below.
0	M0	Timer0 Mode Select bit0: See table below.

WATCHDOG CONTROL

Bit:	7	6	5	4	3	2	1	0
	WDRUN	-	WD1	WD0	WDIF	WTRF	EWRST	WDCLR

Mnemonic: WDCON Address: D8h

BIT	NAME	FUNCTION
7	WDRUN	0: The Watchdog is stopped. 1: The Watchdog is running.
6	-	Reserved.
5	WD1	Watchdog Timer times selected.
4	WD0	Watchdog Timer times selected.
3	WDIF	Watchdog Timer Interrupt Flag 0: If the interrupt is not enabled, then this bit indicates that the time-out period has elapsed. This bit must be cleared by software. 1: If the watchdog interrupt is enabled, hardware will set this bit to indicate that the watchdog interrupt has occurred.
2	WTRF	Watchdog Timer Reset Flag 1: Hardware will set this bit when the watchdog timer causes a reset. Software can read it but must clear it manually. A power-fail reset will also clear the bit. This bit helps software in determining the cause of a reset. If EWRST = 0, the watchdog timer will have no affect on this bit.
1	EWRST	0: Disable Watchdog Timer Reset. 1: Enable Watchdog Timer Reset.
0	WDCLR	Reset Watchdog Timer This bit helps in putting the watchdog timer into a know state. It also helps in resetting the watchdog timer before a time-out occurs. Failing to set the EWRST before time-out will cause an interrupt, if EWDI (IE1.4) is set, and 512 clocks after that a watchdog timer reset will be generated if EWRST is set. This bit is self-clearing by hardware.

The WDCON SFR is set to a 0x0000x0B on an reset. WTRF (WDCON.2) is set to a 1 on a Watchdog timer reset, but to a 0 on power on/down resets. WDIF (WDCON.3) is not altered by an external reset. EWRST (WDCON.1) is set to 0 on a Power-on reset and unaffected by other resets.

All the bits in this SFR have unrestricted read access. EWRST, WDIF and WDCLR require Timed Access procedure to write. The remaining bits have unrestricted write accesses. Please refer TA register description.

TA	REG	C7H
WDCON	REG	D8H

9. INSTRUCTION

The W79E82X series execute all the instructions of the standard 8052 family. The operation of these instructions, their effect on the flag bits and the status bits is exactly the same. However, timing of these instructions is different. The reason for this is two fold. Firstly, in the W79E82X series, each machine cycle consists of 4 clock periods, while in the standard 8052 it consists of 12 clock periods. Also, in the W79E82X series there is only one fetch per machine cycle i.e. 4 clocks per fetch, while in the standard 8052 there can be two fetches per machine cycle, which works out to 6 clocks per fetch.

The advantage the W79E82X series has is that since there is only one fetch per machine cycle, the number of machine cycles in most cases is equal to the number of operands that the instruction has. In case of jumps and calls there will be an additional cycle that will be needed to calculate the new address. But overall the W79E82X serial reduces the number of dummy fetches and wasted cycles, thereby improving efficiency as compared to the standard 8052.

TABLE: INSTRUCTIONS AFFECT FLAG SETTING

INSTRUCTION	CARRY	OVERFLOW	AUXILIARY CARRY	INSTRUCTION	CARRY	OVERFLOW	AUXILIARY CARRY
ADD	X	X	X	CLR C	0		
ADDC	X	X	X	CPL C	X		
SUBB	X	X	X	ANL C, bit	X		
MUL	0	X		ANL C, bit	X		
DIV	0	X		ORL C, bit	X		
DA A	X			ORL C, bit	X		
RRC A	X			MOV C, bit	X		
RLC A	X			CJNE	X		
SETB C	1						

A "X" indicates that the modification is as per the result of instruction.

9.1 INSTRUCTION TIMING

The instruction timing for the W79E82X series are an important aspect, especially for those users who wish to use software instructions to generate timing delays. Also, it provides the user with an insight into the timing differences between the W79E82X series and the standard 8052. In the W79E82X series each machine cycle is four clock periods long. Each clock period is designated a state. Thus each machine cycle is made up of four states, C1, C2, C3 and C4, in that order. Due to the reduced time for each instruction execution, both the clock edges are used for internal timing. Hence it is important that the duty cycle of the clock be as close to 50% as possible to avoid timing conflicts. As mentioned earlier, the W79E82X series does one op-code fetch per machine cycle.

Therefore, in most of the instructions, the number of machine cycles needed to execute the instruction is equal to the number of bytes in the instruction. Of the 256 available op-codes, 128 of them are single cycle instructions. Thus more than half of all op-codes in the W79E82X series are executed in just four clock periods. Most of the two-cycle instructions are those that have two byte instruction codes. However there are some instructions that have only one byte instructions, yet they are two cycle instructions. One instruction which is of importance is the MOVX instruction. In the standard 8052, the MOVX instruction is always two machine cycles long. However, in the W79E82X series each machine cycle is made of only 4 clock periods compared to the 12 clock periods for the standard 8052. Therefore, even though the number of categories has increased, each instruction is at least 1.5 to 3 times faster than the standard 8052 in terms of clock periods.

SFR RESET VALUE

SFR NAME	RESET VALUE	SFR NAME	RESET VALUE
P0	11111111B	I2DAT	xxxxxxxxB
SP	00000111B	I2STATUS	00000xxxB
DPL	00000000B	I2TIMER	00000000B
DPH	00000000B	I2CLK	00000000B
PCON	00xx0000B	I2CON	00000000B
TCON	00000000B	I2ADDR	xxxxxxxxB
TMOD	00000000B	TA	00000000B
TL0	00000000B	PSW	00000000B
TL1	00000000B	PWMP1	xxxxxx00B
TH0	00000000B	PWM0H	xxxxxx00B
TH1	00000000B	PWM1H	xxxxxx00B
CKCON	00000000B	PWM2H	xxxxxx00B
P1	1111xx11B	PWM3H	xxxxxx00B
DIVM	00000000B	WDCON	0x000000B
SCON	00000000B	PWMP0	00000000B
SBUF	xxxxxxxxB	PWM0L	00000000B
P2	xxxxx11B	PWM1L	00000000B
KBI	00000000B	PWMCON1	00000000B
AUXR1	00000000B	PWM2L	00000000B
IE	00000000B	PWM3L	00000000B
SADDR	00000000B	PWMCON2	00000000B
CMP1	00000000B	ACC	00000000B
CMP2	00000000B	ADCCON	xx000x00B
P0M1	00000000B	ADCH	xxxxxxxxB
P0M2	00000000B	IE1	xx000000B
P1M1	00000000B	B	00000000B
P1M2	00000000B	P0IDS	00000000B
P2M1	00000000B	IPH	xx000000B
P2M2	xxxxxx00B	IP1	xx000000B
IP0H	x0000000B		
IP0	x0000000B		
SADEN	00000000B		

12.2 Priority Level Structure

There are four priority levels for the interrupts, highest, high, low and lowest. The interrupt sources can be individually set to either high or low levels. Naturally, a higher priority interrupt cannot be interrupted by a lower priority interrupt. However there exists a pre-defined hierarchy amongst the interrupts themselves. This hierarchy comes into play when the interrupt controller has to resolve simultaneous requests having the same priority level. This hierarchy is defined as shown below; the interrupts are numbered starting from the highest priority to the lowest.

Priority structure of interrupts

SOURCE	FLAG	PRIORITY LEVEL
External Interrupt 0	IE0	1(highest)
Brownout Detect	BOF	2
Watchdog Timer	WDIF	3
Timer 0 Overflow	TF0	4
I2C Interrupt	SI	5
ADC Interrupt	ADCI	6
External Interrupt 1	IE1	7
KBI Interrupt	KBF	8
Comparator 1 Interrupt	CMF1	9
Timer 1 Overflow	TF1	10
Comparator 2 Interrupt	CMF2	11
Serial Port	RI + TI	12
PWM	BKF	13 (lowest)

The interrupt flags are sampled every machine cycle. In the same machine cycle, the sampled interrupts are polled and their priority is resolved. If certain conditions are met then the hardware will execute an internally generated LCALL instruction which will vector the process to the appropriate interrupt vector address. The conditions for generating the LCALL are

1. An interrupt of equal or higher priority is not currently being serviced.

2. The current polling cycle is the last machine cycle of the instruction currently being execute.

3. The current instruction does not involve a write to IE, IE1, IP0, IP0H, IP1 or IPH1 registers and is not a RETI.

If any of these conditions are not met, then the LCALL will not be generated. The polling cycle is repeated every machine cycle, with the interrupts sampled in the same machine cycle. If an interrupt flag is active in one cycle but not responded to, and is not active when the above conditions are met, the denied interrupt will not be serviced. This means that active interrupts are not remembered; every polling cycle is new.

16. SERIAL PORT (UART)

Serial port in the W79E82X series is a full duplex port. The W79E82X series provide the user with additional features such as the Frame Error Detection and the Automatic Address Recognition. The serial ports are capable of synchronous as well as asynchronous communication. In Synchronous mode the W79E82X series generate the clock and operates in a half duplex mode. In the asynchronous mode, full duplex operation is available. This means that it can simultaneously transmit and receive data. The transmit register and the receive buffer are both addressed as SBUF Special Function Register. However any write to SBUF will be to the transmit register, while a read from SBUF will be from the receiver buffer register. The serial port can operate in four different modes as described below.

16.1 MODE 0

This mode provides synchronous communication with external devices. In this mode serial data is transmitted and received on the RXD line. TXD is used to transmit the shift clock. The TxD clock is provided by the W79E82X series whether the device is transmitting or receiving. This mode is therefore a half duplex mode of serial communication. In this mode, 8 bits are transmitted or received per frame. The LSB is Transmitted/Received first. The baud rate is fixed at 1/12 or 1/4 of the oscillator frequency. This Baud Rate is determined by the SM2 bit (SCON.5). When this bit is set to 0, then the serial port runs at 1/12 of the clock. When set to 1, the serial port runs at 1/4 of the clock. This additional facility of programmable baud rate in mode 0 is the only difference between the standard 8051 and the W79E82X series.

The functional block diagram is shown below. Data enters and leaves the Serial port on the RxD line. The TxD line is used to output the shift clock. The shift clock is used to shift data into and out of the W79E82X series and the device at the other end of the line. Any instruction that causes a write to SBUF will start the transmission. The shift clock will be activated and data will be shifted out on the RxD pin till all 8 bits are transmitted. If SM2 = 1, then the data on RxD will appear 1 clock period before the falling edge of shift clock on TxD. The clock on TxD then remains low for 2 clock periods, and then goes high again. If SM2 = 0, the data on RxD will appear 3 clock periods before the falling edge of shift clock on TxD. The clock on TxD then remains low for 6 clock periods, and then goes high again. This ensures that at the receiving end the data on RxD line can either be clocked on the rising edge of the shift clock on TxD or latched when the TxD clock is low.

Example 4: Invalid access

```
MOV     TA, #0AAh       ;3 M/C
MOV     TA, #055h       ;3 M/C
NOP                     ;1 M/C
NOP                     ;1 M/C
CLR     EWT             ;2 M/C
```

Example 5: Invalid Access

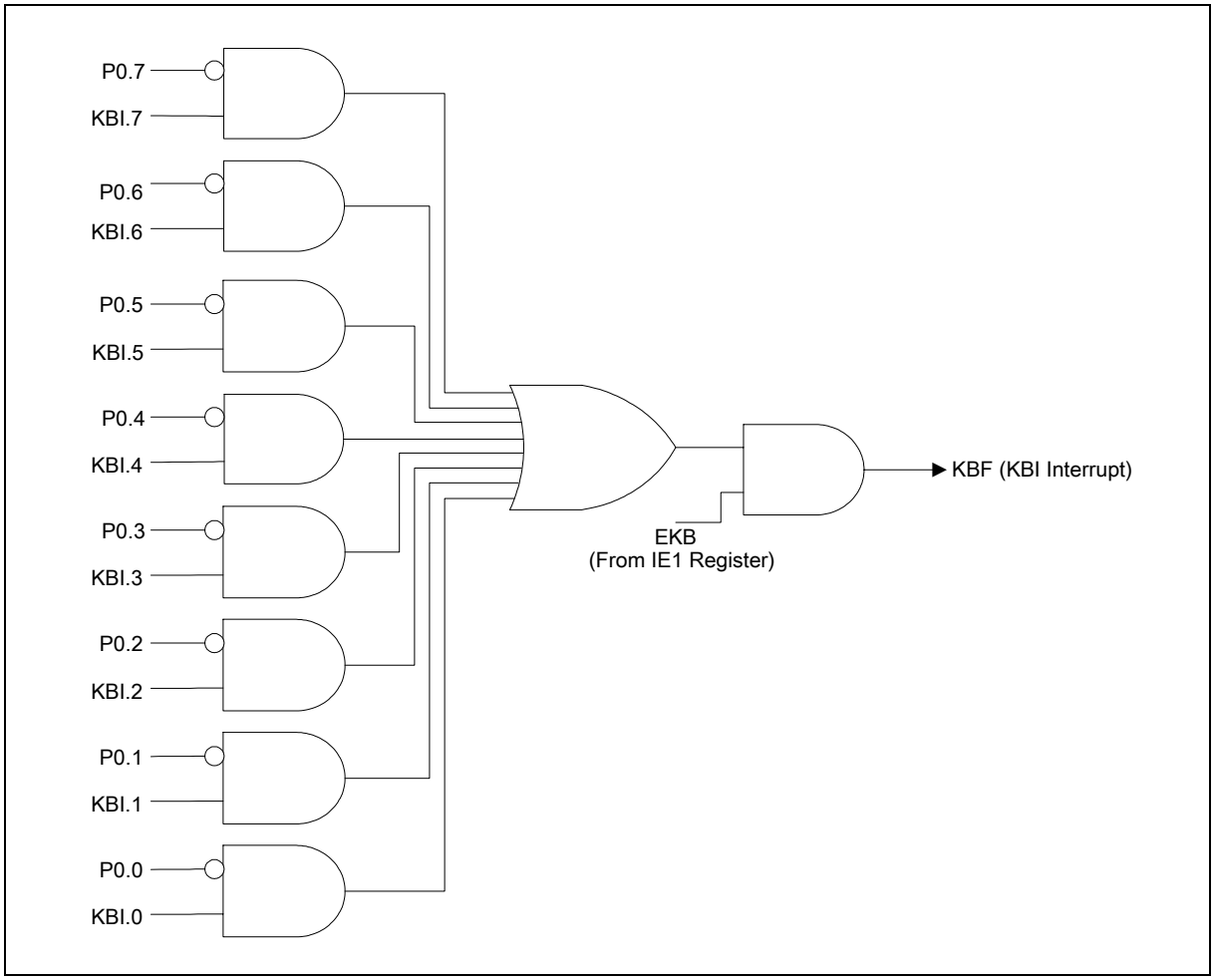
```
MOV     TA, #0AAh       ;3 M/C
NOP                     ;1 M/C
MOV     TA, #055h       ;3 M/C
SETB    EWT             ;2 M/C
```

In the first three examples, the writing to the protected bits is done before the 3 machine cycles window closes. In Example 4, however, the writing to the protected bit occurs after the window has closed, and so there is effectively no change in the status of the protected bit. In Example 5, the second write to TA occurs 4 machine cycles after the first write, therefore the timed access window is not opened at all, and the write to the protected bit fails.

18. KEYBOARD INTERRUPT (KBI)

The W79E82X series are provided 8 keyboard interrupt function to detect keypad status which key is acted, and allow a single interrupt to be generated when any key is pressed on a keyboard or keypad connected to specific pins of the W79E82X series, as shown below Figure. This interrupt may be used to wake up the CPU from Idle or Power Down modes, after chip is in Power Down or Idle Mode.

To support keyboard function is by Port 0. It can allow any or all pins of Port 0 to be enabled to cause this interrupt. Port pins are enabled by the setting of bits of KBI0 ~ KBI7 in the KBI register, as shown below Figure. The Keyboard Interrupt Flag (KBF) in the AUXR1 register is set when any enabled pin is pulled low while the KBI interrupt function is active, and the low pulse must more than 1 machine cycle, an interrupt will be generated if it has been enabled. The KBF bit set by hardware and must be cleared by software. In order to determine which key was pressed, the KBI will allow the interrupt service routine to poll port 0.



20. I/O PORT CONFIGURATION

The W79E82X series have three I/O ports, port 0, port 1 and port 2. All pins of I/O ports can be configured to one of four types by software except P1.5 is only input pin. When P1.5 is configured reset pin by RPD=0 in the CONFIG 1 register, the W79E82X series can support 15 pins by use Crystal. If used on-chip RC oscillator the P1.5 is configured input pin, the W79E82X series can be supported up to 18 pins. The I/O ports configuration setting as below table.

I/O port configuration table

PXM1.Y	PXM2.Y	PORT INPUT/OUTPUT MODE
0	0	Quasi-bidirectional
0	1	Push-Pull
1	0	Input Only (High Impedance) P2M1.PxS=0, TTL input P2M1.PxS=1, Schmitt input
1	1	Open Drain

All port pins can be determined to high or low after reset by configure PRHI bit in the CONFIG1 register. After reset, these pins are in quasi-bidirectional mode. The port pin of P1.5 only is a Schmitt trigger input.

Enabled toggle outputs from Timer 0 and Timer 1 by ENT0 and ENT1 on P2M1 register, the output frequency of Timer 0 or Timer 1 is by Timer overflow.

Each I/O port of the W79E82X series may be selected to use TTL level inputs or Schmitt inputs by P(n)S bit on P2M1 register, where n is 0, 1 or 2. When P(n)S is set to 1, Ports are selected Schmitt trigger inputs on Port(n). The P2.0(XTAL2) can be configured clock output when used on-chip RC or external Oscillator is clock source, and the frequency of clock output is divided by 4 on on-chip RC clock or external Oscillator.

20.1 Quasi-Bidirectional Output Configuration

After chip was power on or reset, the all ports output are this mode, and output is common with the 8051. This mode can be used as both an input and output without the need to reconfigure the port.

When the pin is pulled low, it is driven strongly and able to sink a fairly large current. These features are somewhat similar to an open drain output except that there are three pull-up transistors in the quasi-bidirectional output that serve different purposes.

This mode has three pull-up resisters that are “strong” pull-up, “weak” pull-up and “very weak” pull-up. The “strong” pull-up is used fast transition from logic “0” change to logic “1”, and it is fast latch and transition. When port pins is occur from logic “0” to logic “1”, the strong pull-up will quickly turn on two CPU clocks to pull high then turn off.

21.3 CPU Clock Rate select

The CPU clock of W79E82X series may be selected by the DIVM register. If DIVM = 00H, the CPU clock is running at 4 CPU clock pre machine cycle, and without any division from source clock (Fosc). When the DIVM register is set to N value, the CPU clock is divided by 2(DVIM+1), so CPU clock frequency division is from 4 to 512. The user may use this feature to set CPU at a lower speed rate for reducing power consumption. This is very similar to the situation when CPU has entered Idle mode. In addition this frequency division function affect all peripheral timings as they are all sourcing from the CPU clock(Fcpu).

22. POWER MONITORING FUNCTION

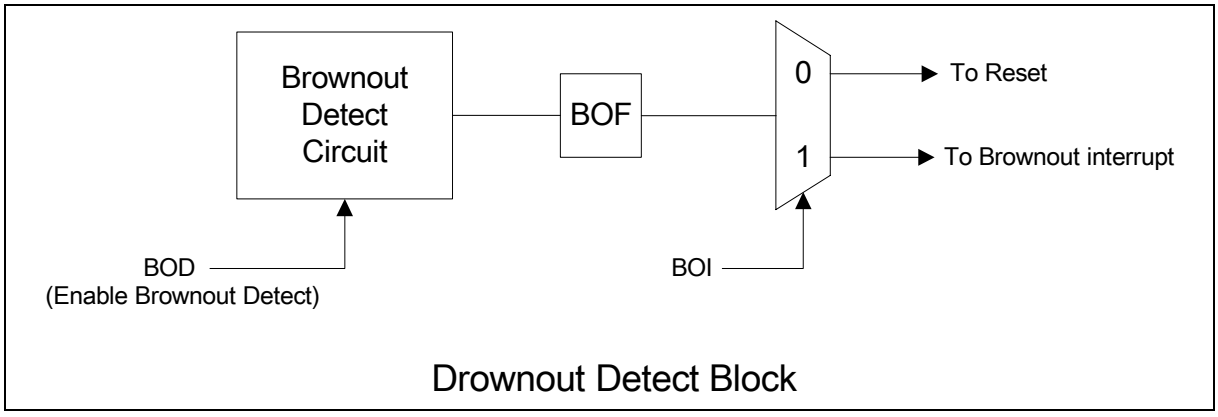
Power-On Detect and Brownout are two additional power monitoring functions implemented in W79E82X to prevent incorrect operation during power up and power drop or loss.

22.1 Power On Detect

The Power–On Detect function is a designed to detect power up after power voltage reaches to a level where Brownout Detect can work. After power on detect, the POR (PCON.4) will be set to “1” to indicate an initial power up condition. The POR flag will be cleared by software.

22.2 Brownout Detect

The Brownout Detect function is detect power voltage is drops to brownout voltage level, and allows preventing some process work or indicate power warming. The W79E82X series have two brownout voltage levels to select by BOV (CONFIG1.4). If BOV =0 that brownout voltage level is 3.8V, If BOV = 1 that brownout voltage level is 2.5V. When the Brownout voltage is drop to select level, the brownout detector will detect and keeps this active until VDD is returns to above brownout Detect voltage. The Brownout Detect block is as follow.



Drownout Detect Block

When Brownout Detect is enabled by BOD (AUXR1.6), the BOF (PCON.5) flag will be set that it cause brownout reset or interrupt, and BOF will be cleared by software. If BOI (AUXR1.5) is set to “1”, the brownout detect will cause interrupt via the EA (IE.7) and EBO (IE.5) bits is set.

In order to guarantee a correct detection of Brownout, The VDD fail time must be slower than 50mV/us, and rise time is slower than 2mV/us to ensure a proper reset.

23. PULSE WIDTH MODULATED OUTPUTS (PWM)

The W79E82X series have four-channels Pulse Width Modulated (PWM), and the PWM outputs are PWM0(P0.1), PWM1(P1.6), PWM2(P1.7) and PWM3(P0.0). When PRHI is set to “1”, after chip reset, the internal output of the each PWM channels are “1”. When PRHI is set to “0”, after chip reset, the internal output of the each PWM channels are “0”. So, in the case, if PWM output pins will output “1”, it must be written a “1” to each PWM pins to high state. A block diagram is shown as below Figure.

The W79E82X series support 10-bits down counter which clock source of counter is use the internal microcontroller clock as its input. The PWM counter clock, has the same frequency as the clock source F_{CPU} = F_{OSC}. When the counter reaches underflow it will automatic reloaded from counter register. The PWM frequency is given by: f_{PWM} = F_{CPU} / (PWMP+1), where PWMP is 10-bits register of PWMPH.1, PWMPH.0 and PWMPL.7~PWMPL.0.

When PWMP register is written, it will automatically load by PWMRUN, Load and CF is “1”, where CF flag is 10-bits down counter reaches underflow, the CF flag will be cleared by software. When PWMP register was load to counter register, the load bit will automatically clear by next cycle. If the first PWM output cycle is correct by PWMP setting, it will be clear by CLRPWM to clear 10-bits counter to 000H, then set PWMRUN and load bits to run PWM.

The pulse width of each PWM output is determined by the Compare registers of PWM0L through PWM3L and PWM0H through PWM3H. When PWM compare register is greater than 10-bits counter register, the PWM output is low. If want to change output width of PWM, after writer PWMn register, must set load bit to “1” then will be loaded to compare register by next underflow. The PWM output high pulses width is given by:

t_{HI} = (PWMP – PWMn+1). Notice, if compare register is set to 000H, the PWMn output is high, and if compare register is set to 3FFH, the PWMn output is low.

PWM Control Register 3 PWMCON3(D7H)

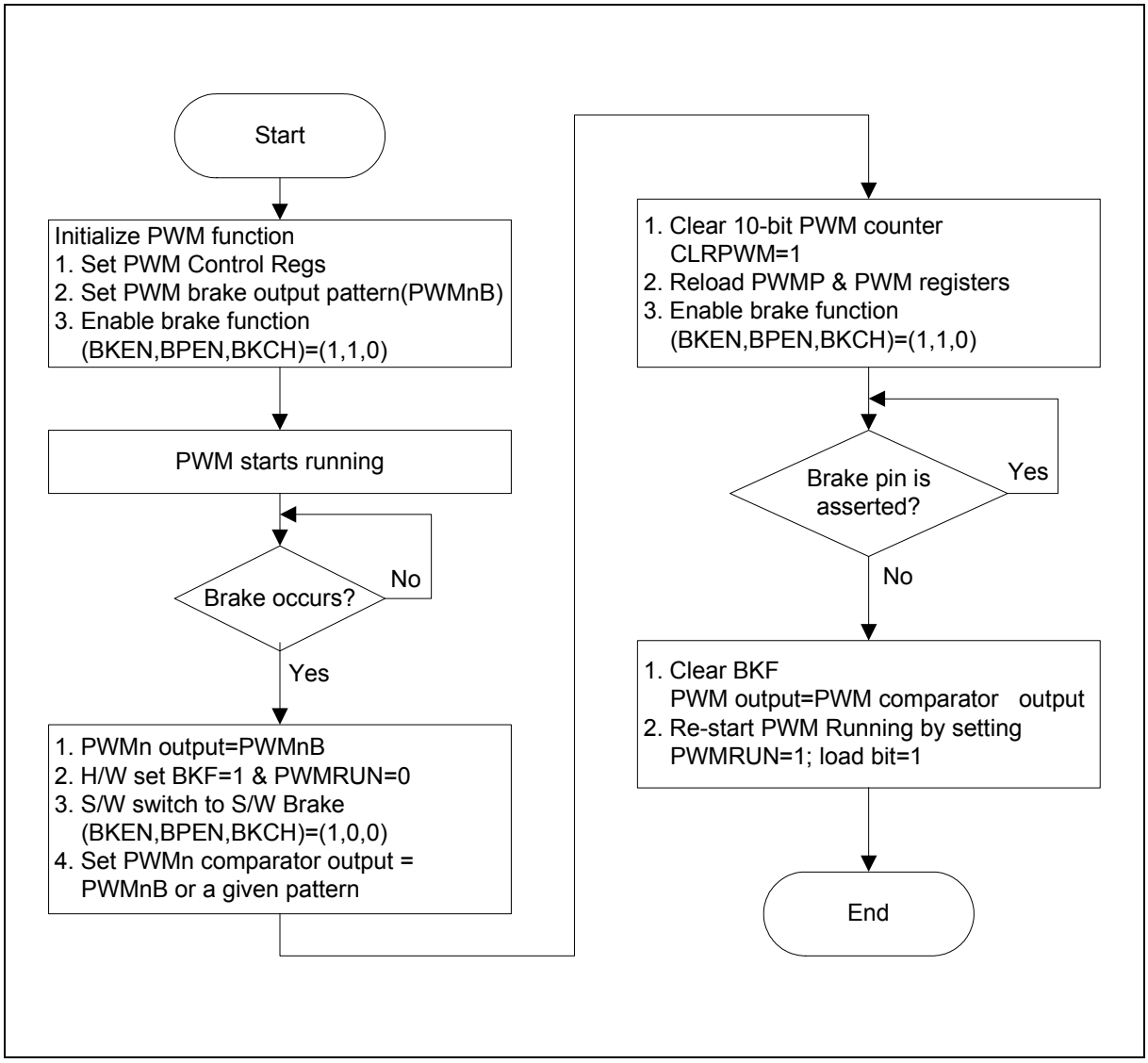
BIT	NAME	FUNCTION
7~1	-	Reserved
0	BKF	The external brake pin flag. 0: The PWM is not brake. 1: The PWM is brake by external brake pin. It will be cleared by software. If this bit is set, PWMRUN can't be set.

The W79E82X series chips have support brake function by software or external pin(P0.2). That brake control is by PWMCON2 register. The software brake and external pin brake setting as refer brake condition table. When brake is asserted, the PWM outputs are by PWMnB setting. By the software brake, the BKEN is set to "1" that will enable brake function and determined by BPEN and BKCH bits. The (BPEN, BKCH) = (0,0), brake is asserted. The (BPEN, BKCH) = (0,1), the PWM outputs are follow PWMRUN bit; When PWM is not running that mean is PWMRUN = 0, the PWM outputs are asserted by PWMnB setting; When PWM is running, the PWMRUN = 1, and keeping PWM outputs.

By the external brake pin(P0.2) brake, W79E82X series chips have brake interrupt service or polling brake flag (BKF) if external pin is asserted. If to decide P0.2 is low is asserted by BKPS = 0, the BKF(PWMCON3.0) will be set to "1" and PWNRUN will be cleared to stop PWM run, the PWM outputs condition are by PWMnB setting. After brake pin is release,

Since the Brake Pin being asserted will automatically clear the Run bit and BKF(PWMCON3.0) flag will be set, PWMCON1.7, the user program can poll this bit or enable PWM's brake interrupt to determine when the Brake Pin causes a brake to occur. The other method for detecting a brake caused by the Brake Pin would be to tie the Brake Pin to one of the external interrupt pins. This latter approach is needed if the Brake signal can be of insufficient length to ensure that it can be captured by a polling routine. When, after being asserted, the condition causing the brake is removed, the PWM outputs go to whatever state that had immediately prior to the brake. This means that in order to go from brake being asserted to having the PWM run without going through an indeterminate state care must be taken. If the

In order to smoothly release brake by external brake pin is asserted then PWM is going to run, the step interval as refer below figure.


Start
Initialize PWM function
1. Set PWM Control Regs
2. Set PWM brake output pattern(PWMnB)
3. Enable brake function
(BKEN,BPEN,BKCH)=(1,1,0)
PWM starts running
Brake occurs?
No
Yes
1. PWMn output=PWMnB
2. H/W set BKF=1 & PWMRUN=0
3. S/W switch to S/W Brake
(BKEN,BPEN,BKCH)=(1,0,0)
4. Set PWMn comparator output =
PWMnB or a given pattern
1. Clear 10-bit PWM counter
CLRPWM=1
2. Reload PWMP & PWM registers
3. Enable brake function
(BKEN,BPEN,BKCH)=(1,1,0)
Brake pin is asserted?
Yes
No
1. Clear BKF
PWM output=PWM comparator output
2. Re-start PWM Running by setting
PWMRUN=1; load bit=1
End

Continued

BIT	NAME	FUNCTION
3	-	Reserved.
2	-	Reserved.
1	Fosc1	CPU Oscillator Type Select bit 1
0	Fosc0	CPU Oscillator Type Select bit 0

Oscillator Configuration bits:

FOSC1	FOSC0	OSC SOURCE
0	0	4MHz ~ 20MHz crystal
0	1	Internal RC Oscillator
1	0	Reserved
1	1	External Oscillator in XTAL1

27.2 CONFIG2

CONFIG 2 :

7	6	5	4	3	2	1	0	
C7	C6	-	-	-	-	-	-	CONFIG Bit

C7: 16K/8K/4K/2K/1K Flash EPROM Code Lock Bit.
C6: 256/128 byte Data Lock Bit.

CONFIG Register 2

C7: 16K/8K/4K/2K/1K Flash EPROM Lock bit

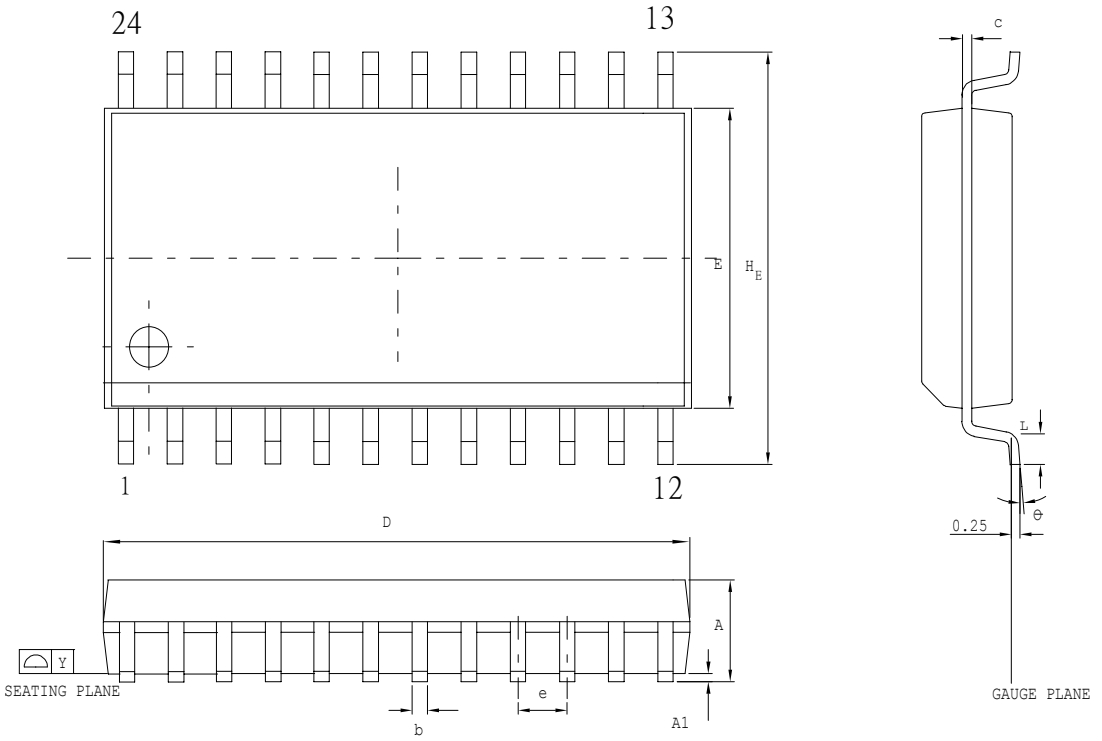
This bit is used to protect the customer's program code. It may be set after the programmer finishes the programming and verifies sequence. Once this bit is set to logic 0, both the Flash EPROM data and CONFIG Registers can not be accessed again.

C6: 256/128 byte Data Flash EPROM Lock bit

This bit is used to protect the customer's data code. It may be set after the programmer finishes the programming and verifies sequence. Once this bit is set to logic 0, both the data Flash EPROM and CONFIG Registers can not be accessed again.

34.3 24-pin SO

24L SOP-300mil



Control demensions are in milmeters .

SYMBOL	DIMENSION IN MM		DIMENSION IN INCH	
	MIN.	MAX.	MIN.	MAX.
A	2.35	2.65	0.093	0.104
A1	0.10	0.30	0.004	0.012
b	0.33	0.51	0.013	0.020
c	0.23	0.32	0.009	0.013
E	7.40	7.60	0.291	0.299
D	15.20	15.60	0.598	0.614
e	1.27 BSC		0.050 BSC	
H_E	10.00	10.65	0.394	0.419
Y	—	0.10	—	0.004
L	0.40	1.27	0.016	0.050
θ	0	8	0	8