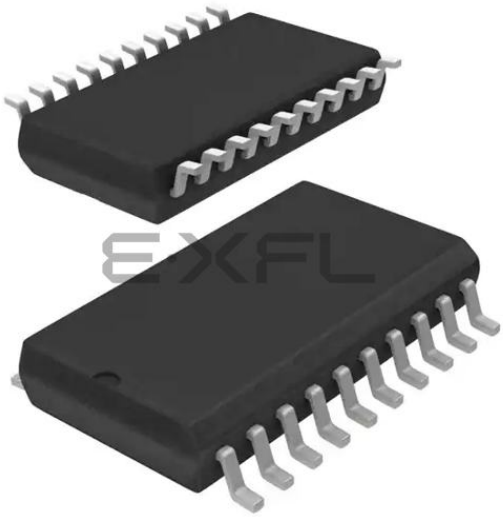
Nuvoton Technology Corporation - W79E823ASG Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

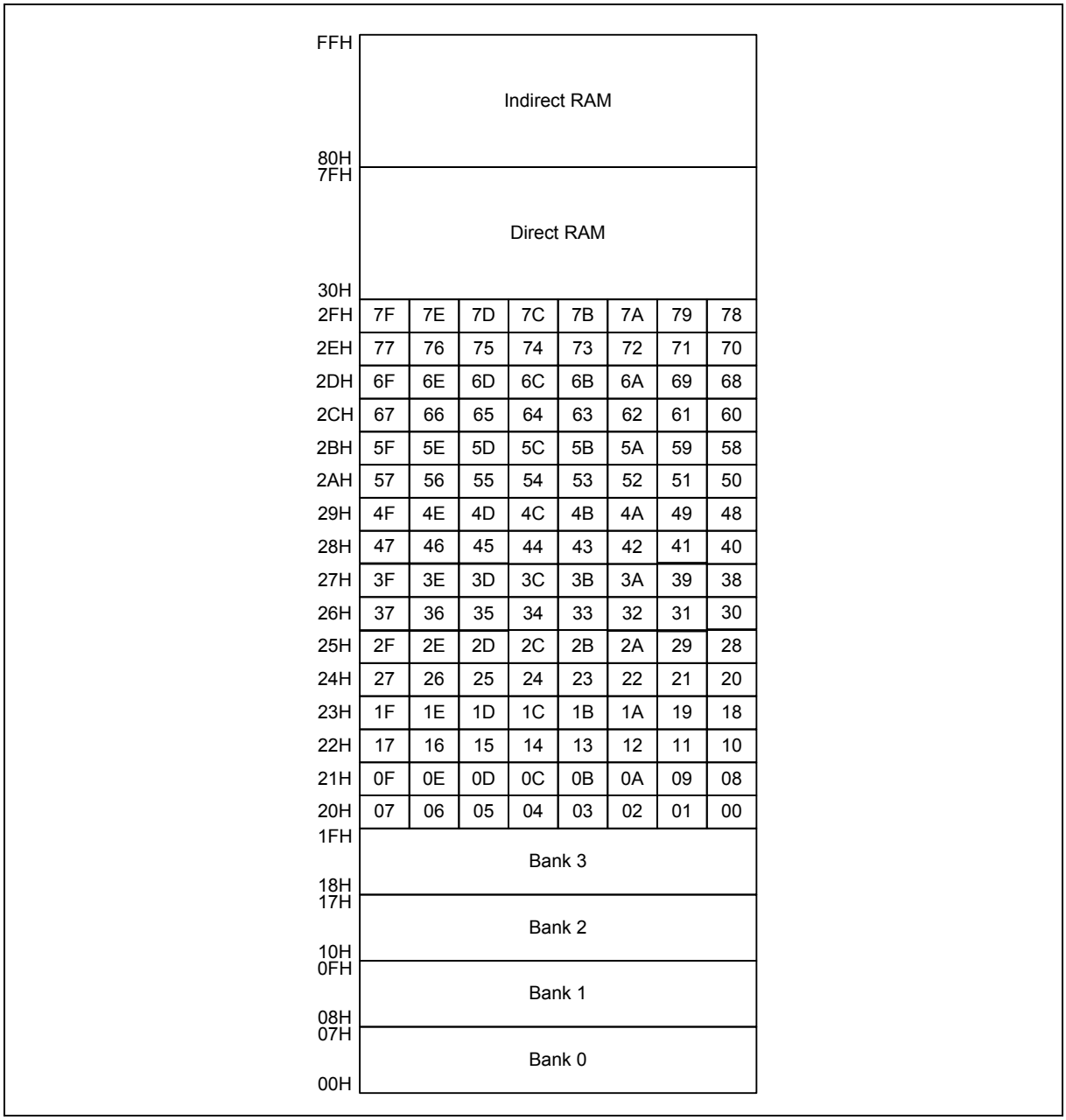
Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, UART/USART
Peripherals	Brown-out Detect/Reset, LED, LVD, POR, PWM, WDT
Number of I/O	18
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/w79e823asg

- Lead Free (RoHS) SOP 20: W79E825ASG
- Lead Free (RoHS) DIP 20: W79E824ADG
- Lead Free (RoHS) SOP 20: W79E824ASG
- Lead Free (RoHS) DIP 20: W79E823ADG
- Lead Free (RoHS) SOP 20: W79E823ASG
- Lead Free (RoHS) DIP 20: W79E822ADG
- Lead Free (RoHS) SOP 20: W79E822ASG
- Lead Free (RoHS) DIP 20: W79E821ADG
- Lead Free (RoHS) SOP 20: W79E821ASG

3. PARTS INFORMATION LIST

3.1 Lead Free (RoHS) Parts information list

PART NO.	EPROM FLASH SIZE	RAM	NVM FLASH EPROM	ADC	PWM	PACKAGE	REMARK
W79E825ADG	16KB	256B	256B	4x10Bit	4x10Bit	DIP-20 Pin	
W79E825ASG	16KB	256B	256B	4x10Bit	4x10Bit	SOP-20 Pin	
W79E824ADG	8KB	256B	256B	4x10Bit	4x10Bit	DIP-20 Pin	
W79E824ASG	8KB	256B	256B	4x10Bit	4x10Bit	SOP-20 Pin	
W79E823ADG	4KB	128B	128B	4x10Bit	4x10Bit	DIP-20 Pin	
W79E823ASG	4KB	128B	128B	4x10Bit	4x10Bit	SOP-20 Pin	
W79E822ADG	2KB	128B	128B	4x10Bit	4x10Bit	DIP-20 Pin	
W79E822ASG	2KB	128B	128B	4x10Bit	4x10Bit	SOP-20 Pin	
W79E821ADG	1KB	128B	128B	4x10Bit	4x10Bit	DIP-20 Pin	
W79E821ASG	1KB	128B	128B	4x10Bit	4x10Bit	SOP-20 Pin	



Working Registers

There are four sets of working registers, each consisting of eight 8-bit registers. These are termed ads Banks 0, 1, 2, and 3. Individual registers within these banks can be directly accessed by separate instructions. These individual registers are named as R0, R1, R2, R3, R4, R5, R6 and R7. However, at one time the W79E82X series can work with only one particular bank. The bank selection is done by setting RS1-RS0 bits in the PSW. The R0 and R1 registers are used to store the address for indirect accessing.

This is the high byte of the standard 8052 16-bit data pointer.

This is the high byte of the DPTR 16-bit data pointer.

POWER CONTROL

Bit:	7	6	5	4	3	2	1	0
	SMOD	SMOD0	BOF	POR	GF1	GF0	PD	IDL

Mnemonic: PCON Address: 87h

BIT	NAME	FUNCTION
7	SMOD	1: This bit doubles the serial port baud rate in mode 1, 2, and 3.
6	SMOD0	0: Framing Error Detection Disable. SCON.7 acts as per the standard 8052 function. 1: Framing Error Detection Enable, then and SCON.7 indicates a Frame Error and acts as the FE flag.
5	BOF	0: Cleared by software. 1: Set automatically when a brownout reset or interrupt has occurred. Also set at power on.
4	POR	0: Cleared by software. 1: Set automatically when a power-on reset has occurred.
3	GF1	General purpose user flags.
2	GF0	General purpose user flags.
1	PD	1: the CPU goes into the POWER DOWN mode. In this mode, all the clocks are stopped and program execution is frozen.
0	IDL	1: The CPU goes into the IDLE mode. In this mode, the clocks CPU clock stopped, so program execution is frozen. But the clock to the serial, timer and interrupt blocks is not stopped, and these blocks continue operating.

TIMER CONTROL

Bit:	7	6	5	4	3	2	1	0
	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

Mnemonic: TCON Address: 88h

BIT	NAME	FUNCTION
7	TF1	Timer 1 overflow flag: This bit is set when Timer 1 overflows. It is cleared automatically when the program does a timer 1 interrupt service routine. Software can also set or clear this bit.
6	TR1	Timer 1 run control: This bit is set or cleared by software to turn timer/counter on or off.
5	TF0	Timer 0 overflow flag: This bit is set when Timer 0 overflows. It is cleared automatically when the program does a timer 0 interrupt service routine. Software can also set or clear this bit.
4	TR0	Timer 0 run control: This bit is set or cleared by software to turn timer/counter on or off.

M1, M0: Mode Select bits:

M1	M0	MODE
0	0	Mode 0: 8-bits with 5-bit prescale.
0	1	Mode 1: 16-bits, no prescale.
1	0	Mode 2: 8-bits with auto-reload from THx
1	1	Mode 3: (Timer 0) TL0 is an 8-bit timer/counter controlled by the standard Timer 0 control bits. TH0 is a 8-bit timer only controlled by Timer 1 control bits. (Timer 1) Timer/counter is stopped.

TIMER 0 LSB

Bit:	7	6	5	4	3	2	1	0
	TL0.7	TL0.6	TL0.5	TL0.4	TL0.3	TL0.2	TL0.1	TL0.0

Mnemonic: TL0 Address: 8Ah

TL0.7-0: Timer 0 LSB

TIMER 1 LSB

Bit:	7	6	5	4	3	2	1	0
	TL1.7	TL1.6	TL1.5	TL1.4	TL1.3	TL1.2	TL1.1	TL1.0

Mnemonic: TL1 Address: 8Bh

TL1.7-0: Timer 1 LSB

TIMER 0 MSB

Bit:	7	6	5	4	3	2	1	0
	TH0.7	TH0.6	TH0.5	TH0.4	TH0.3	TH0.2	TH0.1	TH0.0

Mnemonic: TH0 Address: 8Ch

TH0.7-0: Timer 0 MSB

TIMER 1 MSB

Bit:	7	6	5	4	3	2	1	0
	TH1.7	TH1.6	TH1.5	TH1.4	TH1.3	TH1.2	TH1.1	TH1.0

Mnemonic: TH1 Address: 8Dh

TH1.7-0: Timer 1 MSB

Clock Control

Bit:	7	6	5	4	3	2	1	0
	-	-	-	T1M	T0M	-	-	-

Mnemonic: CKCON Address: 8Eh

BIT	NAME	FUNCTION
7	-	Reserved
6	-	Reserved
5	CE2	Comparator enable: 0: Disable Comparator. 1: Enabled Comparator. Comparator output need wait stable 10 us after CE2 is first set.
4	CP2	Comparator positive input select: 0: CIN2A is selected as the positive comparator input. 1: CIN2B is selected as the positive comparator input.
3	CN2	Comparator negative input select: 0: The comparator reference pin CMPREF is selected as the negative comparator input. 1: The internal comparator reference Vref is selected as the negative comparator input.
2	OE2	Output enable: 1: The comparator output is connected to the CMP2 pin if the comparator is enabled (CE2 = 1). This output is asynchronous to the CPU clock.
1	CO2	Comparator output: Synchronized to the CPU clock to allow reading by software. Cleared when the comparator is disabled (CE2 = 0).
0	CMF2	Comparator interrupt flag: This bit is set by hardware whenever the comparator output CO2 changes state. This bit will cause a hardware interrupt if enabled and of sufficient priority. Cleared by software and when the comparator is disabled (CE2 = 0).

Port 0 Output Mode 1

Bit:	7	6	5	4	3	2	1	0
	P0M1.7	P0M1.6	P0M1.5	P0M1.4	P0M1.3	P0M1.2	P0M1.1	P0M1.0

Mnemonic: P0M1 Address: B1h

Port 0 Output Mode 2

Bit:	7	6	5	4	3	2	1	0
	P0M2.7	P0M2.6	P0M2.5	P0M2.4	P0M2.3	P0M2.2	P0M2.1	P0M2.0

Mnemonic: P0M2 Address: B2h

Port 1 Output Mode 1

Bit:	7	6	5	4	3	2	1	0
	P1M1.7	P1M1.6	-	P1M1.4	-	-	P1M1.1	P1M1.0

Mnemonic: P1M1 Address: B3h

Port 1 Output Mode 2

Bit:	7	6	5	4	3	2	1	0
	P1M2.7	P1M2.6	-	P1M2.4	-	-	P1M2.1	P1M2.0

Mnemonic: P1M2 Address: B4h

Port 2 Output Mode 1

Bit:	7	6	5	4	3	2	1	0
	P2S	P1S	P0S	ENCLK	T1OE	T0OE	P2M1.1	P2M1.0

Mnemonic: P2M1 Address: B5h

BIT	NAME	FUNCTION
7	P2S	1: Enables Schmitt trigger inputs on Port 2.
6	P1S	1: Enables Schmitt trigger inputs on Port 1.
5	P0S	1: Enables Schmitt trigger inputs on Port 0.
4	ENCLK	1: To use the on-chip RC oscillator, a clock output is enabled on the XTAL2 pin (P2.0).
3	T1OE	1: The P0.7 pin is toggled whenever Timer 1 overflows. The output frequency is therefore one half of the Timer 1 overflow rate.
2	T0OE	1: The P1.2 pin is toggled whenever Timer 1 overflows. The output frequency is therefore one half of the Timer 1 overflow rate.
1	P2M1.1	To control the output configuration of P2.1.
0	P2M1.0	To control the output configuration of P2.0.

Port 2 Output Mode 2

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	P2M2.1	P2M2.0

Mnemonic: P2M2 Address: B6h

Port Output Configuration Settings:

PXM1.Y	PXM2.Y	PORT INPUT/OUTPUT MODE
0	0	Quasi-bidirectional
0	1	Push-Pull
1	0	Input Only (High Impedance) P2M1.PxS=0, TTL input P2M1.PxS=1, Schmitt input
1	1	Open Drain

Interrupt High Priority

Bit:	7	6	5	4	3	2	1	0
	-	PADCH	PBOH	PSH	PT1H	PX1H	PT0H	PX0H

Mnemonic: IP0H Address: B7h

BIT	NAME	FUNCTION
7	EER	NVM page(n) erase bit. 0: Without erase NVM page(n). 1: Set this bit to erase NVM data of page(n) to FFH. The NVM has 4 pages and each page have 64 bytes data memory. Before select page by NVMADDR register that will automatic enable page area, after set this bit, the page will be erased and program counter will halt at this instruction. After finished, program counter will kept next instruction then executed. The NVM page's address define as below table.
6	EWR	NVM data write bit 0: Without write NVM data. 1: Set this bit to write NVM bytes and program counter will halt at this instruction. After write is finished, program counter will kept next instruction then executed.
5~0	-	Reserved

NVM Page(n) Area Definition Table:

PAGE	START ADDRESS	END ADDRESS
0	00H	3FH
1	40H	7FH
2	***80H***	***BFH***
3	***C0H***	***FFH***

Note: The W79E823, W79E822 and W79E821 without page 2 and page 3.

NVM DATA

Bit:	7	6	5	4	3	2	1	0
	NVMDAT.7	NVMDAT.6	NVMDAT.5	NVMDAT.4	NVMDAT.3	NVMDAT.2	NVMDAT.1	NVMDAT.0

Mnemonic: NVMDATA Address: CFh

BIT	NAME	FUNCTION
7~0	NVMDAT.7 ~ NVMDAT.0	The NVM data write register. The read NVM data is by MOVC instruction.

PROGRAM STATUS WORD

Bit:	7	6	5	4	3	2	1	0
	CY	AC	F0	RS1	RS0	OV	F1	P

Mnemonic: PSW Address: D0h

BIT	NAME	FUNCTION
7	CY	Carry flag: Set for an arithmetic operation which results in a carry being generated from the ALU. It is also used as the accumulator for the bit operations.
6	AC	Auxiliary carry: Set when the previous operation resulted in a carry from the high order nibble.

Continued.

BIT	NAME	FUNCTION
5	F0	User flag 0: The General purpose flag that can be set or cleared by the user.
4	RS1	Register bank select bits:
3	RS0	Register bank select bits:
2	OV	Overflow flag: Set when a carry was generated from the seventh bit but not from the 8th bit as a result of the previous operation, or vice-versa.
1	F1	User Flag 1: The General purpose flag that can be set or cleared by the user by software.
0	P	Parity flag: Set/cleared by hardware to indicate odd/even number of 1's in the accumulator.

RS.1-0: Register Bank Selection Bits:

RS1	RS0	REGISTER BANK	ADDRESS
0	0	0	00-07h
0	1	1	08-0Fh
1	0	2	10-17h
1	1	3	18-1Fh

PWM Counter High Bits Register

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	PWMP.9	PWMP.8

Mnemonic: PWMPH Address: D1h

BIT	NAME	FUNCTION
7~2	-	Reserved
1~0	PWMP.9 ~PWMP.8	The PWM Counter Register bit9~8.

PWM 0 High Bits Register

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	PWM0.9	PWM0.8

Mnemonic: PWM0H Address: D2h

BIT	NAME	FUNCTION
7~2	-	Reserved
1~0	PWM0.9 ~PWM0.8	The PWM 0 High Bits Register bit 9~8.

BIT	NAME	FUNCTION
7	PWMRUN	0: The PWM is not running. 1: The PWM counter is running.
6	Load	0: The registers value of PWMP and Comparators are never loaded to counter and Comparator registers. 1: The PWMP register will be load value to counter register after counter underflow, and hardware will clear by next clock cycle.
5	CF	0: The 10-bit counter down count is not underflow. 1: The 10-bit counter down count is underflow. It will be cleared by software.
4	CLRPWM	1: Clear 10-bit PWM counter to 000H.
3	PWM3I	0: PWM3 out is non-inverted. 1: PWM3 output is inverted.
2	PWM2I	0: PWM2 out is non-inverted. 1: PWM2 output is inverted.
1	PWM1I	0: PWM1 out is non-inverted. 1: PWM1 output is inverted.
0	PWM0I	0: PWM0 out is non-inverted. 1: PWM0 output is inverted.

PWM 2 Low Bits Register

Bit:	7	6	5	4	3	2	1	0
	PWM2.7	PWM2.6	PWM2.5	PWM2.4	PWM2.3	PWM2.2	PWM2.1	PWM2.0

Mnemonic: PWM2L Address: DDh

BIT	NAME	FUNCTION
7~0	PWM2.7 ~PWM2.0	PWM 2 Low Bits Register.

PWM 3 Low Bits Register

Bit:	7	6	5	4	3	2	1	0
	PWM3.7	PWM3.6	PWM3.5	PWM3.4	PWM3.3	PWM3.2	PWM3.1	PWM3.0

Mnemonic: PWM3L Address: DEh

BIT	NAME	FUNCTION
7~0	PWM3.7 ~PWM3.0	PWM 3 Low Bits Register.

PWM Control Register 2

Bit:	7	6	5	4	3	2	1	0
	BKCH	BKPS	BPEN	BKEN	PWM3B	PWM2B	PWM1B	PWM0B

Mnemonic: PWMCON2 Address: DFh

SFR RESET VALUE

SFR NAME	RESET VALUE	SFR NAME	RESET VALUE
P0	11111111B	I2DAT	xxxxxxxxB
SP	00000111B	I2STATUS	00000xxxB
DPL	00000000B	I2TIMER	00000000B
DPH	00000000B	I2CLK	00000000B
PCON	00xx0000B	I2CON	00000000B
TCON	00000000B	I2ADDR	xxxxxxxxB
TMOD	00000000B	TA	00000000B
TL0	00000000B	PSW	00000000B
TL1	00000000B	PWMP1	xxxxxx00B
TH0	00000000B	PWM0H	xxxxxx00B
TH1	00000000B	PWM1H	xxxxxx00B
CKCON	00000000B	PWM2H	xxxxxx00B
P1	1111xx11B	PWM3H	xxxxxx00B
DIVM	00000000B	WDCON	0x000000B
SCON	00000000B	PWMP0	00000000B
SBUF	xxxxxxxxB	PWM0L	00000000B
P2	xxxxx11B	PWM1L	00000000B
KBI	00000000B	PWMCON1	00000000B
AUXR1	00000000B	PWM2L	00000000B
IE	00000000B	PWM3L	00000000B
SADDR	00000000B	PWMCON2	00000000B
CMP1	00000000B	ACC	00000000B
CMP2	00000000B	ADCCON	xx000x00B
P0M1	00000000B	ADCH	xxxxxxxxB
P0M2	00000000B	IE1	xx000000B
P1M1	00000000B	B	00000000B
P1M2	00000000B	P0IDS	00000000B
P2M1	00000000B	IPH	xx000000B
P2M2	xxxxxx00B	IP1	xx000000B
IP0H	x0000000B		
IP0	x0000000B		
SADEN	00000000B		

The processor responds to a valid interrupt by executing an LCALL instruction to the appropriate service routine. This may or may not clear the flag which caused the interrupt. In case of Timer interrupts, the TF0 or TF1 flags are cleared by hardware whenever the processor vectors to the appropriate timer service routine. In case of external interrupt, INT0 and INT1, the flags are cleared only if they are edge triggered. In case of Serial interrupts, the flags are not cleared by hardware. The Watchdog timer interrupt flag WDIF has to be cleared by software. The hardware LCALL behaves exactly like the software LCALL instruction. This instruction saves the Program Counter contents onto the Stack, but does not save the Program Status Word PSW. The PC is reloaded with the vector address of that interrupt which caused the LCALL. These address of vector for the different sources are as follows

Vector locations for interrupt sources

SOURCE	VECTOR ADDRESS	SOURCE	VECTOR ADDRESS
External Interrupt 0	0003h	Timer 0 Overflow	000Bh
External Interrupt 1	0013h	Timer 1 Overflow	001Bh
Serial Port	0023h	Brownout Interrupt	002Bh
I2C Interrupt	0033h	KBI Interrupt	003Bh
Comparator 2 Interrupt	0043h	-	004Bh
Watchdog Timer	0053h	ADC Interrupt	005Bh
Comparator 1 Interrupt	0063h	-	006Bh
PWM Brake Interrupt	0073h	-	007Bh

Four-level interrupt priority

PRIORITY BITS		INTERRUPT PRIORITY LEVEL
IPXH	IPX	
0	0	Level 0 (lowest priority)
0	1	Level 1
1	0	Level 2
1	1	Level 3 (highest priority)

The vector table is not evenly spaced; this is to accommodate future expansions to the device family.

Execution continues from the vectored address till an RETI instruction is executed. On execution of the RETI instruction the processor pops the Stack and loads the PC with the contents at the top of the stack. The user must take care that the status of the stack is restored to what is was after the hardware LCALL, if the execution is to return to the interrupted program. The processor does not notice anything if the stack contents are modified and will proceed with execution from the address put back into PC. Note that a RET instruction would perform exactly the same process as a RETI instruction, but it would not inform the Interrupt Controller that the interrupt service routine is completed, and would leave the controller still thinking that the service routine is underway.

13. PROGRAMMABLE TIMERS/COUNTERS

The W79E82X series have two 16-bit programmable timer/counters and one programmable Watchdog Timer. The Watchdog Timer is operationally quite different from the other two timers.

13.1 TIMER/COUNTERS 0 & 1

The W79E82X series have two 16-bit Timer/Counters. Each of these Timer/Counters has two 8 bit registers which form the 16 bit counting register. For Timer/Counter 0 they are TH0, the upper 8 bits register, and TL0, the lower 8 bit register. Similarly Timer/Counter 1 has two 8 bit registers, TH1 and TL1. The two can be configured to operate either as timers, counting machine cycles or as counters counting external inputs.

When configured as a "Timer", the timer counts clock cycles. The timer clock can be programmed to be thought of as 1/12 of the system clock or 1/4 of the system clock. In the "Counter" mode, the register is incremented on the falling edge of the external input pin, T0 in case of Timer 0, and T1 for Timer 1. The T0 and T1 inputs are sampled in every machine cycle at C4. If the sampled value is high in one machine cycle and low in the next, then a valid high to low transition on the pin is recognized and the count register is incremented. Since it takes two machine cycles to recognize a negative transition on the pin, the maximum rate at which counting will take place is 1/8 of the master clock frequency. In either the "Timer" or "Counter" mode, the count register will be updated at C3. Therefore, in the "Timer" mode, the recognized negative transition on pin T0 and T1 can cause the count register value to be updated only in the machine cycle following the one in which the negative edge was detected.

The "Timer" or "Counter" function is selected by the "$C/\overline{T}$" bit in the TMOD Special Function Register. Each Timer/Counter has one selection bit for its own; bit 2 of TMOD selects the function for Timer/Counter 0 and bit 6 of TMOD selects the function for Timer/Counter 1. In addition each Timer/Counter can be set to operate in any one of four possible modes. The mode selection is done by bits M0 and M1 in the TMOD SFR.

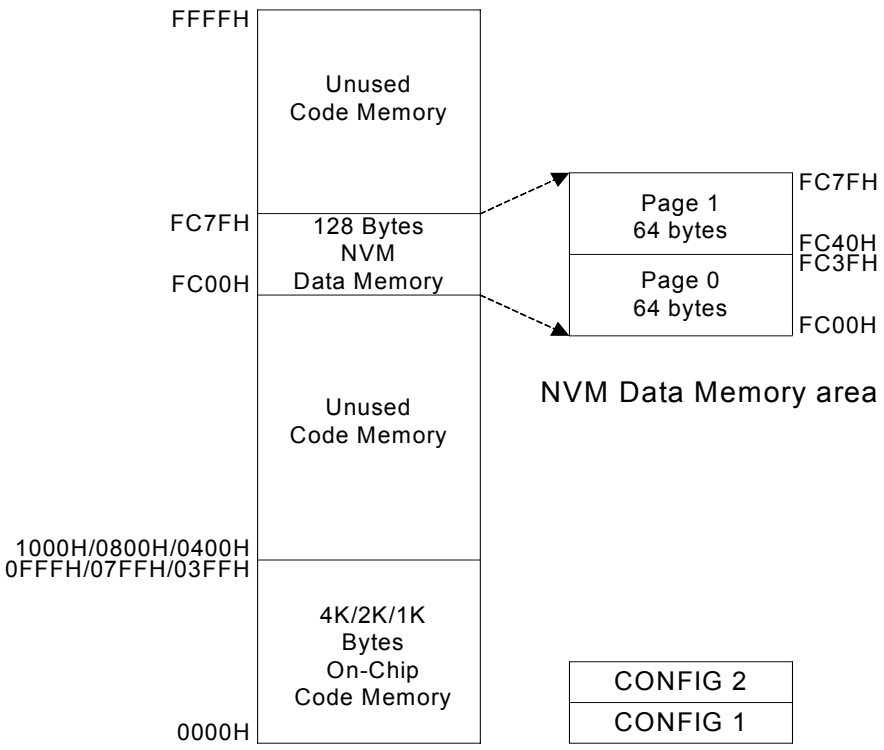
13.2 Time-Base Selection

The W79E82X series give the user two modes of operation for the timer. The timers can be programmed to operate like the standard 8051 family, counting at the rate of 1/12 of the clock speed. This will ensure that timing loops on the W79E82X series and the standard 8051 can be matched. This is the default mode of operation of the W79E82X series timers. The user also has the option to count in the turbo mode, where the timers will increment at the rate of 1/4 clock speed. This will straight-away increase the counting speed three times. This selection is done by the T0M and T1M bit in CKCON SFR. A reset sets these bits to 0, and the timers then operate in the standard 8051 mode. The user should set these bits to 1 if the timers are to operate in turbo mode.

13.3 MODE 0

In Mode 0, the timer/counters act as a 8-bit counter with a 5-bit, divide by 32 pre-scale. In this mode we have a 13-bit timer/counter. The 13-bit counter consists of 8 bits of THx and 5 lower bits of TLx. The upper 3 bits of TLx are ignored.

The negative edge of the clock is increments count in the TLx register. When the fifth bit in TLx moves from 1 to 0, then the count in the THx register is incremented. When count in THx moves from FFh to 00h, then the overflow flag TFx in TCON SFR is set. The counted input is enabled only if TRx is set



W79E823/W79E822/W79E821 Memory Map

BIT	NAME	FUNCTION
7~0	NVMADDR.7 ~ NVMADDR.0	The NVM address: The register is indicated NVM data memory of low byte address on On-Chip code memory space.

Mnemonic: NVMADDR Address: C6h

bit is the stop bit, which is 1 in case of a valid frame. If SM2 is 1, then RI is set only if a valid frame is received and the received byte matches the Given or Broadcast address.

The Master processor can selectively communicate with groups of slaves by using the Given Address. All the slaves can be addressed together using the Broadcast Address. The addresses for each slave are defined by the SADDR and SADEN SFRs. The slave address is an 8-bit value specified in the SADDR SFR. The SADEN SFR is actually a mask for the byte value in SADDR. If a bit position in SADEN is 0, then the corresponding bit position in SADDR is don't care. Only those bit positions in SADDR whose corresponding bits in SADEN are 1 are used to obtain the Given Address. This gives the user flexibility to address multiple slaves without changing the slave address in SADDR.

The following example shows how the user can define the Given Address to address different slaves.

Slave 1:

SADDR	1010 0100
SADEN	1111 1010
Given	1010 0x0x

Slave 2:

SADDR	1010 0111
SADEN	1111 1001
Given	1010 0xx1

The Given address for slave 1 and 2 differ in the LSB. For slave 1, it is a don't care, while for slave 2 it is 1. Thus to communicate only with slave 1, the master must send an address with LSB = 0 (1010 0000). Similarly the bit 1 position is 0 for slave 1 and don't care for slave 2. Hence to communicate only with slave 2 the master has to transmit an address with bit 1 = 1 (1010 0011). If the master wishes to communicate with both slaves simultaneously, then the address must have bit 0 = 1 and bit 1 = 0. The bit 3 position is don't care for both the slaves. This allows two different addresses to select both slaves (1010 0001 and 1010 0101).

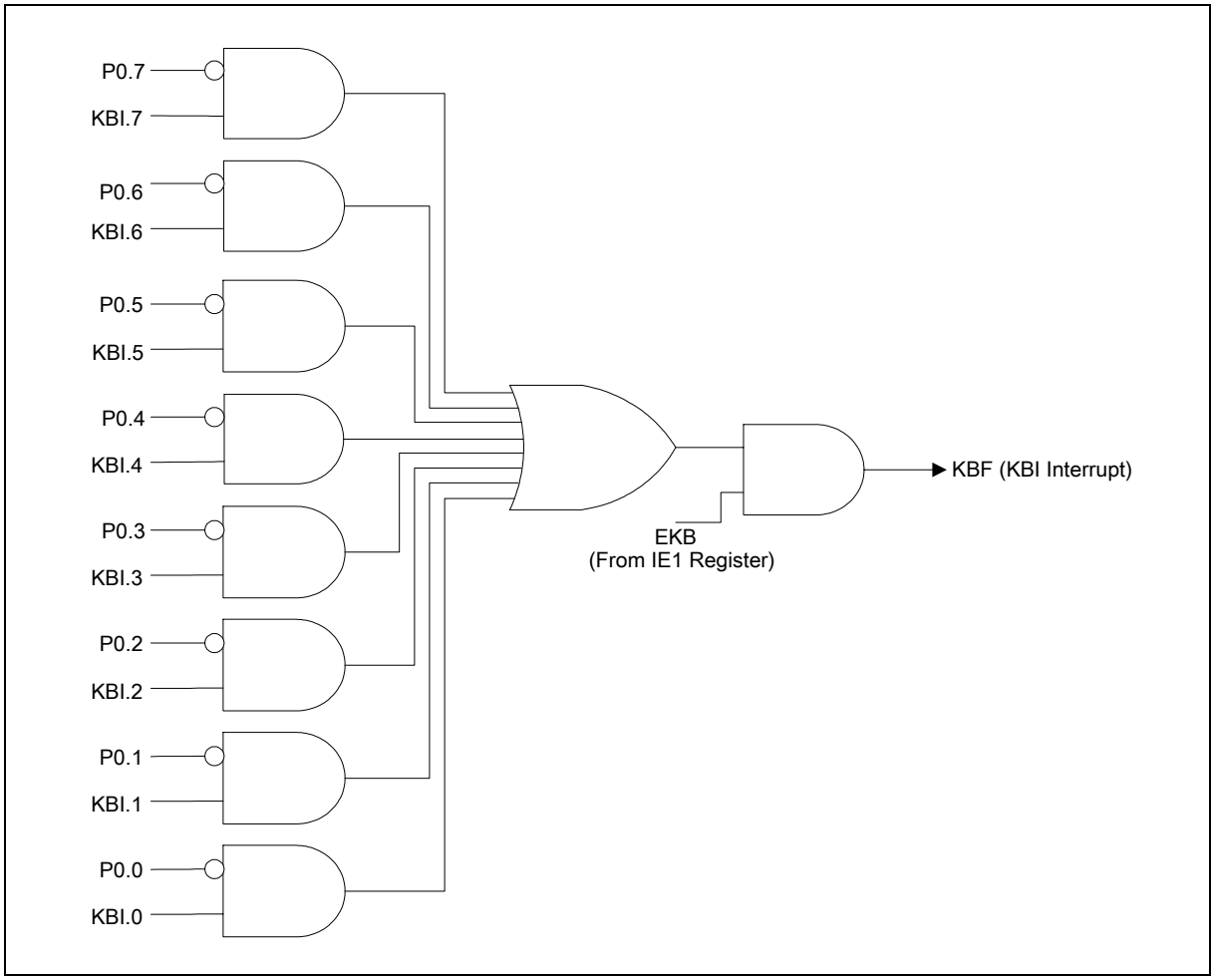
The master can communicate with all the slaves simultaneously with the Broadcast Address. This address is formed from the logical OR of the SADDR and SADEN SFRs. The zeros in the result are defined as don't cares In most cases the Broadcast Address is FFh. In the previous case, the Broadcast Address is (1111111X) for slave 1 and (11111111) for slave 2.

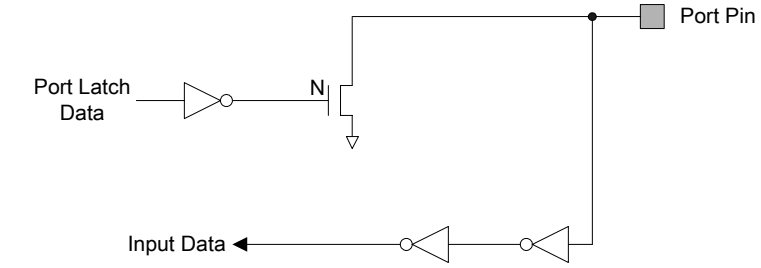
The SADDR and SADEN SFRs are located at address A9h and B9h respectively. On reset, these two SFRs are initialized to 00h. This results in Given Address and Broadcast Address being set as XXXX XXXX(i.e. all bits don't care). This effectively removes the multiprocessor communications feature, since any selectivity is disabled.

18. KEYBOARD INTERRUPT (KBI)

The W79E82X series are provided 8 keyboard interrupt function to detect keypad status which key is acted, and allow a single interrupt to be generated when any key is pressed on a keyboard or keypad connected to specific pins of the W79E82X series, as shown below Figure. This interrupt may be used to wake up the CPU from Idle or Power Down modes, after chip is in Power Down or Idle Mode.

To support keyboard function is by Port 0. It can allow any or all pins of Port 0 to be enabled to cause this interrupt. Port pins are enabled by the setting of bits of KBI0 ~ KBI7 in the KBI register, as shown below Figure. The Keyboard Interrupt Flag (KBF) in the AUXR1 register is set when any enabled pin is pulled low while the KBI interrupt function is active, and the low pulse must more than 1 machine cycle, an interrupt will be generated if it has been enabled. The KBF bit set by hardware and must be cleared by software. In order to determine which key was pressed, the KBI will allow the interrupt service routine to poll port 0.





Open Drain Output

23. PULSE WIDTH MODULATED OUTPUTS (PWM)

The W79E82X series have four-channels Pulse Width Modulated (PWM), and the PWM outputs are PWM0(P0.1), PWM1(P1.6), PWM2(P1.7) and PWM3(P0.0). When PRHI is set to “1”, after chip reset, the internal output of the each PWM channels are “1”. When PRHI is set to “0”, after chip reset, the internal output of the each PWM channels are “0”. So, in the case, if PWM output pins will output “1”, it must be written a “1” to each PWM pins to high state. A block diagram is shown as below Figure.

The W79E82X series support 10-bits down counter which clock source of counter is use the internal microcontroller clock as its input. The PWM counter clock, has the same frequency as the clock source F_{CPU} = F_{OSC}. When the counter reaches underflow it will automatic reloaded from counter register. The PWM frequency is given by: f_{PWM} = F_{CPU} / (PWMP+1), where PWMP is 10-bits register of PWMPH.1, PWMPH.0 and PWMPL.7~PWMPL.0.

When PWMP register is written, it will automatically load by PWMRUN, Load and CF is “1”, where CF flag is 10-bits down counter reaches underflow, the CF flag will be cleared by software. When PWMP register was load to counter register, the load bit will automatically clear by next cycle. If the first PWM output cycle is correct by PWMP setting, it will be clear by CLRPWM to clear 10-bits counter to 000H, then set PWMRUN and load bits to run PWM.

The pulse width of each PWM output is determined by the Compare registers of PWM0L through PWM3L and PWM0H through PWM3H. When PWM compare register is greater than 10-bits counter register, the PWM output is low. If want to change output width of PWM, after writer PWMn register, must set load bit to “1” then will be loaded to compare register by next underflow. The PWM output high pulses width is given by:

t_{HI} = (PWMP – PWMn+1). Notice, if compare register is set to 000H, the PWMn output is high, and if compare register is set to 3FFH, the PWMn output is low.

25.2.4 The I2C Clock Baud Rate Bits, I2CLK

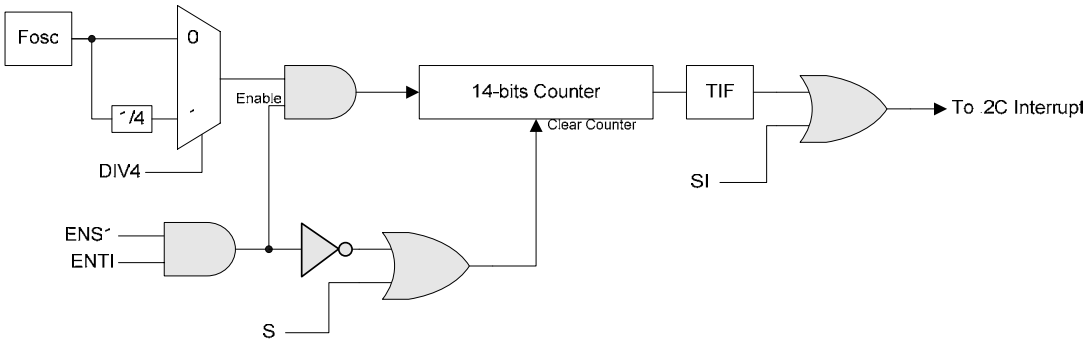
The data baud rate of I2C is determines by I2CLK register when SIO1 is in a master mode. It is not important when SIO1 is in a slave mode. In the slave modes, SIO1 will automatically synchronize with any clock frequency up to 400 KHz from master I2C device.

The data baud rate of I2C setting is Data Baud Rate of I2C = Fcpu / (I2CLK+1). The Fcpu=Fosc/4. If Fosc = 16MHz, the I2CLK = 40(28H), so data baud rate of I2C = 16MHz /(4X (40 +1)) = 97.56Kbits/sec. The block diagram is as below figure.

Bit:	7	6	5	4	3	2	1	0
	I2CLK.7	I2CLK.6	I2CLK.5	I2CLK.4	I2CLK.3	I2CLK.2	I2CLK.1	I2CLK.0

Mnemonic: I2CLK Address: BEh

BIT	NAME	FUNCTION
7 ~ 0	I2CLK	The I2C clock baud rate bits.



I2C Timer Count Block Diagram

25.2.5 The Status Register, I2STATUS

I2STATUS is an 8-bit read-only register. The three least significant bits are always 0. The five most significant bits contain the status code. There are 23 possible status codes. When I2STATUS contains F8H, no serial interrupt is requested. All other I2STATUS values correspond to defined SIO1 states. When each of these states is entered, a status interrupt is requested (SI = 1). A valid status code is present in I2STATUS one machine cycle after SI is set by hardware and is still present one machine cycle after SI has been reset by software.

In addition, state 00H stands for a Bus Error. A Bus Error occurs when a START or STOP condition is present at an illegal position in the format frame. Examples of illegal positions are during the serial transfer of an address byte, a data byte or an acknowledge bit.

Continued

BIT	NAME	FUNCTION
3	-	Reserved.
2	-	Reserved.
1	Fosc1	CPU Oscillator Type Select bit 1
0	Fosc0	CPU Oscillator Type Select bit 0

Oscillator Configuration bits:

FOSC1	FOSC0	OSC SOURCE
0	0	4MHz ~ 20MHz crystal
0	1	Internal RC Oscillator
1	0	Reserved
1	1	External Oscillator in XTAL1

27.2 CONFIG2

CONFIG 2 :

7	6	5	4	3	2	1	0	
C7	C6	-	-	-	-	-	-	CONFIG Bit

C7: 16K/8K/4K/2K/1K Flash EPROM Code Lock Bit.
C6: 256/128 byte Data Lock Bit.

CONFIG Register 2

C7: 16K/8K/4K/2K/1K Flash EPROM Lock bit

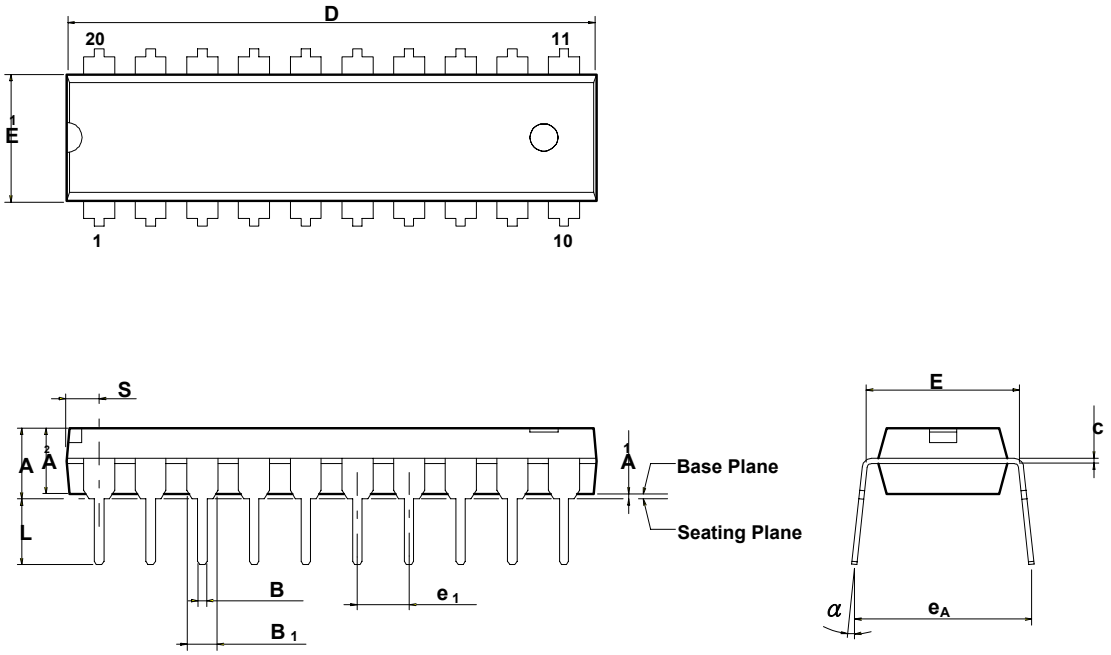
This bit is used to protect the customer's program code. It may be set after the programmer finishes the programming and verifies sequence. Once this bit is set to logic 0, both the Flash EPROM data and CONFIG Registers can not be accessed again.

C6: 256/128 byte Data Flash EPROM Lock bit

This bit is used to protect the customer's data code. It may be set after the programmer finishes the programming and verifies sequence. Once this bit is set to logic 0, both the data Flash EPROM and CONFIG Registers can not be accessed again.

34.2 20-pin DIP

20L PDIP 300mil



Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.175	—	—	4.45
A_1	0.010	—	—	0.25	—	—
A_2	0.125	0.130	0.135	3.18	3.30	3.43
B	0.016	0.018	0.022	0.41	0.46	0.56
B_1	0.058	0.060	0.064	1.47	1.52	1.63
c	0.008	0.010	0.014	0.20	0.25	0.36
D	—	1.026	1.040	—	20.06	26.42
E	0.290	0.300	0.310	7.37	7.62	7.87
E_1	0.245	0.250	0.255	6.22	6.35	6.48
e_1	0.090	0.100	0.110	2.29	2.54	2.79
L	0.120	0.130	0.140	3.05	3.30	3.56
α	0	—	15	0	—	15
e_A	0.335	0.355	0.375	8.51	9.02	9.53
S	—	—	0.075	—	—	1.91