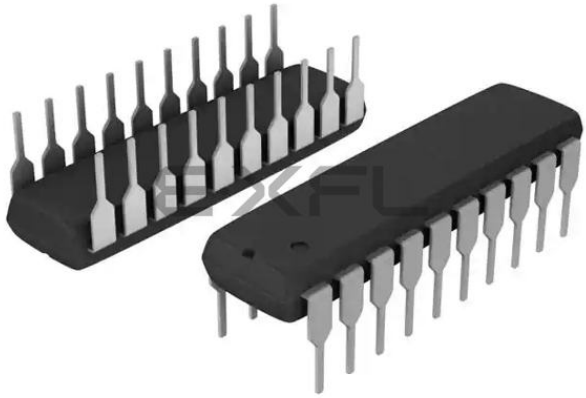

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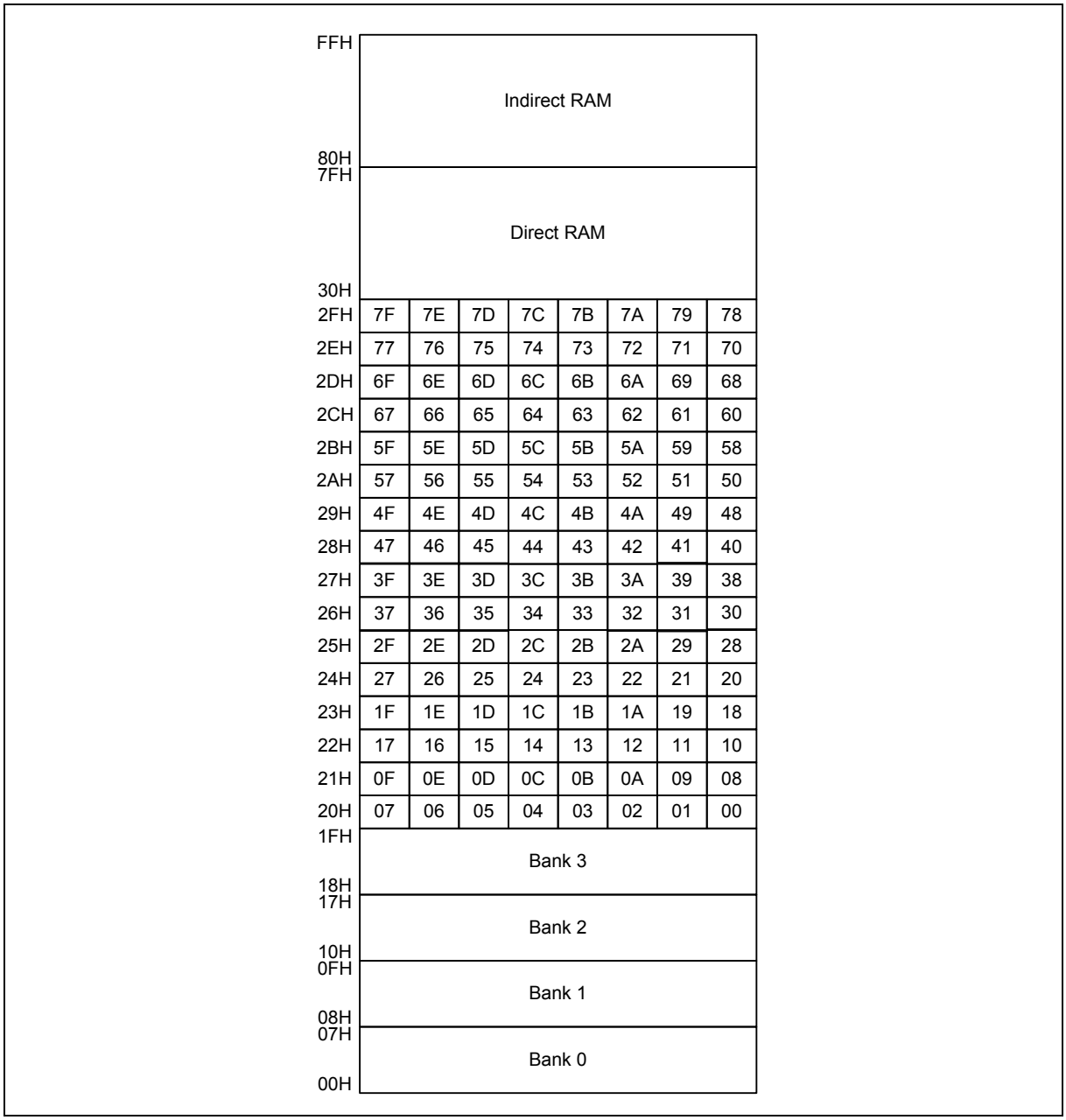
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, UART/USART
Peripherals	Brown-out Detect/Reset, LED, LVD, POR, PWM, WDT
Number of I/O	18
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	20-DIP (0.300", 7.62mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/w79e824adg



Working Registers

There are four sets of working registers, each consisting of eight 8-bit registers. These are termed ads Banks 0, 1, 2, and 3. Individual registers within these banks can be directly accessed by separate instructions. These individual registers are named as R0, R1, R2, R3, R4, R5, R6 and R7. However, at one time the W79E82X series can work with only one particular bank. The bank selection is done by setting RS1-RS0 bits in the PSW. The R0 and R1 registers are used to store the address for indirect accessing.

Bit addressable Locations

The Scratch-pad RAM area from location 20h to 2Fh is byte as well as bit addressable. This means that a bit in this area can be individually addressed. In addition some of the SFRs are also bit addressable. The instruction decoder is able to distinguish a bit access from a byte access by the type of the instruction itself. In the SFR area, any existing SFR whose address ends in a 0 or 8 is bit addressable.

Stack

The scratch-pad RAM can be used for the stack. This area is selected by the Stack Pointer (SP), which stores the address of the top of the stack. Whenever a jump, call or interrupt is invoked the return address is placed on the stack. There is no restriction as to where the stack can begin in the RAM. By default however, the Stack Pointer contains 07h at reset. The user can then change this to any value desired. The SP will point to the last used value. Therefore, the SP will be incremented and then address saved onto the stack. Conversely, while popping from the stack the contents will be read first, then the SP is decreased.

BIT	NAME	FUNCTION
7	SM0/FE	Serial port mode select bit 0 or Framing Error Flag: The SMOD0 bit in PCON SFR determines whether this bit acts as SM0 or as FE. The operation of SM0 is described below. When used as FE, this bit will be set to indicate an invalid stop bit. This bit must be manually cleared in software to clear the FE condition.
6	SM1	Serial port Mode bit 1: **Mode: SM0 SM1 Description Length Baud rate** 0 0 0 Synchronous 8 4/12 Tclk 1 0 1 Asynchronous 10 Variable 2 1 0 Asynchronous 11 64/32 Tclk 3 1 1 Asynchronous 11 Variable
5	SM2	Multiple processors communication. Setting this bit to 1 enables the multiprocessor communication feature in mode 2 and 3. In mode 2 or 3, if SM2 is set to 1, then RI will not be activated if the received 9th data bit (RB8) is 0. In mode 1, if SM2 = 1, then RI will not be activated if a valid stop bit was not received. In mode 0, the SM2 bit controls the serial port clock. If set to 0, then the serial port runs at a divide by 12 clock of the oscillator. This gives compatibility with the standard 8052. When set to 1, the serial clock become divide by 4 of the oscillator clock. This results in faster synchronous serial communication.
4	REN	Receive enable: When set to 1 serial reception is enabled, otherwise reception is disabled.
3	TB8	This is the 9th bit to be transmitted in modes 2 and 3. This bit is set and cleared by software as desired.
2	RB8	In modes 2 and 3 this is the received 9th data bit. In mode 1, if SM2 = 0, RB8 is the stop bit that was received. In mode 0 it has no function.
1	TI	Transmit interrupt flag: This flag is set by hardware at the end of the 8th bit time in mode 0, or at the beginning of the stop bit in all other modes during serial transmission. This bit must be cleared by software.
0	RI	Receive interrupt flag: This flag is set by hardware at the end of the 8th bit time in mode 0, or halfway through the stop bits time in the other modes during serial reception. However the restrictions of SM2 apply to this bit. This bit can be cleared only by software.

SERIAL DATA BUFFER

Bit:	7	6	5	4	3	2	1	0
	SBUF.7	SBUF.6	SBUF.5	SBUF.4	SBUF.3	SBUF.2	SBUF.1	SBUF.0

Mnemonic: SBUF Address: 99h

BIT	NAME	FUNCTION
7~0	SBUF	Serial data on the serial port is read from or written to this location. It actually consists of two separate internal 8-bit registers. One is the receive resister, and the other is the transmit buffer. Any read access gets data from the receive data buffer, while write access is to the transmit data buffer.

PORT 2

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	P2.1	P2.0

Mnemonic: P2 Address: A0h

BIT	NAME	FUNCTION
7~2	-	Reserved
1	P2.1	XTAL2 or CLKOUT pin by alternative.
0	P2.0	XTAL1 clock input pin.

Keyboard Interrupt

Bit:	7	6	5	4	3	2	1	0
	KBI.7	KBI.6	KBI.5	KBI.4	KBI.3	KBI.2	KBI.1	KBI.0

Mnemonic: KBI Address: A1h

Keyboard interrupt enable.

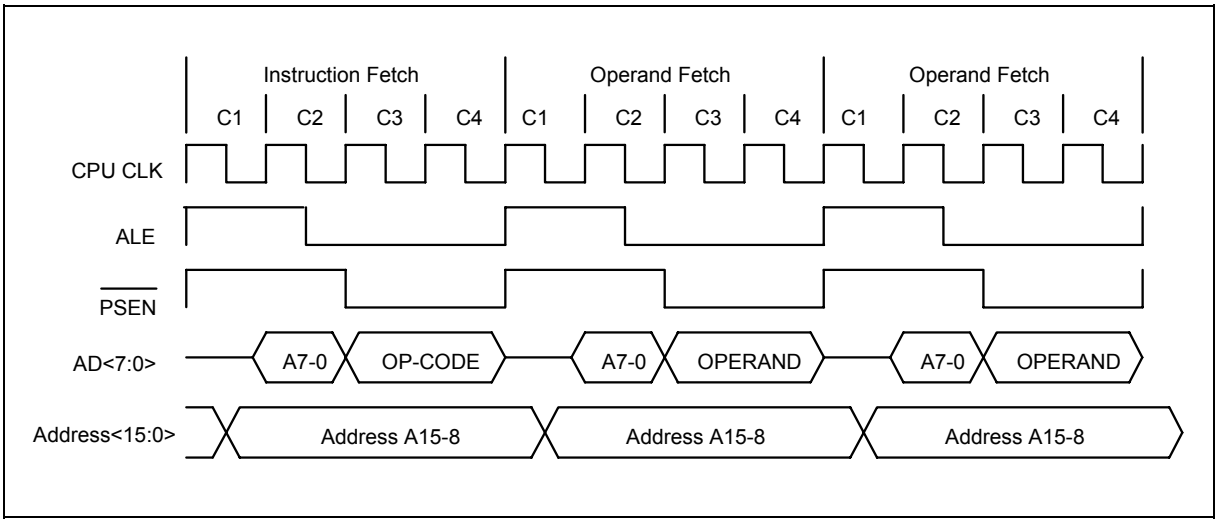
BIT	NAME	FUNCTION
7	KBI.7	1: Enable P0.7 as a cause of a Keyboard interrupt.
6	KBI.6	1: Enable P0.6 as a cause of a Keyboard interrupt.
5	KBI.5	1: Enable P0.5 as a cause of a Keyboard interrupt.
4	KBI.4	1: Enable P0.4 as a cause of a Keyboard interrupt.
3	KBI.3	1: Enable P0.3 as a cause of a Keyboard interrupt.
2	KBI.2	1: Enable P0.2 as a cause of a Keyboard interrupt.
1	KBI.1	1: Enable P0.1 as a cause of a Keyboard interrupt.
0	KBI.0	1: Enable P0.0 as a cause of a Keyboard interrupt.

AUX Function Register 1

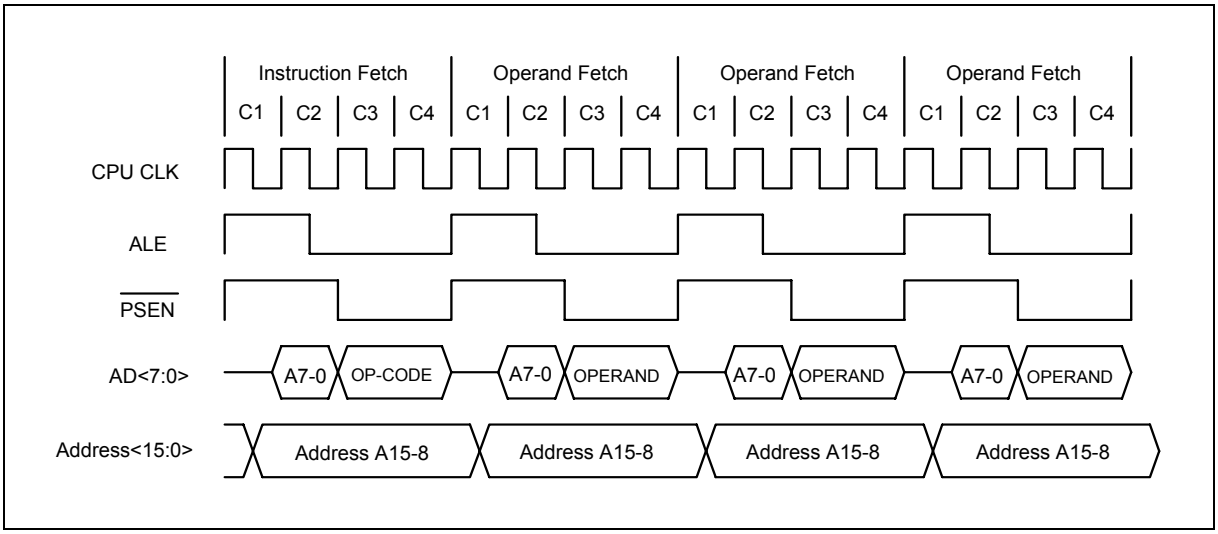
Bit:	7	6	5	4	3	2	1	0
	KBF	BOD	BOI	LPBOV	SRST	ADCEN	0	DPS

Mnemonic: AUXR1 Address: A2h

BIT	NAME	FUNCTION
7	KBF	Keyboard Interrupt Flag: 1: When any pin of port 0 that is enabled for the Keyboard Interrupt function goes low. Must be cleared by software.
6	BOD	Brown Out Disable: 0: Enable Brownout Detect function. 1: Disable Brownout Detect function and save power.



Three Cycle Instruction Timing



Four Cycle Instruction Timing

11. RESET CONDITIONS

The user has several hardware related options for placing the W79E82X series into reset condition. In general, most register bits go to their reset value irrespective of the reset condition, but there are a few flags whose state depends on the source of reset. The user can use these flags to determine the cause of reset using software.

11.1 External Reset

The device continuously samples the RST pin at state C4 of every machine cycle. Therefore the RST pin must be held for at least 2 machine cycles to ensure detection of a valid RST low. The reset circuitry then synchronously applies the internal reset signal. Thus the reset is a synchronous operation and requires the clock to be running to cause an external reset.

Once the device is in reset condition, it will remain so as long as RST is 0. Even after RST is deactivated, the device will continue to be in reset state for up to two machine cycles, and then begin program execution from 0000h. There is no flag associated with the external reset condition. However since the other two reset sources have flags, the external reset can be considered as the default reset if those two flags are cleared.

11.2 Power-On Reset (POR)

The software must clear the POR flag after reading it. Otherwise it will not be possible to correctly determine future reset sources. If the power fails, i.e. falls below Vrst, then the device will once again go into reset state. When the power returns to the proper operating levels, the device will again perform a power on reset delay and set the POR flag.

11.3 Watchdog Timer Reset

The Watchdog timer is a free running timer with programmable time-out intervals. The user can clear the watchdog timer at any time, causing it to restart the count. When the time-out interval is reached an interrupt flag is set. If the Watchdog reset is enabled and the watchdog timer is not cleared, then 512 clocks from the flag being set, the watchdog timer will generate a reset. This places the device into the reset condition. The reset condition is maintained by hardware for two machine cycles. Once the reset is removed the device will begin execution from 0000h.

11.4 Reset State

Most of the SFRs and registers on the device will go to the same condition in the reset state. The Program Counter is forced to 0000h and is held there as long as the reset condition is applied. However, the reset state does not affect the on-chip RAM. The data in the RAM will be preserved during the reset. However, the stack pointer is reset to 07h, and therefore the stack contents will be lost. The RAM contents will be lost if the V_{DD} falls below approximately 2V, as this is the minimum voltage level required for the RAM to operate normally. Therefore after a first time power on reset the RAM contents will be indeterminate. During a power fail condition, if the power falls below 2V, the RAM contents are lost.

After a reset most SFRs are cleared. Interrupts and Timers are disabled. The Watchdog timer is disabled if the reset source was a POR. The SFRs have FFh written into them which puts the port pins in a high state.

12. INTERRUPTS

The W79E82X series have four priority level interrupts structure with 13 interrupt sources. Each of the interrupt sources has an individual priority bit, flag, interrupt vector and enable bit. In addition, the interrupts can be globally enabled or disabled.

12.1 Interrupt Sources

The External Interrupts $\overline{\text{INT0}}$ and $\overline{\text{INT1}}$ can be either edge triggered or level triggered, depending on bits IT0 and IT1. The bits IE0 and IE1 in the TCON register are the flags which are checked to generate the interrupt. In the edge triggered mode, the INTx inputs are sampled in every machine cycle. If the sample is high in one cycle and low in the next, then a high to low transition is detected and the interrupts request flag IEx in TCON is set. The flag bit requests the interrupt. Since the external interrupts are sampled every machine cycle, they have to be held high or low for at least one complete machine cycle. The IEx flag is automatically cleared when the service routine is called. If the level triggered mode is selected, then the requesting source has to hold the pin low till the interrupt is serviced. The IEx flag will not be cleared by the hardware on entering the service routine. If the interrupt continues to be held low even after the service routine is completed, then the processor may acknowledge another interrupt request from the same source.

The Timer 0 and 1 Interrupts are generated by the TF0 and TF1 flags. These flags are set by the overflow in the Timer 0 and Timer 1. The TF0 and TF1 flags are automatically cleared by the hardware when the timer interrupt is serviced. The Watchdog timer can be used as a system monitor or a simple timer. In either case, when the time-out count is reached, the Watchdog Timer interrupt flag WDIF (WDCON.3) is set. If the interrupt is enabled by the enable bit IE1.4, then an interrupt will occur.

The Serial block can generate interrupt on reception or transmission. There are two interrupt sources from the Serial block, which are obtained by the RI and TI bits in the SCON SFR. These bits are not automatically cleared by the hardware, and the user will have to clear these bits using software.

All the bits that generate interrupts can be set or reset by hardware, and thereby software initiated interrupts can be generated. Each of the individual interrupts can be enabled or disabled by setting or clearing a bit in the IE SFR. IE also has a global enable/disable bit EA, which can be cleared to disable all interrupts.

The ADC can generate interrupt after finished ADC converter. There is one interrupt source, which is obtained by the ADCI bit in the ADCCON SFR. This bit is not automatically cleared by the hardware, and the user will have to clear this bit using software.

The two comparators can generate interrupt after comparator output has toggle occurs by CMF1 and CMF2. These bits are not automatically cleared by the hardware, and the user will have to clear these bits using software.

The I2C function can generate interrupt by SI flag, after I2C finished some action, then SI will set by hardware. If interrupt of I2C is enabled, it will generate interrupt. This bit will clear by software.

The PWM function can generate interrupt by BKF flag, after external brake pin has brake occurred. This bit will clear by software.

The W79E82X series use a four priority level interrupt structure. This allows great flexibility in controlling the handling of the W79E82X series many interrupt sources. The W79E82X series supports up to 13 interrupt sources.

Each interrupt source can be individually enabled or disabled by setting or clearing a bit in registers IE0 or IE1. The IE0 register also contains a global disable bit, EA, which disables all interrupts at once.

Each interrupt source can be individually programmed to one of four priority levels by setting or clearing bits in the IP0, IP0H, IP1, and IP1H registers. An interrupt service routine in progress can be interrupted by a higher priority interrupt, but not by another interrupt of the same or lower priority. The highest priority interrupt service cannot be interrupted by any other interrupt source. So, if two requests of different priority levels are received simultaneously, the request of higher priority level is serviced.

If requests of the same priority level are received simultaneously, an internal polling sequence determines which request is serviced. This is called the arbitration ranking. Note that the arbitration ranking is only used to resolve simultaneous requests of the same priority level.

As below Table summarizes the interrupt sources, flag bits, vector addresses, enable bits, priority bits, arbitration ranking, and whether each interrupt may wake up the CPU from Power Down mode.

DESCRIPTION	INTERRUPT FLAG BIT(S)	VECTOR ADDRESS	INTERRUPT ENABLE BIT(S)	INTERRUPT PRIORITY	ARBITRATION RANKING	POWER DOWN WAKEUP
External Interrupt 0	IE0	0003H	EX0 (IE0.0)	IP0H.0, IP0.0	1(highest)	Yes
Brownout Detect	BOF	002BH	EBO (IE.5)	IP0H.5, IP0.5	2	Yes
Watchdog Timer	WDIF	0053H	EWDI (IE1.4)	IP1H.4, IP1.4	3	Yes(1)
Timer 0 Interrupt	TF0	000BH	ET0 (IE.1)	IP0H.1, IP0.1	4	No
I2C Interrupt	SI	0033H	EI2 (IE1.0)	IP1H.0, IP1.0	5	No
ADC Converter	ADCI	005BH	EAD (IE.6)	IP0H.6, IP0.6	6	Yes(1)
External Interrupt 1	IE1	0013H	EX1 (IE.2)	IP0H.2, IP0.2	7	Yes
KBI Interrupt	KBF	003BH	EKB (IE1.1)	IP1H.1, IP1.1	8	Yes
Comparator 1 Interrupt	CMF1	0063H	EC1 (IE1.2)	IP1H.2, IP1.2	9	Yes
Timer 1 Interrupt	TF1	001BH	ET1 (IE.3)	IP0H.3, IP0.3	10	No
Comparator 2 Interrupt	CMF2	0043H	EC2 (IE1.3)	IP1H.3, IP1.3	11	Yes
Serial Port Tx and Rx	TI & RI	0023H	ES (IE.4)	IP0H.4, IP0.4	12	No
PWM Interrupt	BKF	0073H	EPWM (IE1.5)	IP1H.5, IP1.5	13 (lowest)	No

Note: 1. The Watchdog Timer and ADC Converter can wake up Power Down Mode when its clock source is used internal RC.

interrupts. Now the Watchdog Timer reset is enabled and the Watchdog interrupt may be disabled. If any errant code is executed now, then the reset Watchdog Timer instructions will not be executed at the required instants and Watchdog reset will occur.

The Watchdog Timer time-out selection will result in different time-out values depending on the clock speed. The reset, when enabled, will occurs 512 clocks after the time-out has occurred.

Time-out values for the Watchdog timer

WD1	WD0	WATCHDOG INTERVAL	NUMBER OF CLOCKS	TIME @ 10 MHZ
0	0	2^{17}	131072	13.11 mS
0	1	2^{20}	1048576	104.86 mS
1	0	2^{23}	8388608	838.86 mS
1	1	2^{26}	67108864	6710.89 mS

The Watchdog Timer will de disabled by a power-on/fail reset. The Watchdog Timer reset does not disable the Watchdog Timer, but will restart it. In general, software should restart the timer to put it into a known state.

The control bits that support the Watchdog Timer are discussed below.

15.1 WATCHDOG CONTROL

WDIF: WDCON.3 - Watchdog Timer Interrupt flag. This bit is set whenever the time-out occurs in the Watchdog Timer. If the Watchdog interrupt is enabled (IE1.4), then an interrupt will occur (if the global interrupt enable is set and other interrupt requirements are met). Software or any reset can clear this bit.

WDRF: WDCON.2 - Watchdog Timer Reset flag. This bit is set whenever a watchdog reset occurs. This bit is useful for determined the cause of a reset. Software must read it, and clear it manually. A Power-fail reset will clear this bit. If EWDRST = 0, then this bit will not be affected by the Watchdog Timer.

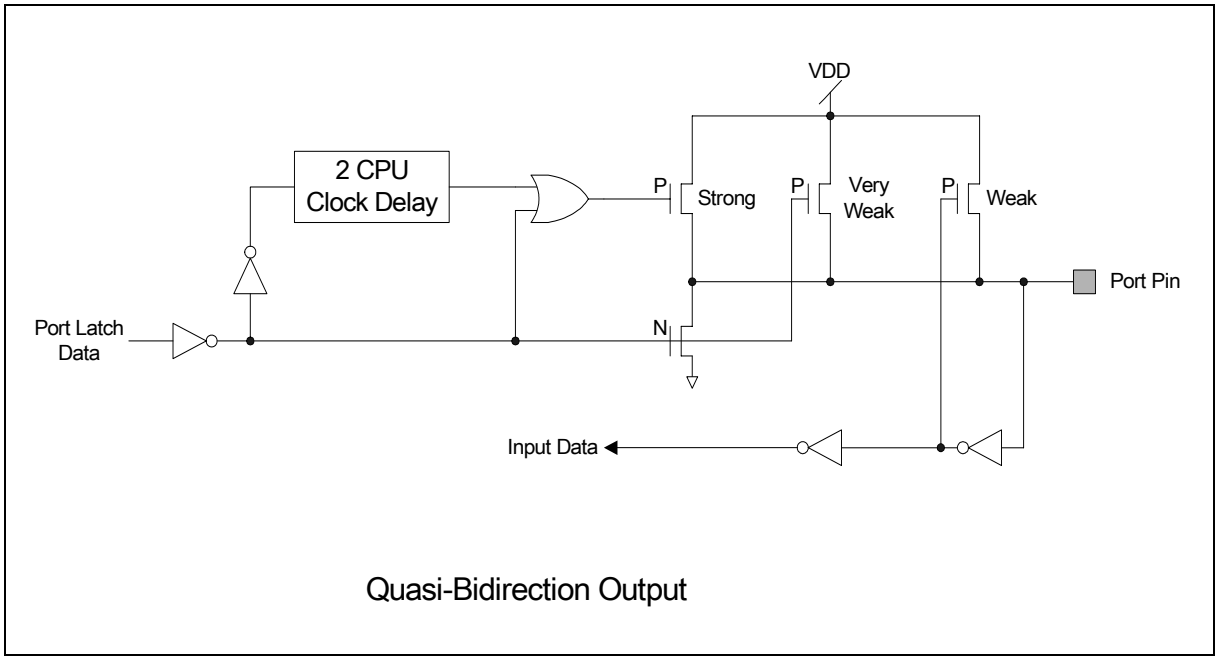
EWRST: WDCON.1 - Enable Watchdog Timer Reset. This bit when set to 1 will enable the Watchdog Timer reset function. Setting this bit to 0 will disable the Watchdog Timer reset function, but will leave the timer running.

WDCLR: WDCON.0 - Reset Watchdog Timer. This bit is used to clear the Watchdog Timer and to restart it. This bit is self-clearing, so after the software writes 1 to it the hardware will automatically clear it. If the Watchdog Timer reset is enabled, then the WDCLR has to be set by the user within 512 clocks of the time-out. If this is not done then a Watchdog Timer reset will occur.

The “weak” pull-up is turned on when the input port pin is logic “1” level or itself is logic “1”, and it provides the most source current for a quasi-bidirectional pin that output is “1” or port latch is logic “0”’.

The “very weak” pull-up is turned on when the port latch is logic “1”. If port latch is logic “0”, it will be turned off. The very weak pull-up is support a very small current that will pull the pin high if it is left floating. And the quasi-bidirectional port configuration is shown as below figure.

If port pin is low, it can drives large sink current for output, and it is similar with push-pull and open drain on sink current output.



Quasi-Bidirection Output

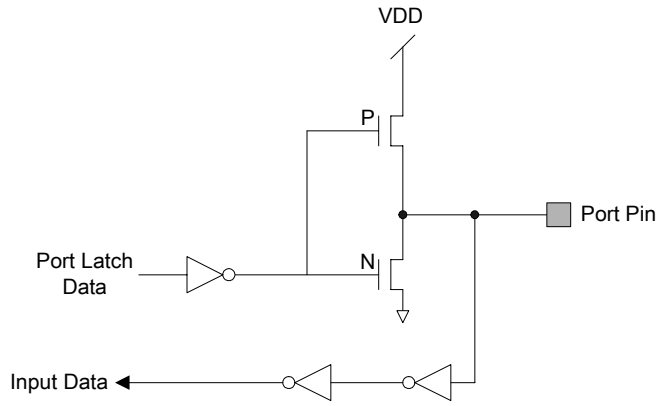
20.2 Open Drain Output Configuration

To configure this mode is turned off all pull-ups. If used similar as a logic output, the port must has an external pull-up resister. The open drain port configuration is shown as below.

20.3 Push-Pull Output Configuration

The push-pull output mode has two strong pull-up and pull-down structure that support large source and sink current output. it remove “weak” pull-up and “very weak” pull-up resister and remain “strong pull-up resister on quasi-bidirectional output mode. The “strong” pull-up is always turns on when port latch is logic “1” to support source current. The push-pull port configuration is shown in below Figure.

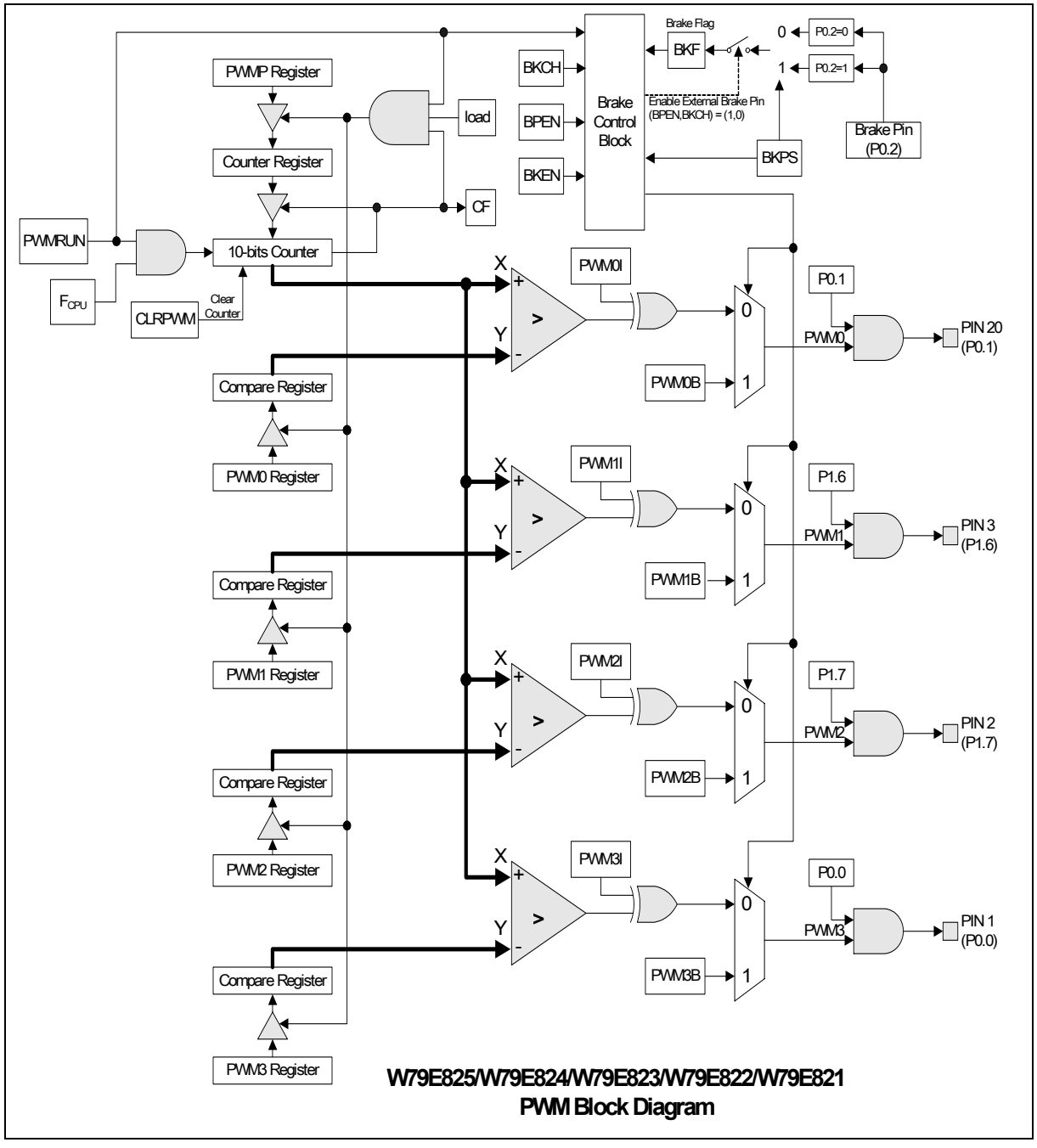
The W79E82X series have three port pins that can’t be configured are P1.2, P1.3, and P1.5. The port pins P1.2 and P1.3 are configured to open drain outputs. They may be used as inputs by writing ones to their respective port latches.



Push-Pull Output

20.4 Input Only Configuration

By configure this mode, the ports are only digital input and disable digital output. The W79E82X series can select input pin to Schmitt trigger or TTL level input by PxM1.y and PxM2.y registers.



W79E825/W79E824/W79E823/W79E822/W79E821
PWM Block Diagram

24. ANALOG-TO-DIGITAL CONVERTER

The ADC contains a DAC which converts the contents of a successive approximation register to a voltage (VDAC) which is compared to the analog input voltage (Vin). The output of the comparator is fed to the successive approximation control logic which controls the successive approximation register. A conversion is initiated by setting ADCS in the ADCCON register. ADCS can be set by software only or by either hardware or software.

The software only start mode is selected when control bit ADCCON.5 (ADCEX) =0. A conversion is then started by setting control bit ADCCON.3 (ADCS) The hardware or software start mode is selected when ADCCON.5 =1, and a conversion may be started by setting ADCCON.3 as above or by applying a rising edge to external pin STADC. When a conversion is started by applying a rising edge, a low level must be applied to STADC for at least one machine cycle followed by a high level for at least one machine cycle.

The low-to-high transition of STADC is recognized at the end of a machine cycle, and the conversion commences at the beginning of the next cycle. When a conversion is initiated by software, the conversion starts at the beginning of the machine cycle which follows the instruction that sets ADCS. ADCS is actually implemented with tpw flip-flops: a command flip-flop which is affected by set operations, and a status flag which is accessed during read operations.

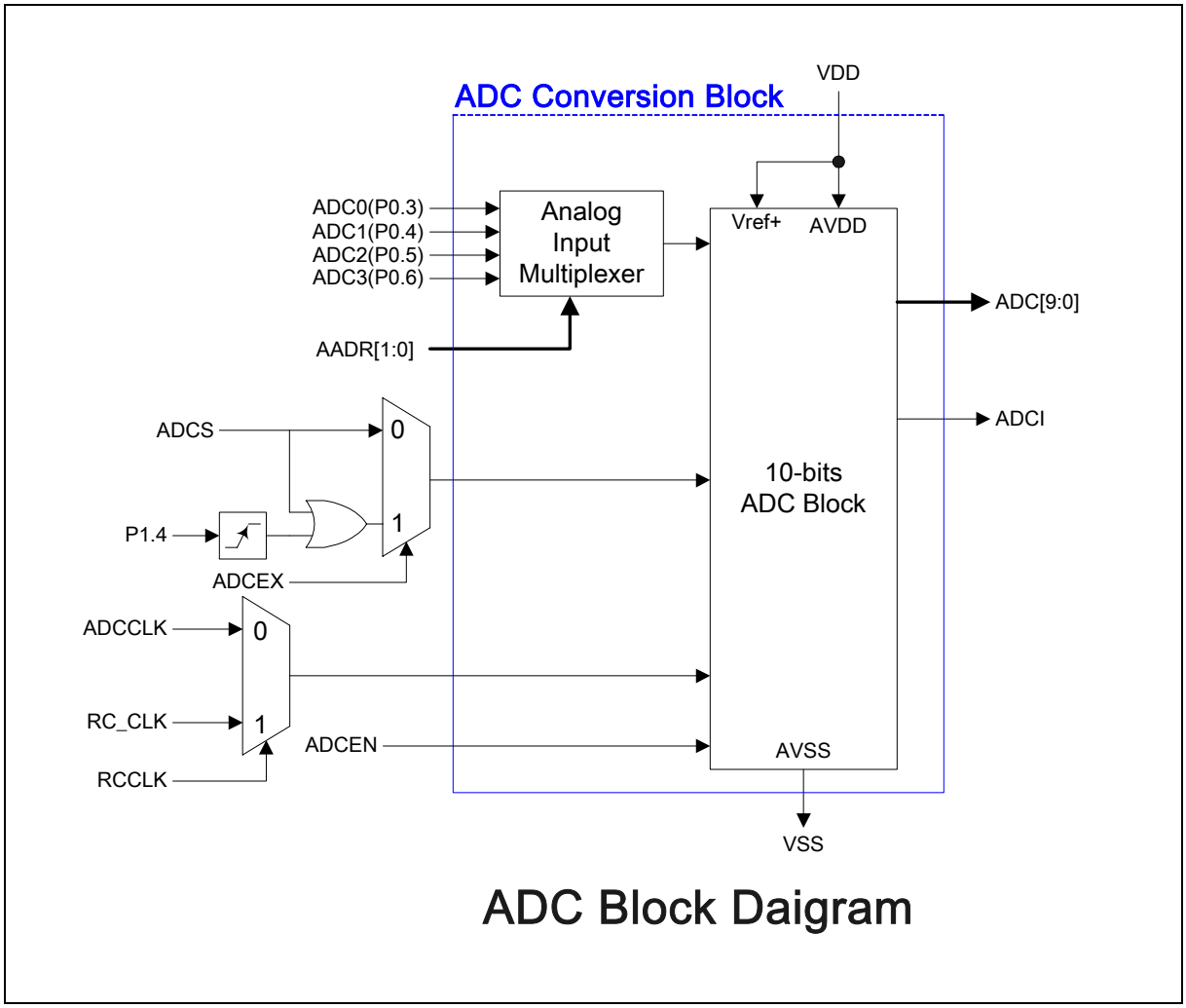
The next two machine cycles are used to initiate the converter. At the end of the first cycle, the ADCS status flag is set end a value of “1” will be returned if the ADCS flag is read while the conversion is in progress. Sampling of the analog input commences at the end of the second cycle.

During the next eight machine cycles, the voltage at the previously selected pin of one of analog input pin is sampled, and this input voltage should be stable in order to obtain a useful sample. In any event, the input voltage slew rate must be less than 10V/ms in order to prevent an undefined result.

The successive approximation control logic first sets the most significant bit and clears all other bits in the successive approximation register (10 0000 0000b). The output of the DAC (50% full scale) is compared to the input voltage Vin. If the input voltage is greater than VDAC, then the bit remains set; otherwise if is cleared.

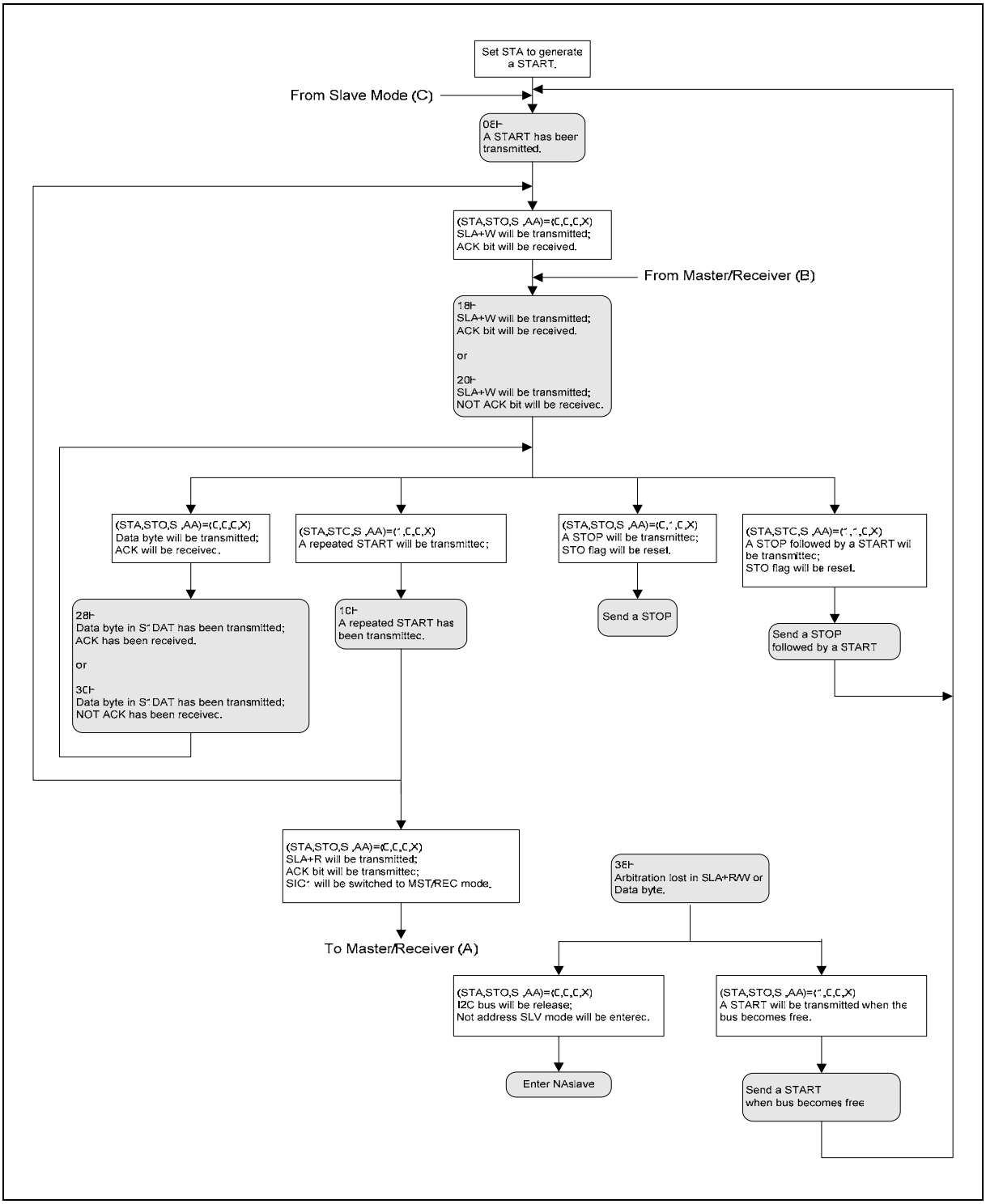
The successive approximation control logic now sets the next most significant bit (11 0000 0000b or 01 0000 0000b, depending on the previous result), and the VDAC is compared to Vin again. If the input voltage is greater then VDAC, then the bit remains set; otherwise it is cleared. This process is repeated until all ten bits have been tested, at which stage the result of the conversion is held in the successive approximation register. The conversion takes four machine cycles per bit.

The end of the 10-bit conversion is flagged by control bit ADCCON.4 (ADCI). The upper 8 bits of the result are held in special function register ADCH, and the two remaining bits are held in ADCCON.7 (ADC.1) and ADCCON.6 (ADC.0). The user may ignore the two least significant bits in ADCCON and use the ADC as an 8-bit converter (8 upper bits in ADCH). In any event, the total actual conversion time is 52 machine cycles. ADCI will be set and the ADCS status flag will be reset 52 cycles after the ADCS is set. Control bits ADCCON.0 and ADCCON.1 are used to control an analog multiplexer which

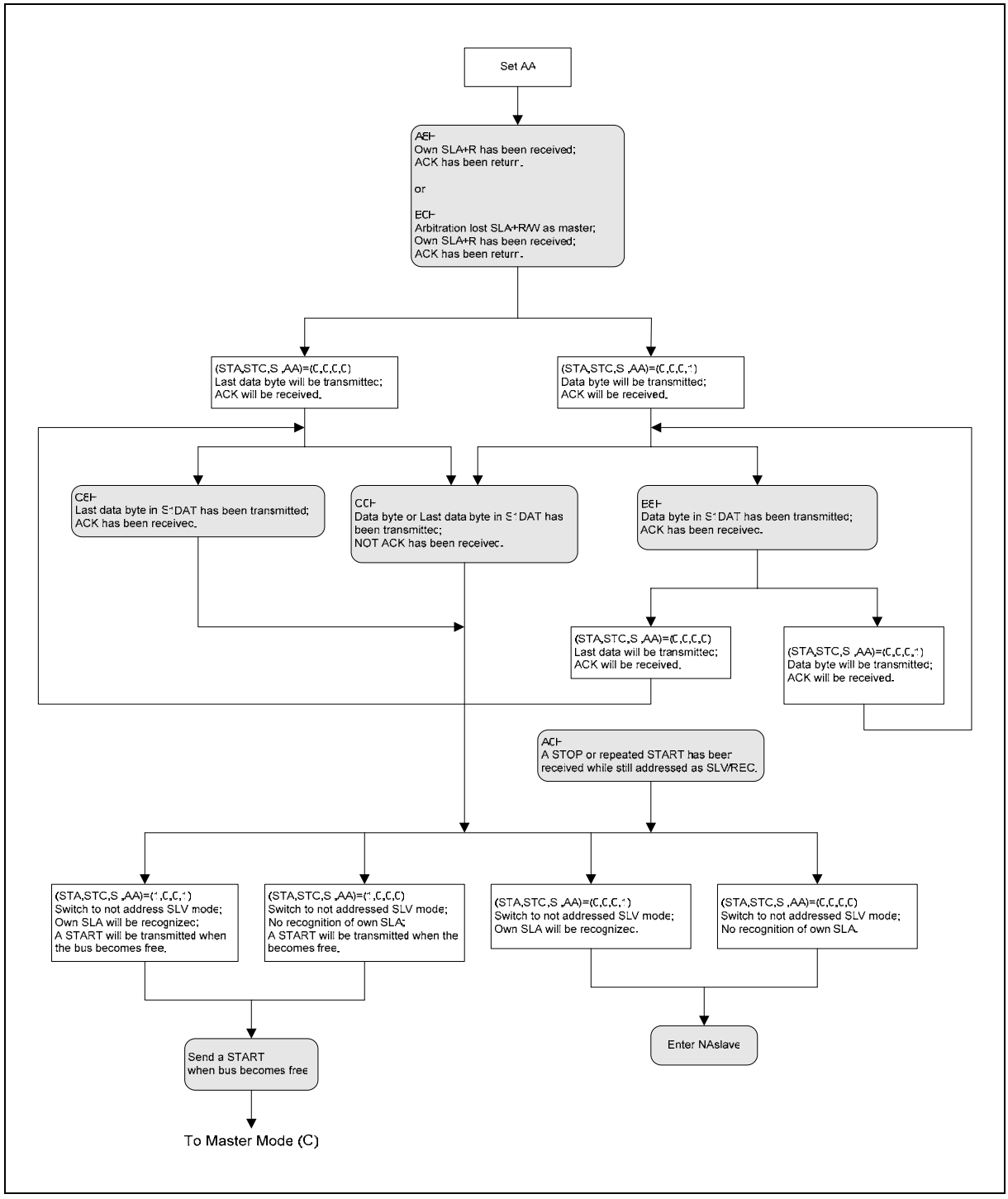


The ADC Block Diagram

Master Transmitter Mode



Slave Transmitter Mode



27. CONFIG BITS

The W79E82X series have two CONFIG bits(CONFIG1, CONFIG2) that must be define at power up and can not be set after the program start of execution. Those features are configured through the use of two flash EPROM bytes, and the flash EPROM can be programmed and verified repeatedly. Until the code inside the Flash EPROM is confirmed OK, the code can be protected. The protection of flash EPROM (CONFIG2) and those operations on it are described below. The data of these bytes may be read by the MOVC instruction at the addresses.

27.1 CONFIG1

CONFIG 1 :

7	6	5	4	3	2	1	0	
WDTE	RPD	PRHI	BOV	-	-	Fosc1	Fosc0	CONFIG Bit

WDTE: Watchdog Timer clock source Bit.
RPD: Reset Pin Disable Bit.
PRHI: Port Reset High or Low Bit.
BOV: Brownout voltage select Bit.
Fosc1: CPU oscillator type select Bit 1.
Fosc0: CPU oscillator type select Bit 0.

CONFIG Register 1

BIT	NAME	FUNCTION
7	WDTE	Clock source of Watchdog Timer select bit: 0: The internal RC oscillator clock is for Watchdog Timer clock used. 1: The uC clock is for Watchdog Timer clock used.
6	RPD	Reset Pin Disable bit: 0: Enable Reset function of Pin 1.5. 1: Disable Reset function of Pin 1.5, and it to be used as an input port pin.
5	PRHI	Port Reset High or Low bit: 0: Port reset to low state. 1: Port reset to high state.
4	BOV	Brownout Voltage Select bit: 0: Brownout detect voltage is 3.8V. 1: Brownout detect voltage is 2.5V.

BIT 7	BIT 6	FUNCTION DESCRIPTION
1	1	Both security of **16KB/8KB/4KB/2KB/1KB** program code and **256/128** Bytes data area are unlocked, those can be erased, programmed or read by Writer or ICP.
0	1	The **16KB/8KB/4KB/2KB/1KB** program code area is locked, it can't be read by Writer or ICP.
1	0	Don't support (Invalid)
0	0	Both security of **16KB/8KB/4KB/2KB/1KB** program code and **256/128** Bytes data area are locked, those can't be read by Writer or ICP.

28. ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	CONDITION	RATING	UNIT
DC Power Supply	VDD–VSS	-0.3	+7.0	V
Input Voltage	VIN	VSS-0.3	VDD+0.3	V
Operating Temperature	TA	-40	+85	°C
Storage Temperature	Tst	-55	+150	°C

Note: Exposure to conditions beyond those listed under absolute maximum ratings may adversely affects the lift and reliability of the device.

DC ELECTRICAL CHARACTERISTICS, continued.

PARAMETER	SYMBOL	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Hysteresis voltage	V_{HY}		$0.2V_{DD}$		V	
Source Current P0, P1, P2 (Quasi-bidirectional Mode)	I_{sr1}	-180	-210	-360	uA	V_{DD} = 4.5V, V_S = 2.4V
Sink Current P0, P1, P2 (Quasi-bidirectional Mode)	I_{SK2}	13	18.5	24	mA	V_{DD} = 4.5V, V_S = 0.45V
Output Low Voltage P0, P1, P2 (PUSH-PULL Mode)	V_{OL1}	-	0.5	0.9	V	V_{DD} = 4.5V, I_{OL} = 20 mA
		-	0.1	0.4	V	V_{DD} = 2.7V, I_{OL} = 3.2 mA
Output High Voltage P0, P1, P2 (PUSH-PULL Mode)	V_{OH}	2.4	3.4	-	V	V_{DD} = 4.5V, I_{OH} = -16mA
		1.9	2.4	-	V	V_{DD} = 2.7V, I_{OH} = -3.2mA
Brownout voltage with BOV=1	$V_{BO2.5}$	2.4	-	2.7	V	TA = -0 to 70°C
Brownout voltage with BOV=0	$V_{BO3.8}$	3.5	-	4.0	V	TA = -0 to 70°C
Comparator Reference Voltage	Vref	1.02	1.20	1.31	V	

Notes: *1. RST pin is a Schmitt trigger input.

*2. XTAL1 is a CMOS input.

*3. Pins of P0, P1,P2 can source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when Vin approximates to 2V.

29.1 The ADC Converter DC ELECTRICAL CHARACTERISTICS

(V_{DD}–V_{SS} = 3.0~5V, TA = -40~85°C, Fosc = 20MHz, unless otherwise specified.)

PARAMETER	SYMBOL	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Analog input	AVIN	V_{SS}-0.2		V_{DD}+0.2	V	
ADC clock	ADCCLK	200KHz		5MHz	Hz	ADC circuit input clock
Conversion time	t_C		$52t_{ADC}$[1]		us	
Differential non-linearity	DNL	-1	-	+1	LSB	
Integral non-linearity	INL	-2	-	+2	LSB	
Offset error	Ofe	-1	-	+1	LSB	
Gain error	Ge	-1	-	+1	%	
Absolute voltage error	Ae	-3	-	+3	LSB	

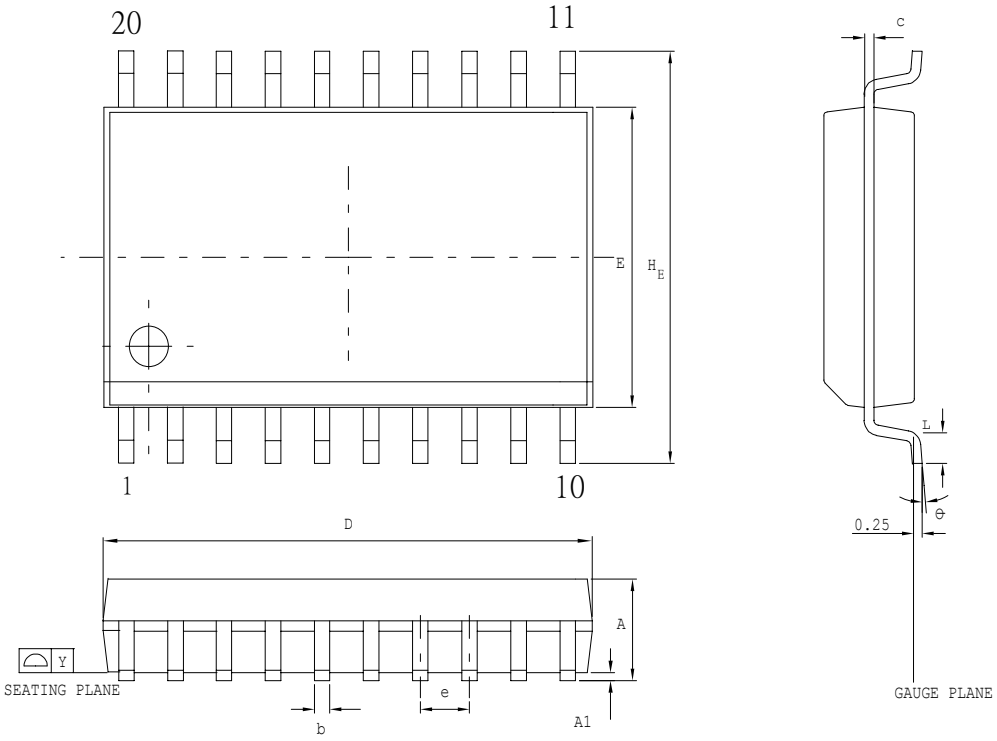
Notes:

1. tADC: The period time of ADC input clock.

34. PACKAGE DIMENSIONS

34.1 20-pin SO

20L SOP-300mil



Control demensions are in milmeters .

SYMBOL	DIMENSION IN MM		DIMENSION IN INCH	
	MIN.	MAX.	MIN.	MAX.
A	2.35	2.65	0.093	0.104
A1	0.10	0.30	0.004	0.012
b	0.33	0.51	0.013	0.020
c	0.23	0.32	0.009	0.013
E	7.40	7.60	0.291	0.299
D	12.60	13.00	0.496	0.512
e	1.27 BSC		0.050 BSC	
H_E	10.00	10.65	0.394	0.419
Y	—	0.10	—	0.004
L	0.40	1.27	0.016	0.050
θ	0	8	0	8