Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	Coldfire V1
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	EBI/EMI, I²C, SCI, SPI, USB OTG
Peripherals	LVD, PWM, WDT
Number of I/O	48
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 12x12b; D/A 1x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	81-LBGA
Supplier Device Package	81-MAPBGA (10x10)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcf51je128cmb

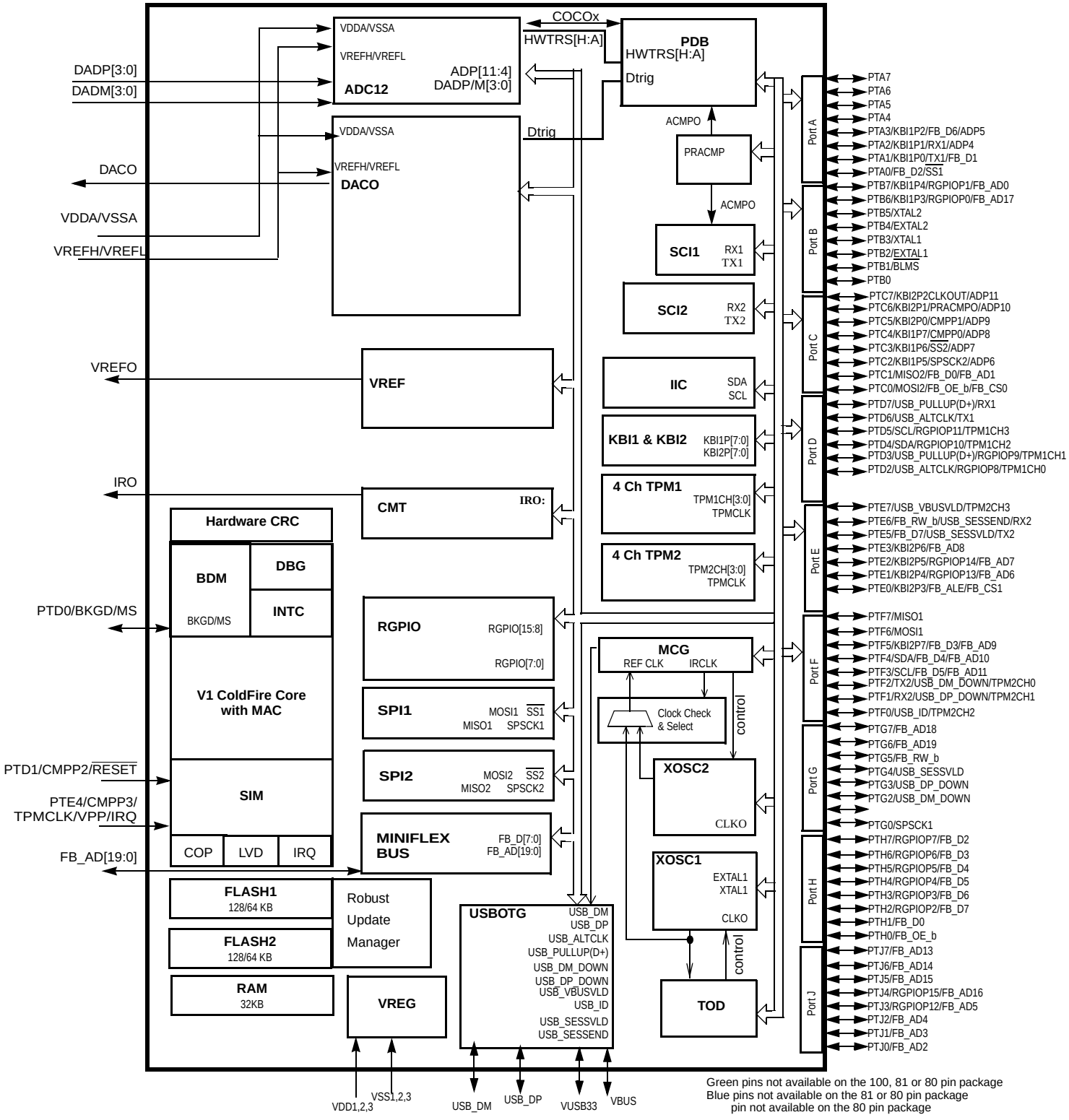


Figure 1. MCF51JE256/128 Block Diagram

1 Features

The following table provides a cross-comparison of the features of the MCF51JE256/128 according to package.

Table 1. MCF51JE Features by MCU and Package

Feature	MCF51JE256				MCF51JE128	
FLASH size (bytes)	262144				131072	
RAM size (bytes)	32K				32K	
Pin quantity	104	100	81	80	81	80
Programmable Analog Comparator (PRACMP)	yes					
Debug Module (DBG)	yes					
Multipurpose Clock Generator (MCG)	yes					
Inter-Integrated Communication (IIC)	yes					
Interrupt Request Pin (IRQ)	yes					
Keyboard Interrupt (KBI)	16					
Digital General purpose I/O[1]	69	65	48	47	48	47
Power and Ground Pins	8					
Time Of Day (TOD)	yes					
Serial Communications (SCI1)	yes					
Serial Communications (SCI2)	yes					
Serial Peripheral Interface (SPI1(FIFO))	yes					
Serial Peripheral Interface(SPI2)	yes					
Carrier Modulator Timer pin (IRO)	yes					
Programmable Delay Block (PDB)	yes					
TPM input clock pin (TPMCLK)	yes					
TPM1 channels	4					
TPM2 channels	4					
XOSC1	yes					
XOSC2	yes					
USBOTG	yes					
MiniFlex Bus	yes		DATA			
Rapid GPIO	16		9			
ADC single-ended channels	12					
DAC ouput pin (DACO)	yes					
Voltage reference output pin (VREFO)	yes					

[1] Port I/O count does not include $\overline{\text{BLMS}}$, BKGD and IRQ. $\overline{\text{BLMS}}$ BKGD are Output only, IRQ is input only.

The following table describes the functional units of the MCF51JE256/128.

2 Pinouts and Pin Assignments

2.1 104-Pin MAPBGA

The following figure shows the 104-pin MAPBGA pinout configuration.

	1	2	3	4	5	6	7	8	9	10	11	
A	PTF6	PTF7	USB_DP	USB_DM	VUSB33	PTF4	PTF3	FB_AD12	PTJ7	PTJ5	PTJ4	A
B	PTG0	PTA0	PTG3	VBUS	PTF5	PTJ6	PTH0	PTE5	PTF0	PTF1	PTF2	B
C	IRO	PTG4	PTA6	PTG2	PTG6	PTG5	PTG7	PTH1	PTE4	PTE6	PTE7	C
D	PTA5	PTA4	PTB1	VDD1		VDD2		VDD3	PTA1	PTE3	PTE2	D
E	VSSA	PTA7	PTB0						PTA2	PTJ3	PTE1	E
F	VREFL			PTG1				PTC7	PTJ2	PTJ0	PTJ1	F
G	ADP2								PTD5	PTD7	PTE0	G
H			PTA3	VSS1		VSS2		VSS3	PTD4	PTD3	PTD2	H
J	ADP0		PTH7	PTH6	PTH4	PTH3	PTH2	PTD6	PTC2	PTC0	PTC1	J
K			ADP1	PTH5	PTB6	PTB7	PTC3	PTD1	PTC4	PTC5	PTC6	K
L	ADP3	DACO		VREFO	VREFH	VDDA	PTB3	PTB2	PTD0	PTB5	PTB4	L
	1	2	3	4	5	6	7	8	9	10	11	

Figure 2. 104-Pin MAPBGA

2.2 100-Pin LQFP

The following figure shows the 100-pin LQFP pinout configuration.

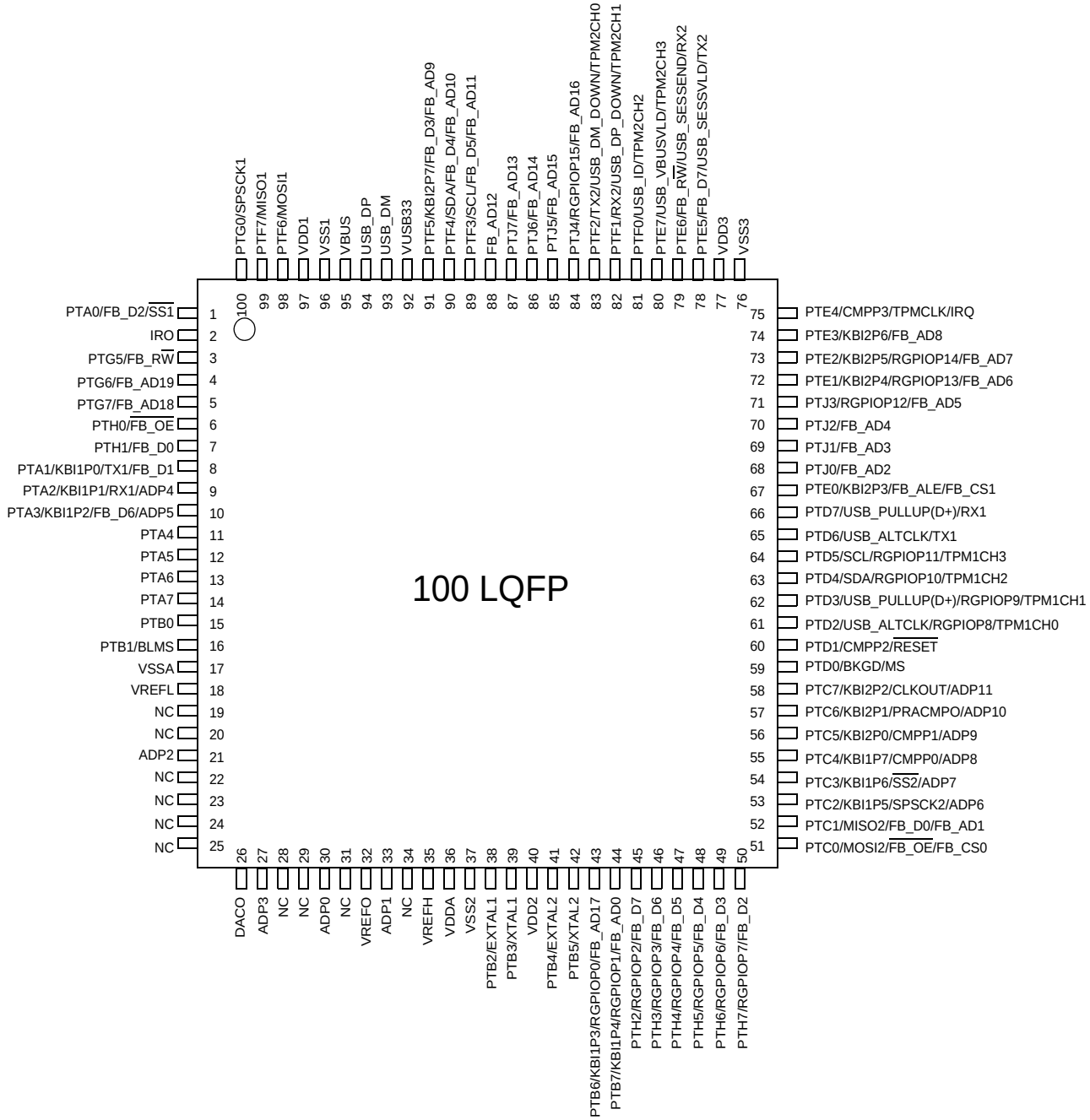


Figure 3. 100-Pin LQFP

2.4 80-Pin LQFP

The following figure shows the 80-pin LQFP pinout configuration.

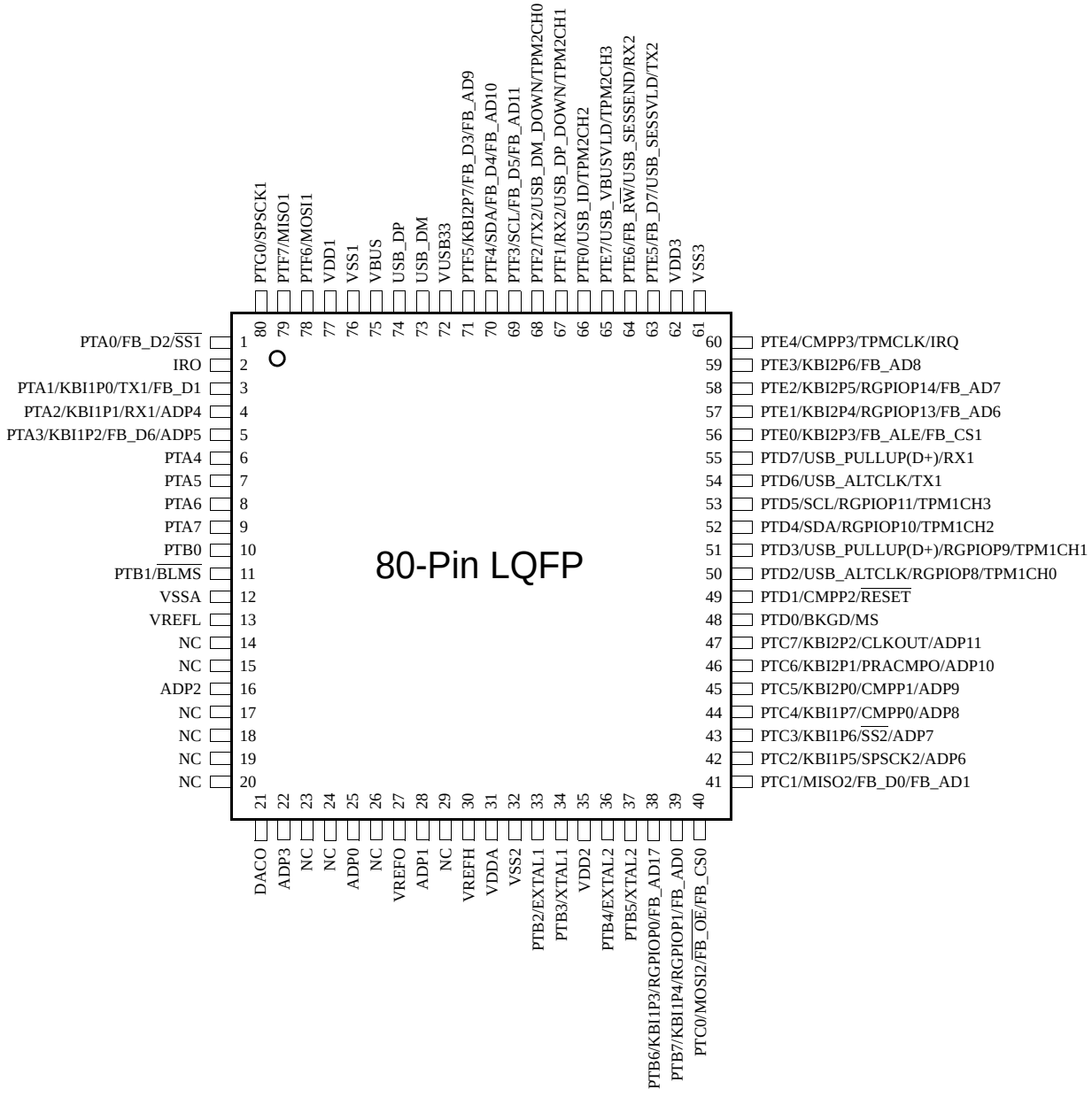


Figure 5. 80-Pin LQFP Pinout

2.5 Pin Assignments

Table 3. Package Pin Assignments

Package				Default Function	Alternate 1	Alternate 2	Alternate 3	Composite Pin Name
104 MAPBGA	100 LQFP	81 MAPBGA	80 LQFP					
B2	1	B2	1	PTA0	FB_D2	$\overline{SS1}$	—	PTA0/FB_D2/$\overline{SS1}$
C1	2	A1	2	IRO	—	—	—	IRO
C6	3	—	—	PTG5	FB_$\overline{RW}$	—	—	PTG5/FB_$\overline{RW}$
C5	4	—	—	PTG6	FB_AD19	—	—	PTG6/FB_AD19
C7	5	—	—	PTG7	FB_AD18	—	—	PTG7/FB_AD18
B7	6	—	—	PTH0	$\overline{FB\_OE}$	—	—	PTH0/$\overline{FB\_OE}$
C8	7	—	—	PTH1	FB_D0	—	—	PTH1/FB_D0
D9	8	C4	3	PTA1	KBI1P0	TX1	FB_D1	PTA1/KBI1P0/TX1/FB_D1
E9	9	D5	4	PTA2	KBI1P1	RX1	ADP4	PTA2/KBI1P1/RX1/ADP4
H3	10	D6	5	PTA3	KBI1P2	FB_D6	ADP5	PTA3/KBI1P2/FB_D6/ADP5
D2	11	C1	6	PTA4	—	—	—	PTA4
D1	12	C2	7	PTA5	—	—	—	PTA5
C3	13	C3	8	PTA6	—	—	—	PTA6
E2	14	D2	9	PTA7	—	—	—	PTA7
E3	15	D3	10	PTB0	—	—	—	PTB0
D3	16	D4	11	PTB1	$\overline{BLMS}$	—	—	PTB1/$\overline{BLMS}$
E1	17	J1	12	VSSA	—	—	—	VSSA
F1	18	J2	13	VREFL	—	—	—	VREFL
F2	19	D1	19	—	—	—	—	NC
G2	20	E2	15	—	—	—	—	NC
G1	21	F2	16	ADP2	—	—	—	ADP2
H1	22	F1	17	—	—	—	—	NC
H2	23	E2	18	NC	—	—	—	NC
F3	24	F3	19	—	—	—	—	NC
G3	25	E3	20	—	—	—	—	NC
L2	26	G2	21	DACO	—	—	—	DACO
L1	27	G3	22	ADP3	—	—	—	ADP3
K1	28	H4	23	—	—	—	—	NC
K2	29	G4	24	NC	—	—	—	NC
J1	30	G1	25	ADP0	—	—	—	ADP0
J2	31	H1	26	—	—	—	—	NC
L4	32	G5	27	VREFO	—	—	—	VREFO
K3	33	H3	28	ADP1	—	—	—	ADP1
L3	34	H2	29	NC	—	—	—	NC

Table 5. Absolute Maximum Ratings

#	Rating	Symbol	Value	Unit
1	Supply voltage	V_{DD}	–0.3 to 3.8	V
2	Maximum current into V_{DD}	I_{DD}	120	mA
3	Digital Input voltage	V_{In}	–0.3 to V_{DD} + 0.3	V
4	Instantaneous maximum current Single pin limit (applies to all port pins)[1, 2, 3]	I_D	±25	mA
5	Storage temperature range	T_{stg}	–55 to 150	°C

1 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive (V_{DD}) and negative (V_{SS}) clamp voltages, then use the larger of the two resistance values.

2 All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.

3 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low (which would reduce overall power consumption).

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}).

3.3 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and it is user-determined rather than being controlled by the MCU design. In order to take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

[8] Maximum is highest voltage that POR is guaranteed.
[9] Run at 1 MHz bus frequency.
[10] Low voltage detection and warning limits measured at 1 MHz bus frequency.
[11] Factory trimmed at V_{DD} = 3.0 V, Temp = 25°C.

3.6 Supply Current Characteristics

Table 10. Supply Current Characteristics

#	Symbol	Parameter	Bus Freq	V_{DD} (V)	Typical[1]	Maximum	Unit	Temperature (°C)	C
1	RI_{DD}	Run supply current FEI mode, all modules ON[2]							
			25.165 MHz	3	44	48	mA	–40 to 25	P
			25.165 MHz	3	44	48	mA	105	P
			20 MHz	3	32.3	—	mA	–40 to 105	T
			8 MHz	3	16.4	—	mA	–40 to 105	T
			1 MHz	3	2.9	—	mA	–40 to 105	T
2	RI_{DD}	Run supply current FEI mode, all modules OFF[3]							
			25.165 MHz	3	29	29.6	mA	–40 to 105	C
			20 MHz	3	25.4	—	mA	–40 to 105	T
			8 MHz	3	12.7	—	mA	–40 to 105	T
			1 MHz	3	2.4	—	mA	–40 to 105	T
3	RI_{DD}	Run supply current LPR=0, all modules OFF[3]							
			16 kHz FBI	3	232	280	μA	–40 to 105	T
			16 kHz FBE	3	231	296	μA	–40 to 105	T
4	RI_{DD}	Run supply current LPR=1, all modules OFF[3]							
			16 kHz BLPE	3	74	75	μA	0 to 70	T
			16 kHz BLPE	3	74	120	μA	–40 to 105	T
5	WI_{DD}	Wait mode supply current FEI mode, all modules OFF[3]							
			25.165 MHz	3	16.5	—	mA	–-40 to 105	C
			20 MHz	3	10.3	—	mA	–-40 to 105	T
			8 MHz	3	6.6	—	mA	–-40 to 105	T
			1 MHz	3	1.7	—	mA	–-40 to 105	T

Table 11. Stop Mode Adders (continued)

#	Parameter	Condition	Temperature (°C)					Units	C
			-40	25	70	85	105		
5	LVD[1]	LVDSE = 1	116	117	126	132	172	µA	T
6	PRACMP[1]	Not using the bandgap (BGBE = 0)	17	18	24	35	74	µA	T
7	ADC[1]	ADLPC = ADLSMP = 1 Not using the bandgap (BGBE = 0)	75	85	100	115	165	µA	T
8	DAC[1]	High power mode; no load on DACO	500	500	500	500	500	µA	T

1 Not available in stop2 mode.

Figure 6. Stop IDD versus Temperature

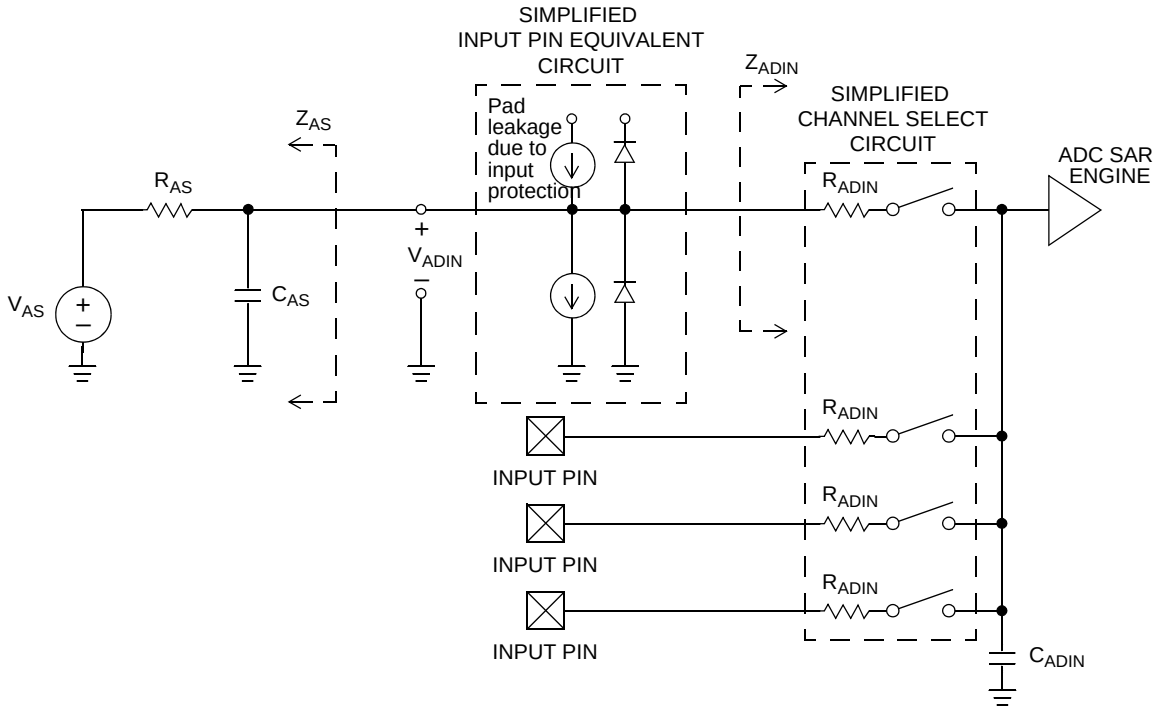


Figure 8. ADC Input Impedance Equivalency Diagram

Table 16. 12-bit SAR ADC Characteristics full operating range ($V_{REFH} = V_{DDAD}$, $V_{REFL} = V_{SSAD}$)

#	Symbol	Characteristic	Conditions[1]	Minimum	Typical[2]	Maximum	Unit	C
1	I_{DDAD}	Supply Current (ADLSMP=0, ADCO=1)	ADLPC=1, ADHSC=0	—	215	—	μA	T
			ADLPC=0, ADHSC=0	—	470	—	μA	T
			ADLPC=0, ADHSC=1	—	610	—	μA	T
			Stop, Reset, Module Off	—	0.01	—	μA	C
2	f_{ADACK}	ADC Asynchronous Clock Source (t_{ADACK} =1/f_{ADACK})	ADLPC=1, ADHSC=0	—	2.4	—	MHz	P
			ADLPC=0, ADHSC=0	—	5.2	—	MHz	P
			ADLPC=0, ADHSC=1	—	6.2	—	MHz	P
3	—	Sample Time — *See Reference Manual for sample times.*						
4	—	Conversion Time — *See Rreference Manual for conversion times.*						
5	TUE	Total Unadjusted Error 32x Hardware Averaging (AVGE = %1 AVGS = %11)	12-bit single-ended mode	—	±1.75	±3.5	LSB[3]	T
			10-bit single-ended mode	—	±0.8	±1.5	LSB[3]	T
			8-bit single-ended mode	—	±0.5	±1.0	LSB[3]	T
6		Differential Non-Linearity	12-bit single-ended mode	—	±0.7	±1	LSB[3]	T
			10-bit single-ended mode	—	±0.5	±0.75	LSB[3]	T
			8-bit single-ended mode	—	±0.2	±0.5	LSB[3]	T

Table 18. XOSC (Temperature Range = –40 to 105°C Ambient)

#	Characteristic		Symbol	Minimum	Typical[1]	Maximum	Unit
1	Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1)	• Low range (RANGE = 0)	f_{lo}	32	—	38.4	kHz
		• High range (RANGE = 1), • FEE or FBE mode [2]	f_{hi-fll}	1	—	5	MHz
		• High range (RANGE = 1), • PEE or PBE mode [3]	f_{hi-pll}	1	—	16	MHz
		• High range (RANGE = 1), • High gain (HGO = 1), • FBELP mode	f_{hi-hgo}	1	—	16	MHz
		• High range (RANGE = 1), • Low power (HGO = 0), • FBELP mode	f_{hi-lp}	1	—	8	MHz
2	Load capacitors		C_1 C_2	See Note [4]			
3	Feedback resistor	Low range (32 kHz to 38.4 kHz)	R_F	—	10	—	MΩ
		High range (1 MHz to 16 MHz)	—	—	1	—	
4	Series resistor — Low range	Low Gain (HGO = 0)	R_S	—	0	—	kΩ
		High Gain (HGO = 1)		—	100	—	
5	Series resistor — High range	• Low Gain (HGO = 0)	R_S	—	0	—	kΩ
		• High Gain (HGO = 1)					
		≥ 8 MHz		—	0	0	
		4 MHz		—	0	10	
		1 MHz		—	0	20	
6	Crystal start-up time [5, 6]	Low range, low gain (RANGE=0,HGO=0)	t_{CSTL}	—	200	—	ms
		Low range, high gain (RANGE=0,HGO=1)		—	400	—	
		High range, low gain (RANGE=1,HGO=0)	t_{CSTH}	—	5	—	
		High range, high gain (RANGE=1, HGO=1)		—	15	—	

1 Data in Typical column was characterized at 3.0 V, 25°C or is typical recommended value.

2 When MCG is configured for FEE or FBE mode, input clock source must be divisible using RDIV to within the range of 31.25 kHz to 39.0625 kHz.

3 When MCG is configured for PEE or PBE mode, input clock source must be divisible using RDIV to within the range of 1 MHz to 2 MHz.

4 See crystal or resonator manufacturer's recommendation.

5 This parameter is characterized and not tested on each device.

6 Proper PC board layout procedures must be followed to achieve specifications.

Figure 9. Mini-FlexBus Read Timing

Figure 10. Mini-FlexBus Write Timing

3.12 AC Characteristics

This section describes ac timing characteristics for each peripheral system.

3.12.1 Control Timing

Table 20. Control Timing

#	Parameter		Symbol	Minimum	Typical[1]	Maximum	Unit	C
1	Bus frequency ($t_{cyc} = 1/f_{Bus}$)							
		$V_{DD} \geq 1.8$ V	f_{Bus}	dc	—	10	MHz	D
		$V_{DD} > 2.1$ V	f_{Bus}	dc	—	20	MHz	D
		$V_{DD} > 2.4$ V	f_{Bus}	dc	—	25.165	MHz	D
2	Internal low-power oscillator period		t_{LPO}	700	1000	1300	µs	P
3	External reset pulse width[2]	($t_{cyc} = 1/f_{Self\_reset}$)	t_{extrst}	100	—	—	ns	D
4	Reset low drive		t_{rstdrv}	66 x t_{cyc}	—	—	ns	D
5	Active background debug mode	latch setup time	t_{MSSU}	500	—	—	ns	D
6	Active background debug mode	latch hold time	t_{MSH}	100	—	—	ns	D
7	IRQ pulse width • Asynchronous path[2] • Synchronous path[3]		t_{ILIH}, t_{IHIL}	100 1.5 x t_{cyc}	—	—	ns	D
8	KBIPx pulse width • Asynchronous path[2] • Synchronous path[3]		t_{ILIH}, t_{IHIL}	100 1.5 x t_{cyc}	—	—	ns	D
9	Port rise and fall time (load = 50 pF)[4], Low Drive							
		Slew rate control disabled (PTxSE = 0)	t_{Rise}, t_{Fall}	—	11	—	ns	D
		Slew rate control enabled (PTxSE = 1)	t_{Rise}, t_{Fall}	—	35	—	ns	D
		Slew rate control disabled (PTxSE = 0)	t_{Rise}, t_{Fall}	—	40	—	ns	D
		Slew rate control enabled (PTxSE = 1)	t_{Rise}, t_{Fall}	—	75	—	ns	D

1 Typical values are based on characterization data at V_{DD} = 5.0 V, 25 °C unless otherwise stated.

2 This is the shortest pulse that is guaranteed to be recognized as a reset pin request. Shorter pulses are not guaranteed to override reset requests from internal sources.

3 This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized in that case.

4 Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range –40 °C to 105 °C.

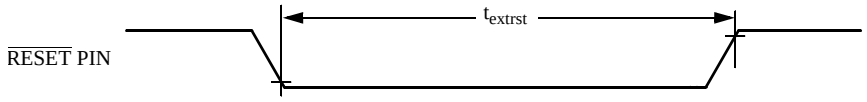


Figure 11. Reset Timing

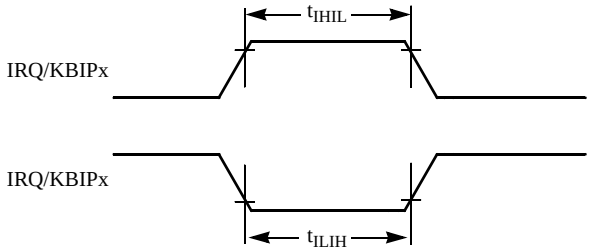
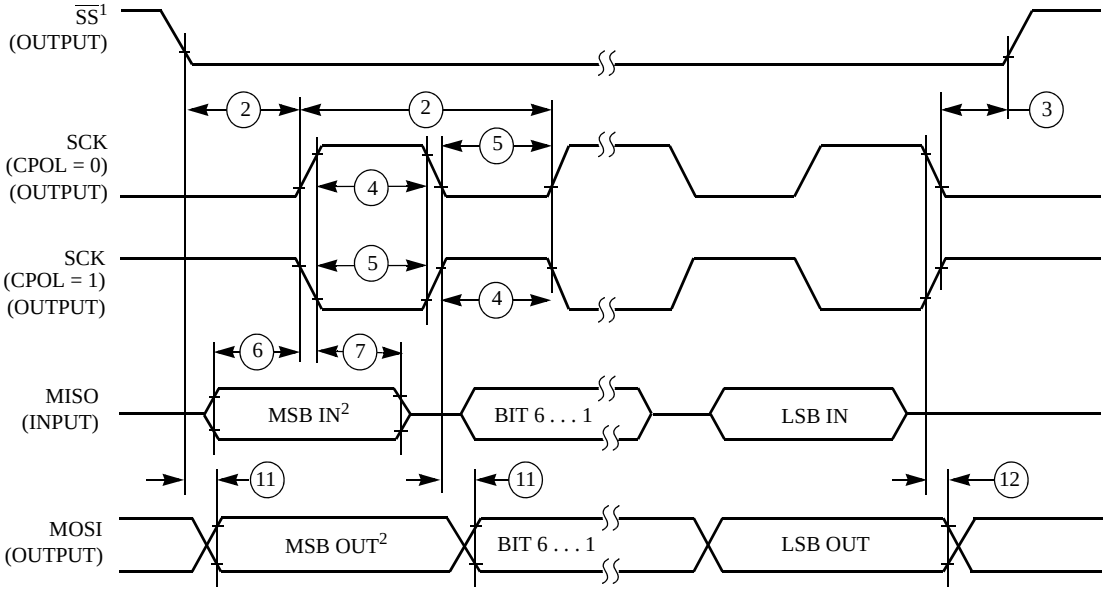
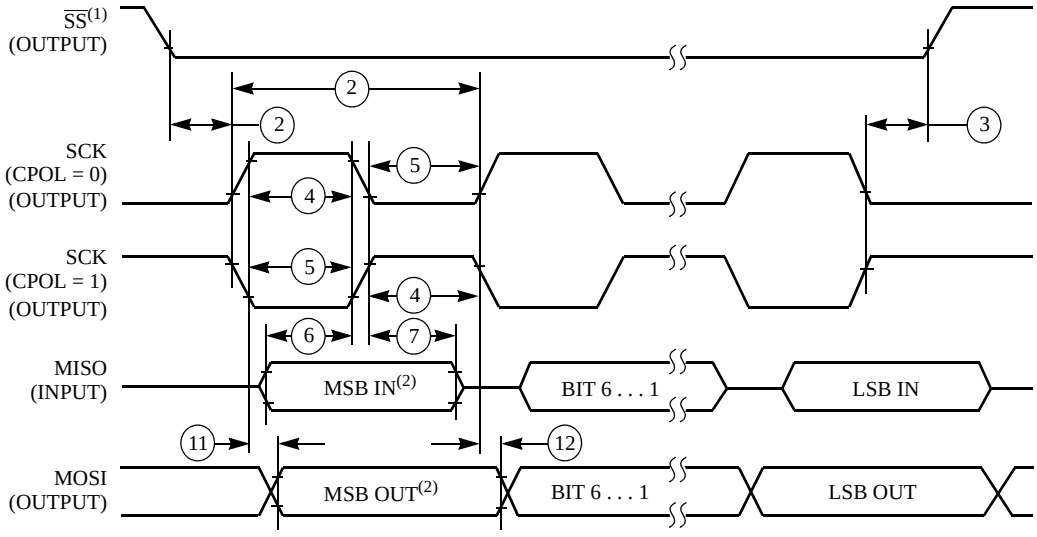


Figure 12. IRQ/KBIPx Timing



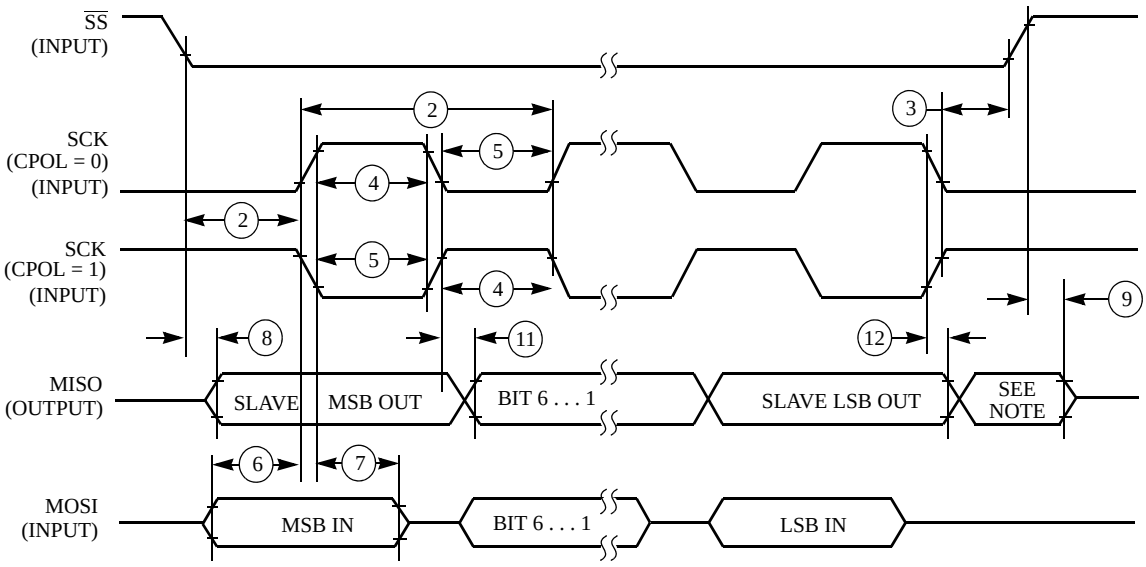
NOTES:
1. $\overline{SS}$ output mode (MODFEN = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 15. SPI Master Timing (CPHA = 0)



NOTES:
1. $\overline{SS}$ output mode (MODFEN = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

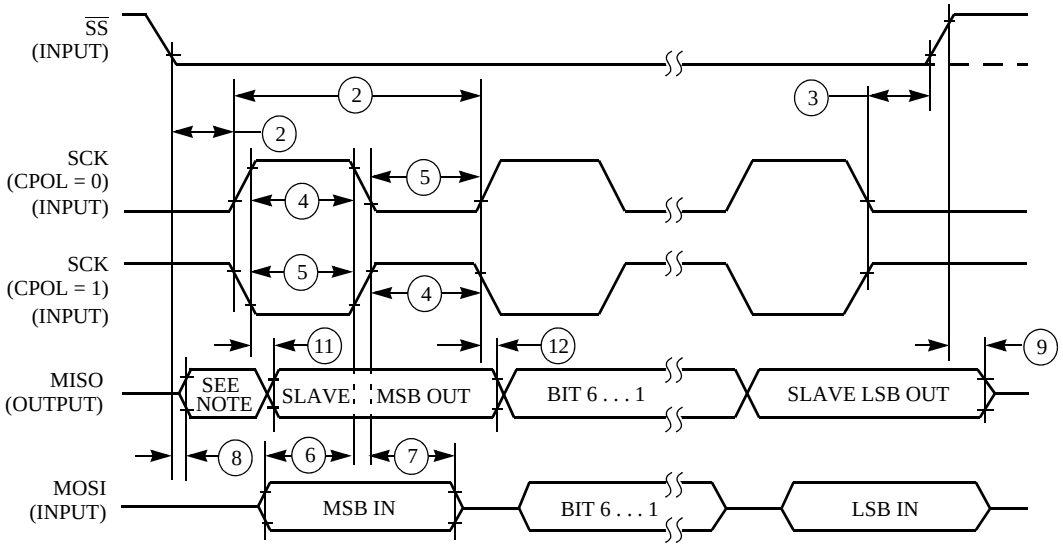
Figure 16. SPI Master Timing (CPHA = 1)



NOTE:

1. Not defined, but normally MSB of character just received

Figure 17. SPI Slave Timing (CPHA = 0)



NOTE:

1. Not defined, but normally LSB of character just received

Figure 18. SPI Slave Timing (CPHA = 1)

3.14 Flash Specifications

This section provides details about program/erase times and program-erase endurance for the Flash memory.

Program and erase operations do not require any special power sources other than the normal V_{DD} supply. For more detailed information about program/erase operations, see the Memory chapter in the Reference Manual for this device (MCF51JE256RM).

Table 23. Flash Characteristics

#	Characteristic	Symbol	Minimum	Typical	Maximum	Unit	C
1	Supply voltage for program/erase -40°C to 105°C	$V_{prog/erase}$	1.8	—	3.6	V	D
2	Supply voltage for read operation	V_{Read}	1.8	—	3.6	V	D
3	Internal FCLK frequency[1]	f_{FCLK}	150	—	200	kHz	D
4	Internal FCLK period (1/FCLK)	t_{Fcyc}	5	—	6.67	µs	D
5	Byte program time (random location)[2]	t_{prog}	9			t_{Fcyc}	P
6	Byte program time (burst mode)[2]	t_{Burst}	4			t_{Fcyc}	P
7	Page erase time[2]	t_{Page}	4000			t_{Fcyc}	P
8	Mass erase time[2]	t_{Mass}	20,000			t_{Fcyc}	P
9	Program/erase endurance[3] T_L to T_H = –40°C to + 105°C T = 25°C		10,000 —	— 100,000	— —	cycles	C
10	Data retention[4]	t_{D_ret}	15	100	—	years	C

1 The frequency of this clock is controlled by a software setting.

2 These values are hardware state machine controlled. User code does not need to count cycles. This information supplied for calculating approximate time to program and erase.

3 **Typical endurance for flash** was evaluated for this product family on the HC9S12Dx64. For additional information on how Freescale defines typical endurance, please refer to Engineering Bulletin EB619, *Typical Endurance for Nonvolatile Memory.*

4 **Typical data retention** values are based on intrinsic capability of the technology measured at high temperature and de-rated to 25°C using the Arrhenius equation. For additional information on how Freescale defines typical data retention, please refer to Engineering Bulletin EB618, *Typical Data Retention for Nonvolatile Memory.*

3.15 USB Electricals

The USB electricals for the USB On-the-Go module conform to the standards documented by the Universal Serial Bus Implementers Forum. For the most up-to-date standards, visit http://www.usb.org.

If the Freescale USB On-the-Go implementation has electrical characteristics that deviate from the standard or require additional information, this space would be used to communicate that information.

Table 24. Internal USB 3.3 V Voltage Regulator Characteristics

#	Characteristic	Symbol	Minimum	Typical	Maximum	Unit	C
1	Regulator operating voltage	V_{regin}	3.9	—	5.5	V	C
2	VREG output	V_{regout}	3	3.3	3.75	V	P

Table 26. VREF Limited Range Operating Behaviors

#	Characteristic	Symbol	Minimum	Maximum	Unit	C
1	Voltage Reference Output with Factory Trim	V_{out}	1.149	1.152	mV	T
2	Temperature Drift (Vmin – Vmax Temperature range from 0° C to 50° C	Tdrift	—	3	mV[1]	T

1 See typical chart that follows (Figure 19).

Figure 19. Typical VREF Output vs Temperature

4 Ordering Information

This section contains ordering information for the device numbering system. See Table 1 for feature summary by package information.

4.1 Part Numbers

Table 27. Orderable Part Number Summary

Freescale Part Number	Description	Flash / SRAM (Kbytes)	Package	Temperature
MCF51JE256VML	MCF51JE256 ColdFire Microcontroller	256K/32K	104 MAPBGA	–40 to 105 °C
MCF51JE256VLL	MCF51JE256 ColdFire Microcontroller	256K/32K	100 LQFP	–40 to 105 °C
MCF51JE256VMB	MCF51JE256 ColdFire Microcontroller	256K/32K	81 MAPBGA	–40 to 105 °C
MCF51JE256VLK	MCF51JE256 ColdFire Microcontroller	256K/32K	80 LQFP	–40 to 105 °C
MCF51JE128VMB	MCF51JE128 ColdFire Microcontroller	128K/32K	81 MAPBGA	–40 to 105 °C
MCF51JE256CML	MCF51JE256 ColdFire Microcontroller	256K/32K	104 MAPBGA	–40 to 85 °C
MCF51JE256CLL	MCF51JE256 ColdFire Microcontroller	256K/32K	10O LQFP	–40 to 85 °C
MCF51JE256CMB	MCF51JE256 ColdFire Microcontroller	256K/32K	81 MAPBGA	–40 to 85 °C
MCF51JE256CLK	MCF51JE256 ColdFire Microcontroller	256K/32K	80 LQFP	–40 to 85 °C
MCF51JE128CMB	MCF51JE128 ColdFire Microcontroller	128K/32K	81 MAPBGA	–40 to 85 °C
MCF51JE128CLK	MCF51JE128 ColdFire Microcontroller	128K/32K	80 LQFP	–40 to 85 °C

4.2 Package Information

Table 28. Package Descriptions

Pin Count	Package Type	Abbreviation	Designator	Case No.	Document No.
100	Low Quad Flat Package	LQFP	LL	983-03	98ASS23308W
80	Low Quad Flat Package	LQFP	LK	1418	98ASS23174W
104	MAP BGA Package	MAPBGA	ML	1285-02	98ARH98267A
81	MAP BGA Package	MAPBGA	MB	1662-01	98ASA10670D

4.3 Mechanical Drawings

Table 28 provides the available package types and their document numbers. The latest package outline/mechanical drawings are available on the MCF51JE256/128 Product Summary pages at http://www.freescale.com.

To view the latest drawing, either:

- Click on the appropriate link in Table 28, or

Table 29. Revision History

Revision	Date	Description
4	August 2012	• In Table 1."MCF51JE256/128 Features by MCU and Package, removed the row of "12-bit SAR ADCDifferential Channels". • In Table 3, "Package Pin Assignments", changed from: 'A1' — PTG1 USB_ SESSEND to:'B3' — PTG1 USB_ SESSEND. • In Table 10,"Supply Current Characteristics", for $S3I_{DD}$ changed the max value from '1.2' to '1.3' and typical value from '0.650' to '0.750' for the first row. • In Table 10,"Supply Current Characteristics": — For parameter 3 and parameter 4 changed LPS to LPR. — For parameter 3,changed "FBILP" to "FBI". — For parameter 4, changed "FBELP" to "BLPE". • Fixed the TBD parameters and added figure"Typical Output vs VDD", following the same setup of MM256DS — Added Figure 7,"Offset at Half Scale vs Temperature". — Updated Table 9,"DC Characteristics**".** — Updated Table 10,"Supply Current Characteristics**".** — Updated Table 11,"Stop Mode Adders". — Added Figure 20,"Typical Output vs. V_{DD}. — Updated Table 14,"DAC 12-Bit Operating Behaviors". — Updated Table 20,"Control Timing". — Removed "SPI Electrical Characteristics" table. — Updated Table 25"VREF Electrical Specifications**".** — Updated Table 26,"VREF Limited Range Operating Behaviors**".** • Updated Figure 3, Figure 4, and Figure 5.