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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Coldfire V1
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	EBI/EMI, I²C, SCI, SPI, USB OTG
Peripherals	LVD, PWM, WDT
Number of I/O	47
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 12x12b; D/A 1x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcf51je128vlk

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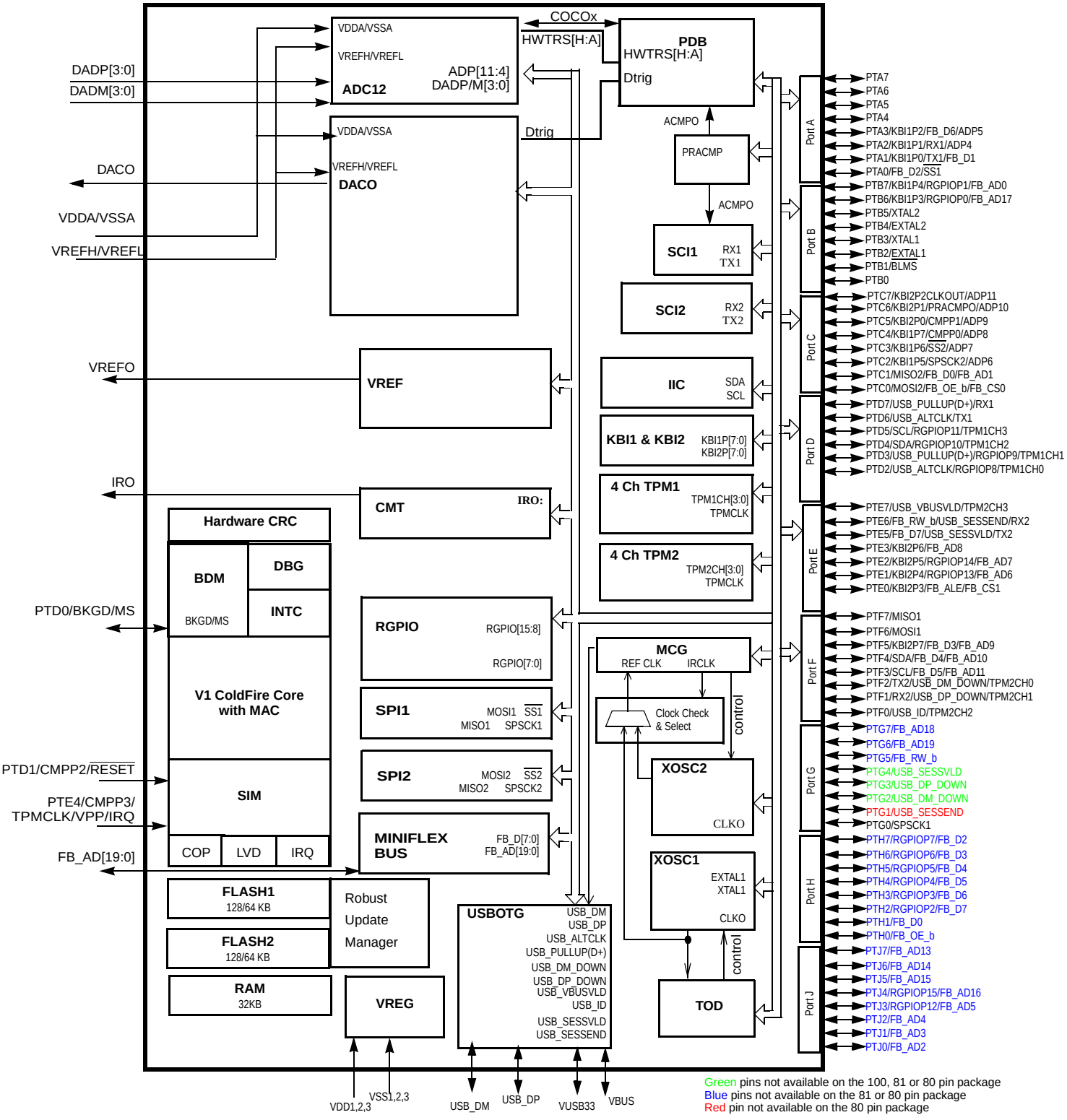


Figure 1. MCF51JE256/128 Block Diagram

2.2 100-Pin LQFP

The following figure shows the 100-pin LQFP pinout configuration.

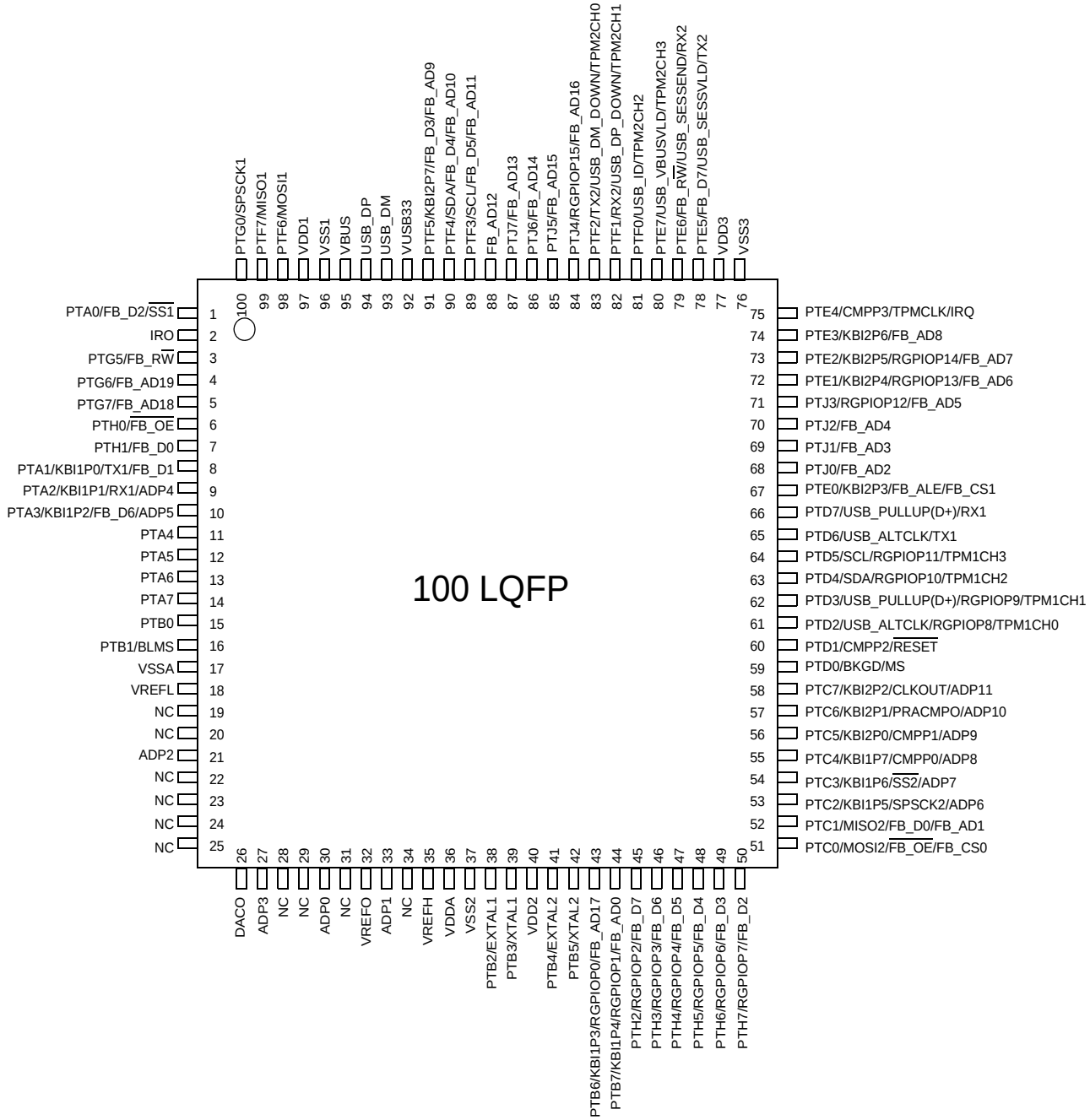


Figure 3. 100-Pin LQFP

Table 3. Package Pin Assignments (continued)

Package				Default Function	Alternate 1	Alternate 2	Alternate 3	Composite Pin Name
104 MAPBGA	100 LQFP	81 MAPBGA	80 LQFP					
H4	96	F6	76	VSS1	—	—	—	VSS1
D4	97	E6	77	VDD1	—	—	—	VDD1
A1	98	A3	78	PTF6	MOSI1	—	—	PTF6/MOSI1
A2	99	B1	79	PTF7	MISO1	—	—	PTF7/MISO1
B1	100	A2	80	PTG0	SPSCK1	—	—	PTG0/SPSCK1
F4	—	B3	—	PTG1	USB_SESSEND	—	—	PTG1/USB_SESSEND
C4	—	—	—	PTG2	USB_DM_DOWN	—	—	PTG2/USB_DM_DOWN
B3	—	—	—	PTG3	USB_DP_DOWN	—	—	PTG3/USB_DP_DOWN
C2	—	—	—	PTG4	USB_SESSVLD	—	—	PTG4/USB_SESSVLD

3 Preliminary Electrical Characteristics

This section contains electrical specification tables and reference timing diagrams for the MCF51JE256/128 microcontroller, including detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications.

The electrical specifications are preliminary and are from previous designs or design simulations. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle. These specifications will, however, be met for production silicon. Finalized specifications will be published after complete characterization and device qualifications have been completed.

NOTE

The parameters specified in this data sheet supersede any values found in the module specifications.

3.1 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 4. Parameter Classifications

P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

3.2 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in the following table may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

Table 5. Absolute Maximum Ratings

#	Rating	Symbol	Value	Unit
1	Supply voltage	V_{DD}	–0.3 to 3.8	V
2	Maximum current into V_{DD}	I_{DD}	120	mA
3	Digital Input voltage	V_{In}	–0.3 to V_{DD} + 0.3	V
4	Instantaneous maximum current Single pin limit (applies to all port pins)[1, 2, 3]	I_D	±25	mA
5	Storage temperature range	T_{stg}	–55 to 150	°C

1 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive (V_{DD}) and negative (V_{SS}) clamp voltages, then use the larger of the two resistance values.

2 All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.

3 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low (which would reduce overall power consumption).

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}).

3.3 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and it is user-determined rather than being controlled by the MCU design. In order to take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 6. Thermal Characteristics

#	Symbol	Rating		Value	Unit
1	T_A	Operating temperature range (packaged):			°C
			MCF51JE256	–40 to 105	
			MCF51JE128	–40 to 105	
2	T_{JMAX}	Maximum junction temperature		135	°C
3	θ_{JA}	Thermal resistance[1,2,3,4] Single-layer board — 1s			°C/W
			104-pin MBGA	67	
			100-pin LQFP	53	
			81-pin MBGA	67	
			80-pin LQFP	53	
4	θ_{JA}	Thermal resistance[1, 2, 3, 4] Four-layer board — 2s2p			°C/W
			104-pin MBGA	39	
			100-pin LQFP	41	
			81-pin MBGA	39	
			80-pin LQFP	39	

1 Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2 Junction to Ambient Natural Convection
3 1s — Single layer board, one signal layer
4 2s2p — Four layer board, 2 signal and 2 power layers

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad \textit{Eqn. 1}$$

where:

T_A = Ambient temperature, °C
θ_{JA} = Package thermal resistance, junction-to-ambient, °C/W
$P_D = P_{int} + P_{I/O}$
$P_{int} = I_{DD} \times V_{DD}$, Watts — chip internal power
$P_{I/O}$ = Power dissipation on input and output pins — user determined

For most applications, $P_{I/O} << P_{int}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad \textit{Eqn. 2}$$

Solving Equation 1 and Equation 2 for K gives:

$$K = P_D \times (T_A + 273°C) + \theta_{JA} \times (P_D)^2 \quad \textit{Eqn. 3}$$

[8] Maximum is highest voltage that POR is guaranteed.
[9] Run at 1 MHz bus frequency.
[10] Low voltage detection and warning limits measured at 1 MHz bus frequency.
[11] Factory trimmed at V_{DD} = 3.0 V, Temp = 25°C.

3.6 Supply Current Characteristics

Table 10. Supply Current Characteristics

#	Symbol	Parameter	Bus Freq	V_{DD} (V)	Typical[1]	Maximum	Unit	Temperature (°C)	C
1	RI_{DD}	Run supply current FEI mode, all modules ON[2]							
			25.165 MHz	3	44	48	mA	–40 to 25	P
			25.165 MHz	3	44	48	mA	105	P
			20 MHz	3	32.3	—	mA	–40 to 105	T
			8 MHz	3	16.4	—	mA	–40 to 105	T
			1 MHz	3	2.9	—	mA	–40 to 105	T
2	RI_{DD}	Run supply current FEI mode, all modules OFF[3]							
			25.165 MHz	3	29	29.6	mA	–40 to 105	C
			20 MHz	3	25.4	—	mA	–40 to 105	T
			8 MHz	3	12.7	—	mA	–40 to 105	T
			1 MHz	3	2.4	—	mA	–40 to 105	T
3	RI_{DD}	Run supply current LPR=0, all modules OFF[3]							
			16 kHz FBI	3	232	280	μA	–40 to 105	T
			16 kHz FBE	3	231	296	μA	–40 to 105	T
4	RI_{DD}	Run supply current LPR=1, all modules OFF[3]							
			16 kHz BLPE	3	74	75	μA	0 to 70	T
			16 kHz BLPE	3	74	120	μA	–40 to 105	T
5	WI_{DD}	Wait mode supply current FEI mode, all modules OFF[3]							
			25.165 MHz	3	16.5	—	mA	–-40 to 105	C
			20 MHz	3	10.3	—	mA	–-40 to 105	T
			8 MHz	3	6.6	—	mA	–-40 to 105	T
			1 MHz	3	1.7	—	mA	–-40 to 105	T

Table 10. Supply Current Characteristics (continued)

#	Symbol	Parameter	Bus Freq	V_{DD} (V)	Typical[1]	Maximum	Unit	Temperature (°C)	C
6	$S2I_{DD}$	Stop2 mode supply current[4]							
			N/A	3	0.410	1	μA	-40 to 25	P
			N/A	3	3.7	10	μA	70	C
			N/A	3	10	20	μA	85	C
			N/A	3	21	31.5	μA	105	P
			N/A	2	0.410	0.640	μA	-40 to 25	C
			N/A	2	3.4	9	μA	70	C
			N/A	2	9.5	18	μA	85	C
			N/A	2	20	30	μA	105	C
7	$S3I_{DD}$	Stop3 mode supply current No clocks active	N/A	3	0.750	1.3	μA	-40 to 25	P
			N/A	3	8.5	18	μA	70	C
			N/A	3	20	28	μA	85	C
			N/A	3	53	63	μA	105	P
			N/A	2	0.400	0.900	μA	-40 to 25	C
			N/A	2	8.2	16	μA	70	C
			N/A	2	18	26	μA	85	C
			N/A	2	47	59	μA	105	C

1 Data in Typical column was characterized at 3.0 V, 25°C or is typical recommended value.

2 ON = System Clock Gating Control registers turn on system clock to the corresponding modules.

3 OFF = System Clock Gating Control registers turn off system clock to the corresponding modules.

4 All digital pins must be configured to a known state to prevent floating pins from adding current. Smaller packages may have some pins that are not bonded out; however, software must still be configured to the largest pin package available so that all pins are in a known state. Otherwise, floating pins that are not bonded in the smaller packages may result in a higher current draw. NOTE: I/O pins are configured to output low; input-only pins are configured to pullup-enabled. IRO pin connects to ground. FB_AD12 pin is pullup-enabled. DACO, and VREFO pins are at reset state and unconnected.

Table 11. Stop Mode Adders

#	Parameter	Condition	Temperature (°C)					Units	C
			-40	25	70	85	105		
1	LPO	—	50	75	100	150	250	nA	D
2	EREFSTEN	RANGE = HGO = 0	600	650	750	850	1000	nA	D
3	IREFSTEN[1]	—	—	73	80	93	125	μA	T
4	TOD	Does not include clock source current	50	75	100	150	250	nA	D

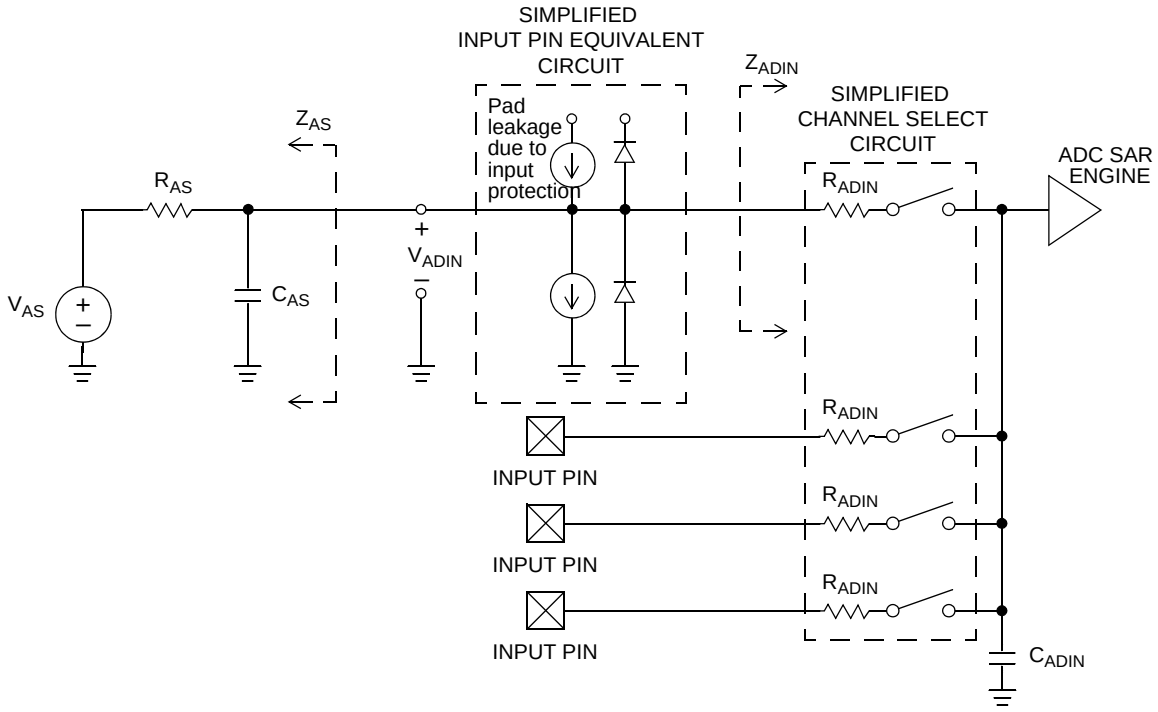


Figure 8. ADC Input Impedance Equivalency Diagram

Table 16. 12-bit SAR ADC Characteristics full operating range ($V_{REFH} = V_{DDAD}$, $V_{REFL} = V_{SSAD}$)

#	Symbol	Characteristic	Conditions[1]	Minimum	Typical[2]	Maximum	Unit	C
1	I_{DDAD}	Supply Current (ADLSMP=0, ADCO=1)	ADLPC=1, ADHSC=0	—	215	—	μA	T
			ADLPC=0, ADHSC=0	—	470	—	μA	T
			ADLPC=0, ADHSC=1	—	610	—	μA	T
			Stop, Reset, Module Off	—	0.01	—	μA	C
2	f_{ADACK}	ADC Asynchronous Clock Source (t_{ADACK} =1/f_{ADACK})	ADLPC=1, ADHSC=0	—	2.4	—	MHz	P
			ADLPC=0, ADHSC=0	—	5.2	—	MHz	P
			ADLPC=0, ADHSC=1	—	6.2	—	MHz	P
3	—	Sample Time — *See Reference Manual for sample times.*						
4	—	Conversion Time — *See Rreference Manual for conversion times.*						
5	TUE	Total Unadjusted Error 32x Hardware Averaging (AVGE = %1 AVGS = %11)	12-bit single-ended mode	—	±1.75	±3.5	LSB[3]	T
			10-bit single-ended mode	—	±0.8	±1.5	LSB[3]	T
			8-bit single-ended mode	—	±0.5	±1.0	LSB[3]	T
6		Differential Non-Linearity	12-bit single-ended mode	—	±0.7	±1	LSB[3]	T
			10-bit single-ended mode	—	±0.5	±0.75	LSB[3]	T
			8-bit single-ended mode	—	±0.2	±0.5	LSB[3]	T

Table 16. 12-bit SAR ADC Characteristics full operating range (V_{REFH} = V_{DDAD}, V_{REFL} = V_{SSAD}) (continued)

#	Symbol	Characteristic	Conditions[1]	Minimum	Typical[2]	Maximum	Unit	C
7	INL	Integral Non-Linearity	12-bit single-ended mode	—	±1.0	±2.5	LSB[3]	T
			10-bit single-ended mode	—	±0.5	±1.0	LSB[3]	T
			8-bit single-ended mode	—	±0.3	±0.5	LSB[3]	T
8	E_{ZS}	Zero-Scale Error (V_{ADIN} = V_{SSAD})	12-bit single-ended mode	—	±0.7	±2.0	LSB[3]	T
			10-bit single-ended mode	—	±0.4	±1.0	LSB[3]	T
			8-bit single-ended mode	—	±0.2	±0.5	LSB[3]	T
9	E_{FS}	Full-Scale Error (V_{ADIN} = V_{DDAD})	12-bit single-ended mode	—	±1.0	±3.5	LSB[3]	T
			10-bit single-ended mode	—	±0.4	±1.5	LSB[3]	T
			8-bit single-ended mode	—	±0.2	±0.5	LSB[3]	T
10	E_Q	Quantization Error	All modes	—	—	±0.5	LSB[3]	D
11	E_{IL}	Input Leakage Error (I_{In} = leakage current (refer to DC Characteristics)	All modes	I_{In} * R_{AS}			mV	D
12	m	Temp Sensor Slope	-40°C to 25°C	—	1.646	—	mV/xC	C
			25°C to 125°C	—	1.769	—	mV/xC	C
13	V_{TEMP25}	Temp Sensor Voltage	25°C	—	701.2	—	mV	C

1 All accuracy numbers assume the ADC is calibrated with V_{REFH}=V_{DDAD}.

2 Typical values assume V_{DDAD} = 3.0V, Temp = 25°C, f_{ADCK}=2.0MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

3 1 LSB = (V_{REFH} - V_{REFL})/2^N

3.10 MCG and External Oscillator (XOSC) Characteristics

Table 17. MCG (Temperature Range = –40 to 105°C Ambient)

#	Rating		Symbol	Min	Typical	Max	Unit	C
1	Internal reference startup time		t_{irefst}	—	55	100	µs	D
2	Average internal reference frequency	factory trimmed at VDD=3.0V and temp=25°C	f_{int_ft}	—	31.25	—	kHz	C
		user trimmed		31.25	—	39.0625	KHz	C
3	DCO output frequency range - trimmed	Low range (DRS=00)	f_{dco_t}	16	—	20	MHz	C
		Mid range (DRS=01)		32	—	40	MHz	C
		High range[1] (DRS=10)		40	—	60	MHz	C
4	Resolution of trimmed DCO output frequency at fixed voltage and temperature	with FTRIM	$\Delta f_{dco\_res\_t}$	—	± 0.1	± 0.2	$\%f_{dco}$	C
		without FTRIM		—	± 0.2	± 0.4	$\%f_{dco}$	C

Table 17. MCG (Temperature Range = –40 to 105°C Ambient) (continued)

#	Rating		Symbol	Min	Typical	Max	Unit	C
5	Total deviation of trimmed DCO output frequency over voltage and temperature	over voltage and temperature	Δf_{dco_t}	—	± 1.0	± 2	$\%f_{dco}$	P
		over fixed voltage and temp range of 0 - 70 °C		—	± 0.5	± 1	$\%f_{dco}$	C
6	Acquisition time	FLL[2]	$t_{fll\_acquire}$	—	—	1	ms	C
		PLL[3]	$t_{pll\_acquire}$	—	—	1	ms	D
7	Long term Jitter of DCO output clock (averaged over 2mS interval) [4]		C_{Jitter}	—	0.02	0.2	$\%f_{dco}$	C
8	VCO operating frequency		f_{vco}	7.0	—	55.0	MHz	D
9	PLL reference frequency range		f_{pll_ref}	1.0	—	2.0	MHz	D
10	Jitter of PLL output clock measured over 625 ns	Long term	$f_{pll\_jitter\_625\ ns}$	—	0.566[4]	—	%fpll	D
11	Lock frequency tolerance	Entry[5]	D_{lock}	± 1.49	—	± 2.98	%	D
		Exit[6]	D_{unl}	± 4.47	—	± 5.97	%	D
12	Lock time	FLL	t_{fll_lock}	—	—	$t_{fll\_acquire}$+ 1075(1/f_{int_t})	s	D
		PLL	t_{pll_lock}	—	—	$t_{pll\_acquire}$+ 1075(1/f_{pll_ref})	s	D
13	Loss of external clock minimum frequency - RANGE = 0		f_{loc_low}	(3/5) x f_{int_t}	—	—	kHz	D
14	Loss of external clock minimum frequency - RANGE = 1		f_{loc_high}	(16/5) x f_{int_t}	—	—	kHz	D

1 This should not exceed the maximum CPU frequency of 50.33 MHz.

2 This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bit is changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

3 This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

4 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{BUS}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

5 Below D_{lock} minimum, the MCG is guaranteed to enter lock. Above D_{lock} maximum, the MCG will not enter lock. But if the MCG is already in lock, then the MCG may stay in lock.

6 Below D_{unl} minimum, the MCG will not exit lock if already in lock. Above D_{unl} maximum, the MCG is guaranteed to exit lock.

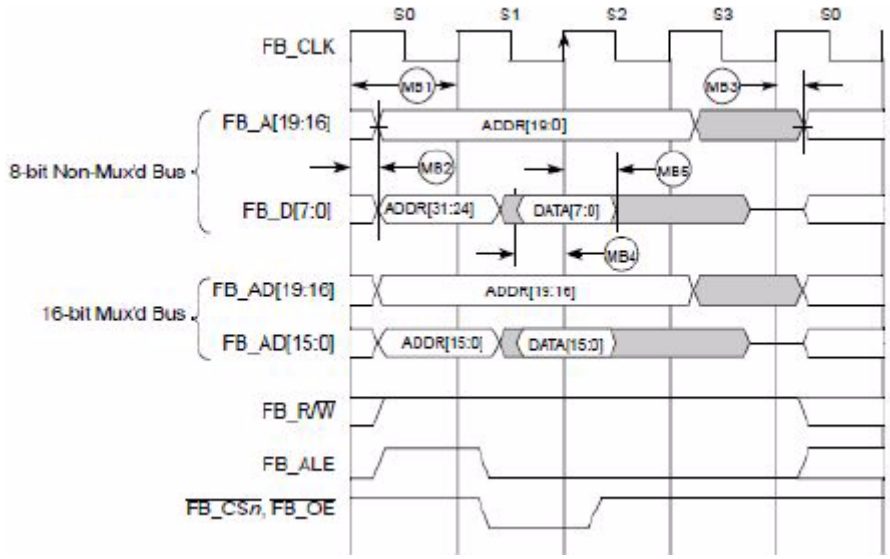


Figure 9. Mini-FlexBus Read Timing

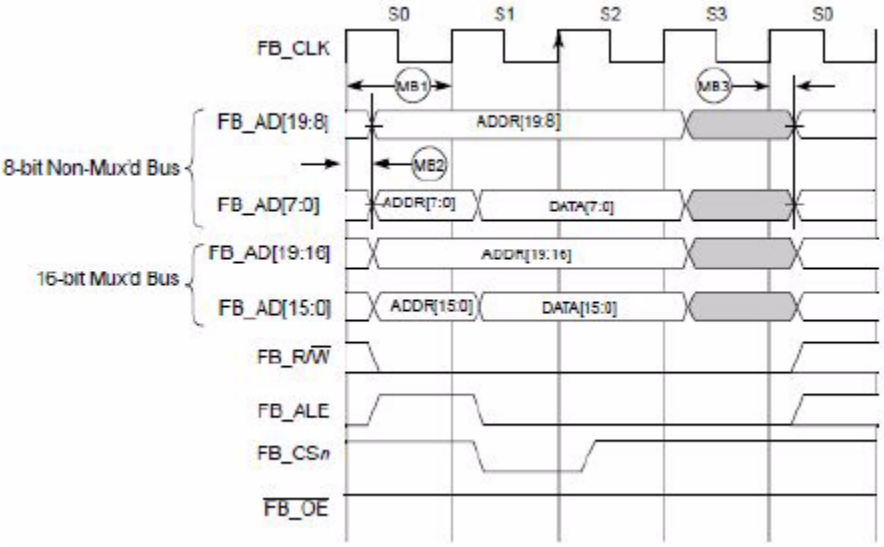


Figure 10. Mini-FlexBus Write Timing

3.12 AC Characteristics

This section describes ac timing characteristics for each peripheral system.

3.12.1 Control Timing

Table 20. Control Timing

#	Parameter		Symbol	Minimum	Typical[1]	Maximum	Unit	C
1	Bus frequency ($t_{cyc} = 1/f_{Bus}$)							
		$V_{DD} \geq 1.8$ V	f_{Bus}	dc	—	10	MHz	D
		$V_{DD} > 2.1$ V	f_{Bus}	dc	—	20	MHz	D
		$V_{DD} > 2.4$ V	f_{Bus}	dc	—	25.165	MHz	D
2	Internal low-power oscillator period		t_{LPO}	700	1000	1300	µs	P
3	External reset pulse width[2]	($t_{cyc} = 1/f_{Self\_reset}$)	t_{extrst}	100	—	—	ns	D
4	Reset low drive		t_{rstdrv}	66 x t_{cyc}	—	—	ns	D
5	Active background debug mode	latch setup time	t_{MSSU}	500	—	—	ns	D
6	Active background debug mode	latch hold time	t_{MSH}	100	—	—	ns	D
7	IRQ pulse width • Asynchronous path[2] • Synchronous path[3]		t_{ILIH}, t_{IHIL}	100 1.5 x t_{cyc}	—	—	ns	D
8	KBIPx pulse width • Asynchronous path[2] • Synchronous path[3]		t_{ILIH}, t_{IHIL}	100 1.5 x t_{cyc}	—	—	ns	D
9	Port rise and fall time (load = 50 pF)[4], Low Drive							
		Slew rate control disabled (PTxSE = 0)	t_{Rise}, t_{Fall}	—	11	—	ns	D
		Slew rate control enabled (PTxSE = 1)	t_{Rise}, t_{Fall}	—	35	—	ns	D
		Slew rate control disabled (PTxSE = 0)	t_{Rise}, t_{Fall}	—	40	—	ns	D
		Slew rate control enabled (PTxSE = 1)	t_{Rise}, t_{Fall}	—	75	—	ns	D

1 Typical values are based on characterization data at V_{DD} = 5.0 V, 25 °C unless otherwise stated.

2 This is the shortest pulse that is guaranteed to be recognized as a reset pin request. Shorter pulses are not guaranteed to override reset requests from internal sources.

3 This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized in that case.

4 Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range –40 °C to 105 °C.

3.12.2 TPM Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 21. TPM Input Timing

#	C	Function	Symbol	Minimum	Maximum	Unit
1	—	External clock frequency	f_{TPMext}	dc	$f_{Bus}/4$	MHz
2	—	External clock period	t_{TPMext}	4	—	t_{cyc}
3	D	External clock high time	t_{clkh}	1.5	—	t_{cyc}
4	D	External clock low time	t_{clkl}	1.5	—	t_{cyc}
5	D	Input capture pulse width	t_{ICPW}	1.5	—	t_{cyc}

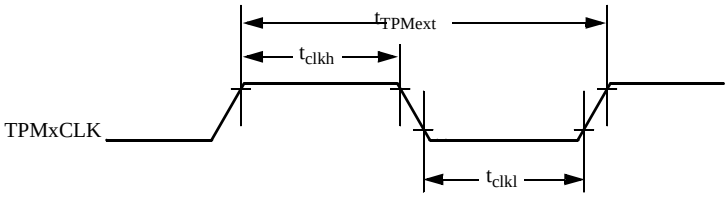


Figure 13. Timer External Clock

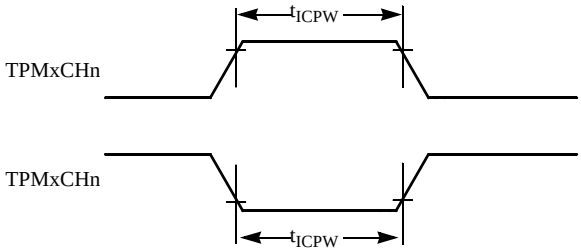
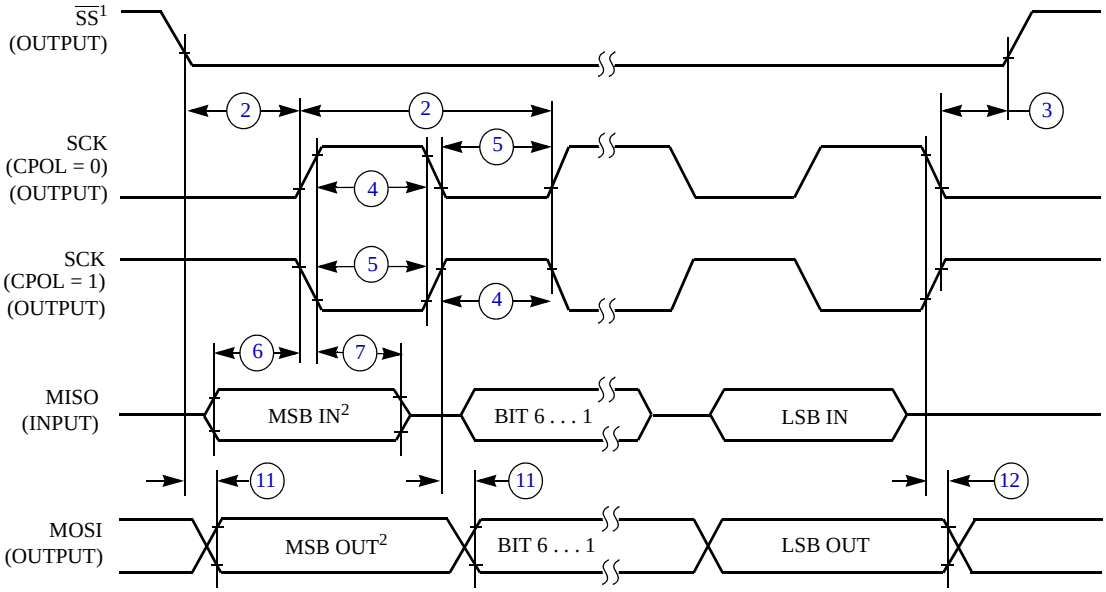
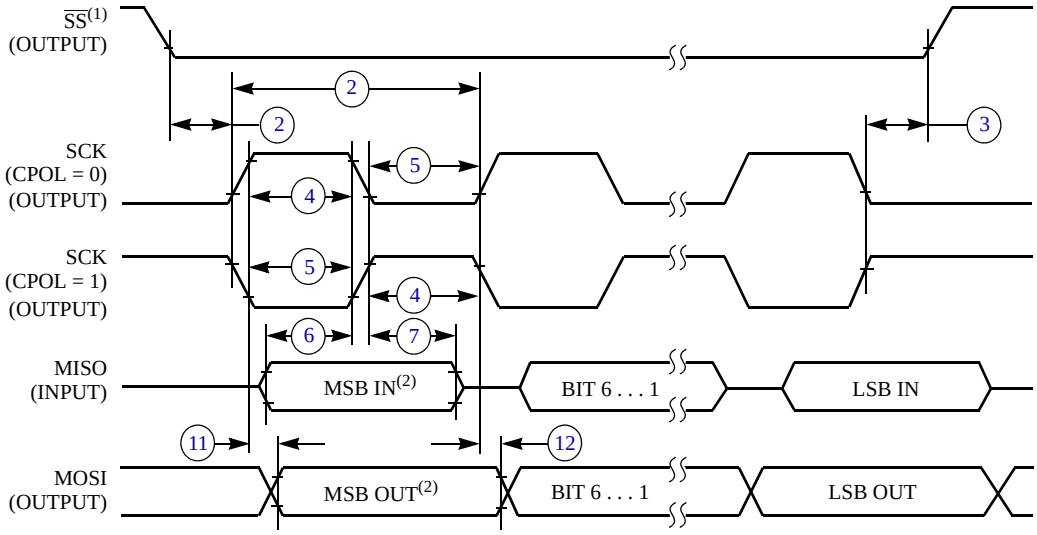


Figure 14. Timer Input Capture Pulse



NOTES:
1. $\overline{SS}$ output mode (MODFEN = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 15. SPI Master Timing (CPHA = 0)



NOTES:
1. $\overline{SS}$ output mode (MODFEN = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 16. SPI Master Timing (CPHA = 1)

3.14 Flash Specifications

This section provides details about program/erase times and program-erase endurance for the Flash memory.

Program and erase operations do not require any special power sources other than the normal V_{DD} supply. For more detailed information about program/erase operations, see the Memory chapter in the Reference Manual for this device (MCF51JE256RM).

Table 23. Flash Characteristics

#	Characteristic	Symbol	Minimum	Typical	Maximum	Unit	C
1	Supply voltage for program/erase -40°C to 105°C	$V_{prog/erase}$	1.8	—	3.6	V	D
2	Supply voltage for read operation	V_{Read}	1.8	—	3.6	V	D
3	Internal FCLK frequency[1]	f_{FCLK}	150	—	200	kHz	D
4	Internal FCLK period (1/FCLK)	t_{Fcyc}	5	—	6.67	µs	D
5	Byte program time (random location)[2]	t_{prog}	9			t_{Fcyc}	P
6	Byte program time (burst mode)[2]	t_{Burst}	4			t_{Fcyc}	P
7	Page erase time[2]	t_{Page}	4000			t_{Fcyc}	P
8	Mass erase time[2]	t_{Mass}	20,000			t_{Fcyc}	P
9	Program/erase endurance[3] T_L to T_H = –40°C to + 105°C T = 25°C		10,000 —	— 100,000	— —	cycles	C
10	Data retention[4]	t_{D_ret}	15	100	—	years	C

1 The frequency of this clock is controlled by a software setting.

2 These values are hardware state machine controlled. User code does not need to count cycles. This information supplied for calculating approximate time to program and erase.

3 **Typical endurance for flash** was evaluated for this product family on the HC9S12Dx64. For additional information on how Freescale defines typical endurance, please refer to Engineering Bulletin EB619, *Typical Endurance for Nonvolatile Memory.*

4 **Typical data retention** values are based on intrinsic capability of the technology measured at high temperature and de-rated to 25°C using the Arrhenius equation. For additional information on how Freescale defines typical data retention, please refer to Engineering Bulletin EB618, *Typical Data Retention for Nonvolatile Memory.*

3.15 USB Electricals

The USB electricals for the USB On-the-Go module conform to the standards documented by the Universal Serial Bus Implementers Forum. For the most up-to-date standards, visit http://www.usb.org.

If the Freescale USB On-the-Go implementation has electrical characteristics that deviate from the standard or require additional information, this space would be used to communicate that information.

Table 24. Internal USB 3.3 V Voltage Regulator Characteristics

#	Characteristic	Symbol	Minimum	Typical	Maximum	Unit	C
1	Regulator operating voltage	V_{regin}	3.9	—	5.5	V	C
2	VREG output	V_{regout}	3	3.3	3.75	V	P

Table 26. VREF Limited Range Operating Behaviors

#	Characteristic	Symbol	Minimum	Maximum	Unit	C
1	Voltage Reference Output with Factory Trim	V_{out}	1.149	1.152	mV	T
2	Temperature Drift (Vmin – Vmax Temperature range from 0° C to 50° C	Tdrift	—	3	mV[1]	T

1 See typical chart that follows (Figure 19).

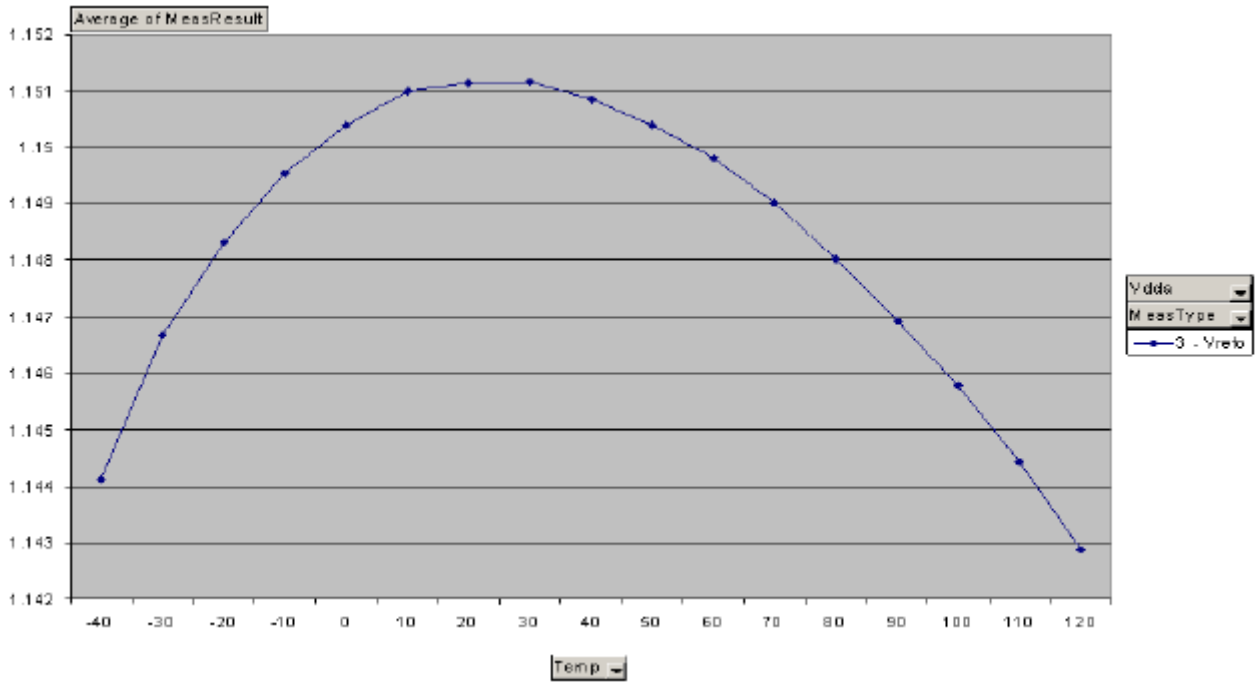


Figure 19. Typical VREF Output vs Temperature

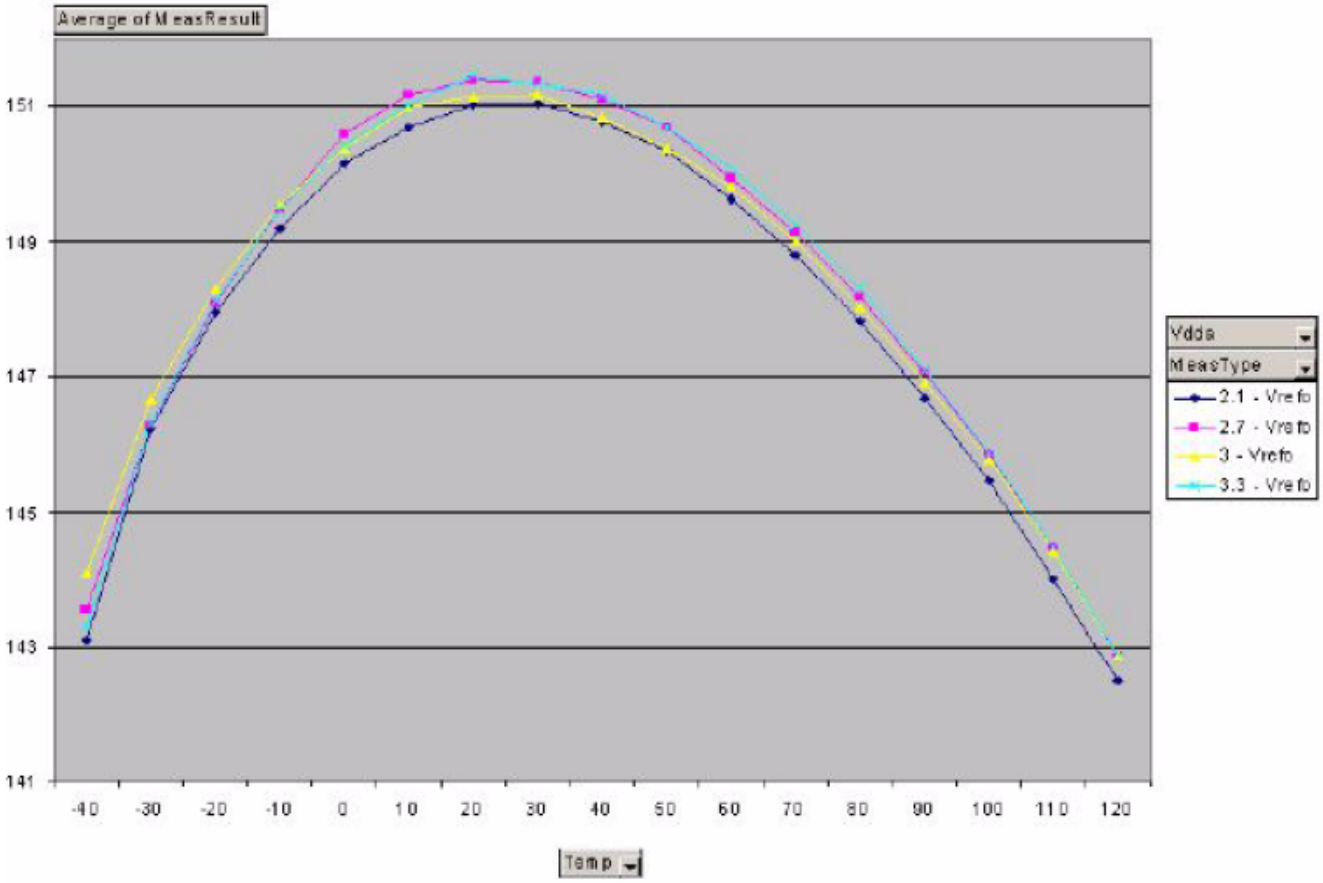


Figure 20. Typical VREF Output vs V_{DD}

- Open a browser to the Freescale® website (http://www.freescale.com), and enter the appropriate document number (from Table 28) in the “Enter Keyword” search box at the top of the page.

5 Revision History

This section lists major changes between versions of the MCF51JE256 Data Sheet.

Table 29. Revision History

Revision	Date	Description
0	March/April 09	Initial Draft
1	July 2009	• Revised to follow standard template. • Removed extraneous headings from the TOC. • Corrected units for Monotoncity to be blank in for the DAC specification. • Updated ADC characteristic tables to include 16-Bit SAR in headings.
2	July 2009	• Changed MCG (XOSC) Electricals Table - Row 2, Average Internal Reference Frequency typical value from 32.768 to 31.25
3	April 2010	• Updated Thermal Characteristics table. Reinserted the 81 and 104 MapBGA devices. • Revised the ESD and Latch-Up Protection Characeristic description to read: Latch-up Current at T_A = 125°C. • Changed Table 9. DC Characteristics rows 2 and 4, to 1.8 V, ILoad = -600 mA conditions to 1.8 V, ILoad = 600μA respectively. • Corrected the 16-bit SAR ADC Operating Condition table Ref Voltage High Min value to be 1.13 instead of 1.15. • Updated the ADC electricals. • Inserted the Mini-FlexBus Timing Specifications. • Added a Temp Drift parameter to the VREF Electrical Specifications. • Removed the S08 Naming Convention diagram. • Updated the Orderable Part Number Summary to include the Freescale Part Number suffixes. • Completed the Package Description table values. • Changed the 80LQFP package drawing from 98ARL10530D to 98ASS23174W. • Updated electrical characteristic data.