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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	Coldfire V1
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	EBI/EMI, I²C, SCI, SPI, USB OTG
Peripherals	LVD, PWM, WDT
Number of I/O	48
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 12x12b; D/A 1x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	81-LBGA
Supplier Device Package	81-MAPBGA (10x10)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcf51je128vmb

1 Features

The following table provides a cross-comparison of the features of the MCF51JE256/128 according to package.

Table 1. MCF51JE Features by MCU and Package

Feature	MCF51JE256				MCF51JE128	
FLASH size (bytes)	262144				131072	
RAM size (bytes)	32K				32K	
Pin quantity	104	100	81	80	81	80
Programmable Analog Comparator (PRACMP)	yes					
Debug Module (DBG)	yes					
Multipurpose Clock Generator (MCG)	yes					
Inter-Integrated Communication (IIC)	yes					
Interrupt Request Pin (IRQ)	yes					
Keyboard Interrupt (KBI)	16					
Digital General purpose I/O[1]	69	65	48	47	48	47
Power and Ground Pins	8					
Time Of Day (TOD)	yes					
Serial Communications (SCI1)	yes					
Serial Communications (SCI2)	yes					
Serial Peripheral Interface (SPI1(FIFO))	yes					
Serial Peripheral Interface(SPI2)	yes					
Carrier Modulator Timer pin (IRO)	yes					
Programmable Delay Block (PDB)	yes					
TPM input clock pin (TPMCLK)	yes					
TPM1 channels	4					
TPM2 channels	4					
XOSC1	yes					
XOSC2	yes					
USBOTG	yes					
MiniFlex Bus	yes		DATA			
Rapid GPIO	16		9			
ADC single-ended channels	12					
DAC ouput pin (DACO)	yes					
Voltage reference output pin (VREFO)	yes					

[1] Port I/O count does not include $\overline{\text{BLMS}}$, BKGD and IRQ. $\overline{\text{BLMS}}$ BKGD are Output only, IRQ is input only.

The following table describes the functional units of the MCF51JE256/128.

Table 2. MCF51JE256/128 Functional Units

Unit	Function
DAC (digital to analog converter)	Used to output voltage levels.
12-BIT SAR ADC (analog-to-digital converter)	Measures analog voltages at up to 12 bits of resolution. The ADC has up to 12 single-ended inputs.
PDB (Programmable Delay Block)	Precisely trigger the DAC FIFO buffer.
Mini-FlexBus	Provides expansion capability for off-chip memory and peripherals.
USB On-the-Go	Supports the USB On-the-Go dual-role controller.
CMT (Carrier Modulator Timer)	Infrared output used for the Remote Controller operation.
MCG (Multipurpose Clock Generator)	Provides clocking options for the device, including a phase-locked loop (PLL) and frequency-locked loop (FLL) for multiplying slower reference clock sources.
BDM (Background Debug Module)	Provides single pin debugging interface (part of the V1 ColdFire core).
CF1 CORE (V1 ColdFire Core)	Executes programs and interrupt handlers.
PRACMP	Analog comparators for comparing external analog signals against each other, or a variety of reference levels.
COP (Computer Operating Properly)	Software Watchdog.
IRQ (Interrupt Request)	Single-pin high-priority interrupt (part of the V1 ColdFire core).
CRC (Cyclic Redundancy Check)	High-speed CRC calculation.
DBG (Debug)	Provides debugging and emulation capabilities (part of the V1 ColdFire core).
FLASH (Flash Memory)	Provides storage for program code, constants, and variables.
IIC (Inter-integrated Circuits)	Supports standard IIC communications protocol and SMBus.
INTC (Interrupt Controller)	Controls and prioritizes all device interrupts.
KBI1 & KBI2	Keyboard Interfaces 1 and 2.
LVD (Low-voltage Detect)	Provides an interrupt to the ColdFire V1 CORE in the event that the supply voltage drops below a critical value. The LVD can also be programmed to reset the device upon a low voltage event.
VREF (Voltage Reference)	The Voltage Reference output is available for both on- and off-chip use.
RAM (Random-Access Memory)	Provides stack and variable storage.
RGPIO (Rapid General-purpose Input/output)	Allows for I/O port access at CPU clock speeds. RGPIO is used to implement GPIO functionality.
SCI1, SCI2 (Serial Communications Interfaces)	Serial communications UARTs capable of supporting RS-232 and LIN protocols.
SIM (system integration unit)	

2.2 100-Pin LQFP

The following figure shows the 100-pin LQFP pinout configuration.

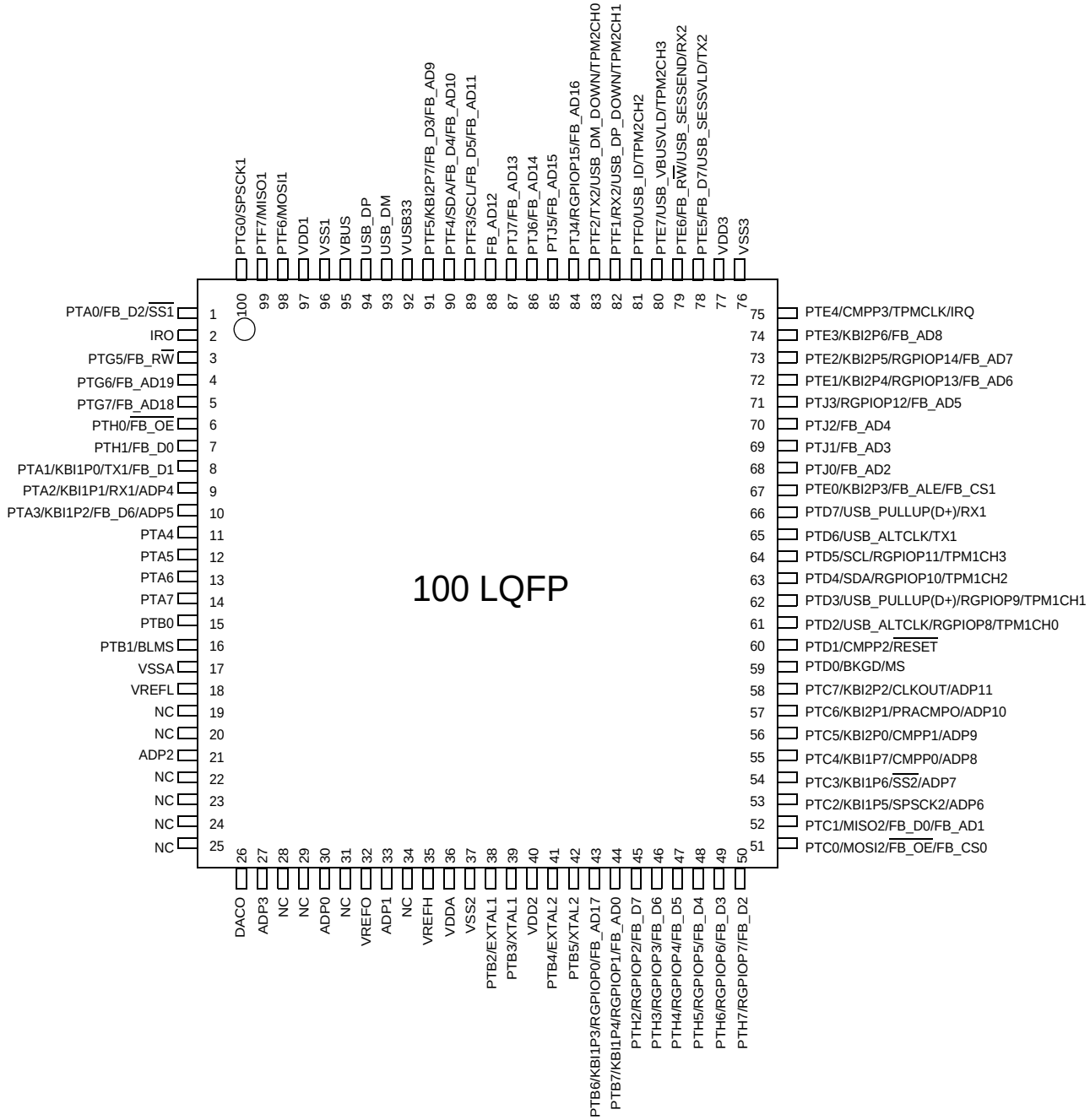


Figure 3. 100-Pin LQFP

2.3 81-Pin MAPBGA

The following figure shows the 81-pin MAPBGA pinout configuration.

	1	2	3	4	5	6	7	8	9	
A	IRO	PTG0	PTF6	USB_DP	VBUS	VUSB33	PTF4	PTF3	PTE4	A
B	PTF7	PTA0	PTG1	USB_DM	PTF5	PTE7	PTF1	PTF0	PTE3	B
C	PTA4	PTA5	PTA6	PTA1	PTF2	PTE6	PTE5	PTE2	PTE1	C
D		PTA7	PTB0	PTB1	PTA2	PTA3	PTD5	PTD7	PTE0	D
E				VDD2	VDD3	VDD1	PTD2	PTD3	PTD6	E
F		ADP2		VSS2	VSS3	VSS1	PTB7	PTC7	PTD4	F
G	ADP0	DACO	ADP3		VREFO	PTB6	PTC0	PTC1	PTC2	G
H			ADP1		PTC3	PTC4	PTD0	PTC5	PTC6	H
J	VSSA	VREFL	VREFH	VDDA	PTB2	PTB3	PTD1	PTB4	PTB5	J
	1	2	3	4	5	6	7	8	9	

Figure 4. 81-Pin MAPBGA

3 Preliminary Electrical Characteristics

This section contains electrical specification tables and reference timing diagrams for the MCF51JE256/128 microcontroller, including detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications.

The electrical specifications are preliminary and are from previous designs or design simulations. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle. These specifications will, however, be met for production silicon. Finalized specifications will be published after complete characterization and device qualifications have been completed.

NOTE

The parameters specified in this data sheet supersede any values found in the module specifications.

3.1 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 4. Parameter Classifications

P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

3.2 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in the following table may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

Table 5. Absolute Maximum Ratings

#	Rating	Symbol	Value	Unit
1	Supply voltage	V_{DD}	–0.3 to 3.8	V
2	Maximum current into V_{DD}	I_{DD}	120	mA
3	Digital Input voltage	V_{In}	–0.3 to V_{DD} + 0.3	V
4	Instantaneous maximum current Single pin limit (applies to all port pins)[1, 2, 3]	I_D	±25	mA
5	Storage temperature range	T_{stg}	–55 to 150	°C

1 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive (V_{DD}) and negative (V_{SS}) clamp voltages, then use the larger of the two resistance values.

2 All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.

3 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low (which would reduce overall power consumption).

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}).

3.3 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and it is user-determined rather than being controlled by the MCU design. In order to take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 6. Thermal Characteristics

#	Symbol	Rating		Value	Unit
1	T_A	Operating temperature range (packaged):			°C
			MCF51JE256	–40 to 105	
			MCF51JE128	–40 to 105	
2	T_{JMAX}	Maximum junction temperature		135	°C
3	θ_{JA}	Thermal resistance[1,2,3,4] Single-layer board — 1s			°C/W
			104-pin MBGA	67	
			100-pin LQFP	53	
			81-pin MBGA	67	
			80-pin LQFP	53	
4	θ_{JA}	Thermal resistance[1, 2, 3, 4] Four-layer board — 2s2p			°C/W
			104-pin MBGA	39	
			100-pin LQFP	41	
			81-pin MBGA	39	
			80-pin LQFP	39	

1 Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2 Junction to Ambient Natural Convection
3 1s — Single layer board, one signal layer
4 2s2p — Four layer board, 2 signal and 2 power layers

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad \textit{Eqn. 1}$$

where:

T_A = Ambient temperature, °C
θ_{JA} = Package thermal resistance, junction-to-ambient, °C/W
$P_D = P_{int} + P_{I/O}$
$P_{int} = I_{DD} \times V_{DD}$, Watts — chip internal power
$P_{I/O}$ = Power dissipation on input and output pins — user determined

For most applications, $P_{I/O} << P_{int}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad \textit{Eqn. 2}$$

Solving Equation 1 and Equation 2 for K gives:

$$K = P_D \times (T_A + 273°C) + \theta_{JA} \times (P_D)^2 \quad \textit{Eqn. 3}$$

Table 9. DC Characteristics

#	Symbol	Characteristic	Condition	Minimum	Typical[1]	Maximum	Unit	C
1	—	Operating Voltage	—	1.8[2]	—	3.6	V	—
2	V_{OH}	Output high voltage — All I/O pins, low-drive strength						
			$V_{DD} \geq 1.8$ V, $I_{Load} = -600$ μA	$V_{DD} - 0.5$	—	—	V	C
		All I/O pins, high-drive strength						
			$V_{DD} \geq 2.7$ V, $I_{Load} = -10$ mA	$V_{DD} - 0.5$	—	—	V	P
			$V_{DD} \geq 2.3$ V, $I_{Load} = -6$ mA	$V_{DD} - 0.5$	—	—	V	T
			$V_{DD} \geq 1.8$V, $I_{Load} = -3$ mA	$V_{DD} - 0.5$	—	—	V	C
3	I_{OHT}	Output high current — Max total I_{OH} for all ports						
			—	—	—	100	mA	D
4	V_{OL}	Output low voltage — All I/O pins, low-drive strength						
			$V_{DD} \geq 1.8$ V, $I_{Load} = 600$ μA	—	—	0.5	V	C
		All I/O pins, high-drive strength						
			$V_{DD} \geq 2.7$ V, $I_{Load} = 10$ mA	—	—	0.5	V	P
			$V_{DD} \geq 2.3$ V, $I_{Load} = 6$ mA	—	—	0.5	V	T
			$V_{DD} \geq 1.8$ V, $I_{Load} = 3$ mA	—	—	0.5	V	C
5	I_{OLT}	Output low current — Max total I_{OL} for all ports						
			—	—	—	100	mA	D
6	V_{IH}	Input high voltage all digital inputs						
			$V_{DD} > 2.7$ V	0.70 x V_{DD}	—	—	V	P
			$V_{DD} > 1.8$ V	0.85 x V_{DD}	—	—	V	C
7	V_{IL}	Input low voltage all digital inputs						
			$V_{DD} > 2.7$ V	—	—	0.35 x V_{DD}	V	P
			$V_{DD} > 1.8$ V	—	—	0.30 x V_{DD}	V	C
8	V_{hys}	Input hysteresis — all digital inputs	—	0.06 x V_{DD}	—	—	mV	C
9	$\|I_{In}\|$	Input leakage current — all input only pins (Per pin)	$V_{In} = V_{DD}$ or V_{SS}	—	—	0.5	μA	P
10	$\|I_{OZ}\|$	Hi-Z (off-state) leakage current[3] — all input/output (per pin)	$V_{In} = V_{DD}$ or V_{SS}	—	0.003	0.5	μA	P

Table 9. DC Characteristics (continued)

#	Symbol	Characteristic	Condition	Minimum	Typical[1]	Maximum	Unit	C
11	R_{PU}	Pull-up resistors all digital inputs, when enabled	—	17.5	—	52.5	kΩ	P
12	R_{PD}	Internal pull-down resistors[4]	—	17.5	—	52.5	kΩ	P
13	I_{IC}	DC injection current [5, 6, 7] — Single pin limit	$V_{SS} > V_{IN} > V_{DD}$	–0.2	—	0.2	mA	D
		DC injection current [5, 6, 7] — Total MCU limit, includes sum of all stressed pins	$V_{SS} > V_{IN} > V_{DD}$	–5	—	5	mA	D
14	C_{In}	Input Capacitance, all pins	—	—	—	8	pF	C
15	V_{RAM}	RAM retention voltage	—	—	0.6	1.0	V	C
16	V_{POR}	POR re-arm voltage[8]	—	0.9	1.4	1.79	V	C
17	t_{POR}	POR re-arm time	—	10	—	—	µs	D
18	V_{LVDH}	Low-voltage detection threshold — high range[9]						
			V_{DD} falling	2.11	2.16	2.22	V	P
			V_{DD} rising	2.16	2.21	2.27	V	P
19	V_{LVDL}	Low-voltage detection threshold — low range[9]						
			V_{DD} falling	1.80	1.82	1.91	V	P
			V_{DD} rising	1.86	1.90	1.99	V	P
20	V_{LVWH}	Low-voltage warning threshold — high range[9]						
			V_{DD} falling	2.36	2.46	2.56	V	P
			V_{DD} rising	2.36	2.46	2.56	V	P
21	V_{LVWL}	Low-voltage warning threshold — low range[9]						
			V_{DD} falling	2.11	2.16	2.22	V	P
			V_{DD} rising	2.16	2.21	2.27	V	P
22	V_{hys}	Low-voltage inhibit reset/recover hysteresis[10]	—	—	50	—	mV	C
23	V_{BG}	Bandgap Voltage Reference[11]	—	1.145	1.17	1.195	V	P

1 Typical values are measured at 25°C. Characterized, not tested

2 As the supply voltage rises, the LVD circuit will hold the MCU in reset until the supply has risen above V_{LVDL}.

3 Does not include analog module pins. Dedicated analog pins should not be pulled to VDD or VSS and should be left floating when not used to reduce current leakage.

4 Measured with $V_{In} = V_{DD}$.

5 All functional non-supply pins are internally clamped to V_{SS} and V_{DD},except PTD1.

6 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

7 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).

[8] Maximum is highest voltage that POR is guaranteed.
[9] Run at 1 MHz bus frequency.
[10] Low voltage detection and warning limits measured at 1 MHz bus frequency.
[11] Factory trimmed at V_{DD} = 3.0 V, Temp = 25°C.

3.6 Supply Current Characteristics

Table 10. Supply Current Characteristics

#	Symbol	Parameter	Bus Freq	V_{DD} (V)	Typical[1]	Maximum	Unit	Temperature (°C)	C
1	RI_{DD}	Run supply current FEI mode, all modules ON[2]							
			25.165 MHz	3	44	48	mA	–40 to 25	P
			25.165 MHz	3	44	48	mA	105	P
			20 MHz	3	32.3	—	mA	–40 to 105	T
			8 MHz	3	16.4	—	mA	–40 to 105	T
			1 MHz	3	2.9	—	mA	–40 to 105	T
2	RI_{DD}	Run supply current FEI mode, all modules OFF[3]							
			25.165 MHz	3	29	29.6	mA	–40 to 105	C
			20 MHz	3	25.4	—	mA	–40 to 105	T
			8 MHz	3	12.7	—	mA	–40 to 105	T
			1 MHz	3	2.4	—	mA	–40 to 105	T
3	RI_{DD}	Run supply current LPR=0, all modules OFF[3]							
			16 kHz FBI	3	232	280	μA	–40 to 105	T
			16 kHz FBE	3	231	296	μA	–40 to 105	T
4	RI_{DD}	Run supply current LPR=1, all modules OFF[3]							
			16 kHz BLPE	3	74	75	μA	0 to 70	T
			16 kHz BLPE	3	74	120	μA	–40 to 105	T
5	WI_{DD}	Wait mode supply current FEI mode, all modules OFF[3]							
			25.165 MHz	3	16.5	—	mA	–-40 to 105	C
			20 MHz	3	10.3	—	mA	–-40 to 105	T
			8 MHz	3	6.6	—	mA	–-40 to 105	T
			1 MHz	3	1.7	—	mA	–-40 to 105	T

Table 11. Stop Mode Adders (continued)

#	Parameter	Condition	Temperature (°C)					Units	C
			-40	25	70	85	105		
5	LVD[1]	LVDSE = 1	116	117	126	132	172	µA	T
6	PRACMP[1]	Not using the bandgap (BGBE = 0)	17	18	24	35	74	µA	T
7	ADC[1]	ADLPC = ADLSMP = 1 Not using the bandgap (BGBE = 0)	75	85	100	115	165	µA	T
8	DAC[1]	High power mode; no load on DACO	500	500	500	500	500	µA	T

1 Not available in stop2 mode.

Figure 6. Stop IDD versus Temperature

Table 14. DAC 12-Bit Operating Behaviors

#	Characteristic	Symbol	Minimum	Typical	Maximum	Unit	C	Notes
1	Resolution	N	12	—	12	bit	T	
2	Supply current low-power mode	I_{DDA_DACLP}	—	50	100	μA	T	
3	Supply current high-power mode	I_{DDA_DACHP}	—	345	500	μA	T	
4	Full-scale Settling time (±1 LSB) (0x080 to 0xF7F or 0xF7F to 0x080) low-power mode	$Ts_{FS}LP$	—	—	200	μs	T	• V_{DDA} = 3 V or 2.2 V • V_{REFSEL} = 1 • Temperature = 25°C
5	Full-scale Settling time (±1 LSB) (0x080 to 0xF7F or 0xF7F to 0x080) high-power mode	$Ts_{FS}HP$	—	—	30	μs	T	• V_{DDA} = 3 V or 2.2 V • V_{REFSEL} = 1 • Temperature = 25°C
6	Code-to-code Settling time (±1 LSB) (0xBF8 to 0xC08 or 0xC08 to 0xBF8) low-power mode	$Ts_{C-C}LP$	—	—	5	μs	T	• V_{DDA} = 3 V or 2.2 V • V_{REFSEL} = 1 • Temperature = 25°C
7	Code-to-code Settling time (±1 LSB) (0xBF8 to 0xC08 or 0xC08 to 0xBF8) high-power mode	$Ts_{C-C}HP$	—	1	—	μs	T	• V_{DDA} = 3 V or 2.2 V • V_{REFSEL} = 1 • Temperature = 25°C
8	DAC output voltage range low (high-power mode, no load, DAC set to 0, 3 V at room temperature)	$V_{dacoutl}$	—	—	100	mV	T	
9	DAC output voltage range high (high-power mode, no load, DAC set to 0x0FFF)	$V_{dacouth}$	V_{DACR}–100	—	—	mV	T	
10	Integral non-linearity error	INL	—	—	±8	LSB	T	
11	Differential non-linearity error V_{DACR} is > 2.4 V	DNL	—	—	±1	LSB	T	
12	Offset error	E_O	—	±0.4	±3	%FSR	T	Calculated by a best fit curve from VSS + 100mV to V_{REFH} –100mV
13	Gain error (V_{REF} = V_{ext} = V_{DD})	E_G	—	±0.1	±0.5	%FSR	T	Calculated by a best fit curve from VSS + 100mV to V_{REFH} –100mV
14	Power supply rejection ratio $V_{DD} \geq 2.4$ V	PSRR	60	—	—	dB	T	

3.13 SPI Characteristics

The following table and Figure 15 through Figure 18 describe the timing requirements for the SPI system.

Table 22. SPI Timing

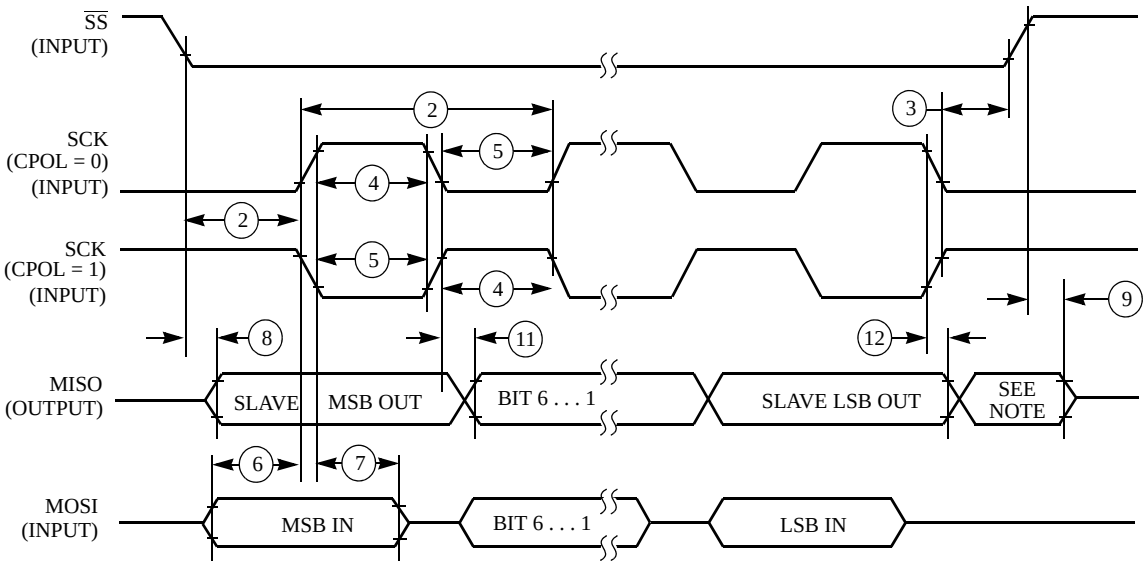
No.[1]	Characteristic[2]	Symbol	Minimum	Maximum	Unit	C
1	Operating frequency Master Slave	 f_{op} f_{op}	 $f_{Bus}/2048$ 0	 $f_{Bus}/2$ $f_{Bus}/4$	 Hz Hz	D
2	SPSCK period Master Slave	 t_{SPSCK} t_{SPSCK}	 2 4	 2048 —	 t_{cyc} t_{cyc}	D
3	Enable lead time Master Slave	 t_{Lead} t_{Lead}	 1/2 1	 — —	 t_{SPSCK} t_{cyc}	D
4	Enable lag time Master Slave	 t_{Lag} t_{Lag}	 1/2 1	 — —	 t_{SPSCK} t_{cyc}	D
5	Clock (SPSCK) high or low time Master Slave	 t_{WSPSCK} t_{WSPSCK}	 $t_{cyc} - 30$ $t_{cyc} - 30$	 1024 t_{cyc} —	 ns ns	D
6	Data setup time (inputs) Master Slave	 t_{SU} t_{SU}	 15 15	 — —	 ns ns	D
7	Data hold time (inputs) Master Slave	 t_{HI} t_{HI}	 0 25	 — —	 ns ns	D
8	Slave access time[3]	t_a	—	1	t_{cyc}	D
9	Slave MISO disable time[4]	t_{dis}	—	1	t_{cyc}	D
10	Data valid (after SPSCK edge) Master Slave	 t_v t_v	 — —	 25 25	 ns ns	D
11	Data hold time (outputs) Master Slave	 t_{HO} t_{HO}	 0 0	 — —	 ns ns	D
12	Rise time Input Output	 t_{RI} t_{RO}	 — —	 $t_{cyc} - 25$ 25	 ns ns	D
13	Fall time Input Output	 t_{FI} t_{FO}	 — —	 $t_{cyc} - 25$ 25	 ns ns	D

1 Numbers in this column identify elements in Figure 15 through Figure 18**.**

2 All timing is shown with respect to 20% V_{DD} and 70% V_{DD}, unless noted; 100 pF load on all SPI pins. All timing assumes slew rate control disabled and high drive strength enabled for SPI output pins.

3 Time to data active from high-impedance state.

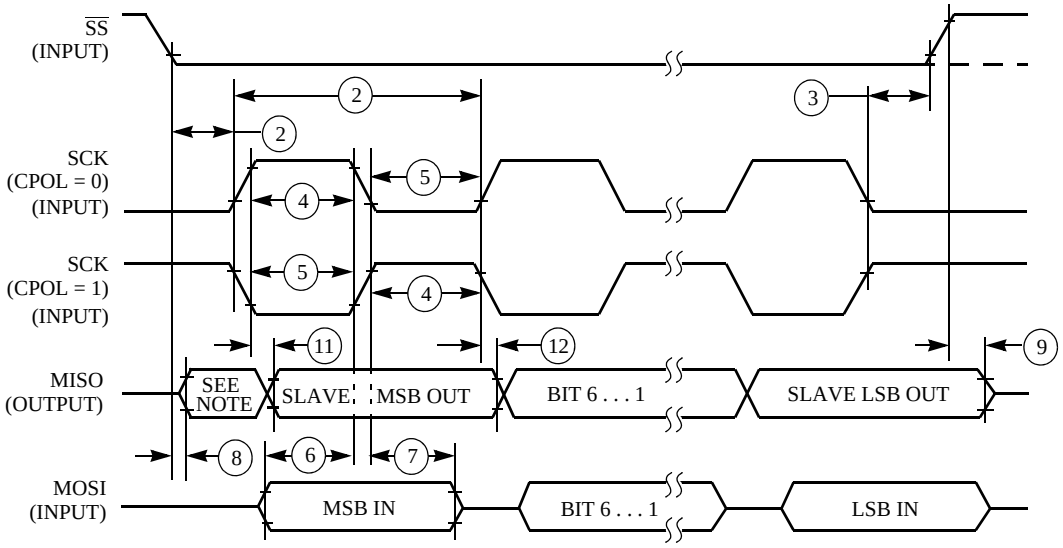
4 Hold time to high-impedance state.



NOTE:

1. Not defined, but normally MSB of character just received

Figure 17. SPI Slave Timing (CPHA = 0)



NOTE:

1. Not defined, but normally LSB of character just received

Figure 18. SPI Slave Timing (CPHA = 1)

3.14 Flash Specifications

This section provides details about program/erase times and program-erase endurance for the Flash memory.

Program and erase operations do not require any special power sources other than the normal V_{DD} supply. For more detailed information about program/erase operations, see the Memory chapter in the Reference Manual for this device (MCF51JE256RM).

Table 23. Flash Characteristics

#	Characteristic	Symbol	Minimum	Typical	Maximum	Unit	C
1	Supply voltage for program/erase -40°C to 105°C	$V_{prog/erase}$	1.8	—	3.6	V	D
2	Supply voltage for read operation	V_{Read}	1.8	—	3.6	V	D
3	Internal FCLK frequency[1]	f_{FCLK}	150	—	200	kHz	D
4	Internal FCLK period (1/FCLK)	t_{Fcyc}	5	—	6.67	µs	D
5	Byte program time (random location)[2]	t_{prog}	9			t_{Fcyc}	P
6	Byte program time (burst mode)[2]	t_{Burst}	4			t_{Fcyc}	P
7	Page erase time[2]	t_{Page}	4000			t_{Fcyc}	P
8	Mass erase time[2]	t_{Mass}	20,000			t_{Fcyc}	P
9	Program/erase endurance[3] T_L to T_H = –40°C to + 105°C T = 25°C		10,000 —	— 100,000	— —	cycles	C
10	Data retention[4]	t_{D_ret}	15	100	—	years	C

1 The frequency of this clock is controlled by a software setting.

2 These values are hardware state machine controlled. User code does not need to count cycles. This information supplied for calculating approximate time to program and erase.

3 **Typical endurance for flash** was evaluated for this product family on the HC9S12Dx64. For additional information on how Freescale defines typical endurance, please refer to Engineering Bulletin EB619, *Typical Endurance for Nonvolatile Memory.*

4 **Typical data retention** values are based on intrinsic capability of the technology measured at high temperature and de-rated to 25°C using the Arrhenius equation. For additional information on how Freescale defines typical data retention, please refer to Engineering Bulletin EB618, *Typical Data Retention for Nonvolatile Memory.*

3.15 USB Electricals

The USB electricals for the USB On-the-Go module conform to the standards documented by the Universal Serial Bus Implementers Forum. For the most up-to-date standards, visit http://www.usb.org.

If the Freescale USB On-the-Go implementation has electrical characteristics that deviate from the standard or require additional information, this space would be used to communicate that information.

Table 24. Internal USB 3.3 V Voltage Regulator Characteristics

#	Characteristic	Symbol	Minimum	Typical	Maximum	Unit	C
1	Regulator operating voltage	V_{regin}	3.9	—	5.5	V	C
2	VREG output	V_{regout}	3	3.3	3.75	V	P

Table 24. Internal USB 3.3 V Voltage Regulator Characteristics (continued)

#	Characteristic	Symbol	Minimum	Typical	Maximum	Unit	C
3	V_{USB33} input with internal VREG disabled	$V_{usb33in}$	3	3.3	3.6	V	C
4	VREG Quiescent Current	I_{VRQ}	—	0.5	—	mA	C

3.16 VREF Electrical Specifications

Table 25. VREF Electrical Specifications

#	Characteristic	Symbol	Minimum	Maximum	Unit	C
1	Supply voltage	V_{DDA}	1.80	3.6	V	C
2	Temperature	T_A	–40	105	°C	C
3	Output Load Capacitance	C_L	—	100	nf	D
4	Maximum Load	—	—	10	mA	—
5	Voltage Reference Output with Factory Trim. V_{DD} = 3 V.	Vout	1.148	1.152	V	P
6	Temperature Drift (Vmin - Vmax across the full temperature range)	Tdrift	—	25	mV[1]	T
7	Aging Coefficient[2]	Ac	—	60	μV/year	C
8	Powered down Current (Off Mode, VREFEN = 0, VRSTEN = 0)	I	—	0.10	μA	C
9	Bandgap only (MODE_LV[1:0] = 00)	I	—	75	μA	T
10	Low-Power buffer (MODE_LV[1:0] = 01)	I	—	125	μA	T
11	Tight-Regulation buffer (MODE_LV[1:0] = 10)	I	—	1.1	mA	T
12	Load Regulation (MODE_LV = 10)	—	—	100	μV/mA	C
13	Line Regulation MODE = 1:0, Tight Regulation VDD < 2.3 V, Delta VDDA = 100 mV, VREFH = 1.2 V driven externally with VREFO disabled. (Power Supply Rejection	DC	70	—	dB	C

1 See typical chart below.

2 Linear reliability model (1008 hours stress at 125°C = 10 years operating life) used to calculate Aging μV/year. Vrefo data recorded per month.

4 Ordering Information

This section contains ordering information for the device numbering system. See Table 1 for feature summary by package information.

4.1 Part Numbers

Table 27. Orderable Part Number Summary

Freescale Part Number	Description	Flash / SRAM (Kbytes)	Package	Temperature
MCF51JE256VML	MCF51JE256 ColdFire Microcontroller	256K/32K	104 MAPBGA	–40 to 105 °C
MCF51JE256VLL	MCF51JE256 ColdFire Microcontroller	256K/32K	100 LQFP	–40 to 105 °C
MCF51JE256VMB	MCF51JE256 ColdFire Microcontroller	256K/32K	81 MAPBGA	–40 to 105 °C
MCF51JE256VLK	MCF51JE256 ColdFire Microcontroller	256K/32K	80 LQFP	–40 to 105 °C
MCF51JE128VMB	MCF51JE128 ColdFire Microcontroller	128K/32K	81 MAPBGA	–40 to 105 °C
MCF51JE256CML	MCF51JE256 ColdFire Microcontroller	256K/32K	104 MAPBGA	–40 to 85 °C
MCF51JE256CLL	MCF51JE256 ColdFire Microcontroller	256K/32K	10O LQFP	–40 to 85 °C
MCF51JE256CMB	MCF51JE256 ColdFire Microcontroller	256K/32K	81 MAPBGA	–40 to 85 °C
MCF51JE256CLK	MCF51JE256 ColdFire Microcontroller	256K/32K	80 LQFP	–40 to 85 °C
MCF51JE128CMB	MCF51JE128 ColdFire Microcontroller	128K/32K	81 MAPBGA	–40 to 85 °C
MCF51JE128CLK	MCF51JE128 ColdFire Microcontroller	128K/32K	80 LQFP	–40 to 85 °C

4.2 Package Information

Table 28. Package Descriptions

Pin Count	Package Type	Abbreviation	Designator	Case No.	Document No.
100	Low Quad Flat Package	LQFP	LL	983-03	98ASS23308W
80	Low Quad Flat Package	LQFP	LK	1418	98ASS23174W
104	MAP BGA Package	MAPBGA	ML	1285-02	98ARH98267A
81	MAP BGA Package	MAPBGA	MB	1662-01	98ASA10670D

4.3 Mechanical Drawings

Table 28 provides the available package types and their document numbers. The latest package outline/mechanical drawings are available on the MCF51JE256/128 Product Summary pages at http://www.freescale.com.

To view the latest drawing, either:

- Click on the appropriate link in Table 28, or

- Open a browser to the Freescale® website (http://www.freescale.com), and enter the appropriate document number (from Table 28) in the “Enter Keyword” search box at the top of the page.

5 Revision History

This section lists major changes between versions of the MCF51JE256 Data Sheet.

Table 29. Revision History

Revision	Date	Description
0	March/April 09	Initial Draft
1	July 2009	• Revised to follow standard template. • Removed extraneous headings from the TOC. • Corrected units for Monotoncity to be blank in for the DAC specification. • Updated ADC characteristic tables to include 16-Bit SAR in headings.
2	July 2009	• Changed MCG (XOSC) Electricals Table - Row 2, Average Internal Reference Frequency typical value from 32.768 to 31.25
3	April 2010	• Updated Thermal Characteristics table. Reinserted the 81 and 104 MapBGA devices. • Revised the ESD and Latch-Up Protection Characeristic description to read: Latch-up Current at T_A = 125°C. • Changed Table 9. DC Characteristics rows 2 and 4, to 1.8 V, ILoad = -600 mA conditions to 1.8 V, ILoad = 600μA respectively. • Corrected the 16-bit SAR ADC Operating Condition table Ref Voltage High Min value to be 1.13 instead of 1.15. • Updated the ADC electricals. • Inserted the Mini-FlexBus Timing Specifications. • Added a Temp Drift parameter to the VREF Electrical Specifications. • Removed the S08 Naming Convention diagram. • Updated the Orderable Part Number Summary to include the Freescale Part Number suffixes. • Completed the Package Description table values. • Changed the 80LQFP package drawing from 98ARL10530D to 98ASS23174W. • Updated electrical characteristic data.

Table 29. Revision History

Revision	Date	Description
4	August 2012	• In Table 1."MCF51JE256/128 Features by MCU and Package, removed the row of "12-bit SAR ADCDifferential Channels". • In Table 3, "Package Pin Assignments", changed from: 'A1' — PTG1 USB_ SESSEND to:'B3' — PTG1 USB_ SESSEND. • In Table 10,"Supply Current Characteristics", for $S3I_{DD}$ changed the max value from '1.2' to '1.3' and typical value from '0.650' to '0.750' for the first row. • In Table 10,"Supply Current Characteristics": — For parameter 3 and parameter 4 changed LPS to LPR. — For parameter 3,changed "FBILP" to "FBI". — For parameter 4, changed "FBELP" to "BLPE". • Fixed the TBD parameters and added figure"Typical Output vs VDD", following the same setup of MM256DS — Added Figure 7,"Offset at Half Scale vs Temperature". — Updated Table 9,"DC Characteristics**".** — Updated Table 10,"Supply Current Characteristics**".** — Updated Table 11,"Stop Mode Adders". — Added Figure 20,"Typical Output vs. V_{DD}. — Updated Table 14,"DAC 12-Bit Operating Behaviors". — Updated Table 20,"Control Timing". — Removed "SPI Electrical Characteristics" table. — Updated Table 25"VREF Electrical Specifications**".** — Updated Table 26,"VREF Limited Range Operating Behaviors**".** • Updated Figure 3, Figure 4, and Figure 5.

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