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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	Coldfire V1
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	EBI/EMI, I²C, SCI, SPI, USB OTG
Peripherals	LVD, PWM, WDT
Number of I/O	65
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 12x12b; D/A 1x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcf51je256cll

1 Features

The following table provides a cross-comparison of the features of the MCF51JE256/128 according to package.

Table 1. MCF51JE Features by MCU and Package

Feature	MCF51JE256				MCF51JE128	
FLASH size (bytes)	262144				131072	
RAM size (bytes)	32K				32K	
Pin quantity	104	100	81	80	81	80
Programmable Analog Comparator (PRACMP)	yes					
Debug Module (DBG)	yes					
Multipurpose Clock Generator (MCG)	yes					
Inter-Integrated Communication (IIC)	yes					
Interrupt Request Pin (IRQ)	yes					
Keyboard Interrupt (KBI)	16					
Digital General purpose I/O[1]	69	65	48	47	48	47
Power and Ground Pins	8					
Time Of Day (TOD)	yes					
Serial Communications (SCI1)	yes					
Serial Communications (SCI2)	yes					
Serial Peripheral Interface (SPI1(FIFO))	yes					
Serial Peripheral Interface(SPI2)	yes					
Carrier Modulator Timer pin (IRO)	yes					
Programmable Delay Block (PDB)	yes					
TPM input clock pin (TPMCLK)	yes					
TPM1 channels	4					
TPM2 channels	4					
XOSC1	yes					
XOSC2	yes					
USBOTG	yes					
MiniFlex Bus	yes		DATA			
Rapid GPIO	16		9			
ADC single-ended channels	12					
DAC ouput pin (DACO)	yes					
Voltage reference output pin (VREFO)	yes					

[1] Port I/O count does not include $\overline{\text{BLMS}}$, BKGD and IRQ. $\overline{\text{BLMS}}$ BKGD are Output only, IRQ is input only.

The following table describes the functional units of the MCF51JE256/128.

Table 2. MCF51JE256/128 Functional Units (continued)

Unit	Function
SPI1 (FIFO), SPI2 (Serial Peripheral Interfaces)	SPI1 and SPI2 provide standard master/slave capability. SPI contains a FIFO buffer in order to increase the throughput for this peripheral.
TPM1, TPM2 (Timer/PWM Module)	Timer/PWM module can be used for a variety of generic timer operations as well as pulse-width modulation.
VREG (Voltage Regulator)	Controls power management across the device.
XOSC1 and XOSC2 (Crystal Oscillators)	These devices incorporate redundant crystal oscillators. One is intended primarily for use by the TOD, and the other by the CPU and other peripherals.

2 Pinouts and Pin Assignments

2.1 104-Pin MAPBGA

The following figure shows the 104-pin MAPBGA pinout configuration.

	1	2	3	4	5	6	7	8	9	10	11	
A	PTF6	PTF7	USB_DP	USB_DM	VUSB33	PTF4	PTF3	FB_AD12	PTJ7	PTJ5	PTJ4	A
B	PTG0	PTA0	PTG3	VBUS	PTF5	PTJ6	PTH0	PTE5	PTF0	PTF1	PTF2	B
C	IRO	PTG4	PTA6	PTG2	PTG6	PTG5	PTG7	PTH1	PTE4	PTE6	PTE7	C
D	PTA5	PTA4	PTB1	VDD1		VDD2		VDD3	PTA1	PTE3	PTE2	D
E	VSSA	PTA7	PTB0						PTA2	PTJ3	PTE1	E
F	VREFL			PTG1				PTC7	PTJ2	PTJ0	PTJ1	F
G	ADP2								PTD5	PTD7	PTE0	G
H			PTA3	VSS1		VSS2		VSS3	PTD4	PTD3	PTD2	H
J	ADP0		PTH7	PTH6	PTH4	PTH3	PTH2	PTD6	PTC2	PTC0	PTC1	J
K			ADP1	PTH5	PTB6	PTB7	PTC3	PTD1	PTC4	PTC5	PTC6	K
L	ADP3	DACO		VREFO	VREFH	VDDA	PTB3	PTB2	PTD0	PTB5	PTB4	L
	1	2	3	4	5	6	7	8	9	10	11	

Figure 2. 104-Pin MAPBGA

2.2 100-Pin LQFP

The following figure shows the 100-pin LQFP pinout configuration.

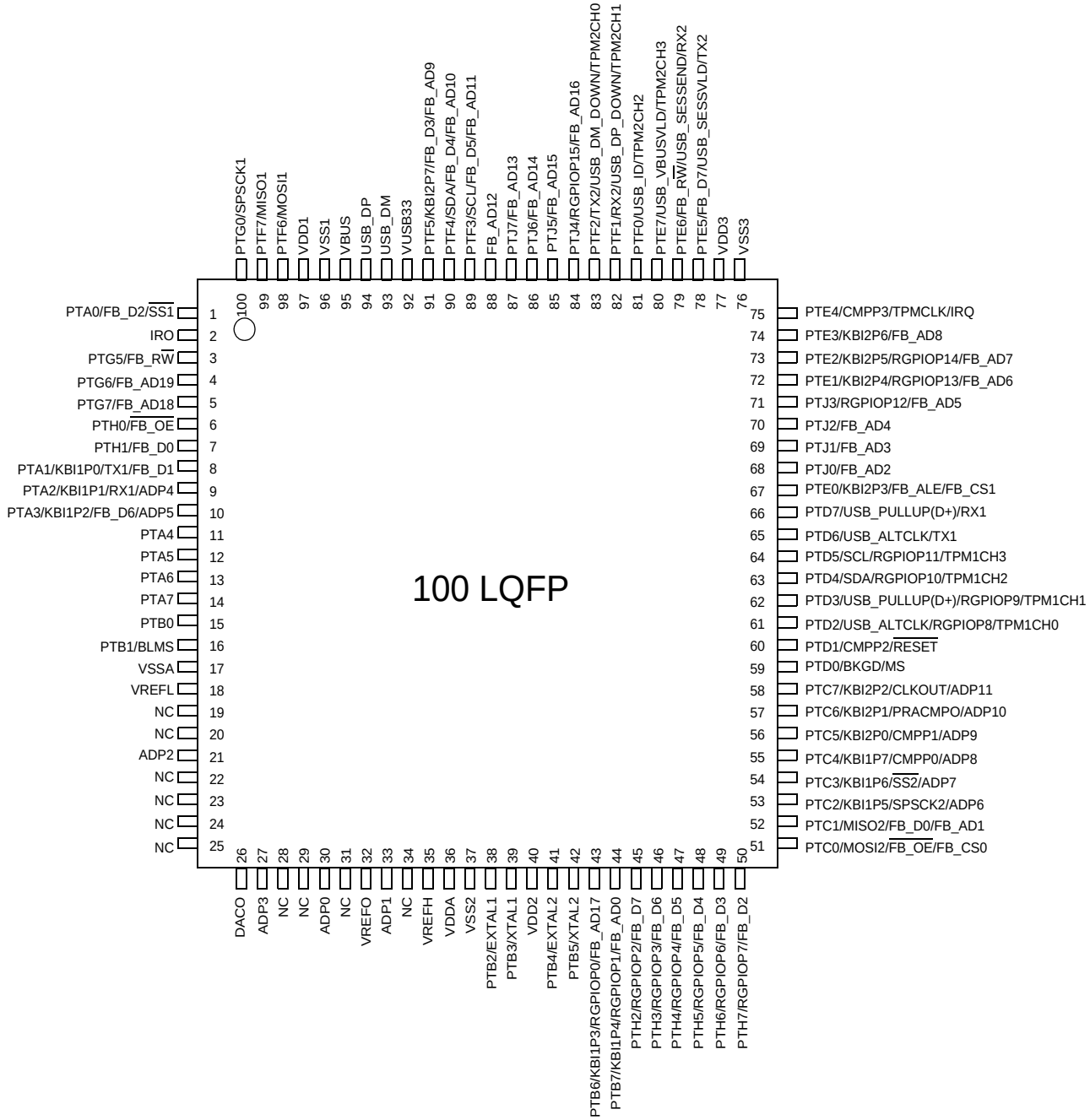

Figure 3. 100-Pin LQFP

2.5 Pin Assignments

Table 3. Package Pin Assignments

Package				Default Function	Alternate 1	Alternate 2	Alternate 3	Composite Pin Name
104 MAPBGA	100 LQFP	81 MAPBGA	80 LQFP					
B2	1	B2	1	PTA0	FB_D2	$\overline{SS1}$	—	PTA0/FB_D2/$\overline{SS1}$
C1	2	A1	2	IRO	—	—	—	IRO
C6	3	—	—	PTG5	FB_$\overline{RW}$	—	—	PTG5/FB_$\overline{RW}$
C5	4	—	—	PTG6	FB_AD19	—	—	PTG6/FB_AD19
C7	5	—	—	PTG7	FB_AD18	—	—	PTG7/FB_AD18
B7	6	—	—	PTH0	$\overline{FB\_OE}$	—	—	PTH0/$\overline{FB\_OE}$
C8	7	—	—	PTH1	FB_D0	—	—	PTH1/FB_D0
D9	8	C4	3	PTA1	KBI1P0	TX1	FB_D1	PTA1/KBI1P0/TX1/FB_D1
E9	9	D5	4	PTA2	KBI1P1	RX1	ADP4	PTA2/KBI1P1/RX1/ADP4
H3	10	D6	5	PTA3	KBI1P2	FB_D6	ADP5	PTA3/KBI1P2/FB_D6/ADP5
D2	11	C1	6	PTA4	—	—	—	PTA4
D1	12	C2	7	PTA5	—	—	—	PTA5
C3	13	C3	8	PTA6	—	—	—	PTA6
E2	14	D2	9	PTA7	—	—	—	PTA7
E3	15	D3	10	PTB0	—	—	—	PTB0
D3	16	D4	11	PTB1	$\overline{BLMS}$	—	—	PTB1/$\overline{BLMS}$
E1	17	J1	12	VSSA	—	—	—	VSSA
F1	18	J2	13	VREFL	—	—	—	VREFL
F2	19	D1	19	—	—	—	—	NC
G2	20	E2	15	—	—	—	—	NC
G1	21	F2	16	ADP2	—	—	—	ADP2
H1	22	F1	17	—	—	—	—	NC
H2	23	E2	18	NC	—	—	—	NC
F3	24	F3	19	—	—	—	—	NC
G3	25	E3	20	—	—	—	—	NC
L2	26	G2	21	DACO	—	—	—	DACO
L1	27	G3	22	ADP3	—	—	—	ADP3
K1	28	H4	23	—	—	—	—	NC
K2	29	G4	24	NC	—	—	—	NC
J1	30	G1	25	ADP0	—	—	—	ADP0
J2	31	H1	26	—	—	—	—	NC
L4	32	G5	27	VREFO	—	—	—	VREFO
K3	33	H3	28	ADP1	—	—	—	ADP1
L3	34	H2	29	NC	—	—	—	NC

Table 3. Package Pin Assignments (continued)

Package				Default Function	Alternate 1	Alternate 2	Alternate 3	Composite Pin Name
104 MAPBGA	100 LQFP	81 MAPBGA	80 LQFP					
H4	96	F6	76	VSS1	—	—	—	VSS1
D4	97	E6	77	VDD1	—	—	—	VDD1
A1	98	A3	78	PTF6	MOSI1	—	—	PTF6/MOSI1
A2	99	B1	79	PTF7	MISO1	—	—	PTF7/MISO1
B1	100	A2	80	PTG0	SPSCK1	—	—	PTG0/SPSCK1
F4	—	B3	—	PTG1	USB_SESSEND	—	—	PTG1/USB_SESSEND
C4	—	—	—	PTG2	USB_DM_DOWN	—	—	PTG2/USB_DM_DOWN
B3	—	—	—	PTG3	USB_DP_DOWN	—	—	PTG3/USB_DP_DOWN
C2	—	—	—	PTG4	USB_SESSVLD	—	—	PTG4/USB_SESSVLD

3 Preliminary Electrical Characteristics

This section contains electrical specification tables and reference timing diagrams for the MCF51JE256/128 microcontroller, including detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications.

The electrical specifications are preliminary and are from previous designs or design simulations. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle. These specifications will, however, be met for production silicon. Finalized specifications will be published after complete characterization and device qualifications have been completed.

NOTE

The parameters specified in this data sheet supersede any values found in the module specifications.

3.1 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 4. Parameter Classifications

P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

3.2 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in the following table may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

Table 9. DC Characteristics

#	Symbol	Characteristic	Condition	Minimum	Typical[1]	Maximum	Unit	C
1	—	Operating Voltage	—	1.8[2]	—	3.6	V	—
2	V_{OH}	Output high voltage — All I/O pins, low-drive strength						
			$V_{DD} \geq 1.8$ V, $I_{Load} = -600$ μA	$V_{DD} - 0.5$	—	—	V	C
		All I/O pins, high-drive strength						
			$V_{DD} \geq 2.7$ V, $I_{Load} = -10$ mA	$V_{DD} - 0.5$	—	—	V	P
			$V_{DD} \geq 2.3$ V, $I_{Load} = -6$ mA	$V_{DD} - 0.5$	—	—	V	T
			$V_{DD} \geq 1.8$V, $I_{Load} = -3$ mA	$V_{DD} - 0.5$	—	—	V	C
3	I_{OHT}	Output high current — Max total I_{OH} for all ports						
			—	—	—	100	mA	D
4	V_{OL}	Output low voltage — All I/O pins, low-drive strength						
			$V_{DD} \geq 1.8$ V, $I_{Load} = 600$ μA	—	—	0.5	V	C
		All I/O pins, high-drive strength						
			$V_{DD} \geq 2.7$ V, $I_{Load} = 10$ mA	—	—	0.5	V	P
			$V_{DD} \geq 2.3$ V, $I_{Load} = 6$ mA	—	—	0.5	V	T
			$V_{DD} \geq 1.8$ V, $I_{Load} = 3$ mA	—	—	0.5	V	C
5	I_{OLT}	Output low current — Max total I_{OL} for all ports						
			—	—	—	100	mA	D
6	V_{IH}	Input high voltage all digital inputs						
			$V_{DD} > 2.7$ V	0.70 x V_{DD}	—	—	V	P
			$V_{DD} > 1.8$ V	0.85 x V_{DD}	—	—	V	C
7	V_{IL}	Input low voltage all digital inputs						
			$V_{DD} > 2.7$ V	—	—	0.35 x V_{DD}	V	P
			$V_{DD} > 1.8$ V	—	—	0.30 x V_{DD}	V	C
8	V_{hys}	Input hysteresis — all digital inputs	—	0.06 x V_{DD}	—	—	mV	C
9	$\|I_{In}\|$	Input leakage current — all input only pins (Per pin)	$V_{In} = V_{DD}$ or V_{SS}	—	—	0.5	μA	P
10	$\|I_{OZ}\|$	Hi-Z (off-state) leakage current[3] — all input/output (per pin)	$V_{In} = V_{DD}$ or V_{SS}	—	0.003	0.5	μA	P

Table 14. DAC 12-Bit Operating Behaviors

#	Characteristic	Symbol	Minimum	Typical	Maximum	Unit	C	Notes
1	Resolution	N	12	—	12	bit	T	
2	Supply current low-power mode	I_{DDA_DACLP}	—	50	100	μA	T	
3	Supply current high-power mode	I_{DDA_DACHP}	—	345	500	μA	T	
4	Full-scale Settling time (±1 LSB) (0x080 to 0xF7F or 0xF7F to 0x080) low-power mode	$Ts_{FS}LP$	—	—	200	μs	T	• V_{DDA} = 3 V or 2.2 V • V_{REFSEL} = 1 • Temperature = 25°C
5	Full-scale Settling time (±1 LSB) (0x080 to 0xF7F or 0xF7F to 0x080) high-power mode	$Ts_{FS}HP$	—	—	30	μs	T	• V_{DDA} = 3 V or 2.2 V • V_{REFSEL} = 1 • Temperature = 25°C
6	Code-to-code Settling time (±1 LSB) (0xBF8 to 0xC08 or 0xC08 to 0xBF8) low-power mode	$Ts_{C-C}LP$	—	—	5	μs	T	• V_{DDA} = 3 V or 2.2 V • V_{REFSEL} = 1 • Temperature = 25°C
7	Code-to-code Settling time (±1 LSB) (0xBF8 to 0xC08 or 0xC08 to 0xBF8) high-power mode	$Ts_{C-C}HP$	—	1	—	μs	T	• V_{DDA} = 3 V or 2.2 V • V_{REFSEL} = 1 • Temperature = 25°C
8	DAC output voltage range low (high-power mode, no load, DAC set to 0, 3 V at room temperature)	$V_{dacoutl}$	—	—	100	mV	T	
9	DAC output voltage range high (high-power mode, no load, DAC set to 0x0FFF)	$V_{dacouth}$	V_{DACR}–100	—	—	mV	T	
10	Integral non-linearity error	INL	—	—	±8	LSB	T	
11	Differential non-linearity error V_{DACR} is > 2.4 V	DNL	—	—	±1	LSB	T	
12	Offset error	E_O	—	±0.4	±3	%FSR	T	Calculated by a best fit curve from VSS + 100mV to V_{REFH} –100mV
13	Gain error (V_{REF} = V_{ext} = V_{DD})	E_G	—	±0.1	±0.5	%FSR	T	Calculated by a best fit curve from VSS + 100mV to V_{REFH} –100mV
14	Power supply rejection ratio $V_{DD} \geq 2.4$ V	PSRR	60	—	—	dB	T	

Table 14. DAC 12-Bit Operating Behaviors

#	Characteristic	Symbol	Minimum	Typical	Maximum	Unit	C	Notes
15	Temperature drift of offset voltage (DAC set to 0x0800)[1]	T_{co}	—	—	2	mV	T	See Typical Drift figure that follows.
16	Offset aging coefficient	A_C	—	—	8	μV/yr	T	

1 See Typical Drift figure that follows.

Figure 7. Offset at Half Scale vs Temperature

3.9 ADC Characteristics

Table 15. 12-bit ADC Operating Conditions

#	Symb	Characteristic	Conditions	Minimum	Typical[1]	Maximum	Unit	C
1	V_{DDAD}	Supply voltage	Absolute	1.8	—	3.6	V	D
2	ΔV_{DDAD}	Supply voltage	Delta to V_{DD} (V_{DD}-V_{DDAD})[2]	-100	0	+100	mV	D
3	ΔV_{SSAD}	Ground voltage	Delta to V_{SS} (V_{SS}-V_{SSAD})[2]	-100	0	+100	mV	D
4	V_{REFH}	Ref Voltage High	—	1.13	V_{DDAD}	V_{DDAD}	V	D

Table 15. 12-bit ADC Operating Conditions (continued)

#	Symb	Characteristic	Conditions	Minimum	Typical[1]	Maximum	Unit	C
5	V_{REFL}	Ref Voltage Low	—	V_{SSAD}	V_{SSAD}	V_{SSAD}	V	D
6	V_{ADIN}	Input Voltage	—	V_{REFL}	—	V_{REFH}	V	D
7	C_{ADIN}	Input Capacitance	—	—	4	5	pF	C
8	R_{ADIN}	Input Resistance	—	—	2	5	kΩ	C
9	R_{AS}	Analog Source Resistance[3]						
			12 bit mode f_{ADCK} > 8 MHz	—	—	1	kΩ	C
			4 MHz < f_{ADCK} > 8 MHz	—	—	2	kΩ	C
			f_{ADCK} < 4 MHz	—	—	5	kΩ	C
			10-bit mode f_{ADCK} > 8MHz	—	—	2	kΩ	C
			4 MHz < f_{ADCK} < 8 MHz	—	—	5	kΩ	C
			f_{ADCK} < 4 MHz	—	—	10	kΩ	C
			8-bit mode f_{ADCK} > 8 MHz	—	—	5	kΩ	C
			f_{ADCK} < 8 MHz	—	—	10	kΩ	C
10	f_{ADCK}	ADC Conversion Clock Freq.						
			High Speed (ADLPC=0, ADHSC=1)	1.0	—	8.0	MHz	D
			High Speed (ADLPC=0, ADHSC=0)	1.0	—	5.0	MHz	D
			Low Power (ADLPC=1, ADHSC=1)	1.0	—	2.5	MHz	D

1 Typical values assume V_{DDAD} = 3.0V, Temp = 25°C, f_{ADCK}=1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 DC potential difference.

3 External to MCU. Assumes ADLSMP=0.

Table 16. 12-bit SAR ADC Characteristics full operating range (V_{REFH} = V_{DDAD}, V_{REFL} = V_{SSAD}) (continued)

#	Symbol	Characteristic	Conditions[1]	Minimum	Typical[2]	Maximum	Unit	C
7	INL	Integral Non-Linearity	12-bit single-ended mode	—	±1.0	±2.5	LSB[3]	T
			10-bit single-ended mode	—	±0.5	±1.0	LSB[3]	T
			8-bit single-ended mode	—	±0.3	±0.5	LSB[3]	T
8	E_{ZS}	Zero-Scale Error (V_{ADIN} = V_{SSAD})	12-bit single-ended mode	—	±0.7	±2.0	LSB[3]	T
			10-bit single-ended mode	—	±0.4	±1.0	LSB[3]	T
			8-bit single-ended mode	—	±0.2	±0.5	LSB[3]	T
9	E_{FS}	Full-Scale Error (V_{ADIN} = V_{DDAD})	12-bit single-ended mode	—	±1.0	±3.5	LSB[3]	T
			10-bit single-ended mode	—	±0.4	±1.5	LSB[3]	T
			8-bit single-ended mode	—	±0.2	±0.5	LSB[3]	T
10	E_Q	Quantization Error	All modes	—	—	±0.5	LSB[3]	D
11	E_{IL}	Input Leakage Error (I_{In} = leakage current (refer to DC Characteristics)	All modes	I_{In} * R_{AS}			mV	D
12	m	Temp Sensor Slope	-40°C to 25°C	—	1.646	—	mV/xC	C
			25°C to 125°C	—	1.769	—	mV/xC	C
13	V_{TEMP25}	Temp Sensor Voltage	25°C	—	701.2	—	mV	C

1 All accuracy numbers assume the ADC is calibrated with V_{REFH}=V_{DDAD}.

2 Typical values assume V_{DDAD} = 3.0V, Temp = 25°C, f_{ADCK}=2.0MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

3 1 LSB = (V_{REFH} - V_{REFL})/2^N

3.10 MCG and External Oscillator (XOSC) Characteristics

Table 17. MCG (Temperature Range = –40 to 105°C Ambient)

#	Rating		Symbol	Min	Typical	Max	Unit	C
1	Internal reference startup time		t_{irefst}	—	55	100	µs	D
2	Average internal reference frequency	factory trimmed at VDD=3.0V and temp=25°C	f_{int_ft}	—	31.25	—	kHz	C
		user trimmed		31.25	—	39.0625	KHz	C
3	DCO output frequency range - trimmed	Low range (DRS=00)	f_{dco_t}	16	—	20	MHz	C
		Mid range (DRS=01)		32	—	40	MHz	C
		High range[1] (DRS=10)		40	—	60	MHz	C
4	Resolution of trimmed DCO output frequency at fixed voltage and temperature	with FTRIM	$\Delta f_{dco\_res\_t}$	—	± 0.1	± 0.2	$\%f_{dco}$	C
		without FTRIM		—	± 0.2	± 0.4	$\%f_{dco}$	C

Table 18. XOSC (Temperature Range = –40 to 105°C Ambient)

#	Characteristic		Symbol	Minimum	Typical[1]	Maximum	Unit
1	Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1)	• Low range (RANGE = 0)	f_{lo}	32	—	38.4	kHz
		• High range (RANGE = 1), • FEE or FBE mode [2]	f_{hi-fll}	1	—	5	MHz
		• High range (RANGE = 1), • PEE or PBE mode [3]	f_{hi-pll}	1	—	16	MHz
		• High range (RANGE = 1), • High gain (HGO = 1), • FBELP mode	f_{hi-hgo}	1	—	16	MHz
		• High range (RANGE = 1), • Low power (HGO = 0), • FBELP mode	f_{hi-lp}	1	—	8	MHz
2	Load capacitors		C_1 C_2	See Note [4]			
3	Feedback resistor	Low range (32 kHz to 38.4 kHz)	R_F	—	10	—	MΩ
		High range (1 MHz to 16 MHz)	—	—	1	—	
4	Series resistor — Low range	Low Gain (HGO = 0)	R_S	—	0	—	kΩ
		High Gain (HGO = 1)		—	100	—	
5	Series resistor — High range	• Low Gain (HGO = 0)	R_S	—	0	—	kΩ
		• High Gain (HGO = 1)					
		≥ 8 MHz		—	0	0	
		4 MHz		—	0	10	
		1 MHz		—	0	20	
6	Crystal start-up time [5, 6]	Low range, low gain (RANGE=0,HGO=0)	t_{CSTL}	—	200	—	ms
		Low range, high gain (RANGE=0,HGO=1)		—	400	—	
		High range, low gain (RANGE=1,HGO=0)	t_{CSTH}	—	5	—	
		High range, high gain (RANGE=1, HGO=1)		—	15	—	

1 Data in Typical column was characterized at 3.0 V, 25°C or is typical recommended value.

2 When MCG is configured for FEE or FBE mode, input clock source must be divisible using RDIV to within the range of 31.25 kHz to 39.0625 kHz.

3 When MCG is configured for PEE or PBE mode, input clock source must be divisible using RDIV to within the range of 1 MHz to 2 MHz.

4 See crystal or resonator manufacturer's recommendation.

5 This parameter is characterized and not tested on each device.

6 Proper PC board layout procedures must be followed to achieve specifications.

3.11 Mini-FlexBus Timing Specifications

A multi-function external bus interface called Mini-FlexBus is provided with basic functionality to interface to slave-only devices up to a maximum bus frequency of 25.1666 MHz. It can be directly connected to asynchronous or synchronous devices such as external boot ROMs, flash memories, gate-array logic, or other simple target (slave) devices with little or no additional circuitry. For asynchronous devices, a simple chip-select based interface can be used.

All processor bus timings are synchronous; that is, input setup/hold and output delay are given in respect to the rising edge of a reference clock, MB_CLK. The MB_CLK frequency is half the internal system bus frequency.

The following timing numbers indicate when data is latched or driven onto the external bus, relative to the Mini-FlexBus output clock (MB_CLK). All other timing relationships can be derived from these values.

Table 19. Mini-FlexBus AC Timing Specifications

#	Characteristic	Symbol	Min	Max	Unit	C
1	Frequency of Operation	—	—	25.1666	MHz	—
2	Clock Period	MB1	39.73	—	ns	D
3	Output Valid[1]	MB2	—	20	ns	T
4	Output Hold[1]	MB3	1.0	—	ns	D
5	Input Setup[2]	MB4	22	—	ns	T
6	Input Hold[2]	MB5	10	—	ns	D

1 Specification is valid for all MB_A[19:0], MB_D[7:0], $\overline{\text{MB\_CS}}$[1:0], $\overline{\text{MB\_OE}}$, MB_R/$\overline{\text{W}}$, and MB_ALE.

2 Specification is valid for all MB_D[7:0].

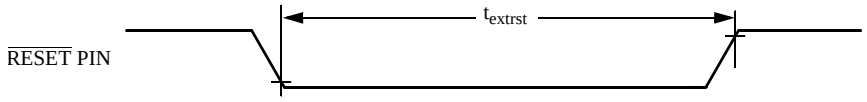

Figure 11. Reset Timing

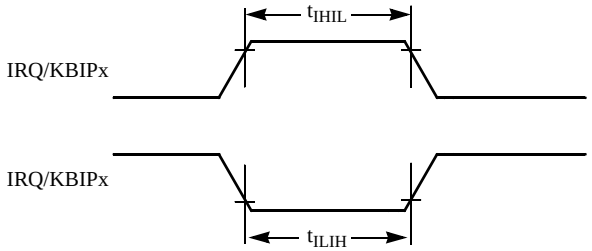

Figure 12. IRQ/KBIPx Timing

3.12.2 TPM Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 21. TPM Input Timing

#	C	Function	Symbol	Minimum	Maximum	Unit
1	—	External clock frequency	f_{TPMext}	dc	$f_{Bus}/4$	MHz
2	—	External clock period	t_{TPMext}	4	—	t_{cyc}
3	D	External clock high time	t_{clkh}	1.5	—	t_{cyc}
4	D	External clock low time	t_{clkl}	1.5	—	t_{cyc}
5	D	Input capture pulse width	t_{ICPW}	1.5	—	t_{cyc}

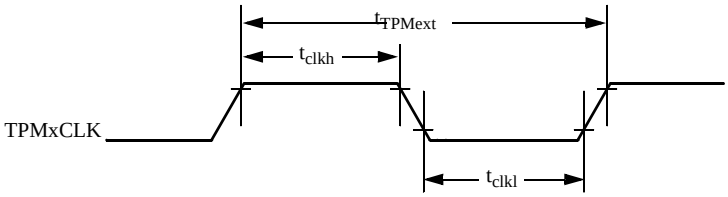

Figure 13. Timer External Clock

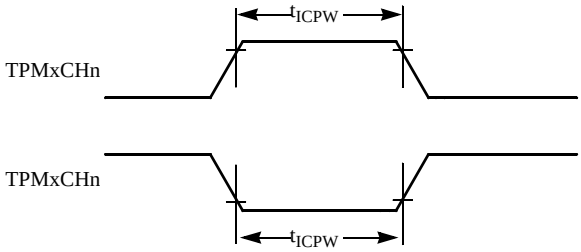

Figure 14. Timer Input Capture Pulse

3.13 SPI Characteristics

The following table and Figure 15 through Figure 18 describe the timing requirements for the SPI system.

Table 22. SPI Timing

No.[1]	Characteristic[2]	Symbol	Minimum	Maximum	Unit	C
1	Operating frequency Master Slave	 f_{op} f_{op}	 $f_{Bus}/2048$ 0	 $f_{Bus}/2$ $f_{Bus}/4$	 Hz Hz	D
2	SPSCK period Master Slave	 t_{SPSCK} t_{SPSCK}	 2 4	 2048 —	 t_{cyc} t_{cyc}	D
3	Enable lead time Master Slave	 t_{Lead} t_{Lead}	 1/2 1	 — —	 t_{SPSCK} t_{cyc}	D
4	Enable lag time Master Slave	 t_{Lag} t_{Lag}	 1/2 1	 — —	 t_{SPSCK} t_{cyc}	D
5	Clock (SPSCK) high or low time Master Slave	 t_{WSPSCK} t_{WSPSCK}	 $t_{cyc} - 30$ $t_{cyc} - 30$	 1024 t_{cyc} —	 ns ns	D
6	Data setup time (inputs) Master Slave	 t_{SU} t_{SU}	 15 15	 — —	 ns ns	D
7	Data hold time (inputs) Master Slave	 t_{HI} t_{HI}	 0 25	 — —	 ns ns	D
8	Slave access time[3]	t_a	—	1	t_{cyc}	D
9	Slave MISO disable time[4]	t_{dis}	—	1	t_{cyc}	D
10	Data valid (after SPSCK edge) Master Slave	 t_v t_v	 — —	 25 25	 ns ns	D
11	Data hold time (outputs) Master Slave	 t_{HO} t_{HO}	 0 0	 — —	 ns ns	D
12	Rise time Input Output	 t_{RI} t_{RO}	 — —	 $t_{cyc} - 25$ 25	 ns ns	D
13	Fall time Input Output	 t_{FI} t_{FO}	 — —	 $t_{cyc} - 25$ 25	 ns ns	D

1 Numbers in this column identify elements in Figure 15 through Figure 18**.**

2 All timing is shown with respect to 20% V_{DD} and 70% V_{DD}, unless noted; 100 pF load on all SPI pins. All timing assumes slew rate control disabled and high drive strength enabled for SPI output pins.

3 Time to data active from high-impedance state.

4 Hold time to high-impedance state.

Table 24. Internal USB 3.3 V Voltage Regulator Characteristics (continued)

#	Characteristic	Symbol	Minimum	Typical	Maximum	Unit	C
3	V_{USB33} input with internal VREG disabled	$V_{usb33in}$	3	3.3	3.6	V	C
4	VREG Quiescent Current	I_{VRQ}	—	0.5	—	mA	C

3.16 VREF Electrical Specifications

Table 25. VREF Electrical Specifications

#	Characteristic	Symbol	Minimum	Maximum	Unit	C
1	Supply voltage	V_{DDA}	1.80	3.6	V	C
2	Temperature	T_A	–40	105	°C	C
3	Output Load Capacitance	C_L	—	100	nf	D
4	Maximum Load	—	—	10	mA	—
5	Voltage Reference Output with Factory Trim. V_{DD} = 3 V.	Vout	1.148	1.152	V	P
6	Temperature Drift (Vmin - Vmax across the full temperature range)	Tdrift	—	25	mV[1]	T
7	Aging Coefficient[2]	Ac	—	60	μV/year	C
8	Powered down Current (Off Mode, VREFEN = 0, VRSTEN = 0)	I	—	0.10	μA	C
9	Bandgap only (MODE_LV[1:0] = 00)	I	—	75	μA	T
10	Low-Power buffer (MODE_LV[1:0] = 01)	I	—	125	μA	T
11	Tight-Regulation buffer (MODE_LV[1:0] = 10)	I	—	1.1	mA	T
12	Load Regulation (MODE_LV = 10)	—	—	100	μV/mA	C
13	Line Regulation MODE = 1:0, Tight Regulation VDD < 2.3 V, Delta VDDA = 100 mV, VREFH = 1.2 V driven externally with VREFO disabled. (Power Supply Rejection	DC	70	—	dB	C

1 See typical chart below.

2 Linear reliability model (1008 hours stress at 125°C = 10 years operating life) used to calculate Aging μV/year. Vrefo data recorded per month.

Figure 20. Typical VREF Output vs V_{DD}

Table 29. Revision History

Revision	Date	Description
4	August 2012	• In Table 1."MCF51JE256/128 Features by MCU and Package, removed the row of "12-bit SAR ADCDifferential Channels". • In Table 3, "Package Pin Assignments", changed from: 'A1' — PTG1 USB_ SESSEND to:'B3' — PTG1 USB_ SESSEND. • In Table 10,"Supply Current Characteristics", for $S3I_{DD}$ changed the max value from '1.2' to '1.3' and typical value from '0.650' to '0.750' for the first row. • In Table 10,"Supply Current Characteristics": — For parameter 3 and parameter 4 changed LPS to LPR. — For parameter 3,changed "FBILP" to "FBI". — For parameter 4, changed "FBELP" to "BLPE". • Fixed the TBD parameters and added figure"Typical Output vs VDD", following the same setup of MM256DS — Added Figure 7,"Offset at Half Scale vs Temperature". — Updated Table 9,"DC Characteristics**".** — Updated Table 10,"Supply Current Characteristics**".** — Updated Table 11,"Stop Mode Adders". — Added Figure 20,"Typical Output vs. V_{DD}. — Updated Table 14,"DAC 12-Bit Operating Behaviors". — Updated Table 20,"Control Timing". — Removed "SPI Electrical Characteristics" table. — Updated Table 25"VREF Electrical Specifications**".** — Updated Table 26,"VREF Limited Range Operating Behaviors**".** • Updated Figure 3, Figure 4, and Figure 5.