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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	Coldfire V1
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	EBI/EMI, I²C, SCI, SPI, USB OTG
Peripherals	LVD, PWM, WDT
Number of I/O	48
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 12x12b; D/A 1x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	81-LBGA
Supplier Device Package	81-MAPBGA (10x10)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcf51je256cmb

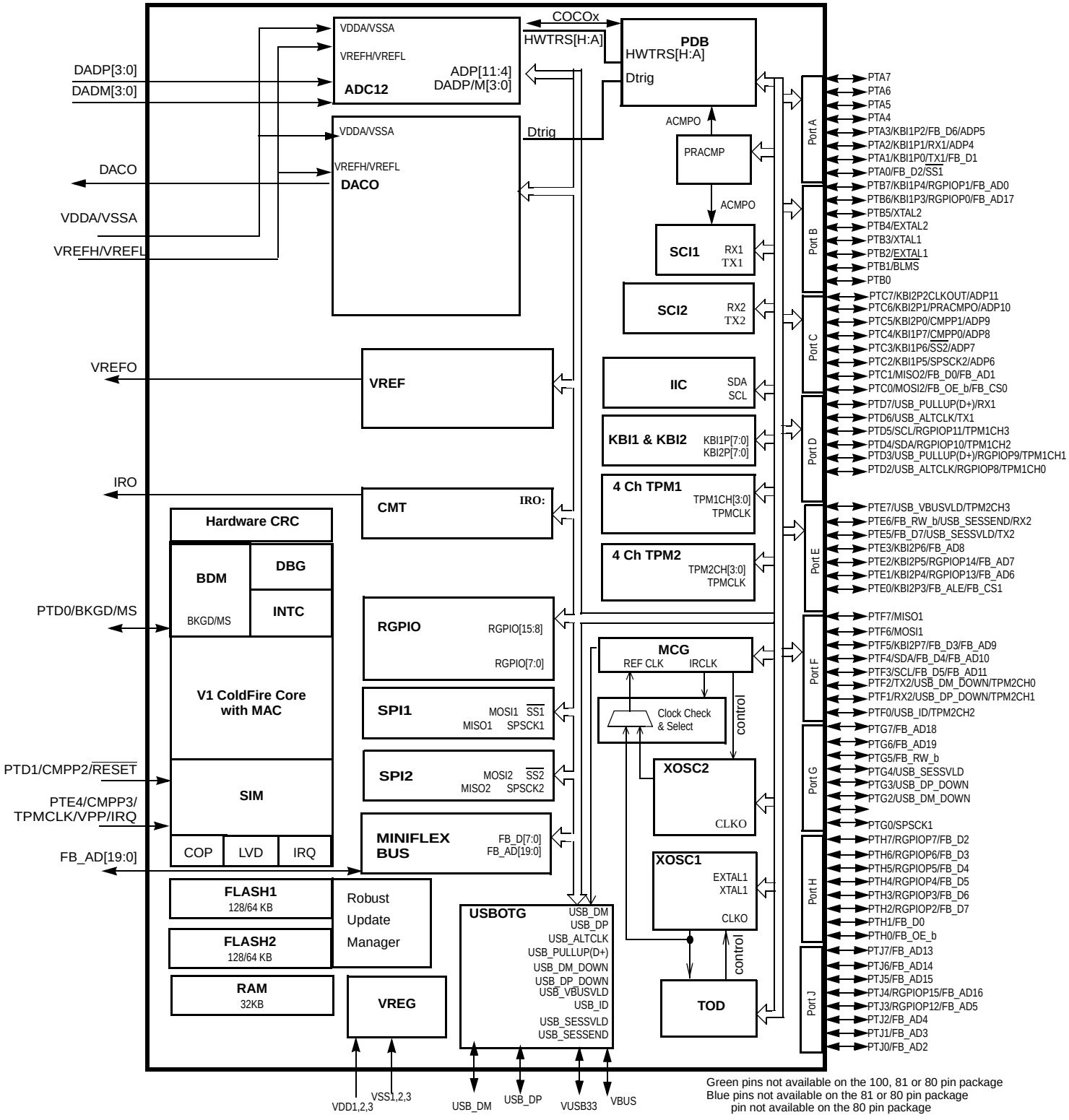


Figure 1. MCF51JE256/128 Block Diagram

2.3 81-Pin MAPBGA

The following figure shows the 81-pin MAPBGA pinout configuration.

	1	2	3	4	5	6	7	8	9	
A	IRO	PTG0	PTF6	USB_DP	VBUS	VUSB33	PTF4	PTF3	PTE4	A
B	PTF7	PTA0	PTG1	USB_DM	PTF5	PTE7	PTF1	PTF0	PTE3	B
C	PTA4	PTA5	PTA6	PTA1	PTF2	PTE6	PTE5	PTE2	PTE1	C
D		PTA7	PTB0	PTB1	PTA2	PTA3	PTD5	PTD7	PTE0	D
E				VDD2	VDD3	VDD1	PTD2	PTD3	PTD6	E
F		ADP2		VSS2	VSS3	VSS1	PTB7	PTC7	PTD4	F
G	ADP0	DACO	ADP3		VREFO	PTB6	PTC0	PTC1	PTC2	G
H			ADP1		PTC3	PTC4	PTD0	PTC5	PTC6	H
J	VSSA	VREFL	VREFH	VDDA	PTB2	PTB3	PTD1	PTB4	PTB5	J
	1	2	3	4	5	6	7	8	9	

Figure 4. 81-Pin MAPBGA

Table 3. Package Pin Assignments (continued)

Package				Default Function	Alternate 1	Alternate 2	Alternate 3	Composite Pin Name
104 MAPBGA	100 LQFP	81 MAPBGA	80 LQFP					
L5	35	J3	30	VREFH	—	—	—	VREFH
L6	36	J4	31	VDDA	—	—	—	VDDA
H6	37	F4	32	VSS2	—	—	—	VSS2
L8	38	J5	33	PTB2	EXTAL1	—	—	PTB2/EXTAL1
L7	39	J6	34	PTB3	XTAL1	—	—	PTB3/XTAL1
D6	40	E4	35	VDD2	—	—	—	VDD2
L11	41	J8	36	PTB4	EXTAL2	—	—	PTB4/EXTAL2
L10	42	J9	37	PTB5	XTAL2	—	—	PTB5/XTAL2
K5	43	G6	38	PTB6	KBI1P3	RGPIOP0	FB_AD17	PTB6/KBI1P3/RGPIOP0/ FB_AD17
K6	44	F7	39	PTB7	KBI1P4	RGPIOP1	FB_AD0	PTB7/KBI1P4/RGPIOP1/ FB_AD0
J7	45	—	—	PTH2	RGPIOP2	FB_D7	—	PTH2/RGPIOP2/FB_D7
J6	46	—	—	PTH3	RGPIOP3	FB_D6	—	PTH3/RGPIOP3/FB_D6
J5	47	—	—	PTH4	RGPIOP4	FB_D5	—	PTH4/RGPIOP4/FB_D5
K4	48	—	—	PTH5	RGPIOP5	FB_D4	—	PTH5/RGPIOP5/FB_D4
J4	49	—	—	PTH6	RGPIOP6	FB_D3	—	PTH6/RGPIOP6/FB_D3
J3	50	—	—	PTH7	RGPIOP7	FB_D2	—	PTH7/RGPIOP7/FB_D2
J10	51	G7	40	PTC0	MOSI2	$\overline{\text{FB\_OE}}$	FB_CS0	PTC0/MOSI2/$\overline{\text{FB\_OE}}$/ FB_CS0
J11	52	G8	41	PTC1	MISO2	FB_D0	FB_AD1	PTC1/MISO2/FB_D0/FB_AD1
J9	53	G9	42	PTC2	KBI1P5	SPSCK2	ADP6	PTC2/KBI1P5/SPSCK2/ADP6
K7	54	H5	43	PTC3	KBI1P6	$\overline{\text{SS2}}$	ADP7	PTC3/KBI1P6/$\overline{\text{SS2}}$/ADP7
K9	55	H6	44	PTC4	KBI1P7	CMPP0	ADP8	PTC4/KBI1P7/CMPP0/ADP8
K10	56	H8	45	PTC5	KBI2P0	CMPP1	ADP9	PTC5/KBI2P0/CMPP1/ADP9
K11	57	H9	46	PTC6	KBI2P1	PRACMPO	ADP10	PTC6/KBI2P1/PRACMPO/ ADP10
F8	58	F8	47	PTC7	KBI2P2	CLKOUT	ADP11	PTC7/KBI2P2/CLKOUT/ADP11
L9	59	H7	48	PTD0	BKGD	MS	—	PTD0/BKGD/MS
K8	60	J7	49	PTD1	CMPP2	$\overline{\text{RESET}}$	—	PTD1/CMPP2/$\overline{\text{RESET}}$
H11	61	E7	50	PTD2	USB_ALTCLK	RGPIOP8	TPM1CH0	PTD2/USB_ALTCLK/RGPIOP8/ TPM1CH0
H10	62	E8	51	PTD3	USB_PULLUP(D+)	RGPIOP9	TPM1CH1	PTD3/USB_PULLUP(D+)/ RGPIOP9/TPM1CH1
H9	63	F9	52	PTD4	SDA	RGPIOP10	TPM1CH2	PTD4/SDA/RGPIOP10/ TPM1CH2
G9	64	D7	53	PTD5	SCL	RGPIOP11	TPM1CH3	PTD5/SCL/RGPIOP11/ TPM1CH3
J8	65	E9	54	PTD6	USB_ALTCLK	TX1	—	PTD6/USB_ALTCLK/TX1

Table 3. Package Pin Assignments (continued)

Package				Default Function	Alternate 1	Alternate 2	Alternate 3	Composite Pin Name
104 MAPBGA	100 LQFP	81 MAPBGA	80 LQFP					
G10	66	D8	55	PTD7	USB_PULLUP(D+)	RX1	—	PTD7/USB_PULLUP(D+) /RX1
G11	67	D9	56	PTE0	KBI2P3	FB_ALE	FB_CS1	PTE0/KBI2P3/FB_ALE/ FB_CS1
F10	68	—	—	PTJ0	FB_AD2	—	—	PTJ0/FB_AD2
F11	69	—	—	PTJ1	FB_AD3	—	—	PTJ1/FB_AD3
F9	70	—	—	PTJ2	FB_AD4	—	—	PTJ2/FB_AD4
E10	71	—	—	PTJ3	RGPIOP12	FB_AD5	—	PTJ3/RGPIOP12/FB_AD5
E11	72	C9	57	PTE1	KBI2P4	RGPIOP13	FB_AD6	PTE1/KBI2P4/RGPIOP13/ FB_AD6
D11	73	C8	58	PTE2	KBI2P5	RGPIOP14	FB_AD7	PTE2/KBI2P5/RGPIOP14/ FB_AD7
D10	74	B9	59	PTE3	KBI2P6	FB_AD8	—	PTE3/KBI2P6/FB_AD8
C9	75	A9	60	PTE4	CMPP3	TPMCLK	IRQ	PTE4/CMPP3/TPMCLK/VPP/ IRQ
H8	76	F5	61	VSS3	—	—	—	VSS3
D8	77	E5	62	VDD3	—	—	—	VDD3
B8	78	C7	63	PTE5	FB_D7	USB_ SESSVLD	TX2	PTE5/FB_D7/USB_SESSVLD/ TX2
C10	79	C6	64	PTE6	FB_$\overline{RW}$	USB_ SESSEND	RX2	PTE6/FB_RW_b/ USB_SESSEND/RX2
C11	80	B6	65	PTE7	USB_VBUSVLD	TPM2CH3	—	PTE7/USB_VBUSVLD/ TPM2CH3
B9	81	B8	66	PTF0	USB_ID	TPM2CH2	—	PTF0/USB_ID/TPM2CH2
B10	82	B7	67	PTF1	RX2	USB_DP_ DOWN	TPM2CH1	PTF1/RX2/USB_DP_DOWN/ TPM2CH1
B11	83	C5	68	PTF2	TX2	USB_DM_ DOWN	TPM2CH0	PTF2/TX2/USB_DM_DOWN/ TPM2CH0
A11	84	—	—	PTJ4	RGPIOP15	FB_AD16	—	PTJ4/RGPIOP15/FB_AD16
A10	85	—	—	PTJ5	FB_AD15	—	—	PTJ5/FB_AD15
B6	86	—	—	PTJ6	FB_AD14	—	—	PTJ6/FB_AD14
A9	87	—	—	PTJ7	FB_AD13	—	—	PTJ7/FB_AD13
A8	88	—	—	FB_AD12	—	—	—	FB_AD12
A7	89	A8	69	PTF3	SCL	FB_D5	FB_AD11	PTF3/SCL/FB_D5/FB_AD11
A6	90	A7	70	PTF4	SDA	FB_D4	FB_AD10	PTF4/SDA/FB_D4/FB_AD10
B5	91	B5	71	PTF5	KBI2P7	FB_D3	FB_AD9	PTF5/KBI2P7/FB_D3/FB_AD9
A5	92	A6	72	VUSB33	—	—	—	VUSB33
A4	93	B4	73	USB_DM	—	—	—	USB_DM
A3	94	A4	74	USB_DP	—	—	—	USB_DP
B4	95	A5	75	VBUS	—	—	—	VBUS

Table 3. Package Pin Assignments (continued)

Package				Default Function	Alternate 1	Alternate 2	Alternate 3	Composite Pin Name
104 MAPBGA	100 LQFP	81 MAPBGA	80 LQFP					
H4	96	F6	76	VSS1	—	—	—	VSS1
D4	97	E6	77	VDD1	—	—	—	VDD1
A1	98	A3	78	PTF6	MOSI1	—	—	PTF6/MOSI1
A2	99	B1	79	PTF7	MISO1	—	—	PTF7/MISO1
B1	100	A2	80	PTG0	SPSCK1	—	—	PTG0/SPSCK1
F4	—	B3	—	PTG1	USB_SESSEND	—	—	PTG1/USB_SESSEND
C4	—	—	—	PTG2	USB_DM_DOWN	—	—	PTG2/USB_DM_DOWN
B3	—	—	—	PTG3	USB_DP_DOWN	—	—	PTG3/USB_DP_DOWN
C2	—	—	—	PTG4	USB_SESSVLD	—	—	PTG4/USB_SESSVLD

where K is a constant pertaining to the particular part. K can be determined from Equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A.

3.4 ESD Protection Characteristics

Although damage from static discharge is much less common on these devices than on early CMOS circuits, normal handling precautions should be used to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with CDF-AEC-Q00 Stress Test Qualification for Automotive Grade Integrated Circuits. (http://www.aecouncil.com/) This device was qualified to AEC-Q100 Rev E.

A device is considered to have failed if, after exposure to ESD pulses, the device no longer meets the device specification requirements. Complete dc parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table 7. ESD and Latch-up Test Conditions

Model	Description	Symbol	Value	Unit
Human Body	Series Resistance	R1	1500	Ω
	Storage Capacitance	C	100	pF
	Number of Pulse per pin	—	3	—
Machine	Series Resistance	R1	0	Ω
	Storage Capacitance	C	200	pF
	Number of Pulse per pin	—	3	—
Latch-up	Minimum input voltage limit	—	–2.5	V
	Maximum input voltage limit	—	7.5	V

Table 8. ESD and Latch-Up Protection Characteristics

#	Rating	Symbol	Minimum	Maximum	Unit	C
1	Human Body Model (HBM)	V_{HBM}	±2000	—	V	T
2	Machine Model (MM)	V_{MM}	±200	—	V	T
3	Charge Device Model (CDM)	V_{CDM}	±500	—	V	T
4	Latch-up Current at T_A = 125°C	I_{LAT}	±100	—	mA	T

3.5 DC Characteristics

This section includes information about power supply requirements, I/O pin characteristics, and power supply current in various operating modes.

Table 9. DC Characteristics (continued)

#	Symbol	Characteristic	Condition	Minimum	Typical[1]	Maximum	Unit	C
11	R_{PU}	Pull-up resistors all digital inputs, when enabled	—	17.5	—	52.5	kΩ	P
12	R_{PD}	Internal pull-down resistors[4]	—	17.5	—	52.5	kΩ	P
13	I_{IC}	DC injection current [5, 6, 7] — Single pin limit	$V_{SS} > V_{IN} > V_{DD}$	–0.2	—	0.2	mA	D
		DC injection current [5, 6, 7] — Total MCU limit, includes sum of all stressed pins	$V_{SS} > V_{IN} > V_{DD}$	–5	—	5	mA	D
14	C_{In}	Input Capacitance, all pins	—	—	—	8	pF	C
15	V_{RAM}	RAM retention voltage	—	—	0.6	1.0	V	C
16	V_{POR}	POR re-arm voltage[8]	—	0.9	1.4	1.79	V	C
17	t_{POR}	POR re-arm time	—	10	—	—	µs	D
18	V_{LVDH}	Low-voltage detection threshold — high range[9]						
			V_{DD} falling	2.11	2.16	2.22	V	P
			V_{DD} rising	2.16	2.21	2.27	V	P
19	V_{LVDL}	Low-voltage detection threshold — low range[9]						
			V_{DD} falling	1.80	1.82	1.91	V	P
			V_{DD} rising	1.86	1.90	1.99	V	P
20	V_{LVWH}	Low-voltage warning threshold — high range[9]						
			V_{DD} falling	2.36	2.46	2.56	V	P
			V_{DD} rising	2.36	2.46	2.56	V	P
21	V_{LVWL}	Low-voltage warning threshold — low range[9]						
			V_{DD} falling	2.11	2.16	2.22	V	P
			V_{DD} rising	2.16	2.21	2.27	V	P
22	V_{hys}	Low-voltage inhibit reset/recover hysteresis[10]	—	—	50	—	mV	C
23	V_{BG}	Bandgap Voltage Reference[11]	—	1.145	1.17	1.195	V	P

1 Typical values are measured at 25°C. Characterized, not tested

2 As the supply voltage rises, the LVD circuit will hold the MCU in reset until the supply has risen above V_{LVDL}.

3 Does not include analog module pins. Dedicated analog pins should not be pulled to VDD or VSS and should be left floating when not used to reduce current leakage.

4 Measured with $V_{In} = V_{DD}$.

5 All functional non-supply pins are internally clamped to V_{SS} and V_{DD},except PTD1.

6 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

7 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).

Table 11. Stop Mode Adders (continued)

#	Parameter	Condition	Temperature (°C)					Units	C
			-40	25	70	85	105		
5	LVD[1]	LVDSE = 1	116	117	126	132	172	µA	T
6	PRACMP[1]	Not using the bandgap (BGBE = 0)	17	18	24	35	74	µA	T
7	ADC[1]	ADLPC = ADLSMP = 1 Not using the bandgap (BGBE = 0)	75	85	100	115	165	µA	T
8	DAC[1]	High power mode; no load on DACO	500	500	500	500	500	µA	T

1 Not available in stop2 mode.

Figure 6. Stop IDD versus Temperature

Table 14. DAC 12-Bit Operating Behaviors

#	Characteristic	Symbol	Minimum	Typical	Maximum	Unit	C	Notes
1	Resolution	N	12	—	12	bit	T	
2	Supply current low-power mode	I_{DDA_DACLP}	—	50	100	μA	T	
3	Supply current high-power mode	I_{DDA_DACHP}	—	345	500	μA	T	
4	Full-scale Settling time (±1 LSB) (0x080 to 0xF7F or 0xF7F to 0x080) low-power mode	$Ts_{FS}LP$	—	—	200	μs	T	• V_{DDA} = 3 V or 2.2 V • V_{REFSEL} = 1 • Temperature = 25°C
5	Full-scale Settling time (±1 LSB) (0x080 to 0xF7F or 0xF7F to 0x080) high-power mode	$Ts_{FS}HP$	—	—	30	μs	T	• V_{DDA} = 3 V or 2.2 V • V_{REFSEL} = 1 • Temperature = 25°C
6	Code-to-code Settling time (±1 LSB) (0xBF8 to 0xC08 or 0xC08 to 0xBF8) low-power mode	$Ts_{C-C}LP$	—	—	5	μs	T	• V_{DDA} = 3 V or 2.2 V • V_{REFSEL} = 1 • Temperature = 25°C
7	Code-to-code Settling time (±1 LSB) (0xBF8 to 0xC08 or 0xC08 to 0xBF8) high-power mode	$Ts_{C-C}HP$	—	1	—	μs	T	• V_{DDA} = 3 V or 2.2 V • V_{REFSEL} = 1 • Temperature = 25°C
8	DAC output voltage range low (high-power mode, no load, DAC set to 0, 3 V at room temperature)	$V_{dacoutl}$	—	—	100	mV	T	
9	DAC output voltage range high (high-power mode, no load, DAC set to 0x0FFF)	$V_{dacouth}$	V_{DACR}–100	—	—	mV	T	
10	Integral non-linearity error	INL	—	—	±8	LSB	T	
11	Differential non-linearity error V_{DACR} is > 2.4 V	DNL	—	—	±1	LSB	T	
12	Offset error	E_O	—	±0.4	±3	%FSR	T	Calculated by a best fit curve from VSS + 100mV to V_{REFH} –100mV
13	Gain error (V_{REF} = V_{ext} = V_{DD})	E_G	—	±0.1	±0.5	%FSR	T	Calculated by a best fit curve from VSS + 100mV to V_{REFH} –100mV
14	Power supply rejection ratio $V_{DD} \geq 2.4$ V	PSRR	60	—	—	dB	T	

Table 15. 12-bit ADC Operating Conditions (continued)

#	Symb	Characteristic	Conditions	Minimum	Typical[1]	Maximum	Unit	C
5	V_{REFL}	Ref Voltage Low	—	V_{SSAD}	V_{SSAD}	V_{SSAD}	V	D
6	V_{ADIN}	Input Voltage	—	V_{REFL}	—	V_{REFH}	V	D
7	C_{ADIN}	Input Capacitance	—	—	4	5	pF	C
8	R_{ADIN}	Input Resistance	—	—	2	5	kΩ	C
9	R_{AS}	Analog Source Resistance[3]						
			12 bit mode f_{ADCK} > 8 MHz	—	—	1	kΩ	C
			4 MHz < f_{ADCK} > 8 MHz	—	—	2	kΩ	C
			f_{ADCK} < 4 MHz	—	—	5	kΩ	C
			10-bit mode f_{ADCK} > 8MHz	—	—	2	kΩ	C
			4 MHz < f_{ADCK} < 8 MHz	—	—	5	kΩ	C
			f_{ADCK} < 4 MHz	—	—	10	kΩ	C
			8-bit mode f_{ADCK} > 8 MHz	—	—	5	kΩ	C
			f_{ADCK} < 8 MHz	—	—	10	kΩ	C
10	f_{ADCK}	ADC Conversion Clock Freq.						
			High Speed (ADLPC=0, ADHSC=1)	1.0	—	8.0	MHz	D
			High Speed (ADLPC=0, ADHSC=0)	1.0	—	5.0	MHz	D
			Low Power (ADLPC=1, ADHSC=1)	1.0	—	2.5	MHz	D

1 Typical values assume V_{DDAD} = 3.0V, Temp = 25°C, f_{ADCK}=1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 DC potential difference.

3 External to MCU. Assumes ADLSMP=0.

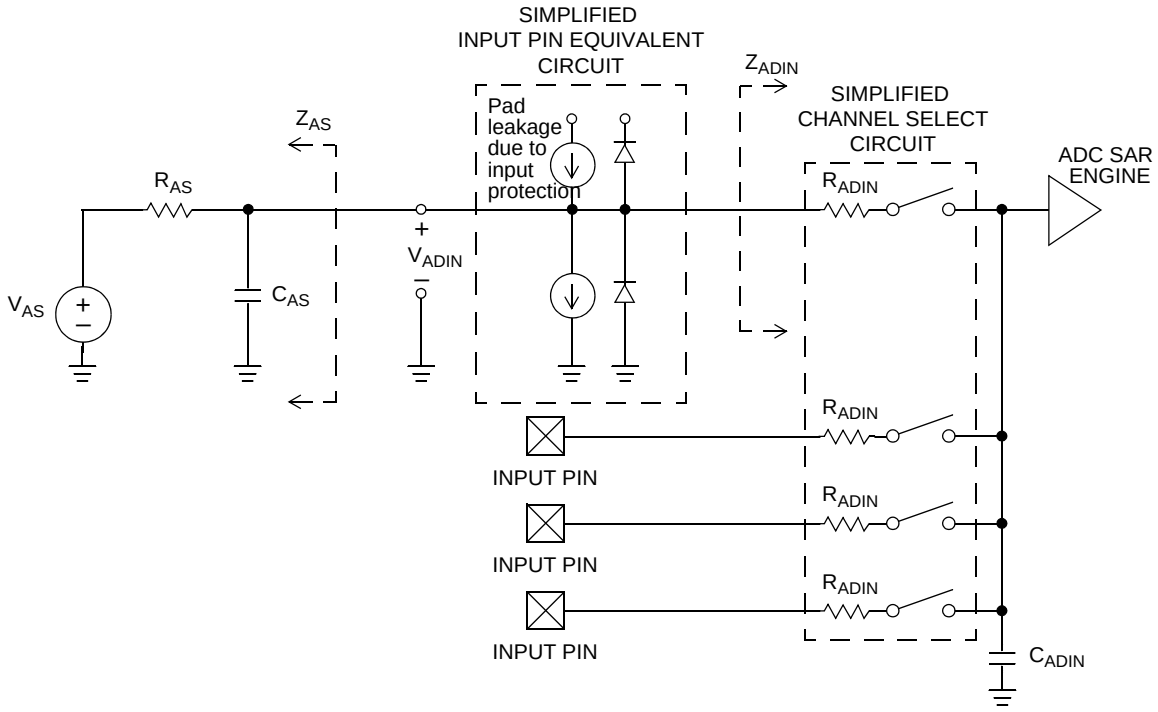


Figure 8. ADC Input Impedance Equivalency Diagram

Table 16. 12-bit SAR ADC Characteristics full operating range ($V_{REFH} = V_{DDAD}$, $V_{REFL} = V_{SSAD}$)

#	Symbol	Characteristic	Conditions[1]	Minimum	Typical[2]	Maximum	Unit	C
1	I_{DDAD}	Supply Current (ADLSMP=0, ADCO=1)	ADLPC=1, ADHSC=0	—	215	—	μA	T
			ADLPC=0, ADHSC=0	—	470	—	μA	T
			ADLPC=0, ADHSC=1	—	610	—	μA	T
			Stop, Reset, Module Off	—	0.01	—	μA	C
2	f_{ADACK}	ADC Asynchronous Clock Source (t_{ADACK} =1/f_{ADACK})	ADLPC=1, ADHSC=0	—	2.4	—	MHz	P
			ADLPC=0, ADHSC=0	—	5.2	—	MHz	P
			ADLPC=0, ADHSC=1	—	6.2	—	MHz	P
3	—	Sample Time — *See Reference Manual for sample times.*						
4	—	Conversion Time — *See Rreference Manual for conversion times.*						
5	TUE	Total Unadjusted Error 32x Hardware Averaging (AVGE = %1 AVGS = %11)	12-bit single-ended mode	—	±1.75	±3.5	LSB[3]	T
			10-bit single-ended mode	—	±0.8	±1.5	LSB[3]	T
			8-bit single-ended mode	—	±0.5	±1.0	LSB[3]	T
6		Differential Non-Linearity	12-bit single-ended mode	—	±0.7	±1	LSB[3]	T
			10-bit single-ended mode	—	±0.5	±0.75	LSB[3]	T
			8-bit single-ended mode	—	±0.2	±0.5	LSB[3]	T

Table 18. XOSC (Temperature Range = –40 to 105°C Ambient)

#	Characteristic		Symbol	Minimum	Typical[1]	Maximum	Unit
1	Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1)	• Low range (RANGE = 0)	f_{lo}	32	—	38.4	kHz
		• High range (RANGE = 1), • FEE or FBE mode [2]	f_{hi-fll}	1	—	5	MHz
		• High range (RANGE = 1), • PEE or PBE mode [3]	f_{hi-pll}	1	—	16	MHz
		• High range (RANGE = 1), • High gain (HGO = 1), • FBELP mode	f_{hi-hgo}	1	—	16	MHz
		• High range (RANGE = 1), • Low power (HGO = 0), • FBELP mode	f_{hi-lp}	1	—	8	MHz
2	Load capacitors		C_1 C_2	See Note [4]			
3	Feedback resistor	Low range (32 kHz to 38.4 kHz)	R_F	—	10	—	MΩ
		High range (1 MHz to 16 MHz)	—	—	1	—	
4	Series resistor — Low range	Low Gain (HGO = 0)	R_S	—	0	—	kΩ
		High Gain (HGO = 1)		—	100	—	
5	Series resistor — High range	• Low Gain (HGO = 0)	R_S	—	0	—	kΩ
		• High Gain (HGO = 1)					
		≥ 8 MHz		—	0	0	
		4 MHz		—	0	10	
		1 MHz		—	0	20	
6	Crystal start-up time [5, 6]	Low range, low gain (RANGE=0,HGO=0)	t_{CSTL}	—	200	—	ms
		Low range, high gain (RANGE=0,HGO=1)		—	400	—	
		High range, low gain (RANGE=1,HGO=0)	t_{CSTH}	—	5	—	
		High range, high gain (RANGE=1, HGO=1)		—	15	—	

1 Data in Typical column was characterized at 3.0 V, 25°C or is typical recommended value.

2 When MCG is configured for FEE or FBE mode, input clock source must be divisible using RDIV to within the range of 31.25 kHz to 39.0625 kHz.

3 When MCG is configured for PEE or PBE mode, input clock source must be divisible using RDIV to within the range of 1 MHz to 2 MHz.

4 See crystal or resonator manufacturer's recommendation.

5 This parameter is characterized and not tested on each device.

6 Proper PC board layout procedures must be followed to achieve specifications.

Figure 9. Mini-FlexBus Read Timing

Figure 10. Mini-FlexBus Write Timing

3.12.2 TPM Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 21. TPM Input Timing

#	C	Function	Symbol	Minimum	Maximum	Unit
1	—	External clock frequency	f_{TPMext}	dc	$f_{Bus}/4$	MHz
2	—	External clock period	t_{TPMext}	4	—	t_{cyc}
3	D	External clock high time	t_{clkh}	1.5	—	t_{cyc}
4	D	External clock low time	t_{clkl}	1.5	—	t_{cyc}
5	D	Input capture pulse width	t_{ICPW}	1.5	—	t_{cyc}

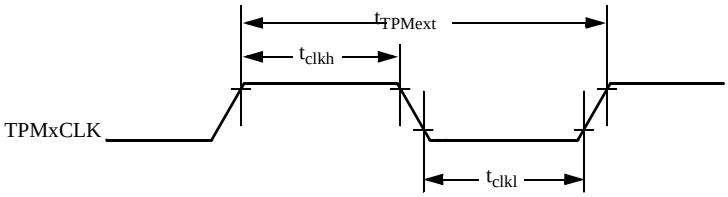


Figure 13. Timer External Clock

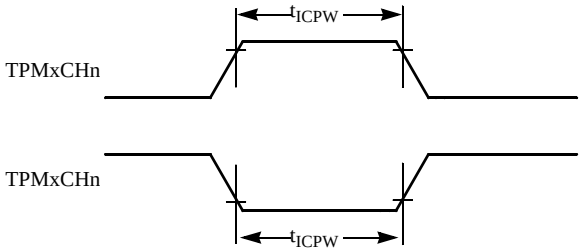


Figure 14. Timer Input Capture Pulse

3.13 SPI Characteristics

The following table and Figure 15 through Figure 18 describe the timing requirements for the SPI system.

Table 22. SPI Timing

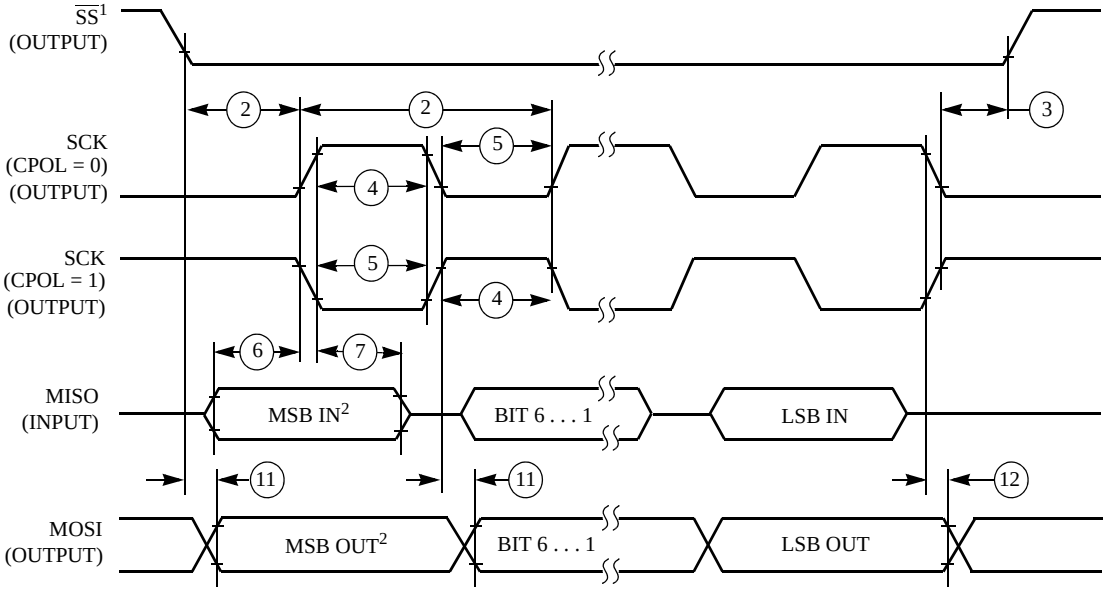
No.[1]	Characteristic[2]	Symbol	Minimum	Maximum	Unit	C
1	Operating frequency Master Slave	 f_{op} f_{op}	 $f_{Bus}/2048$ 0	 $f_{Bus}/2$ $f_{Bus}/4$	 Hz Hz	D
2	SPSCK period Master Slave	 t_{SPSCK} t_{SPSCK}	 2 4	 2048 —	 t_{cyc} t_{cyc}	D
3	Enable lead time Master Slave	 t_{Lead} t_{Lead}	 1/2 1	 — —	 t_{SPSCK} t_{cyc}	D
4	Enable lag time Master Slave	 t_{Lag} t_{Lag}	 1/2 1	 — —	 t_{SPSCK} t_{cyc}	D
5	Clock (SPSCK) high or low time Master Slave	 t_{WSPSCK} t_{WSPSCK}	 $t_{cyc} - 30$ $t_{cyc} - 30$	 1024 t_{cyc} —	 ns ns	D
6	Data setup time (inputs) Master Slave	 t_{SU} t_{SU}	 15 15	 — —	 ns ns	D
7	Data hold time (inputs) Master Slave	 t_{HI} t_{HI}	 0 25	 — —	 ns ns	D
8	Slave access time[3]	t_a	—	1	t_{cyc}	D
9	Slave MISO disable time[4]	t_{dis}	—	1	t_{cyc}	D
10	Data valid (after SPSCK edge) Master Slave	 t_v t_v	 — —	 25 25	 ns ns	D
11	Data hold time (outputs) Master Slave	 t_{HO} t_{HO}	 0 0	 — —	 ns ns	D
12	Rise time Input Output	 t_{RI} t_{RO}	 — —	 $t_{cyc} - 25$ 25	 ns ns	D
13	Fall time Input Output	 t_{FI} t_{FO}	 — —	 $t_{cyc} - 25$ 25	 ns ns	D

1 Numbers in this column identify elements in Figure 15 through Figure 18**.**

2 All timing is shown with respect to 20% V_{DD} and 70% V_{DD}, unless noted; 100 pF load on all SPI pins. All timing assumes slew rate control disabled and high drive strength enabled for SPI output pins.

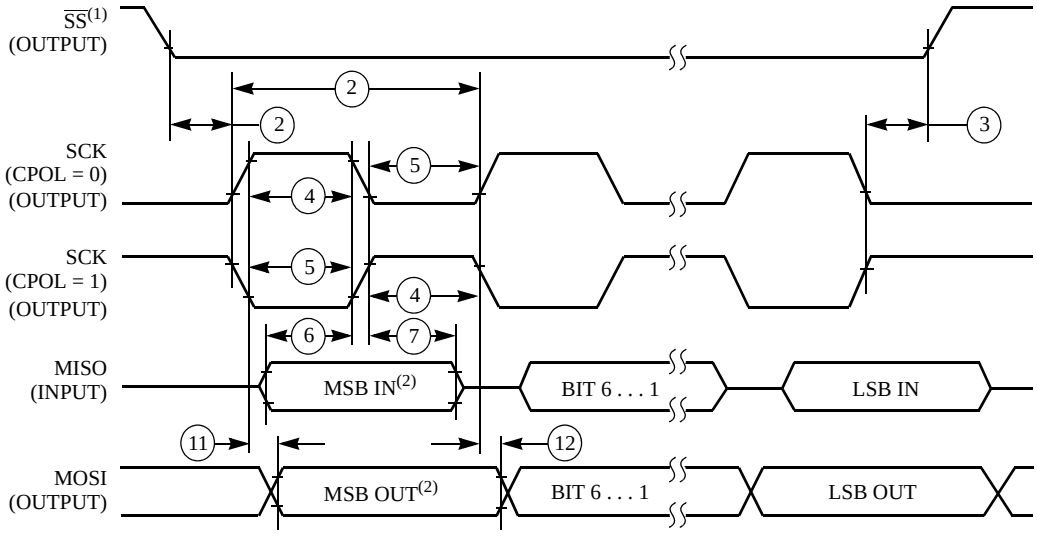
3 Time to data active from high-impedance state.

4 Hold time to high-impedance state.



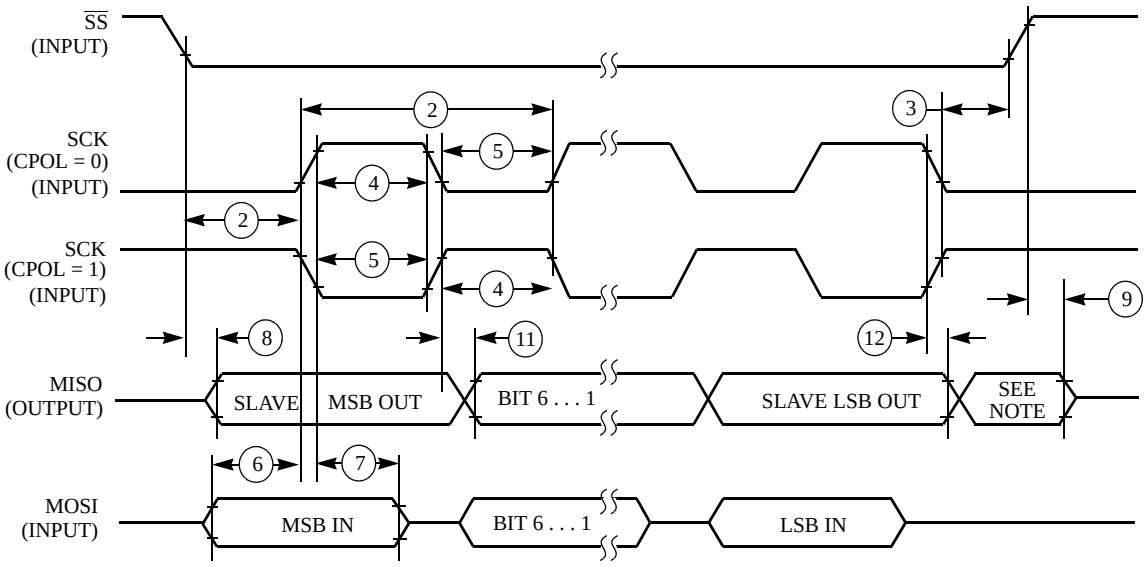
NOTES:
1. $\overline{SS}$ output mode (MODFEN = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 15. SPI Master Timing (CPHA = 0)



NOTES:
1. $\overline{SS}$ output mode (MODFEN = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

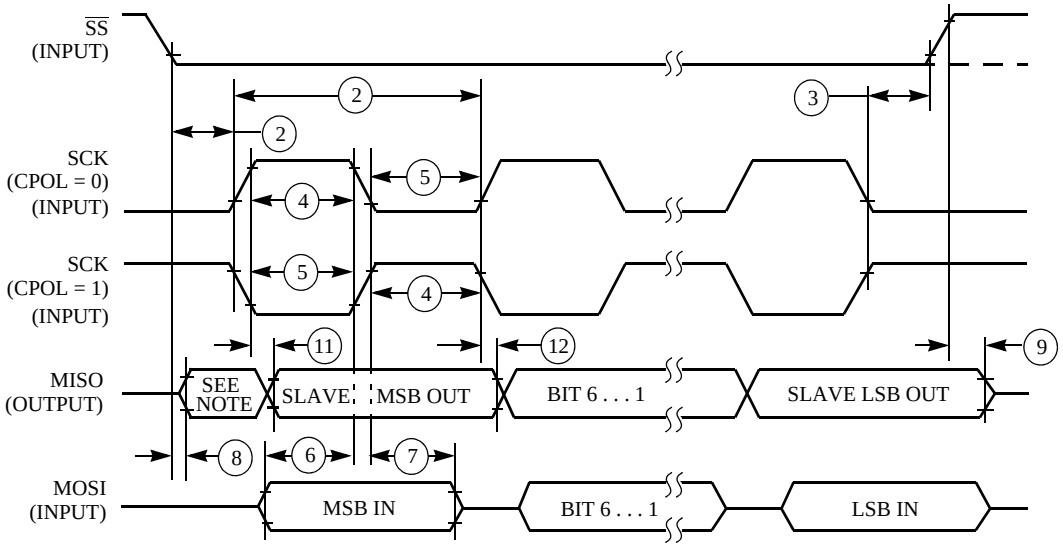
Figure 16. SPI Master Timing (CPHA = 1)



NOTE:

1. Not defined, but normally MSB of character just received

Figure 17. SPI Slave Timing (CPHA = 0)



NOTE:

1. Not defined, but normally LSB of character just received

Figure 18. SPI Slave Timing (CPHA = 1)

3.14 Flash Specifications

This section provides details about program/erase times and program-erase endurance for the Flash memory.

Program and erase operations do not require any special power sources other than the normal V_{DD} supply. For more detailed information about program/erase operations, see the Memory chapter in the Reference Manual for this device (MCF51JE256RM).

Table 23. Flash Characteristics

#	Characteristic	Symbol	Minimum	Typical	Maximum	Unit	C
1	Supply voltage for program/erase -40°C to 105°C	$V_{prog/erase}$	1.8	—	3.6	V	D
2	Supply voltage for read operation	V_{Read}	1.8	—	3.6	V	D
3	Internal FCLK frequency[1]	f_{FCLK}	150	—	200	kHz	D
4	Internal FCLK period (1/FCLK)	t_{Fcyc}	5	—	6.67	µs	D
5	Byte program time (random location)[2]	t_{prog}	9			t_{Fcyc}	P
6	Byte program time (burst mode)[2]	t_{Burst}	4			t_{Fcyc}	P
7	Page erase time[2]	t_{Page}	4000			t_{Fcyc}	P
8	Mass erase time[2]	t_{Mass}	20,000			t_{Fcyc}	P
9	Program/erase endurance[3] T_L to T_H = –40°C to + 105°C T = 25°C		10,000 —	— 100,000	— —	cycles	C
10	Data retention[4]	t_{D_ret}	15	100	—	years	C

1 The frequency of this clock is controlled by a software setting.

2 These values are hardware state machine controlled. User code does not need to count cycles. This information supplied for calculating approximate time to program and erase.

3 **Typical endurance for flash** was evaluated for this product family on the HC9S12Dx64. For additional information on how Freescale defines typical endurance, please refer to Engineering Bulletin EB619, *Typical Endurance for Nonvolatile Memory.*

4 **Typical data retention** values are based on intrinsic capability of the technology measured at high temperature and de-rated to 25°C using the Arrhenius equation. For additional information on how Freescale defines typical data retention, please refer to Engineering Bulletin EB618, *Typical Data Retention for Nonvolatile Memory.*

3.15 USB Electricals

The USB electricals for the USB On-the-Go module conform to the standards documented by the Universal Serial Bus Implementers Forum. For the most up-to-date standards, visit http://www.usb.org.

If the Freescale USB On-the-Go implementation has electrical characteristics that deviate from the standard or require additional information, this space would be used to communicate that information.

Table 24. Internal USB 3.3 V Voltage Regulator Characteristics

#	Characteristic	Symbol	Minimum	Typical	Maximum	Unit	C
1	Regulator operating voltage	V_{regin}	3.9	—	5.5	V	C
2	VREG output	V_{regout}	3	3.3	3.75	V	P

Table 24. Internal USB 3.3 V Voltage Regulator Characteristics (continued)

#	Characteristic	Symbol	Minimum	Typical	Maximum	Unit	C
3	V_{USB33} input with internal VREG disabled	$V_{usb33in}$	3	3.3	3.6	V	C
4	VREG Quiescent Current	I_{VRQ}	—	0.5	—	mA	C

3.16 VREF Electrical Specifications

Table 25. VREF Electrical Specifications

#	Characteristic	Symbol	Minimum	Maximum	Unit	C
1	Supply voltage	V_{DDA}	1.80	3.6	V	C
2	Temperature	T_A	–40	105	°C	C
3	Output Load Capacitance	C_L	—	100	nf	D
4	Maximum Load	—	—	10	mA	—
5	Voltage Reference Output with Factory Trim. V_{DD} = 3 V.	Vout	1.148	1.152	V	P
6	Temperature Drift (Vmin - Vmax across the full temperature range)	Tdrift	—	25	mV[1]	T
7	Aging Coefficient[2]	Ac	—	60	μV/year	C
8	Powered down Current (Off Mode, VREFEN = 0, VRSTEN = 0)	I	—	0.10	μA	C
9	Bandgap only (MODE_LV[1:0] = 00)	I	—	75	μA	T
10	Low-Power buffer (MODE_LV[1:0] = 01)	I	—	125	μA	T
11	Tight-Regulation buffer (MODE_LV[1:0] = 10)	I	—	1.1	mA	T
12	Load Regulation (MODE_LV = 10)	—	—	100	μV/mA	C
13	Line Regulation MODE = 1:0, Tight Regulation VDD < 2.3 V, Delta VDDA = 100 mV, VREFH = 1.2 V driven externally with VREFO disabled. (Power Supply Rejection	DC	70	—	dB	C

1 See typical chart below.

2 Linear reliability model (1008 hours stress at 125°C = 10 years operating life) used to calculate Aging μV/year. Vrefo data recorded per month.

4 Ordering Information

This section contains ordering information for the device numbering system. See Table 1 for feature summary by package information.

4.1 Part Numbers

Table 27. Orderable Part Number Summary

Freescale Part Number	Description	Flash / SRAM (Kbytes)	Package	Temperature
MCF51JE256VML	MCF51JE256 ColdFire Microcontroller	256K/32K	104 MAPBGA	–40 to 105 °C
MCF51JE256VLL	MCF51JE256 ColdFire Microcontroller	256K/32K	100 LQFP	–40 to 105 °C
MCF51JE256VMB	MCF51JE256 ColdFire Microcontroller	256K/32K	81 MAPBGA	–40 to 105 °C
MCF51JE256VLK	MCF51JE256 ColdFire Microcontroller	256K/32K	80 LQFP	–40 to 105 °C
MCF51JE128VMB	MCF51JE128 ColdFire Microcontroller	128K/32K	81 MAPBGA	–40 to 105 °C
MCF51JE256CML	MCF51JE256 ColdFire Microcontroller	256K/32K	104 MAPBGA	–40 to 85 °C
MCF51JE256CLL	MCF51JE256 ColdFire Microcontroller	256K/32K	10O LQFP	–40 to 85 °C
MCF51JE256CMB	MCF51JE256 ColdFire Microcontroller	256K/32K	81 MAPBGA	–40 to 85 °C
MCF51JE256CLK	MCF51JE256 ColdFire Microcontroller	256K/32K	80 LQFP	–40 to 85 °C
MCF51JE128CMB	MCF51JE128 ColdFire Microcontroller	128K/32K	81 MAPBGA	–40 to 85 °C
MCF51JE128CLK	MCF51JE128 ColdFire Microcontroller	128K/32K	80 LQFP	–40 to 85 °C

4.2 Package Information

Table 28. Package Descriptions

Pin Count	Package Type	Abbreviation	Designator	Case No.	Document No.
100	Low Quad Flat Package	LQFP	LL	983-03	98ASS23308W
80	Low Quad Flat Package	LQFP	LK	1418	98ASS23174W
104	MAP BGA Package	MAPBGA	ML	1285-02	98ARH98267A
81	MAP BGA Package	MAPBGA	MB	1662-01	98ASA10670D

4.3 Mechanical Drawings

Table 28 provides the available package types and their document numbers. The latest package outline/mechanical drawings are available on the MCF51JE256/128 Product Summary pages at http://www.freescale.com.

To view the latest drawing, either:

- Click on the appropriate link in Table 28, or