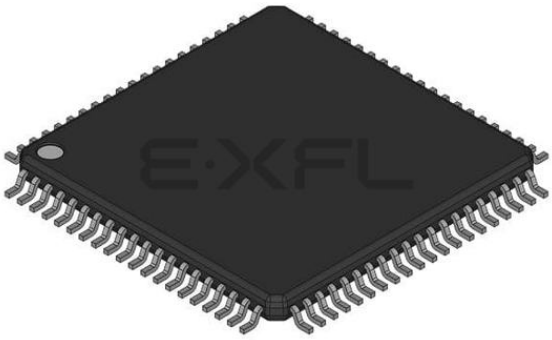

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	Coldfire V1
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	EBI/EMI, I²C, SCI, SPI, USB OTG
Peripherals	LVD, PWM, WDT
Number of I/O	47
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 12x12b; D/A 1x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcf51je256vlk

Table 2. MCF51JE256/128 Functional Units

Unit	Function
DAC (digital to analog converter)	Used to output voltage levels.
12-BIT SAR ADC (analog-to-digital converter)	Measures analog voltages at up to 12 bits of resolution. The ADC has up to 12 single-ended inputs.
PDB (Programmable Delay Block)	Precisely trigger the DAC FIFO buffer.
Mini-FlexBus	Provides expansion capability for off-chip memory and peripherals.
USB On-the-Go	Supports the USB On-the-Go dual-role controller.
CMT (Carrier Modulator Timer)	Infrared output used for the Remote Controller operation.
MCG (Multipurpose Clock Generator)	Provides clocking options for the device, including a phase-locked loop (PLL) and frequency-locked loop (FLL) for multiplying slower reference clock sources.
BDM (Background Debug Module)	Provides single pin debugging interface (part of the V1 ColdFire core).
CF1 CORE (V1 ColdFire Core)	Executes programs and interrupt handlers.
PRACMP	Analog comparators for comparing external analog signals against each other, or a variety of reference levels.
COP (Computer Operating Properly)	Software Watchdog.
IRQ (Interrupt Request)	Single-pin high-priority interrupt (part of the V1 ColdFire core).
CRC (Cyclic Redundancy Check)	High-speed CRC calculation.
DBG (Debug)	Provides debugging and emulation capabilities (part of the V1 ColdFire core).
FLASH (Flash Memory)	Provides storage for program code, constants, and variables.
IIC (Inter-integrated Circuits)	Supports standard IIC communications protocol and SMBus.
INTC (Interrupt Controller)	Controls and prioritizes all device interrupts.
KBI1 & KBI2	Keyboard Interfaces 1 and 2.
LVD (Low-voltage Detect)	Provides an interrupt to the ColdFire V1 CORE in the event that the supply voltage drops below a critical value. The LVD can also be programmed to reset the device upon a low voltage event.
VREF (Voltage Reference)	The Voltage Reference output is available for both on- and off-chip use.
RAM (Random-Access Memory)	Provides stack and variable storage.
RGPIO (Rapid General-purpose Input/output)	Allows for I/O port access at CPU clock speeds. RGPIO is used to implement GPIO functionality.
SCI1, SCI2 (Serial Communications Interfaces)	Serial communications UARTs capable of supporting RS-232 and LIN protocols.
SIM (system integration unit)	

Table 2. MCF51JE256/128 Functional Units (continued)

Unit	Function
SPI1 (FIFO), SPI2 (Serial Peripheral Interfaces)	SPI1 and SPI2 provide standard master/slave capability. SPI contains a FIFO buffer in order to increase the throughput for this peripheral.
TPM1, TPM2 (Timer/PWM Module)	Timer/PWM module can be used for a variety of generic timer operations as well as pulse-width modulation.
VREG (Voltage Regulator)	Controls power management across the device.
XOSC1 and XOSC2 (Crystal Oscillators)	These devices incorporate redundant crystal oscillators. One is intended primarily for use by the TOD, and the other by the CPU and other peripherals.

2 Pinouts and Pin Assignments

2.1 104-Pin MAPBGA

The following figure shows the 104-pin MAPBGA pinout configuration.

	1	2	3	4	5	6	7	8	9	10	11	
A	PTF6	PTF7	USB_DP	USB_DM	VUSB33	PTF4	PTF3	FB_AD12	PTJ7	PTJ5	PTJ4	A
B	PTG0	PTA0	PTG3	VBUS	PTF5	PTJ6	PTH0	PTE5	PTF0	PTF1	PTF2	B
C	IRO	PTG4	PTA6	PTG2	PTG6	PTG5	PTG7	PTH1	PTE4	PTE6	PTE7	C
D	PTA5	PTA4	PTB1	VDD1		VDD2		VDD3	PTA1	PTE3	PTE2	D
E	VSSA	PTA7	PTB0						PTA2	PTJ3	PTE1	E
F	VREFL			PTG1				PTC7	PTJ2	PTJ0	PTJ1	F
G	ADP2								PTD5	PTD7	PTE0	G
H			PTA3	VSS1		VSS2		VSS3	PTD4	PTD3	PTD2	H
J	ADP0		PTH7	PTH6	PTH4	PTH3	PTH2	PTD6	PTC2	PTC0	PTC1	J
K			ADP1	PTH5	PTB6	PTB7	PTC3	PTD1	PTC4	PTC5	PTC6	K
L	ADP3	DACO		VREFO	VREFH	VDDA	PTB3	PTB2	PTD0	PTB5	PTB4	L
	1	2	3	4	5	6	7	8	9	10	11	

Figure 2. 104-Pin MAPBGA

2.5 Pin Assignments

Table 3. Package Pin Assignments

Package				Default Function	Alternate 1	Alternate 2	Alternate 3	Composite Pin Name
104 MAPBGA	100 LQFP	81 MAPBGA	80 LQFP					
B2	1	B2	1	PTA0	FB_D2	$\overline{SS1}$	—	PTA0/FB_D2/$\overline{SS1}$
C1	2	A1	2	IRO	—	—	—	IRO
C6	3	—	—	PTG5	FB_$\overline{RW}$	—	—	PTG5/FB_$\overline{RW}$
C5	4	—	—	PTG6	FB_AD19	—	—	PTG6/FB_AD19
C7	5	—	—	PTG7	FB_AD18	—	—	PTG7/FB_AD18
B7	6	—	—	PTH0	$\overline{FB\_OE}$	—	—	PTH0/$\overline{FB\_OE}$
C8	7	—	—	PTH1	FB_D0	—	—	PTH1/FB_D0
D9	8	C4	3	PTA1	KBI1P0	TX1	FB_D1	PTA1/KBI1P0/TX1/FB_D1
E9	9	D5	4	PTA2	KBI1P1	RX1	ADP4	PTA2/KBI1P1/RX1/ADP4
H3	10	D6	5	PTA3	KBI1P2	FB_D6	ADP5	PTA3/KBI1P2/FB_D6/ADP5
D2	11	C1	6	PTA4	—	—	—	PTA4
D1	12	C2	7	PTA5	—	—	—	PTA5
C3	13	C3	8	PTA6	—	—	—	PTA6
E2	14	D2	9	PTA7	—	—	—	PTA7
E3	15	D3	10	PTB0	—	—	—	PTB0
D3	16	D4	11	PTB1	$\overline{BLMS}$	—	—	PTB1/$\overline{BLMS}$
E1	17	J1	12	VSSA	—	—	—	VSSA
F1	18	J2	13	VREFL	—	—	—	VREFL
F2	19	D1	19	—	—	—	—	NC
G2	20	E2	15	—	—	—	—	NC
G1	21	F2	16	ADP2	—	—	—	ADP2
H1	22	F1	17	—	—	—	—	NC
H2	23	E2	18	NC	—	—	—	NC
F3	24	F3	19	—	—	—	—	NC
G3	25	E3	20	—	—	—	—	NC
L2	26	G2	21	DACO	—	—	—	DACO
L1	27	G3	22	ADP3	—	—	—	ADP3
K1	28	H4	23	—	—	—	—	NC
K2	29	G4	24	NC	—	—	—	NC
J1	30	G1	25	ADP0	—	—	—	ADP0
J2	31	H1	26	—	—	—	—	NC
L4	32	G5	27	VREFO	—	—	—	VREFO
K3	33	H3	28	ADP1	—	—	—	ADP1
L3	34	H2	29	NC	—	—	—	NC

Table 3. Package Pin Assignments (continued)

Package				Default Function	Alternate 1	Alternate 2	Alternate 3	Composite Pin Name
104 MAPBGA	100 LQFP	81 MAPBGA	80 LQFP					
G10	66	D8	55	PTD7	USB_PULLUP(D+)	RX1	—	PTD7/USB_PULLUP(D+) /RX1
G11	67	D9	56	PTE0	KBI2P3	FB_ALE	FB_CS1	PTE0/KBI2P3/FB_ALE/ FB_CS1
F10	68	—	—	PTJ0	FB_AD2	—	—	PTJ0/FB_AD2
F11	69	—	—	PTJ1	FB_AD3	—	—	PTJ1/FB_AD3
F9	70	—	—	PTJ2	FB_AD4	—	—	PTJ2/FB_AD4
E10	71	—	—	PTJ3	RGPIOP12	FB_AD5	—	PTJ3/RGPIOP12/FB_AD5
E11	72	C9	57	PTE1	KBI2P4	RGPIOP13	FB_AD6	PTE1/KBI2P4/RGPIOP13/ FB_AD6
D11	73	C8	58	PTE2	KBI2P5	RGPIOP14	FB_AD7	PTE2/KBI2P5/RGPIOP14/ FB_AD7
D10	74	B9	59	PTE3	KBI2P6	FB_AD8	—	PTE3/KBI2P6/FB_AD8
C9	75	A9	60	PTE4	CMPP3	TPMCLK	IRQ	PTE4/CMPP3/TPMCLK/VPP/ IRQ
H8	76	F5	61	VSS3	—	—	—	VSS3
D8	77	E5	62	VDD3	—	—	—	VDD3
B8	78	C7	63	PTE5	FB_D7	USB_ SESSVLD	TX2	PTE5/FB_D7/USB_SESSVLD/ TX2
C10	79	C6	64	PTE6	FB_$\overline{RW}$	USB_ SESSEND	RX2	PTE6/FB_RW_b/ USB_SESSEND/RX2
C11	80	B6	65	PTE7	USB_VBUSVLD	TPM2CH3	—	PTE7/USB_VBUSVLD/ TPM2CH3
B9	81	B8	66	PTF0	USB_ID	TPM2CH2	—	PTF0/USB_ID/TPM2CH2
B10	82	B7	67	PTF1	RX2	USB_DP_ DOWN	TPM2CH1	PTF1/RX2/USB_DP_DOWN/ TPM2CH1
B11	83	C5	68	PTF2	TX2	USB_DM_ DOWN	TPM2CH0	PTF2/TX2/USB_DM_DOWN/ TPM2CH0
A11	84	—	—	PTJ4	RGPIOP15	FB_AD16	—	PTJ4/RGPIOP15/FB_AD16
A10	85	—	—	PTJ5	FB_AD15	—	—	PTJ5/FB_AD15
B6	86	—	—	PTJ6	FB_AD14	—	—	PTJ6/FB_AD14
A9	87	—	—	PTJ7	FB_AD13	—	—	PTJ7/FB_AD13
A8	88	—	—	FB_AD12	—	—	—	FB_AD12
A7	89	A8	69	PTF3	SCL	FB_D5	FB_AD11	PTF3/SCL/FB_D5/FB_AD11
A6	90	A7	70	PTF4	SDA	FB_D4	FB_AD10	PTF4/SDA/FB_D4/FB_AD10
B5	91	B5	71	PTF5	KBI2P7	FB_D3	FB_AD9	PTF5/KBI2P7/FB_D3/FB_AD9
A5	92	A6	72	VUSB33	—	—	—	VUSB33
A4	93	B4	73	USB_DM	—	—	—	USB_DM
A3	94	A4	74	USB_DP	—	—	—	USB_DP
B4	95	A5	75	VBUS	—	—	—	VBUS

Table 5. Absolute Maximum Ratings

#	Rating	Symbol	Value	Unit
1	Supply voltage	V_{DD}	–0.3 to 3.8	V
2	Maximum current into V_{DD}	I_{DD}	120	mA
3	Digital Input voltage	V_{In}	–0.3 to V_{DD} + 0.3	V
4	Instantaneous maximum current Single pin limit (applies to all port pins)[1, 2, 3]	I_D	±25	mA
5	Storage temperature range	T_{stg}	–55 to 150	°C

1 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive (V_{DD}) and negative (V_{SS}) clamp voltages, then use the larger of the two resistance values.

2 All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.

3 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low (which would reduce overall power consumption).

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}).

3.3 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and it is user-determined rather than being controlled by the MCU design. In order to take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

where K is a constant pertaining to the particular part. K can be determined from Equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A.

3.4 ESD Protection Characteristics

Although damage from static discharge is much less common on these devices than on early CMOS circuits, normal handling precautions should be used to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with CDF-AEC-Q00 Stress Test Qualification for Automotive Grade Integrated Circuits. (http://www.aecouncil.com/) This device was qualified to AEC-Q100 Rev E.

A device is considered to have failed if, after exposure to ESD pulses, the device no longer meets the device specification requirements. Complete dc parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table 7. ESD and Latch-up Test Conditions

Model	Description	Symbol	Value	Unit
Human Body	Series Resistance	R1	1500	Ω
	Storage Capacitance	C	100	pF
	Number of Pulse per pin	—	3	—
Machine	Series Resistance	R1	0	Ω
	Storage Capacitance	C	200	pF
	Number of Pulse per pin	—	3	—
Latch-up	Minimum input voltage limit	—	–2.5	V
	Maximum input voltage limit	—	7.5	V

Table 8. ESD and Latch-Up Protection Characteristics

#	Rating	Symbol	Minimum	Maximum	Unit	C
1	Human Body Model (HBM)	V_{HBM}	±2000	—	V	T
2	Machine Model (MM)	V_{MM}	±200	—	V	T
3	Charge Device Model (CDM)	V_{CDM}	±500	—	V	T
4	Latch-up Current at T_A = 125°C	I_{LAT}	±100	—	mA	T

3.5 DC Characteristics

This section includes information about power supply requirements, I/O pin characteristics, and power supply current in various operating modes.

Table 9. DC Characteristics (continued)

#	Symbol	Characteristic	Condition	Minimum	Typical[1]	Maximum	Unit	C
11	R_{PU}	Pull-up resistors all digital inputs, when enabled	—	17.5	—	52.5	kΩ	P
12	R_{PD}	Internal pull-down resistors[4]	—	17.5	—	52.5	kΩ	P
13	I_{IC}	DC injection current [5, 6, 7] — Single pin limit	$V_{SS} > V_{IN} > V_{DD}$	–0.2	—	0.2	mA	D
		DC injection current [5, 6, 7] — Total MCU limit, includes sum of all stressed pins	$V_{SS} > V_{IN} > V_{DD}$	–5	—	5	mA	D
14	C_{In}	Input Capacitance, all pins	—	—	—	8	pF	C
15	V_{RAM}	RAM retention voltage	—	—	0.6	1.0	V	C
16	V_{POR}	POR re-arm voltage[8]	—	0.9	1.4	1.79	V	C
17	t_{POR}	POR re-arm time	—	10	—	—	µs	D
18	V_{LVDH}	Low-voltage detection threshold — high range[9]						
			V_{DD} falling	2.11	2.16	2.22	V	P
			V_{DD} rising	2.16	2.21	2.27	V	P
19	V_{LVDL}	Low-voltage detection threshold — low range[9]						
			V_{DD} falling	1.80	1.82	1.91	V	P
			V_{DD} rising	1.86	1.90	1.99	V	P
20	V_{LVWH}	Low-voltage warning threshold — high range[9]						
			V_{DD} falling	2.36	2.46	2.56	V	P
			V_{DD} rising	2.36	2.46	2.56	V	P
21	V_{LVWL}	Low-voltage warning threshold — low range[9]						
			V_{DD} falling	2.11	2.16	2.22	V	P
			V_{DD} rising	2.16	2.21	2.27	V	P
22	V_{hys}	Low-voltage inhibit reset/recover hysteresis[10]	—	—	50	—	mV	C
23	V_{BG}	Bandgap Voltage Reference[11]	—	1.145	1.17	1.195	V	P

1 Typical values are measured at 25°C. Characterized, not tested

2 As the supply voltage rises, the LVD circuit will hold the MCU in reset until the supply has risen above V_{LVDL}.

3 Does not include analog module pins. Dedicated analog pins should not be pulled to VDD or VSS and should be left floating when not used to reduce current leakage.

4 Measured with $V_{In} = V_{DD}$.

5 All functional non-supply pins are internally clamped to V_{SS} and V_{DD},except PTD1.

6 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

7 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).

[8] Maximum is highest voltage that POR is guaranteed.
[9] Run at 1 MHz bus frequency.
[10] Low voltage detection and warning limits measured at 1 MHz bus frequency.
[11] Factory trimmed at V_{DD} = 3.0 V, Temp = 25°C.

3.6 Supply Current Characteristics

Table 10. Supply Current Characteristics

#	Symbol	Parameter	Bus Freq	V_{DD} (V)	Typical[1]	Maximum	Unit	Temperature (°C)	C
1	RI_{DD}	Run supply current FEI mode, all modules ON[2]							
			25.165 MHz	3	44	48	mA	–40 to 25	P
			25.165 MHz	3	44	48	mA	105	P
			20 MHz	3	32.3	—	mA	–40 to 105	T
			8 MHz	3	16.4	—	mA	–40 to 105	T
			1 MHz	3	2.9	—	mA	–40 to 105	T
2	RI_{DD}	Run supply current FEI mode, all modules OFF[3]							
			25.165 MHz	3	29	29.6	mA	–40 to 105	C
			20 MHz	3	25.4	—	mA	–40 to 105	T
			8 MHz	3	12.7	—	mA	–40 to 105	T
			1 MHz	3	2.4	—	mA	–40 to 105	T
3	RI_{DD}	Run supply current LPR=0, all modules OFF[3]							
			16 kHz FBI	3	232	280	μA	–40 to 105	T
			16 kHz FBE	3	231	296	μA	–40 to 105	T
4	RI_{DD}	Run supply current LPR=1, all modules OFF[3]							
			16 kHz BLPE	3	74	75	μA	0 to 70	T
			16 kHz BLPE	3	74	120	μA	–40 to 105	T
5	WI_{DD}	Wait mode supply current FEI mode, all modules OFF[3]							
			25.165 MHz	3	16.5	—	mA	–-40 to 105	C
			20 MHz	3	10.3	—	mA	–-40 to 105	T
			8 MHz	3	6.6	—	mA	–-40 to 105	T
			1 MHz	3	1.7	—	mA	–-40 to 105	T

Table 15. 12-bit ADC Operating Conditions (continued)

#	Symb	Characteristic	Conditions	Minimum	Typical[1]	Maximum	Unit	C
5	V_{REFL}	Ref Voltage Low	—	V_{SSAD}	V_{SSAD}	V_{SSAD}	V	D
6	V_{ADIN}	Input Voltage	—	V_{REFL}	—	V_{REFH}	V	D
7	C_{ADIN}	Input Capacitance	—	—	4	5	pF	C
8	R_{ADIN}	Input Resistance	—	—	2	5	kΩ	C
9	R_{AS}	Analog Source Resistance[3]						
			12 bit mode f_{ADCK} > 8 MHz	—	—	1	kΩ	C
			4 MHz < f_{ADCK} > 8 MHz	—	—	2	kΩ	C
			f_{ADCK} < 4 MHz	—	—	5	kΩ	C
			10-bit mode f_{ADCK} > 8MHz	—	—	2	kΩ	C
			4 MHz < f_{ADCK} < 8 MHz	—	—	5	kΩ	C
			f_{ADCK} < 4 MHz	—	—	10	kΩ	C
			8-bit mode f_{ADCK} > 8 MHz	—	—	5	kΩ	C
			f_{ADCK} < 8 MHz	—	—	10	kΩ	C
10	f_{ADCK}	ADC Conversion Clock Freq.						
			High Speed (ADLPC=0, ADHSC=1)	1.0	—	8.0	MHz	D
			High Speed (ADLPC=0, ADHSC=0)	1.0	—	5.0	MHz	D
			Low Power (ADLPC=1, ADHSC=1)	1.0	—	2.5	MHz	D

1 Typical values assume V_{DDAD} = 3.0V, Temp = 25°C, f_{ADCK}=1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 DC potential difference.

3 External to MCU. Assumes ADLSMP=0.

Table 16. 12-bit SAR ADC Characteristics full operating range (V_{REFH} = V_{DDAD}, V_{REFL} = V_{SSAD}) (continued)

#	Symbol	Characteristic	Conditions[1]	Minimum	Typical[2]	Maximum	Unit	C
7	INL	Integral Non-Linearity	12-bit single-ended mode	—	±1.0	±2.5	LSB[3]	T
			10-bit single-ended mode	—	±0.5	±1.0	LSB[3]	T
			8-bit single-ended mode	—	±0.3	±0.5	LSB[3]	T
8	E_{ZS}	Zero-Scale Error (V_{ADIN} = V_{SSAD})	12-bit single-ended mode	—	±0.7	±2.0	LSB[3]	T
			10-bit single-ended mode	—	±0.4	±1.0	LSB[3]	T
			8-bit single-ended mode	—	±0.2	±0.5	LSB[3]	T
9	E_{FS}	Full-Scale Error (V_{ADIN} = V_{DDAD})	12-bit single-ended mode	—	±1.0	±3.5	LSB[3]	T
			10-bit single-ended mode	—	±0.4	±1.5	LSB[3]	T
			8-bit single-ended mode	—	±0.2	±0.5	LSB[3]	T
10	E_Q	Quantization Error	All modes	—	—	±0.5	LSB[3]	D
11	E_{IL}	Input Leakage Error (I_{In} = leakage current (refer to DC Characteristics)	All modes	I_{In} * R_{AS}			mV	D
12	m	Temp Sensor Slope	-40°C to 25°C	—	1.646	—	mV/xC	C
			25°C to 125°C	—	1.769	—	mV/xC	C
13	V_{TEMP25}	Temp Sensor Voltage	25°C	—	701.2	—	mV	C

1 All accuracy numbers assume the ADC is calibrated with V_{REFH}=V_{DDAD}.

2 Typical values assume V_{DDAD} = 3.0V, Temp = 25°C, f_{ADCK}=2.0MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

3 1 LSB = (V_{REFH} - V_{REFL})/2^N

3.10 MCG and External Oscillator (XOSC) Characteristics

Table 17. MCG (Temperature Range = –40 to 105°C Ambient)

#	Rating		Symbol	Min	Typical	Max	Unit	C
1	Internal reference startup time		t_{irefst}	—	55	100	µs	D
2	Average internal reference frequency	factory trimmed at VDD=3.0V and temp=25°C	f_{int_ft}	—	31.25	—	kHz	C
		user trimmed		31.25	—	39.0625	KHz	C
3	DCO output frequency range - trimmed	Low range (DRS=00)	f_{dco_t}	16	—	20	MHz	C
		Mid range (DRS=01)		32	—	40	MHz	C
		High range[1] (DRS=10)		40	—	60	MHz	C
4	Resolution of trimmed DCO output frequency at fixed voltage and temperature	with FTRIM	$\Delta f_{dco\_res\_t}$	—	± 0.1	± 0.2	$\%f_{dco}$	C
		without FTRIM		—	± 0.2	± 0.4	$\%f_{dco}$	C

Table 17. MCG (Temperature Range = –40 to 105°C Ambient) (continued)

#	Rating		Symbol	Min	Typical	Max	Unit	C
5	Total deviation of trimmed DCO output frequency over voltage and temperature	over voltage and temperature	Δf_{dco_t}	—	± 1.0	± 2	$\%f_{dco}$	P
		over fixed voltage and temp range of 0 - 70 °C		—	± 0.5	± 1	$\%f_{dco}$	C
6	Acquisition time	FLL[2]	$t_{fll\_acquire}$	—	—	1	ms	C
		PLL[3]	$t_{pll\_acquire}$	—	—	1	ms	D
7	Long term Jitter of DCO output clock (averaged over 2mS interval) [4]		C_{Jitter}	—	0.02	0.2	$\%f_{dco}$	C
8	VCO operating frequency		f_{vco}	7.0	—	55.0	MHz	D
9	PLL reference frequency range		f_{pll_ref}	1.0	—	2.0	MHz	D
10	Jitter of PLL output clock measured over 625 ns	Long term	$f_{pll\_jitter\_625\ ns}$	—	0.566[4]	—	%fpll	D
11	Lock frequency tolerance	Entry[5]	D_{lock}	± 1.49	—	± 2.98	%	D
		Exit[6]	D_{unl}	± 4.47	—	± 5.97	%	D
12	Lock time	FLL	t_{fll_lock}	—	—	$t_{fll\_acquire}$+ 1075(1/f_{int_t})	s	D
		PLL	t_{pll_lock}	—	—	$t_{pll\_acquire}$+ 1075(1/f_{pll_ref})	s	D
13	Loss of external clock minimum frequency - RANGE = 0		f_{loc_low}	(3/5) x f_{int_t}	—	—	kHz	D
14	Loss of external clock minimum frequency - RANGE = 1		f_{loc_high}	(16/5) x f_{int_t}	—	—	kHz	D

1 This should not exceed the maximum CPU frequency of 50.33 MHz.

2 This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bit is changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

3 This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

4 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{BUS}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

5 Below D_{lock} minimum, the MCG is guaranteed to enter lock. Above D_{lock} maximum, the MCG will not enter lock. But if the MCG is already in lock, then the MCG may stay in lock.

6 Below D_{unl} minimum, the MCG will not exit lock if already in lock. Above D_{unl} maximum, the MCG is guaranteed to exit lock.

Table 18. XOSC (Temperature Range = –40 to 105°C Ambient)

#	Characteristic		Symbol	Minimum	Typical[1]	Maximum	Unit
1	Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1)	• Low range (RANGE = 0)	f_{lo}	32	—	38.4	kHz
		• High range (RANGE = 1), • FEE or FBE mode [2]	f_{hi-fll}	1	—	5	MHz
		• High range (RANGE = 1), • PEE or PBE mode [3]	f_{hi-pll}	1	—	16	MHz
		• High range (RANGE = 1), • High gain (HGO = 1), • FBELP mode	f_{hi-hgo}	1	—	16	MHz
		• High range (RANGE = 1), • Low power (HGO = 0), • FBELP mode	f_{hi-lp}	1	—	8	MHz
2	Load capacitors		C_1 C_2	See Note [4]			
3	Feedback resistor	Low range (32 kHz to 38.4 kHz)	R_F	—	10	—	MΩ
		High range (1 MHz to 16 MHz)	—	—	1	—	
4	Series resistor — Low range	Low Gain (HGO = 0)	R_S	—	0	—	kΩ
		High Gain (HGO = 1)		—	100	—	
5	Series resistor — High range	• Low Gain (HGO = 0)	R_S	—	0	—	kΩ
		• High Gain (HGO = 1)					
		≥ 8 MHz		—	0	0	
		4 MHz		—	0	10	
		1 MHz		—	0	20	
6	Crystal start-up time [5, 6]	Low range, low gain (RANGE=0,HGO=0)	t_{CSTL}	—	200	—	ms
		Low range, high gain (RANGE=0,HGO=1)		—	400	—	
		High range, low gain (RANGE=1,HGO=0)	t_{CSTH}	—	5	—	
		High range, high gain (RANGE=1, HGO=1)		—	15	—	

1 Data in Typical column was characterized at 3.0 V, 25°C or is typical recommended value.

2 When MCG is configured for FEE or FBE mode, input clock source must be divisible using RDIV to within the range of 31.25 kHz to 39.0625 kHz.

3 When MCG is configured for PEE or PBE mode, input clock source must be divisible using RDIV to within the range of 1 MHz to 2 MHz.

4 See crystal or resonator manufacturer's recommendation.

5 This parameter is characterized and not tested on each device.

6 Proper PC board layout procedures must be followed to achieve specifications.

3.11 Mini-FlexBus Timing Specifications

A multi-function external bus interface called Mini-FlexBus is provided with basic functionality to interface to slave-only devices up to a maximum bus frequency of 25.1666 MHz. It can be directly connected to asynchronous or synchronous devices such as external boot ROMs, flash memories, gate-array logic, or other simple target (slave) devices with little or no additional circuitry. For asynchronous devices, a simple chip-select based interface can be used.

All processor bus timings are synchronous; that is, input setup/hold and output delay are given in respect to the rising edge of a reference clock, MB_CLK. The MB_CLK frequency is half the internal system bus frequency.

The following timing numbers indicate when data is latched or driven onto the external bus, relative to the Mini-FlexBus output clock (MB_CLK). All other timing relationships can be derived from these values.

Table 19. Mini-FlexBus AC Timing Specifications

#	Characteristic	Symbol	Min	Max	Unit	C
1	Frequency of Operation	—	—	25.1666	MHz	—
2	Clock Period	MB1	39.73	—	ns	D
3	Output Valid[1]	MB2	—	20	ns	T
4	Output Hold[1]	MB3	1.0	—	ns	D
5	Input Setup[2]	MB4	22	—	ns	T
6	Input Hold[2]	MB5	10	—	ns	D

1 Specification is valid for all MB_A[19:0], MB_D[7:0], $\overline{\text{MB\_CS}}$[1:0], $\overline{\text{MB\_OE}}$, MB_R/$\overline{\text{W}}$, and MB_ALE.

2 Specification is valid for all MB_D[7:0].

Figure 9. Mini-FlexBus Read Timing

Figure 10. Mini-FlexBus Write Timing

3.12 AC Characteristics

This section describes ac timing characteristics for each peripheral system.

3.12.1 Control Timing

Table 20. Control Timing

#	Parameter		Symbol	Minimum	Typical[1]	Maximum	Unit	C
1	Bus frequency ($t_{cyc} = 1/f_{Bus}$)							
		$V_{DD} \geq 1.8$ V	f_{Bus}	dc	—	10	MHz	D
		$V_{DD} > 2.1$ V	f_{Bus}	dc	—	20	MHz	D
		$V_{DD} > 2.4$ V	f_{Bus}	dc	—	25.165	MHz	D
2	Internal low-power oscillator period		t_{LPO}	700	1000	1300	µs	P
3	External reset pulse width[2]	($t_{cyc} = 1/f_{Self\_reset}$)	t_{extrst}	100	—	—	ns	D
4	Reset low drive		t_{rstdrv}	66 x t_{cyc}	—	—	ns	D
5	Active background debug mode	latch setup time	t_{MSSU}	500	—	—	ns	D
6	Active background debug mode	latch hold time	t_{MSH}	100	—	—	ns	D
7	IRQ pulse width • Asynchronous path[2] • Synchronous path[3]		t_{ILIH}, t_{IHIL}	100 1.5 x t_{cyc}	—	—	ns	D
8	KBIPx pulse width • Asynchronous path[2] • Synchronous path[3]		t_{ILIH}, t_{IHIL}	100 1.5 x t_{cyc}	—	—	ns	D
9	Port rise and fall time (load = 50 pF)[4], Low Drive							
		Slew rate control disabled (PTxSE = 0)	t_{Rise}, t_{Fall}	—	11	—	ns	D
		Slew rate control enabled (PTxSE = 1)	t_{Rise}, t_{Fall}	—	35	—	ns	D
		Slew rate control disabled (PTxSE = 0)	t_{Rise}, t_{Fall}	—	40	—	ns	D
		Slew rate control enabled (PTxSE = 1)	t_{Rise}, t_{Fall}	—	75	—	ns	D

1 Typical values are based on characterization data at V_{DD} = 5.0 V, 25 °C unless otherwise stated.

2 This is the shortest pulse that is guaranteed to be recognized as a reset pin request. Shorter pulses are not guaranteed to override reset requests from internal sources.

3 This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized in that case.

4 Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range –40 °C to 105 °C.

3.12.2 TPM Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 21. TPM Input Timing

#	C	Function	Symbol	Minimum	Maximum	Unit
1	—	External clock frequency	f_{TPMext}	dc	$f_{Bus}/4$	MHz
2	—	External clock period	t_{TPMext}	4	—	t_{cyc}
3	D	External clock high time	t_{clkh}	1.5	—	t_{cyc}
4	D	External clock low time	t_{clkl}	1.5	—	t_{cyc}
5	D	Input capture pulse width	t_{ICPW}	1.5	—	t_{cyc}

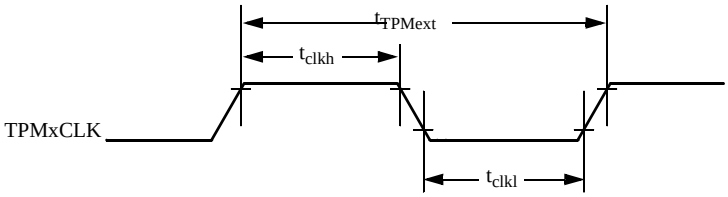

Figure 13. Timer External Clock

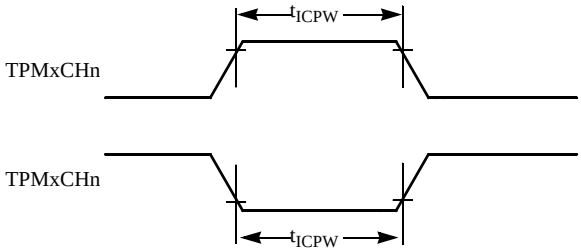

Figure 14. Timer Input Capture Pulse

3.13 SPI Characteristics

The following table and Figure 15 through Figure 18 describe the timing requirements for the SPI system.

Table 22. SPI Timing

No.[1]	Characteristic[2]	Symbol	Minimum	Maximum	Unit	C
1	Operating frequency Master Slave	 f_{op} f_{op}	 $f_{Bus}/2048$ 0	 $f_{Bus}/2$ $f_{Bus}/4$	 Hz Hz	D
2	SPSCK period Master Slave	 t_{SPSCK} t_{SPSCK}	 2 4	 2048 —	 t_{cyc} t_{cyc}	D
3	Enable lead time Master Slave	 t_{Lead} t_{Lead}	 1/2 1	 — —	 t_{SPSCK} t_{cyc}	D
4	Enable lag time Master Slave	 t_{Lag} t_{Lag}	 1/2 1	 — —	 t_{SPSCK} t_{cyc}	D
5	Clock (SPSCK) high or low time Master Slave	 t_{WSPSCK} t_{WSPSCK}	 $t_{cyc} - 30$ $t_{cyc} - 30$	 1024 t_{cyc} —	 ns ns	D
6	Data setup time (inputs) Master Slave	 t_{SU} t_{SU}	 15 15	 — —	 ns ns	D
7	Data hold time (inputs) Master Slave	 t_{HI} t_{HI}	 0 25	 — —	 ns ns	D
8	Slave access time[3]	t_a	—	1	t_{cyc}	D
9	Slave MISO disable time[4]	t_{dis}	—	1	t_{cyc}	D
10	Data valid (after SPSCK edge) Master Slave	 t_v t_v	 — —	 25 25	 ns ns	D
11	Data hold time (outputs) Master Slave	 t_{HO} t_{HO}	 0 0	 — —	 ns ns	D
12	Rise time Input Output	 t_{RI} t_{RO}	 — —	 $t_{cyc} - 25$ 25	 ns ns	D
13	Fall time Input Output	 t_{FI} t_{FO}	 — —	 $t_{cyc} - 25$ 25	 ns ns	D

1 Numbers in this column identify elements in Figure 15 through Figure 18**.**

2 All timing is shown with respect to 20% V_{DD} and 70% V_{DD}, unless noted; 100 pF load on all SPI pins. All timing assumes slew rate control disabled and high drive strength enabled for SPI output pins.

3 Time to data active from high-impedance state.

4 Hold time to high-impedance state.

3.14 Flash Specifications

This section provides details about program/erase times and program-erase endurance for the Flash memory.

Program and erase operations do not require any special power sources other than the normal V_{DD} supply. For more detailed information about program/erase operations, see the Memory chapter in the Reference Manual for this device (MCF51JE256RM).

Table 23. Flash Characteristics

#	Characteristic	Symbol	Minimum	Typical	Maximum	Unit	C
1	Supply voltage for program/erase -40°C to 105°C	$V_{prog/erase}$	1.8	—	3.6	V	D
2	Supply voltage for read operation	V_{Read}	1.8	—	3.6	V	D
3	Internal FCLK frequency[1]	f_{FCLK}	150	—	200	kHz	D
4	Internal FCLK period (1/FCLK)	t_{Fcyc}	5	—	6.67	µs	D
5	Byte program time (random location)[2]	t_{prog}	9			t_{Fcyc}	P
6	Byte program time (burst mode)[2]	t_{Burst}	4			t_{Fcyc}	P
7	Page erase time[2]	t_{Page}	4000			t_{Fcyc}	P
8	Mass erase time[2]	t_{Mass}	20,000			t_{Fcyc}	P
9	Program/erase endurance[3] T_L to T_H = –40°C to + 105°C T = 25°C		10,000 —	— 100,000	— —	cycles	C
10	Data retention[4]	t_{D_ret}	15	100	—	years	C

1 The frequency of this clock is controlled by a software setting.

2 These values are hardware state machine controlled. User code does not need to count cycles. This information supplied for calculating approximate time to program and erase.

3 **Typical endurance for flash** was evaluated for this product family on the HC9S12Dx64. For additional information on how Freescale defines typical endurance, please refer to Engineering Bulletin EB619, *Typical Endurance for Nonvolatile Memory.*

4 **Typical data retention** values are based on intrinsic capability of the technology measured at high temperature and de-rated to 25°C using the Arrhenius equation. For additional information on how Freescale defines typical data retention, please refer to Engineering Bulletin EB618, *Typical Data Retention for Nonvolatile Memory.*

3.15 USB Electricals

The USB electricals for the USB On-the-Go module conform to the standards documented by the Universal Serial Bus Implementers Forum. For the most up-to-date standards, visit http://www.usb.org.

If the Freescale USB On-the-Go implementation has electrical characteristics that deviate from the standard or require additional information, this space would be used to communicate that information.

Table 24. Internal USB 3.3 V Voltage Regulator Characteristics

#	Characteristic	Symbol	Minimum	Typical	Maximum	Unit	C
1	Regulator operating voltage	V_{regin}	3.9	—	5.5	V	C
2	VREG output	V_{regout}	3	3.3	3.75	V	P

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ARCO Tower 15F
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Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
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Asia/Pacific:
Freescale Semiconductor China Ltd.
Exchange Building 23F
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Beijing 100022
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