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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	Coldfire V1
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	EBI/EMI, I²C, SCI, SPI, USB OTG
Peripherals	LVD, PWM, WDT
Number of I/O	65
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 12x12b; D/A 1x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcf51je256vll

Table 2. MCF51JE256/128 Functional Units

Unit	Function
DAC (digital to analog converter)	Used to output voltage levels.
12-BIT SAR ADC (analog-to-digital converter)	Measures analog voltages at up to 12 bits of resolution. The ADC has up to 12 single-ended inputs.
PDB (Programmable Delay Block)	Precisely trigger the DAC FIFO buffer.
Mini-FlexBus	Provides expansion capability for off-chip memory and peripherals.
USB On-the-Go	Supports the USB On-the-Go dual-role controller.
CMT (Carrier Modulator Timer)	Infrared output used for the Remote Controller operation.
MCG (Multipurpose Clock Generator)	Provides clocking options for the device, including a phase-locked loop (PLL) and frequency-locked loop (FLL) for multiplying slower reference clock sources.
BDM (Background Debug Module)	Provides single pin debugging interface (part of the V1 ColdFire core).
CF1 CORE (V1 ColdFire Core)	Executes programs and interrupt handlers.
PRACMP	Analog comparators for comparing external analog signals against each other, or a variety of reference levels.
COP (Computer Operating Properly)	Software Watchdog.
IRQ (Interrupt Request)	Single-pin high-priority interrupt (part of the V1 ColdFire core).
CRC (Cyclic Redundancy Check)	High-speed CRC calculation.
DBG (Debug)	Provides debugging and emulation capabilities (part of the V1 ColdFire core).
FLASH (Flash Memory)	Provides storage for program code, constants, and variables.
IIC (Inter-integrated Circuits)	Supports standard IIC communications protocol and SMBus.
INTC (Interrupt Controller)	Controls and prioritizes all device interrupts.
KBI1 & KBI2	Keyboard Interfaces 1 and 2.
LVD (Low-voltage Detect)	Provides an interrupt to the ColdFire V1 CORE in the event that the supply voltage drops below a critical value. The LVD can also be programmed to reset the device upon a low voltage event.
VREF (Voltage Reference)	The Voltage Reference output is available for both on- and off-chip use.
RAM (Random-Access Memory)	Provides stack and variable storage.
RGPIO (Rapid General-purpose Input/output)	Allows for I/O port access at CPU clock speeds. RGPIO is used to implement GPIO functionality.
SCI1, SCI2 (Serial Communications Interfaces)	Serial communications UARTs capable of supporting RS-232 and LIN protocols.
SIM (system integration unit)	

2 Pinouts and Pin Assignments

2.1 104-Pin MAPBGA

The following figure shows the 104-pin MAPBGA pinout configuration.

	1	2	3	4	5	6	7	8	9	10	11	
A	PTF6	PTF7	USB_DP	USB_DM	VUSB33	PTF4	PTF3	FB_AD12	PTJ7	PTJ5	PTJ4	A
B	PTG0	PTA0	PTG3	VBUS	PTF5	PTJ6	PTH0	PTE5	PTF0	PTF1	PTF2	B
C	IRO	PTG4	PTA6	PTG2	PTG6	PTG5	PTG7	PTH1	PTE4	PTE6	PTE7	C
D	PTA5	PTA4	PTB1	VDD1		VDD2		VDD3	PTA1	PTE3	PTE2	D
E	VSSA	PTA7	PTB0						PTA2	PTJ3	PTE1	E
F	VREFL			PTG1				PTC7	PTJ2	PTJ0	PTJ1	F
G	ADP2								PTD5	PTD7	PTE0	G
H			PTA3	VSS1		VSS2		VSS3	PTD4	PTD3	PTD2	H
J	ADP0		PTH7	PTH6	PTH4	PTH3	PTH2	PTD6	PTC2	PTC0	PTC1	J
K			ADP1	PTH5	PTB6	PTB7	PTC3	PTD1	PTC4	PTC5	PTC6	K
L	ADP3	DACO		VREFO	VREFH	VDDA	PTB3	PTB2	PTD0	PTB5	PTB4	L
	1	2	3	4	5	6	7	8	9	10	11	

Figure 2. 104-Pin MAPBGA

2.3 81-Pin MAPBGA

The following figure shows the 81-pin MAPBGA pinout configuration.

	1	2	3	4	5	6	7	8	9	
A	IRO	PTG0	PTF6	USB_DP	VBUS	VUSB33	PTF4	PTF3	PTE4	A
B	PTF7	PTA0	PTG1	USB_DM	PTF5	PTE7	PTF1	PTF0	PTE3	B
C	PTA4	PTA5	PTA6	PTA1	PTF2	PTE6	PTE5	PTE2	PTE1	C
D		PTA7	PTB0	PTB1	PTA2	PTA3	PTD5	PTD7	PTE0	D
E				VDD2	VDD3	VDD1	PTD2	PTD3	PTD6	E
F		ADP2		VSS2	VSS3	VSS1	PTB7	PTC7	PTD4	F
G	ADP0	DACO	ADP3		VREFO	PTB6	PTC0	PTC1	PTC2	G
H			ADP1		PTC3	PTC4	PTD0	PTC5	PTC6	H
J	VSSA	VREFL	VREFH	VDDA	PTB2	PTB3	PTD1	PTB4	PTB5	J
	1	2	3	4	5	6	7	8	9	

Figure 4. 81-Pin MAPBGA

2.4 80-Pin LQFP

The following figure shows the 80-pin LQFP pinout configuration.

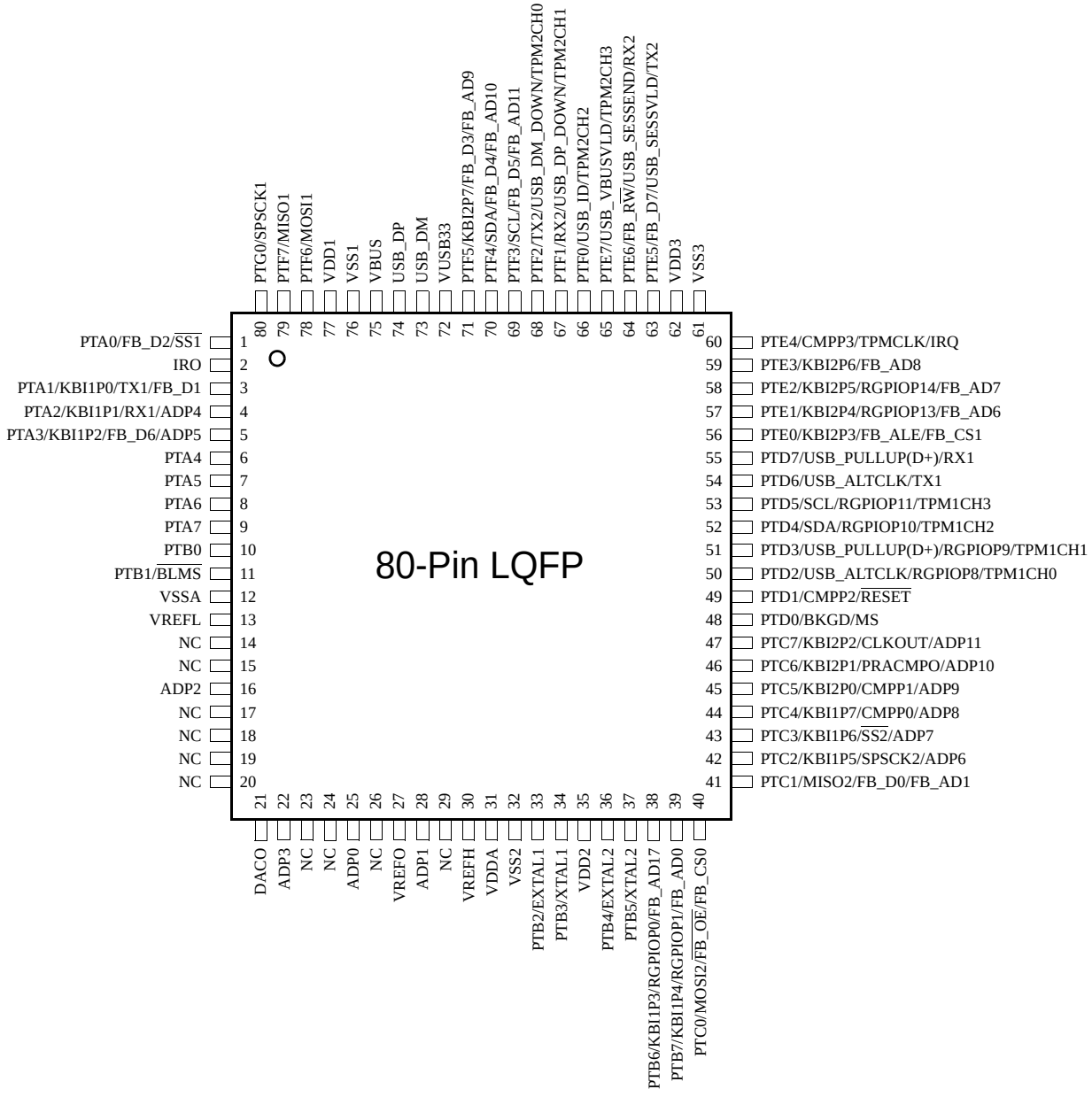


Figure 5. 80-Pin LQFP Pinout

Table 3. Package Pin Assignments (continued)

Package				Default Function	Alternate 1	Alternate 2	Alternate 3	Composite Pin Name
104 MAPBGA	100 LQFP	81 MAPBGA	80 LQFP					
G10	66	D8	55	PTD7	USB_PULLUP(D+)	RX1	—	PTD7/USB_PULLUP(D+) /RX1
G11	67	D9	56	PTE0	KBI2P3	FB_ALE	FB_CS1	PTE0/KBI2P3/FB_ALE/ FB_CS1
F10	68	—	—	PTJ0	FB_AD2	—	—	PTJ0/FB_AD2
F11	69	—	—	PTJ1	FB_AD3	—	—	PTJ1/FB_AD3
F9	70	—	—	PTJ2	FB_AD4	—	—	PTJ2/FB_AD4
E10	71	—	—	PTJ3	RGPIOP12	FB_AD5	—	PTJ3/RGPIOP12/FB_AD5
E11	72	C9	57	PTE1	KBI2P4	RGPIOP13	FB_AD6	PTE1/KBI2P4/RGPIOP13/ FB_AD6
D11	73	C8	58	PTE2	KBI2P5	RGPIOP14	FB_AD7	PTE2/KBI2P5/RGPIOP14/ FB_AD7
D10	74	B9	59	PTE3	KBI2P6	FB_AD8	—	PTE3/KBI2P6/FB_AD8
C9	75	A9	60	PTE4	CMPP3	TPMCLK	IRQ	PTE4/CMPP3/TPMCLK/VPP/ IRQ
H8	76	F5	61	VSS3	—	—	—	VSS3
D8	77	E5	62	VDD3	—	—	—	VDD3
B8	78	C7	63	PTE5	FB_D7	USB_ SESSVLD	TX2	PTE5/FB_D7/USB_SESSVLD/ TX2
C10	79	C6	64	PTE6	FB_$\overline{RW}$	USB_ SESSEND	RX2	PTE6/FB_RW_b/ USB_SESSEND/RX2
C11	80	B6	65	PTE7	USB_VBUSVLD	TPM2CH3	—	PTE7/USB_VBUSVLD/ TPM2CH3
B9	81	B8	66	PTF0	USB_ID	TPM2CH2	—	PTF0/USB_ID/TPM2CH2
B10	82	B7	67	PTF1	RX2	USB_DP_ DOWN	TPM2CH1	PTF1/RX2/USB_DP_DOWN/ TPM2CH1
B11	83	C5	68	PTF2	TX2	USB_DM_ DOWN	TPM2CH0	PTF2/TX2/USB_DM_DOWN/ TPM2CH0
A11	84	—	—	PTJ4	RGPIOP15	FB_AD16	—	PTJ4/RGPIOP15/FB_AD16
A10	85	—	—	PTJ5	FB_AD15	—	—	PTJ5/FB_AD15
B6	86	—	—	PTJ6	FB_AD14	—	—	PTJ6/FB_AD14
A9	87	—	—	PTJ7	FB_AD13	—	—	PTJ7/FB_AD13
A8	88	—	—	FB_AD12	—	—	—	FB_AD12
A7	89	A8	69	PTF3	SCL	FB_D5	FB_AD11	PTF3/SCL/FB_D5/FB_AD11
A6	90	A7	70	PTF4	SDA	FB_D4	FB_AD10	PTF4/SDA/FB_D4/FB_AD10
B5	91	B5	71	PTF5	KBI2P7	FB_D3	FB_AD9	PTF5/KBI2P7/FB_D3/FB_AD9
A5	92	A6	72	VUSB33	—	—	—	VUSB33
A4	93	B4	73	USB_DM	—	—	—	USB_DM
A3	94	A4	74	USB_DP	—	—	—	USB_DP
B4	95	A5	75	VBUS	—	—	—	VBUS

Table 3. Package Pin Assignments (continued)

Package				Default Function	Alternate 1	Alternate 2	Alternate 3	Composite Pin Name
104 MAPBGA	100 LQFP	81 MAPBGA	80 LQFP					
H4	96	F6	76	VSS1	—	—	—	VSS1
D4	97	E6	77	VDD1	—	—	—	VDD1
A1	98	A3	78	PTF6	MOSI1	—	—	PTF6/MOSI1
A2	99	B1	79	PTF7	MISO1	—	—	PTF7/MISO1
B1	100	A2	80	PTG0	SPSCK1	—	—	PTG0/SPSCK1
F4	—	B3	—	PTG1	USB_SESSEND	—	—	PTG1/USB_SESSEND
C4	—	—	—	PTG2	USB_DM_DOWN	—	—	PTG2/USB_DM_DOWN
B3	—	—	—	PTG3	USB_DP_DOWN	—	—	PTG3/USB_DP_DOWN
C2	—	—	—	PTG4	USB_SESSVLD	—	—	PTG4/USB_SESSVLD

Table 5. Absolute Maximum Ratings

#	Rating	Symbol	Value	Unit
1	Supply voltage	V_{DD}	–0.3 to 3.8	V
2	Maximum current into V_{DD}	I_{DD}	120	mA
3	Digital Input voltage	V_{In}	–0.3 to V_{DD} + 0.3	V
4	Instantaneous maximum current Single pin limit (applies to all port pins)[1, 2, 3]	I_D	±25	mA
5	Storage temperature range	T_{stg}	–55 to 150	°C

1 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive (V_{DD}) and negative (V_{SS}) clamp voltages, then use the larger of the two resistance values.

2 All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.

3 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low (which would reduce overall power consumption).

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}).

3.3 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and it is user-determined rather than being controlled by the MCU design. In order to take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

where K is a constant pertaining to the particular part. K can be determined from Equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A.

3.4 ESD Protection Characteristics

Although damage from static discharge is much less common on these devices than on early CMOS circuits, normal handling precautions should be used to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with CDF-AEC-Q00 Stress Test Qualification for Automotive Grade Integrated Circuits. (http://www.aecouncil.com/) This device was qualified to AEC-Q100 Rev E.

A device is considered to have failed if, after exposure to ESD pulses, the device no longer meets the device specification requirements. Complete dc parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table 7. ESD and Latch-up Test Conditions

Model	Description	Symbol	Value	Unit
Human Body	Series Resistance	R1	1500	Ω
	Storage Capacitance	C	100	pF
	Number of Pulse per pin	—	3	—
Machine	Series Resistance	R1	0	Ω
	Storage Capacitance	C	200	pF
	Number of Pulse per pin	—	3	—
Latch-up	Minimum input voltage limit	—	–2.5	V
	Maximum input voltage limit	—	7.5	V

Table 8. ESD and Latch-Up Protection Characteristics

#	Rating	Symbol	Minimum	Maximum	Unit	C
1	Human Body Model (HBM)	V_{HBM}	±2000	—	V	T
2	Machine Model (MM)	V_{MM}	±200	—	V	T
3	Charge Device Model (CDM)	V_{CDM}	±500	—	V	T
4	Latch-up Current at T_A = 125°C	I_{LAT}	±100	—	mA	T

3.5 DC Characteristics

This section includes information about power supply requirements, I/O pin characteristics, and power supply current in various operating modes.

Table 9. DC Characteristics

#	Symbol	Characteristic	Condition	Minimum	Typical[1]	Maximum	Unit	C
1	—	Operating Voltage	—	1.8[2]	—	3.6	V	—
2	V_{OH}	Output high voltage — All I/O pins, low-drive strength						
			$V_{DD} \geq 1.8$ V, $I_{Load} = -600$ μA	$V_{DD} - 0.5$	—	—	V	C
		All I/O pins, high-drive strength						
			$V_{DD} \geq 2.7$ V, $I_{Load} = -10$ mA	$V_{DD} - 0.5$	—	—	V	P
			$V_{DD} \geq 2.3$ V, $I_{Load} = -6$ mA	$V_{DD} - 0.5$	—	—	V	T
			$V_{DD} \geq 1.8$V, $I_{Load} = -3$ mA	$V_{DD} - 0.5$	—	—	V	C
3	I_{OHT}	Output high current — Max total I_{OH} for all ports						
			—	—	—	100	mA	D
4	V_{OL}	Output low voltage — All I/O pins, low-drive strength						
			$V_{DD} \geq 1.8$ V, $I_{Load} = 600$ μA	—	—	0.5	V	C
		All I/O pins, high-drive strength						
			$V_{DD} \geq 2.7$ V, $I_{Load} = 10$ mA	—	—	0.5	V	P
			$V_{DD} \geq 2.3$ V, $I_{Load} = 6$ mA	—	—	0.5	V	T
			$V_{DD} \geq 1.8$ V, $I_{Load} = 3$ mA	—	—	0.5	V	C
5	I_{OLT}	Output low current — Max total I_{OL} for all ports						
			—	—	—	100	mA	D
6	V_{IH}	Input high voltage all digital inputs						
			$V_{DD} > 2.7$ V	0.70 x V_{DD}	—	—	V	P
			$V_{DD} > 1.8$ V	0.85 x V_{DD}	—	—	V	C
7	V_{IL}	Input low voltage all digital inputs						
			$V_{DD} > 2.7$ V	—	—	0.35 x V_{DD}	V	P
			$V_{DD} > 1.8$ V	—	—	0.30 x V_{DD}	V	C
8	V_{hys}	Input hysteresis — all digital inputs	—	0.06 x V_{DD}	—	—	mV	C
9	$\|I_{In}\|$	Input leakage current — all input only pins (Per pin)	$V_{In} = V_{DD}$ or V_{SS}	—	—	0.5	μA	P
10	$\|I_{OZ}\|$	Hi-Z (off-state) leakage current[3] — all input/output (per pin)	$V_{In} = V_{DD}$ or V_{SS}	—	0.003	0.5	μA	P

Table 9. DC Characteristics (continued)

#	Symbol	Characteristic	Condition	Minimum	Typical[1]	Maximum	Unit	C
11	R_{PU}	Pull-up resistors all digital inputs, when enabled	—	17.5	—	52.5	kΩ	P
12	R_{PD}	Internal pull-down resistors[4]	—	17.5	—	52.5	kΩ	P
13	I_{IC}	DC injection current [5, 6, 7] — Single pin limit	$V_{SS} > V_{IN} > V_{DD}$	–0.2	—	0.2	mA	D
		DC injection current [5, 6, 7] — Total MCU limit, includes sum of all stressed pins	$V_{SS} > V_{IN} > V_{DD}$	–5	—	5	mA	D
14	C_{In}	Input Capacitance, all pins	—	—	—	8	pF	C
15	V_{RAM}	RAM retention voltage	—	—	0.6	1.0	V	C
16	V_{POR}	POR re-arm voltage[8]	—	0.9	1.4	1.79	V	C
17	t_{POR}	POR re-arm time	—	10	—	—	µs	D
18	V_{LVDH}	Low-voltage detection threshold — high range[9]						
			V_{DD} falling	2.11	2.16	2.22	V	P
			V_{DD} rising	2.16	2.21	2.27	V	P
19	V_{LVDL}	Low-voltage detection threshold — low range[9]						
			V_{DD} falling	1.80	1.82	1.91	V	P
			V_{DD} rising	1.86	1.90	1.99	V	P
20	V_{LVWH}	Low-voltage warning threshold — high range[9]						
			V_{DD} falling	2.36	2.46	2.56	V	P
			V_{DD} rising	2.36	2.46	2.56	V	P
21	V_{LVWL}	Low-voltage warning threshold — low range[9]						
			V_{DD} falling	2.11	2.16	2.22	V	P
			V_{DD} rising	2.16	2.21	2.27	V	P
22	V_{hys}	Low-voltage inhibit reset/recover hysteresis[10]	—	—	50	—	mV	C
23	V_{BG}	Bandgap Voltage Reference[11]	—	1.145	1.17	1.195	V	P

1 Typical values are measured at 25°C. Characterized, not tested

2 As the supply voltage rises, the LVD circuit will hold the MCU in reset until the supply has risen above V_{LVDL}.

3 Does not include analog module pins. Dedicated analog pins should not be pulled to VDD or VSS and should be left floating when not used to reduce current leakage.

4 Measured with $V_{In} = V_{DD}$.

5 All functional non-supply pins are internally clamped to V_{SS} and V_{DD},except PTD1.

6 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

7 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).

[8] Maximum is highest voltage that POR is guaranteed.
[9] Run at 1 MHz bus frequency.
[10] Low voltage detection and warning limits measured at 1 MHz bus frequency.
[11] Factory trimmed at V_{DD} = 3.0 V, Temp = 25°C.

3.6 Supply Current Characteristics

Table 10. Supply Current Characteristics

#	Symbol	Parameter	Bus Freq	V_{DD} (V)	Typical[1]	Maximum	Unit	Temperature (°C)	C
1	RI_{DD}	Run supply current FEI mode, all modules ON[2]							
			25.165 MHz	3	44	48	mA	–40 to 25	P
			25.165 MHz	3	44	48	mA	105	P
			20 MHz	3	32.3	—	mA	–40 to 105	T
			8 MHz	3	16.4	—	mA	–40 to 105	T
			1 MHz	3	2.9	—	mA	–40 to 105	T
2	RI_{DD}	Run supply current FEI mode, all modules OFF[3]							
			25.165 MHz	3	29	29.6	mA	–40 to 105	C
			20 MHz	3	25.4	—	mA	–40 to 105	T
			8 MHz	3	12.7	—	mA	–40 to 105	T
			1 MHz	3	2.4	—	mA	–40 to 105	T
3	RI_{DD}	Run supply current LPR=0, all modules OFF[3]							
			16 kHz FBI	3	232	280	μA	–40 to 105	T
			16 kHz FBE	3	231	296	μA	–40 to 105	T
4	RI_{DD}	Run supply current LPR=1, all modules OFF[3]							
			16 kHz BLPE	3	74	75	μA	0 to 70	T
			16 kHz BLPE	3	74	120	μA	–40 to 105	T
5	WI_{DD}	Wait mode supply current FEI mode, all modules OFF[3]							
			25.165 MHz	3	16.5	—	mA	–-40 to 105	C
			20 MHz	3	10.3	—	mA	–-40 to 105	T
			8 MHz	3	6.6	—	mA	–-40 to 105	T
			1 MHz	3	1.7	—	mA	–-40 to 105	T

Table 10. Supply Current Characteristics (continued)

#	Symbol	Parameter	Bus Freq	V_{DD} (V)	Typical[1]	Maximum	Unit	Temperature (°C)	C
6	$S2I_{DD}$	Stop2 mode supply current[4]							
			N/A	3	0.410	1	μA	-40 to 25	P
			N/A	3	3.7	10	μA	70	C
			N/A	3	10	20	μA	85	C
			N/A	3	21	31.5	μA	105	P
			N/A	2	0.410	0.640	μA	-40 to 25	C
			N/A	2	3.4	9	μA	70	C
			N/A	2	9.5	18	μA	85	C
			N/A	2	20	30	μA	105	C
7	$S3I_{DD}$	Stop3 mode supply current No clocks active	N/A	3	0.750	1.3	μA	-40 to 25	P
			N/A	3	8.5	18	μA	70	C
			N/A	3	20	28	μA	85	C
			N/A	3	53	63	μA	105	P
			N/A	2	0.400	0.900	μA	-40 to 25	C
			N/A	2	8.2	16	μA	70	C
			N/A	2	18	26	μA	85	C
			N/A	2	47	59	μA	105	C

1 Data in Typical column was characterized at 3.0 V, 25°C or is typical recommended value.

2 ON = System Clock Gating Control registers turn on system clock to the corresponding modules.

3 OFF = System Clock Gating Control registers turn off system clock to the corresponding modules.

4 All digital pins must be configured to a known state to prevent floating pins from adding current. Smaller packages may have some pins that are not bonded out; however, software must still be configured to the largest pin package available so that all pins are in a known state. Otherwise, floating pins that are not bonded in the smaller packages may result in a higher current draw. NOTE: I/O pins are configured to output low; input-only pins are configured to pullup-enabled. IRO pin connects to ground. FB_AD12 pin is pullup-enabled. DACO, and VREFO pins are at reset state and unconnected.

Table 11. Stop Mode Adders

#	Parameter	Condition	Temperature (°C)					Units	C
			-40	25	70	85	105		
1	LPO	—	50	75	100	150	250	nA	D
2	EREFSTEN	RANGE = HGO = 0	600	650	750	850	1000	nA	D
3	IREFSTEN[1]	—	—	73	80	93	125	μA	T
4	TOD	Does not include clock source current	50	75	100	150	250	nA	D

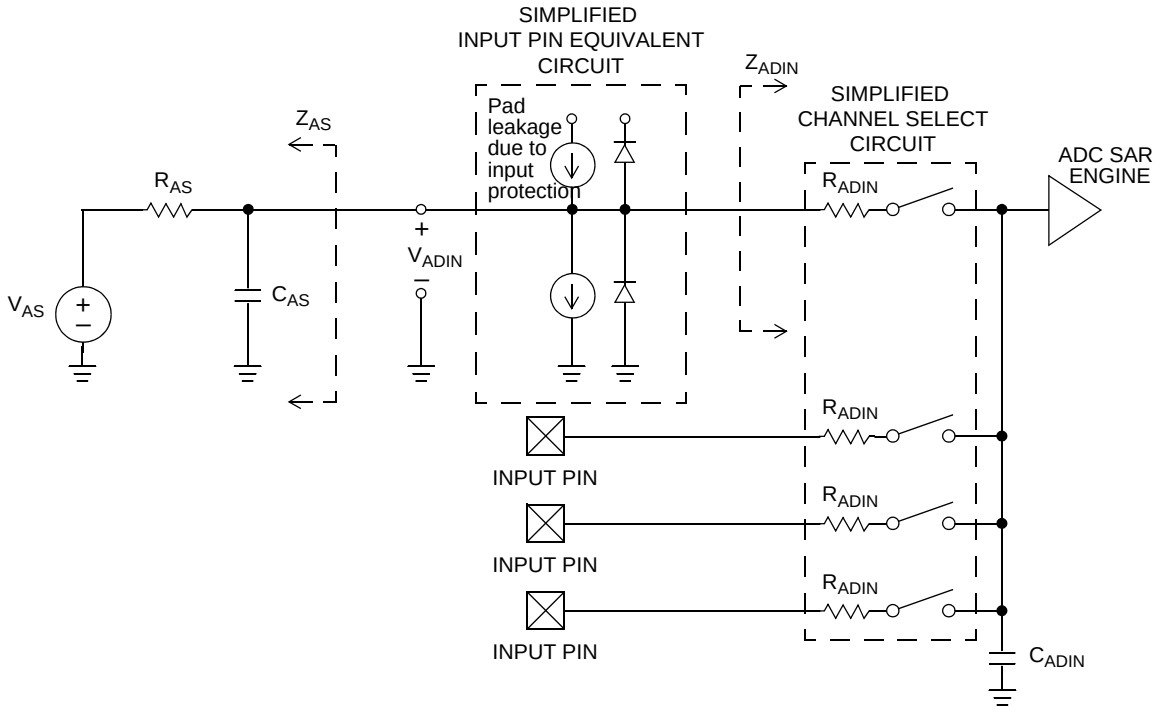


Figure 8. ADC Input Impedance Equivalency Diagram

Table 16. 12-bit SAR ADC Characteristics full operating range ($V_{REFH} = V_{DDAD}$, $V_{REFL} = V_{SSAD}$)

#	Symbol	Characteristic	Conditions[1]	Minimum	Typical[2]	Maximum	Unit	C
1	I_{DDAD}	Supply Current (ADLSMP=0, ADCO=1)	ADLPC=1, ADHSC=0	—	215	—	μA	T
			ADLPC=0, ADHSC=0	—	470	—	μA	T
			ADLPC=0, ADHSC=1	—	610	—	μA	T
			Stop, Reset, Module Off	—	0.01	—	μA	C
2	f_{ADACK}	ADC Asynchronous Clock Source (t_{ADACK} =1/f_{ADACK})	ADLPC=1, ADHSC=0	—	2.4	—	MHz	P
			ADLPC=0, ADHSC=0	—	5.2	—	MHz	P
			ADLPC=0, ADHSC=1	—	6.2	—	MHz	P
3	—	Sample Time — *See Reference Manual for sample times.*						
4	—	Conversion Time — *See Rreference Manual for conversion times.*						
5	TUE	Total Unadjusted Error 32x Hardware Averaging (AVGE = %1 AVGS = %11)	12-bit single-ended mode	—	±1.75	±3.5	LSB[3]	T
			10-bit single-ended mode	—	±0.8	±1.5	LSB[3]	T
			8-bit single-ended mode	—	±0.5	±1.0	LSB[3]	T
6		Differential Non-Linearity	12-bit single-ended mode	—	±0.7	±1	LSB[3]	T
			10-bit single-ended mode	—	±0.5	±0.75	LSB[3]	T
			8-bit single-ended mode	—	±0.2	±0.5	LSB[3]	T

Table 16. 12-bit SAR ADC Characteristics full operating range (V_{REFH} = V_{DDAD}, V_{REFL} = V_{SSAD}) (continued)

#	Symbol	Characteristic	Conditions[1]	Minimum	Typical[2]	Maximum	Unit	C
7	INL	Integral Non-Linearity	12-bit single-ended mode	—	±1.0	±2.5	LSB[3]	T
			10-bit single-ended mode	—	±0.5	±1.0	LSB[3]	T
			8-bit single-ended mode	—	±0.3	±0.5	LSB[3]	T
8	E_{ZS}	Zero-Scale Error (V_{ADIN} = V_{SSAD})	12-bit single-ended mode	—	±0.7	±2.0	LSB[3]	T
			10-bit single-ended mode	—	±0.4	±1.0	LSB[3]	T
			8-bit single-ended mode	—	±0.2	±0.5	LSB[3]	T
9	E_{FS}	Full-Scale Error (V_{ADIN} = V_{DDAD})	12-bit single-ended mode	—	±1.0	±3.5	LSB[3]	T
			10-bit single-ended mode	—	±0.4	±1.5	LSB[3]	T
			8-bit single-ended mode	—	±0.2	±0.5	LSB[3]	T
10	E_Q	Quantization Error	All modes	—	—	±0.5	LSB[3]	D
11	E_{IL}	Input Leakage Error (I_{In} = leakage current (refer to DC Characteristics)	All modes	I_{In} * R_{AS}			mV	D
12	m	Temp Sensor Slope	-40°C to 25°C	—	1.646	—	mV/xC	C
			25°C to 125°C	—	1.769	—	mV/xC	C
13	V_{TEMP25}	Temp Sensor Voltage	25°C	—	701.2	—	mV	C

1 All accuracy numbers assume the ADC is calibrated with V_{REFH}=V_{DDAD}.

2 Typical values assume V_{DDAD} = 3.0V, Temp = 25°C, f_{ADCK}=2.0MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

3 1 LSB = (V_{REFH} - V_{REFL})/2^N

3.10 MCG and External Oscillator (XOSC) Characteristics

Table 17. MCG (Temperature Range = –40 to 105°C Ambient)

#	Rating		Symbol	Min	Typical	Max	Unit	C
1	Internal reference startup time		t_{irefst}	—	55	100	µs	D
2	Average internal reference frequency	factory trimmed at VDD=3.0V and temp=25°C	f_{int_ft}	—	31.25	—	kHz	C
		user trimmed		31.25	—	39.0625	KHz	C
3	DCO output frequency range - trimmed	Low range (DRS=00)	f_{dco_t}	16	—	20	MHz	C
		Mid range (DRS=01)		32	—	40	MHz	C
		High range[1] (DRS=10)		40	—	60	MHz	C
4	Resolution of trimmed DCO output frequency at fixed voltage and temperature	with FTRIM	$\Delta f_{dco\_res\_t}$	—	± 0.1	± 0.2	$\%f_{dco}$	C
		without FTRIM		—	± 0.2	± 0.4	$\%f_{dco}$	C

Table 17. MCG (Temperature Range = –40 to 105°C Ambient) (continued)

#	Rating		Symbol	Min	Typical	Max	Unit	C
5	Total deviation of trimmed DCO output frequency over voltage and temperature	over voltage and temperature	Δf_{dco_t}	—	± 1.0	± 2	$\%f_{dco}$	P
		over fixed voltage and temp range of 0 - 70 °C		—	± 0.5	± 1	$\%f_{dco}$	C
6	Acquisition time	FLL[2]	$t_{fll\_acquire}$	—	—	1	ms	C
		PLL[3]	$t_{pll\_acquire}$	—	—	1	ms	D
7	Long term Jitter of DCO output clock (averaged over 2mS interval) [4]		C_{Jitter}	—	0.02	0.2	$\%f_{dco}$	C
8	VCO operating frequency		f_{vco}	7.0	—	55.0	MHz	D
9	PLL reference frequency range		f_{pll_ref}	1.0	—	2.0	MHz	D
10	Jitter of PLL output clock measured over 625 ns	Long term	$f_{pll\_jitter\_625\ ns}$	—	0.566[4]	—	%fpll	D
11	Lock frequency tolerance	Entry[5]	D_{lock}	± 1.49	—	± 2.98	%	D
		Exit[6]	D_{unl}	± 4.47	—	± 5.97	%	D
12	Lock time	FLL	t_{fll_lock}	—	—	$t_{fll\_acquire}$+ 1075(1/f_{int_t})	s	D
		PLL	t_{pll_lock}	—	—	$t_{pll\_acquire}$+ 1075(1/f_{pll_ref})	s	D
13	Loss of external clock minimum frequency - RANGE = 0		f_{loc_low}	(3/5) x f_{int_t}	—	—	kHz	D
14	Loss of external clock minimum frequency - RANGE = 1		f_{loc_high}	(16/5) x f_{int_t}	—	—	kHz	D

1 This should not exceed the maximum CPU frequency of 50.33 MHz.

2 This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bit is changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

3 This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

4 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{BUS}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

5 Below D_{lock} minimum, the MCG is guaranteed to enter lock. Above D_{lock} maximum, the MCG will not enter lock. But if the MCG is already in lock, then the MCG may stay in lock.

6 Below D_{unl} minimum, the MCG will not exit lock if already in lock. Above D_{unl} maximum, the MCG is guaranteed to exit lock.

Table 18. XOSC (Temperature Range = –40 to 105°C Ambient)

#	Characteristic		Symbol	Minimum	Typical[1]	Maximum	Unit
1	Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1)	• Low range (RANGE = 0)	f_{lo}	32	—	38.4	kHz
		• High range (RANGE = 1), • FEE or FBE mode [2]	f_{hi-fll}	1	—	5	MHz
		• High range (RANGE = 1), • PEE or PBE mode [3]	f_{hi-pll}	1	—	16	MHz
		• High range (RANGE = 1), • High gain (HGO = 1), • FBELP mode	f_{hi-hgo}	1	—	16	MHz
		• High range (RANGE = 1), • Low power (HGO = 0), • FBELP mode	f_{hi-lp}	1	—	8	MHz
2	Load capacitors		C_1 C_2	See Note [4]			
3	Feedback resistor	Low range (32 kHz to 38.4 kHz)	R_F	—	10	—	MΩ
		High range (1 MHz to 16 MHz)	—	—	1	—	
4	Series resistor — Low range	Low Gain (HGO = 0)	R_S	—	0	—	kΩ
		High Gain (HGO = 1)		—	100	—	
5	Series resistor — High range	• Low Gain (HGO = 0)	R_S	—	0	—	kΩ
		• High Gain (HGO = 1)					
		≥ 8 MHz		—	0	0	
		4 MHz		—	0	10	
		1 MHz		—	0	20	
6	Crystal start-up time [5, 6]	Low range, low gain (RANGE=0,HGO=0)	t_{CSTL}	—	200	—	ms
		Low range, high gain (RANGE=0,HGO=1)		—	400	—	
		High range, low gain (RANGE=1,HGO=0)	t_{CSTH}	—	5	—	
		High range, high gain (RANGE=1, HGO=1)		—	15	—	

1 Data in Typical column was characterized at 3.0 V, 25°C or is typical recommended value.

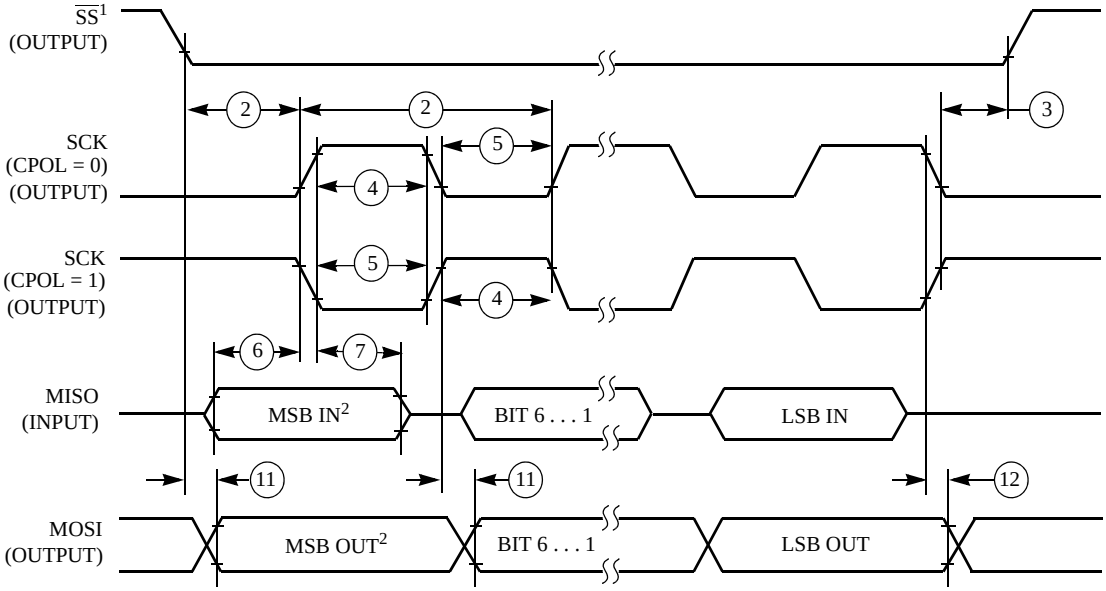
2 When MCG is configured for FEE or FBE mode, input clock source must be divisible using RDIV to within the range of 31.25 kHz to 39.0625 kHz.

3 When MCG is configured for PEE or PBE mode, input clock source must be divisible using RDIV to within the range of 1 MHz to 2 MHz.

4 See crystal or resonator manufacturer's recommendation.

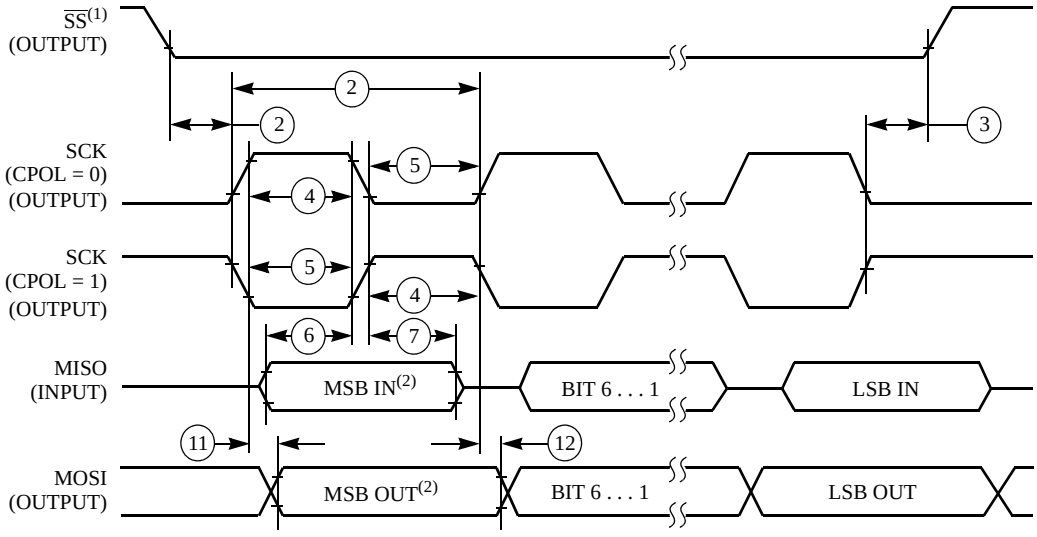
5 This parameter is characterized and not tested on each device.

6 Proper PC board layout procedures must be followed to achieve specifications.



NOTES:
1. $\overline{SS}$ output mode (MODFEN = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 15. SPI Master Timing (CPHA = 0)



NOTES:
1. $\overline{SS}$ output mode (MODFEN = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 16. SPI Master Timing (CPHA = 1)

Table 26. VREF Limited Range Operating Behaviors

#	Characteristic	Symbol	Minimum	Maximum	Unit	C
1	Voltage Reference Output with Factory Trim	V_{out}	1.149	1.152	mV	T
2	Temperature Drift (Vmin – Vmax Temperature range from 0° C to 50° C	Tdrift	—	3	mV[1]	T

1 See typical chart that follows (Figure 19).

Figure 19. Typical VREF Output vs Temperature

- Open a browser to the Freescale® website (http://www.freescale.com), and enter the appropriate document number (from Table 28) in the “Enter Keyword” search box at the top of the page.

5 Revision History

This section lists major changes between versions of the MCF51JE256 Data Sheet.

Table 29. Revision History

Revision	Date	Description
0	March/April 09	Initial Draft
1	July 2009	• Revised to follow standard template. • Removed extraneous headings from the TOC. • Corrected units for Monotoncity to be blank in for the DAC specification. • Updated ADC characteristic tables to include 16-Bit SAR in headings.
2	July 2009	• Changed MCG (XOSC) Electricals Table - Row 2, Average Internal Reference Frequency typical value from 32.768 to 31.25
3	April 2010	• Updated Thermal Characteristics table. Reinserted the 81 and 104 MapBGA devices. • Revised the ESD and Latch-Up Protection Characeristic description to read: Latch-up Current at T_A = 125°C. • Changed Table 9. DC Characteristics rows 2 and 4, to 1.8 V, ILoad = -600 mA conditions to 1.8 V, ILoad = 600μA respectively. • Corrected the 16-bit SAR ADC Operating Condition table Ref Voltage High Min value to be 1.13 instead of 1.15. • Updated the ADC electricals. • Inserted the Mini-FlexBus Timing Specifications. • Added a Temp Drift parameter to the VREF Electrical Specifications. • Removed the S08 Naming Convention diagram. • Updated the Orderable Part Number Summary to include the Freescale Part Number suffixes. • Completed the Package Description table values. • Changed the 80LQFP package drawing from 98ARL10530D to 98ASS23174W. • Updated electrical characteristic data.

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Japan
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support.japan@freescale.com

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