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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details	
Product Status	Active
Core Processor	Coldfire V1
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	EBI/EMI, I ² C, SCI, SPI, USB OTG
Peripherals	LVD, PWM, WDT
Number of I/O	48
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 12x12b; D/A 1x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	81-LBGA
Supplier Device Package	81-MAPBGA (10x10)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcf51je256vmb

1 Features

The following table provides a cross-comparison of the features of the MCF51JE256/128 according to package.

Table 1. MCF51JE Features by MCU and Package

Feature	MCF51JE256				MCF51JE128	
FLASH size (bytes)	262144				131072	
RAM size (bytes)	32K				32K	
Pin quantity	104	100	81	80	81	80
Programmable Analog Comparator (PRACMP)	yes					
Debug Module (DBG)	yes					
Multipurpose Clock Generator (MCG)	yes					
Inter-Integrated Communication (IIC)	yes					
Interrupt Request Pin (IRQ)	yes					
Keyboard Interrupt (KBI)	16					
Digital General purpose I/O ¹	69	65	48	47	48	47
Power and Ground Pins	8					
Time Of Day (TOD)	yes					
Serial Communications (SCI1)	yes					
Serial Communications (SCI2)	yes					
Serial Peripheral Interface (SPI1(FIFO))	yes					
Serial Peripheral Interface(SPI2)	yes					
Carrier Modulator Timer pin (IRO)	yes					
Programmable Delay Block (PDB)	yes					
TPM input clock pin (TPMCLK)	yes					
TPM1 channels	4					
TPM2 channels	4					
XOSC1	yes					
XOSC2	yes					
USBOTG	yes					
MiniFlex Bus	yes			DATA		
Rapid GPIO	16			9		
ADC single-ended channels	12					
DAC output pin (DACO)	yes					
Voltage reference output pin (VREFO)	yes					

¹ Port I/O count does not include $\overline{\text{BLMS}}$, BKGD and IRQ. $\overline{\text{BLMS}}$ BKGD are Output only, IRQ is input only.

The following table describes the functional units of the MCF51JE256/128.

Table 2. MCF51JE256/128 Functional Units

Unit	Function
DAC (digital to analog converter)	Used to output voltage levels.
12-BIT SAR ADC (analog-to-digital converter)	Measures analog voltages at up to 12 bits of resolution. The ADC has up to 12 single-ended inputs.
PDB (Programmable Delay Block)	Precisely trigger the DAC FIFO buffer.
Mini-FlexBus	Provides expansion capability for off-chip memory and peripherals.
USB On-the-Go	Supports the USB On-the-Go dual-role controller.
CMT (Carrier Modulator Timer)	Infrared output used for the Remote Controller operation.
MCG (Multipurpose Clock Generator)	Provides clocking options for the device, including a phase-locked loop (PLL) and frequency-locked loop (FLL) for multiplying slower reference clock sources.
BDM (Background Debug Module)	Provides single pin debugging interface (part of the V1 ColdFire core).
CF1 CORE (V1 ColdFire Core)	Executes programs and interrupt handlers.
PRACMP	Analog comparators for comparing external analog signals against each other, or a variety of reference levels.
COP (Computer Operating Properly)	Software Watchdog.
IRQ (Interrupt Request)	Single-pin high-priority interrupt (part of the V1 ColdFire core).
CRC (Cyclic Redundancy Check)	High-speed CRC calculation.
DBG (Debug)	Provides debugging and emulation capabilities (part of the V1 ColdFire core).
FLASH (Flash Memory)	Provides storage for program code, constants, and variables.
IIC (Inter-integrated Circuits)	Supports standard IIC communications protocol and SMBus.
INTC (Interrupt Controller)	Controls and prioritizes all device interrupts.
KBI1 & KBI2	Keyboard Interfaces 1 and 2.
LVD (Low-voltage Detect)	Provides an interrupt to the ColdFire V1 CORE in the event that the supply voltage drops below a critical value. The LVD can also be programmed to reset the device upon a low voltage event.
VREF (Voltage Reference)	The Voltage Reference output is available for both on- and off-chip use.
RAM (Random-Access Memory)	Provides stack and variable storage.
RGPIO (Rapid General-purpose Input/output)	Allows for I/O port access at CPU clock speeds. RGPIO is used to implement GPIO functionality.
SCI1, SCI2 (Serial Communications Interfaces)	Serial communications UARTs capable of supporting RS-232 and LIN protocols.
SIM (system integration unit)	

Table 2. MCF51JE256/128 Functional Units (continued)

Unit	Function
SPI1 (FIFO), SPI2 (Serial Peripheral Interfaces)	SPI1 and SPI2 provide standard master/slave capability. SPI contains a FIFO buffer in order to increase the throughput for this peripheral.
TPM1, TPM2 (Timer/PWM Module)	Timer/PWM module can be used for a variety of generic timer operations as well as pulse-width modulation.
VREG (Voltage Regulator)	Controls power management across the device.
XOSC1 and XOSC2 (Crystal Oscillators)	These devices incorporate redundant crystal oscillators. One is intended primarily for use by the TOD, and the other by the CPU and other peripherals.

2 Pinouts and Pin Assignments

2.1 104-Pin MAPBGA

The following figure shows the 104-pin MAPBGA pinout configuration.

	1	2	3	4	5	6	7	8	9	10	11	
A	PTF6	PTF7	USB_DP	USB_DM	VUSB33	PTF4	PTF3	FB_AD12	PTJ7	PTJ5	PTJ4	A
B	PTG0	PTA0	PTG3	VBUS	PTF5	PTJ6	PTH0	PTE5	PTF0	PTF1	PTF2	B
C	IRO	PTG4	PTA6	PTG2	PTG6	PTG5	PTG7	PTH1	PTE4	PTE6	PTE7	C
D	PTA5	PTA4	PTB1	VDD1		VDD2		VDD3	PTA1	PTE3	PTE2	D
E	VSSA	PTA7	PTB0						PTA2	PTJ3	PTE1	E
F	VREFL			PTG1				PTC7	PTJ2	PTJ0	PTJ1	F
G	ADP2								PTD5	PTD7	PTE0	G
H			PTA3	VSS1		VSS2		VSS3	PTD4	PTD3	PTD2	H
J	ADP0		PTH7	PTH6	PTH4	PTH3	PTH2	PTD6	PTC2	PTC0	PTC1	J
K			ADP1	PTH5	PTB6	PTB7	PTC3	PTD1	PTC4	PTC5	PTC6	K
L	ADP3	DACO		VREFO	VREFH	VDDA	PTB3	PTB2	PTD0	PTB5	PTB4	L
	1	2	3	4	5	6	7	8	9	10	11	

Figure 2. 104-Pin MAPBGA

2.4 80-Pin LQFP

The following figure shows the 80-pin LQFP pinout configuration.

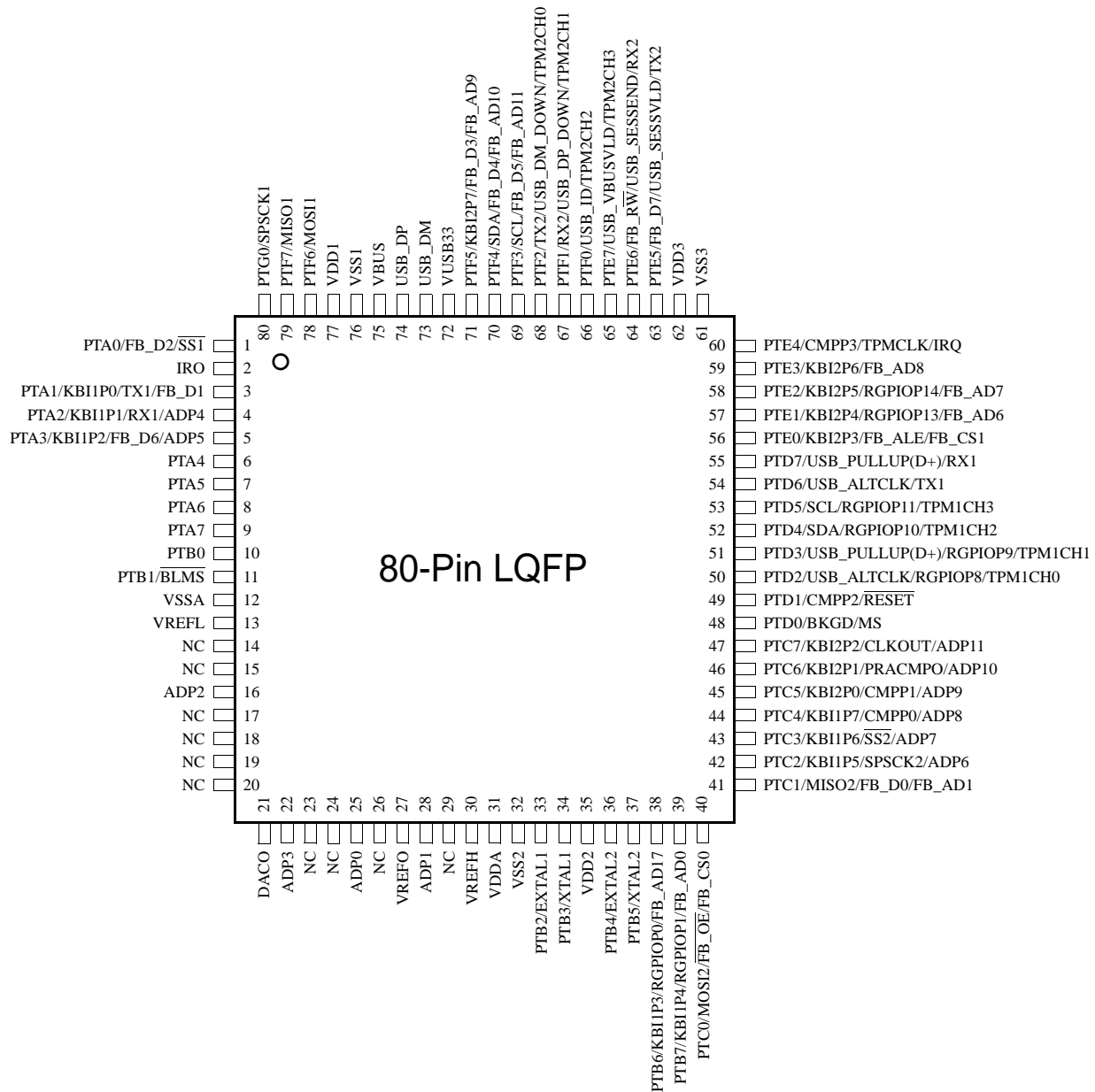


Figure 5. 80-Pin LQFP Pinout

Table 3. Package Pin Assignments (continued)

Package				Default Function	Alternate 1	Alternate 2	Alternate 3	Composite Pin Name
104 MAPB GA	100 LQFP	81 MAPB GA	80 LQFP					
L5	35	J3	30	VREFH	—	—	—	VREFH
L6	36	J4	31	VDDA	—	—	—	VDDA
H6	37	F4	32	VSS2	—	—	—	VSS2
L8	38	J5	33	PTB2	EXTAL1	—	—	PTB2/EXTAL1
L7	39	J6	34	PTB3	XTAL1	—	—	PTB3/XTAL1
D6	40	E4	35	VDD2	—	—	—	VDD2
L11	41	J8	36	PTB4	EXTAL2	—	—	PTB4/EXTAL2
L10	42	J9	37	PTB5	XTAL2	—	—	PTB5/XTAL2
K5	43	G6	38	PTB6	KBI1P3	RGPIOP0	FB_AD17	PTB6/KBI1P3/RGPIOP0/ FB_AD17
K6	44	F7	39	PTB7	KBI1P4	RGPIOP1	FB_AD0	PTB7/KBI1P4/RGPIOP1/ FB_AD0
J7	45	—	—	PTH2	RGPIOP2	FB_D7	—	PTH2/RGPIOP2/FB_D7
J6	46	—	—	PTH3	RGPIOP3	FB_D6	—	PTH3/RGPIOP3/FB_D6
J5	47	—	—	PTH4	RGPIOP4	FB_D5	—	PTH4/RGPIOP4/FB_D5
K4	48	—	—	PTH5	RGPIOP5	FB_D4	—	PTH5/RGPIOP5/FB_D4
J4	49	—	—	PTH6	RGPIOP6	FB_D3	—	PTH6/RGPIOP6/FB_D3
J3	50	—	—	PTH7	RGPIOP7	FB_D2	—	PTH7/RGPIOP7/FB_D2
J10	51	G7	40	PTC0	MOSI2	FB_OE	FB_CS0	PTC0/MOSI2/FB_OE/ FB_CS0
J11	52	G8	41	PTC1	MISO2	FB_D0	FB_AD1	PTC1/MISO2/FB_D0/ FB_AD1
J9	53	G9	42	PTC2	KBI1P5	SPSCK2	ADP6	PTC2/KBI1P5/SPSCK2/ ADP6
K7	54	H5	43	PTC3	KBI1P6	SS2	ADP7	PTC3/KBI1P6/SS2/ ADP7
K9	55	H6	44	PTC4	KBI1P7	CMPP0	ADP8	PTC4/KBI1P7/CMPP0/ ADP8
K10	56	H8	45	PTC5	KBI2P0	CMPP1	ADP9	PTC5/KBI2P0/CMPP1/ ADP9
K11	57	H9	46	PTC6	KBI2P1	PRACMPO	ADP10	PTC6/KBI2P1/PRACMPO/ ADP10
F8	58	F8	47	PTC7	KBI2P2	CLKOUT	ADP11	PTC7/KBI2P2/CLKOUT/ ADP11
L9	59	H7	48	PTD0	BKGD	MS	—	PTD0/BKGD/MS
K8	60	J7	49	PTD1	CMPP2	RESET	—	PTD1/CMPP2/RESET
H11	61	E7	50	PTD2	USB_ALTCLK	RGPIOP8	TPM1CH0	PTD2/USB_ALTCLK/RGPIOP8/ TPM1CH0
H10	62	E8	51	PTD3	USB_PULLUP(D+)	RGPIOP9	TPM1CH1	PTD3/USB_PULLUP(D+)/ RGPIOP9/TPM1CH1
H9	63	F9	52	PTD4	SDA	RGPIOP10	TPM1CH2	PTD4/SDA/RGPIOP10/ TPM1CH2
G9	64	D7	53	PTD5	SCL	RGPIOP11	TPM1CH3	PTD5/SCL/RGPIOP11/ TPM1CH3
J8	65	E9	54	PTD6	USB_ALTCLK	TX1	—	PTD6/USB_ALTCLK/TX1

Table 3. Package Pin Assignments (continued)

Package				Default Function	Alternate 1	Alternate 2	Alternate 3	Composite Pin Name
104 MAPB GA	100 LQFP	81 MAPB GA	80 LQFP					
G10	66	D8	55	PTD7	USB_PULLUP(D+)	RX1	—	PTD7/USB_PULLUP(D+)/RX1
G11	67	D9	56	PTE0	KBI2P3	FB_ALE	FB_CS1	PTE0/KBI2P3/FB_ALE/ FB_CS1
F10	68	—	—	PTJ0	FB_AD2	—	—	PTJ0/FB_AD2
F11	69	—	—	PTJ1	FB_AD3	—	—	PTJ1/FB_AD3
F9	70	—	—	PTJ2	FB_AD4	—	—	PTJ2/FB_AD4
E10	71	—	—	PTJ3	RGPIOP12	FB_AD5	—	PTJ3/RGPIOP12/FB_AD5
E11	72	C9	57	PTE1	KBI2P4	RGPIOP13	FB_AD6	PTE1/KBI2P4/RGPIOP13/ FB_AD6
D11	73	C8	58	PTE2	KBI2P5	RGPIOP14	FB_AD7	PTE2/KBI2P5/RGPIOP14/ FB_AD7
D10	74	B9	59	PTE3	KBI2P6	FB_AD8	—	PTE3/KBI2P6/FB_AD8
C9	75	A9	60	PTE4	CMPP3	TPMCLK	IRQ	PTE4/CMPP3/TPMCLK/VPP/ IRQ
H8	76	F5	61	VSS3	—	—	—	VSS3
D8	77	E5	62	VDD3	—	—	—	VDD3
B8	78	C7	63	PTE5	FB_D7	USB_SESSVLD	TX2	PTE5/FB_D7/USB_SESSVLD/ TX2
C10	79	C6	64	PTE6	FB_R \bar{W}	USB_SESEND	RX2	PTE6/FB_R \bar{W} _b/ USB_SESEND/RX2
C11	80	B6	65	PTE7	USB_VBUSVLD	TPM2CH3	—	PTE7/USB_VBUSVLD/ TPM2CH3
B9	81	B8	66	PTF0	USB_ID	TPM2CH2	—	PTF0/USB_ID/TPM2CH2
B10	82	B7	67	PTF1	RX2	USB_DP_DOWN	TPM2CH1	PTF1/RX2/USB_DP_DOWN/ TPM2CH1
B11	83	C5	68	PTF2	TX2	USB_DM_DOWN	TPM2CH0	PTF2/TX2/USB_DM_DOWN/ TPM2CH0
A11	84	—	—	PTJ4	RGPIOP15	FB_AD16	—	PTJ4/RGPIOP15/FB_AD16
A10	85	—	—	PTJ5	FB_AD15	—	—	PTJ5/FB_AD15
B6	86	—	—	PTJ6	FB_AD14	—	—	PTJ6/FB_AD14
A9	87	—	—	PTJ7	FB_AD13	—	—	PTJ7/FB_AD13
A8	88	—	—	FB_AD12	—	—	—	FB_AD12
A7	89	A8	69	PTF3	SCL	FB_D5	FB_AD11	PTF3/SCL/FB_D5/FB_AD11
A6	90	A7	70	PTF4	SDA	FB_D4	FB_AD10	PTF4/SDA/FB_D4/FB_AD10
B5	91	B5	71	PTF5	KBI2P7	FB_D3	FB_AD9	PTF5/KBI2P7/FB_D3/FB_AD9
A5	92	A6	72	VUSB33	—	—	—	VUSB33
A4	93	B4	73	USB_DM	—	—	—	USB_DM
A3	94	A4	74	USB_DP	—	—	—	USB_DP
B4	95	A5	75	VBUS	—	—	—	VBUS

Table 10. Supply Current Characteristics (continued)

#	Symbol	Parameter	Bus Freq	V _{DD} (V)	Typical ¹	Maximum	Unit	Temperature (°C)	C
6	S2I _{DD}	Stop2 mode supply current ⁴	N/A	3	0.410	1	μA	-40 to 25	P
			N/A	3	3.7	10	μA	70	C
			N/A	3	10	20	μA	85	C
			N/A	3	21	31.5	μA	105	P
			N/A	2	0.410	0.640	μA	-40 to 25	C
			N/A	2	3.4	9	μA	70	C
			N/A	2	9.5	18	μA	85	C
			N/A	2	20	30	μA	105	C
7	S3I _{DD}	Stop3 mode supply current No clocks active	N/A	3	0.750	1.3	μA	-40 to 25	P
			N/A	3	8.5	18	μA	70	C
			N/A	3	20	28	μA	85	C
			N/A	3	53	63	μA	105	P
			N/A	2	0.400	0.900	μA	-40 to 25	C
			N/A	2	8.2	16	μA	70	C
			N/A	2	18	26	μA	85	C
			N/A	2	47	59	μA	105	C

¹ Data in Typical column was characterized at 3.0 V, 25°C or is typical recommended value.

² ON = System Clock Gating Control registers turn on system clock to the corresponding modules.

³ OFF = System Clock Gating Control registers turn off system clock to the corresponding modules.

⁴ All digital pins must be configured to a known state to prevent floating pins from adding current. Smaller packages may have some pins that are not bonded out; however, software must still be configured to the largest pin package available so that all pins are in a known state. Otherwise, floating pins that are not bonded in the smaller packages may result in a higher current draw. NOTE: I/O pins are configured to output low; input-only pins are configured to pullup-enabled. IRO pin connects to ground. FB_AD12 pin is pullup-enabled. DAC0, and VREFO pins are at reset state and unconnected.

Table 11. Stop Mode Adders

#	Parameter	Condition	Temperature (°C)					Units	C
			-40	25	70	85	105		
1	LPO	—	50	75	100	150	250	nA	D
2	EREFSTEN	RANGE = HGO = 0	600	650	750	850	1000	nA	D
3	IREFSTEN ¹	—	—	73	80	93	125	μA	T
4	TOD	Does not include clock source current	50	75	100	150	250	nA	D

Table 14. DAC 12-Bit Operating Behaviors

#	Characteristic	Symbol	Minimum	Typical	Maximum	Unit	C	Notes
1	Resolution	N	12	—	12	bit	T	
2	Supply current low-power mode	$I_{DDA_DAC_LP}$	—	50	100	μA	T	
3	Supply current high-power mode	$I_{DDA_DAC_HP}$	—	345	500	μA	T	
4	Full-scale Settling time (± 1 LSB) (0x080 to 0xF7F or 0xF7F to 0x080) low-power mode	$T_{s_{FS}LP}$	—	—	200	μs	T	<ul style="list-style-type: none"> $V_{DDA} = 3 V$ or $2.2 V$ $V_{REFSEL} = 1$ Temperature = $25^{\circ}C$
5	Full-scale Settling time (± 1 LSB) (0x080 to 0xF7F or 0xF7F to 0x080) high-power mode	$T_{s_{FS}HP}$	—	—	30	μs	T	<ul style="list-style-type: none"> $V_{DDA} = 3 V$ or $2.2 V$ $V_{REFSEL} = 1$ Temperature = $25^{\circ}C$
6	Code-to-code Settling time (± 1 LSB) (0xBF8 to 0xC08 or 0xC08 to 0xBF8) low-power mode	$T_{s_{C-C}LP}$	—	—	5	μs	T	<ul style="list-style-type: none"> $V_{DDA} = 3 V$ or $2.2 V$ $V_{REFSEL} = 1$ Temperature = $25^{\circ}C$
7	Code-to-code Settling time (± 1 LSB) (0xBF8 to 0xC08 or 0xC08 to 0xBF8) high-power mode	$T_{s_{C-C}HP}$	—	1	—	μs	T	<ul style="list-style-type: none"> $V_{DDA} = 3 V$ or $2.2 V$ $V_{REFSEL} = 1$ Temperature = $25^{\circ}C$
8	DAC output voltage range low (high-power mode, no load, DAC set to 0, 3 V at room temperature)	$V_{dacoutl}$	—	—	100	mV	T	
9	DAC output voltage range high (high-power mode, no load, DAC set to 0x0FFF)	$V_{dacouth}$	$V_{DACR}-100$	—	—	mV	T	
10	Integral non-linearity error	INL	—	—	± 8	LSB	T	
11	Differential non-linearity error V_{DACR} is $> 2.4 V$	DNL	—	—	± 1	LSB	T	
12	Offset error	E_O	—	± 0.4	± 3	%FSR	T	Calculated by a best fit curve from $V_{SS} + 100mV$ to $V_{REFH} - 100mV$
13	Gain error ($V_{REF} = V_{ext} = V_{DD}$)	E_G	—	± 0.1	± 0.5	%FSR	T	Calculated by a best fit curve from $V_{SS} + 100mV$ to $V_{REFH} - 100mV$
14	Power supply rejection ratio $V_{DD} \geq 2.4 V$	PSRR	60	—	—	dB	T	

Table 15. 12-bit ADC Operating Conditions (continued)

#	Symb	Characteristic	Conditions	Minimum	Typical ¹	Maximum	Unit	C
5	V _{REFL}	Ref Voltage Low	—	V _{SSAD}	V _{SSAD}	V _{SSAD}	V	D
6	V _{ADIN}	Input Voltage	—	V _{REFL}	—	V _{REFH}	V	D
7	C _{ADIN}	Input Capacitance	—	—	4	5	pF	C
8	R _{ADIN}	Input Resistance	—	—	2	5	kΩ	C
9	R _{AS}	Analog Source Resistance ³						
		12 bit mode						
		f _{ADCK} > 8 MHz	—	—	1	kΩ	C	
		4 MHz < f _{ADCK} > 8 MHz	—	—	2	kΩ	C	
		f _{ADCK} < 4 MHz	—	—	5	kΩ	C	
		10-bit mode						
		f _{ADCK} > 8MHz	—	—	2	kΩ	C	
		4 MHz < f _{ADCK} < 8 MHz	—	—	5	kΩ	C	
		f _{ADCK} < 4 MHz	—	—	10	kΩ	C	
		8-bit mode						
		f _{ADCK} > 8 MHz	—	—	5	kΩ	C	
		f _{ADCK} < 8 MHz	—	—	10	kΩ	C	
10	f _{ADCK}	ADC Conversion Clock Freq.						
		High Speed (ADLPC=0, ADHSC=1)	1.0	—	8.0	MHz	D	
		High Speed (ADLPC=0, ADHSC=0)	1.0	—	5.0	MHz	D	
		Low Power (ADLPC=1, ADHSC=1)	1.0	—	2.5	MHz	D	

¹ Typical values assume V_{DDAD} = 3.0V, Temp = 25°C, f_{ADCK}=1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

² DC potential difference.

³ External to MCU. Assumes ADLSMP=0.

Table 16. 12-bit SAR ADC Characteristics full operating range
($V_{REFH} = V_{DDAD}$, $V_{REFL} = V_{SSAD}$) (continued)

#	Symbol	Characteristic	Conditions ¹	Minimum	Typical ²	Maximum	Unit	C
7	INL	Integral Non-Linearity	12-bit single-ended mode	—	±1.0	±2.5	LSB ³	T
			10-bit single-ended mode	—	±0.5	±1.0	LSB ³	T
			8-bit single-ended mode	—	±0.3	±0.5	LSB ³	T
8	E _{ZS}	Zero-Scale Error ($V_{ADIN} = V_{SSAD}$)	12-bit single-ended mode	—	±0.7	±2.0	LSB ³	T
			10-bit single-ended mode	—	±0.4	±1.0	LSB ³	T
			8-bit single-ended mode	—	±0.2	±0.5	LSB ³	T
9	E _{FS}	Full-Scale Error ($V_{ADIN} = V_{DDAD}$)	12-bit single-ended mode	—	±1.0	±3.5	LSB ³	T
			10-bit single-ended mode	—	±0.4	±1.5	LSB ³	T
			8-bit single-ended mode	—	±0.2	±0.5	LSB ³	T
10	E _Q	Quantization Error	All modes	—	—	±0.5	LSB ³	D
11	E _{IL}	Input Leakage Error (I_{in} = leakage current (refer to DC Characteristics))	All modes	$I_{in} * R_{AS}$			mV	D
12	m	Temp Sensor Slope	-40°C to 25°C	—	1.646	—	mV/xC	C
			25°C to 125°C	—	1.769	—	mV/xC	C
13	V _{TEMP25}	Temp Sensor Voltage	25°C	—	701.2	—	mV	C

¹ All accuracy numbers assume the ADC is calibrated with $V_{REFH}=V_{DDAD}$.

² Typical values assume $V_{DDAD} = 3.0V$, Temp = 25°C, $f_{ADCK}=2.0MHz$ unless otherwise stated. Typical values are for reference only and are not tested in production.

³ 1 LSB = $(V_{REFH} - V_{REFL})/2^N$

3.10 MCG and External Oscillator (XOSC) Characteristics

Table 17. MCG (Temperature Range = -40 to 105°C Ambient)

#	Rating	Symbol	Min	Typical	Max	Unit	C	
1	Internal reference startup time	t_{irefst}	—	55	100	μs	D	
2	Average internal reference frequency	f_{int_ft}	factory trimmed at $V_{DD}=3.0V$ and temp=25°C	—	31.25	—	kHz	C
			user trimmed	31.25	—	39.0625	KHz	C
3	DCO output frequency range - trimmed	f_{dco_t}	Low range (DRS=00)	16	—	20	MHz	C
			Mid range (DRS=01)	32	—	40	MHz	C
			High range ¹ (DRS=10)	40	—	60	MHz	C
4	Resolution of trimmed DCO output frequency at fixed voltage and temperature	$\Delta f_{dco_res_t}$	with FTRIM	—	± 0.1	± 0.2	% f_{dco}	C
			without FTRIM	—	± 0.2	± 0.4	% f_{dco}	C

Table 18. XOSC (Temperature Range = -40 to 105°C Ambient)

#	Characteristic		Symbol	Minimum	Typical ¹	Maximum	Unit
1	Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1)	• Low range (RANGE = 0)	f_{lo}	32	—	38.4	kHz
		• High range (RANGE = 1), • FEE or FBE mode ²	f_{hi-lll}	1	—	5	MHz
		• High range (RANGE = 1), • PEE or PBE mode ³	f_{hi-pll}	1	—	16	MHz
		• High range (RANGE = 1), • High gain (HGO = 1), • FBELP mode	f_{hi-hgo}	1	—	16	MHz
		• High range (RANGE = 1), • Low power (HGO = 0), • FBELP mode	f_{hi-lp}	1	—	8	MHz
2	Load capacitors	C_1 C_2	See Note ⁴				
3	Feedback resistor	Low range (32 kHz to 38.4 kHz)	R_F	—	10	—	M Ω
		High range (1 MHz to 16 MHz)	—	—	1	—	
4	Series resistor — Low range	Low Gain (HGO = 0)	R_S	—	0	—	k Ω
		High Gain (HGO = 1)		—	100	—	
5	Series resistor — High range	• Low Gain (HGO = 0)	R_S	—	0	—	k Ω
		• High Gain (HGO = 1)		—	—	—	
		≥ 8 MHz		—	0	0	
		4 MHz		—	0	10	
		1 MHz		—	0	20	
6	Crystal start-up time ^{5, 6}	Low range, low gain (RANGE=0,HGO=0)	t_{CSTL}	—	200	—	ms
		Low range, high gain (RANGE=0,HGO=1)		—	400	—	
		High range, low gain (RANGE=1,HGO=0)	t_{CSTH}	—	5	—	
		High range, high gain (RANGE=1, HGO=1)		—	15	—	

¹ Data in Typical column was characterized at 3.0 V, 25°C or is typical recommended value.

² When MCG is configured for FEE or FBE mode, input clock source must be divisible using RDIV to within the range of 31.25 kHz to 39.0625 kHz.

³ When MCG is configured for PEE or PBE mode, input clock source must be divisible using RDIV to within the range of 1 MHz to 2 MHz.

⁴ See crystal or resonator manufacturer's recommendation.

⁵ This parameter is characterized and not tested on each device.

⁶ Proper PC board layout procedures must be followed to achieve specifications.

3.11 Mini-FlexBus Timing Specifications

A multi-function external bus interface called Mini-FlexBus is provided with basic functionality to interface to slave-only devices up to a maximum bus frequency of 25.1666 MHz. It can be directly connected to asynchronous or synchronous devices such as external boot ROMs, flash memories, gate-array logic, or other simple target (slave) devices with little or no additional circuitry. For asynchronous devices, a simple chip-select based interface can be used.

All processor bus timings are synchronous; that is, input setup/hold and output delay are given in respect to the rising edge of a reference clock, MB_CLK. The MB_CLK frequency is half the internal system bus frequency.

The following timing numbers indicate when data is latched or driven onto the external bus, relative to the Mini-FlexBus output clock (MB_CLK). All other timing relationships can be derived from these values.

Table 19. Mini-FlexBus AC Timing Specifications

#	Characteristic	Symbol	Min	Max	Unit	C
1	Frequency of Operation	—	—	25.1666	MHz	—
2	Clock Period	MB1	39.73	—	ns	D
3	Output Valid ¹	MB2	—	20	ns	T
4	Output Hold ¹	MB3	1.0	—	ns	D
5	Input Setup ²	MB4	22	—	ns	T
6	Input Hold ²	MB5	10	—	ns	D

¹ Specification is valid for all MB_A[19:0], MB_D[7:0], MB_CS[1:0], MB_OE, MB_R/W, and MB_ALE.

² Specification is valid for all MB_D[7:0].

3.12 AC Characteristics

This section describes ac timing characteristics for each peripheral system.

3.12.1 Control Timing

Table 20. Control Timing

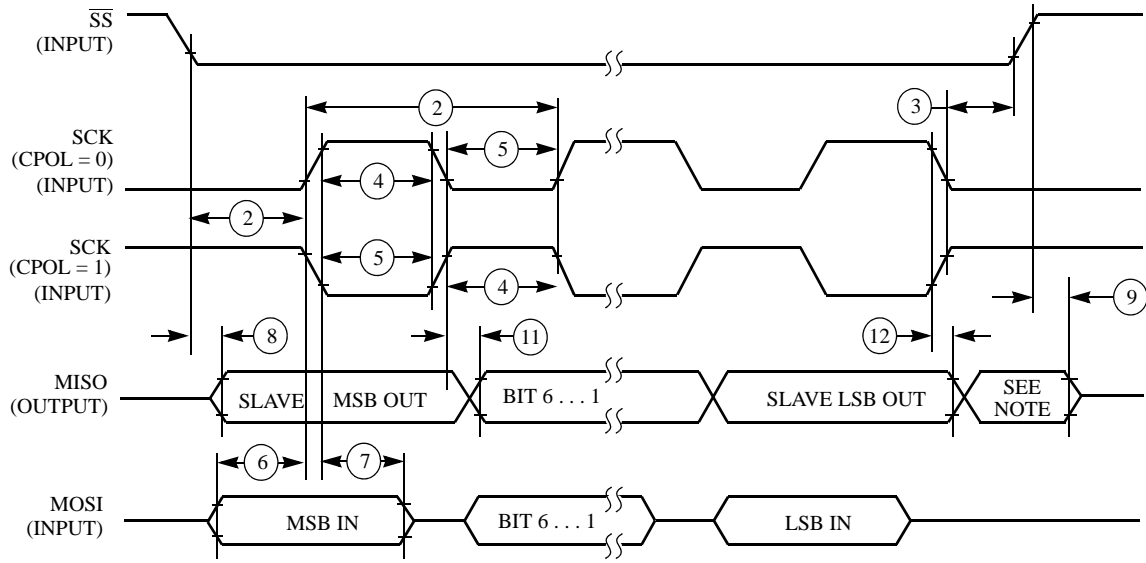
#	Parameter	Symbol	Minimum	Typical ¹	Maximum	Unit	C	
1	Bus frequency ($t_{cyc} = 1/f_{Bus}$)							
		$V_{DD} \geq 1.8\text{ V}$	f_{Bus}	dc	—	10	MHz	D
		$V_{DD} > 2.1\text{ V}$	f_{Bus}	dc	—	20	MHz	D
		$V_{DD} > 2.4\text{ V}$	f_{Bus}	dc	—	25.165	MHz	D
2	Internal low-power oscillator period	t_{LPO}	700	1000	1300	μs	P	
3	External reset pulse width ²	t_{extrst}	100	—	—	ns	D	
	($t_{cyc} = 1/f_{Self_reset}$)							
4	Reset low drive	t_{rstdrv}	$66 \times t_{cyc}$	—	—	ns	D	
5	Active background debug mode latch setup time	t_{MSSU}	500	—	—	ns	D	
6	Active background debug mode latch hold time	t_{MSH}	100	—	—	ns	D	
7	IRQ pulse width	t_{LIH}, t_{IHIL}	100 $1.5 \times t_{cyc}$	—	—	ns	D	
	• Asynchronous path ²							
	• Synchronous path ³							
8	KBIPx pulse width	t_{LIH}, t_{IHIL}	100 $1.5 \times t_{cyc}$	—	—	ns	D	
	• Asynchronous path ²							
	• Synchronous path ³							
9	Port rise and fall time (load = 50 pF) ⁴ , Low Drive							
		Slew rate control disabled (PTxSE = 0)	t_{Rise}, t_{Fall}	—	11	—	ns	D
		Slew rate control enabled (PTxSE = 1)	t_{Rise}, t_{Fall}	—	35	—	ns	D
		Slew rate control disabled (PTxSE = 0)	t_{Rise}, t_{Fall}	—	40	—	ns	D
		Slew rate control enabled (PTxSE = 1)	t_{Rise}, t_{Fall}	—	75	—	ns	D

¹ Typical values are based on characterization data at $V_{DD} = 5.0\text{ V}$, $25\text{ }^\circ\text{C}$ unless otherwise stated.

² This is the shortest pulse that is guaranteed to be recognized as a reset pin request. Shorter pulses are not guaranteed to override reset requests from internal sources.

³ This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized in that case.

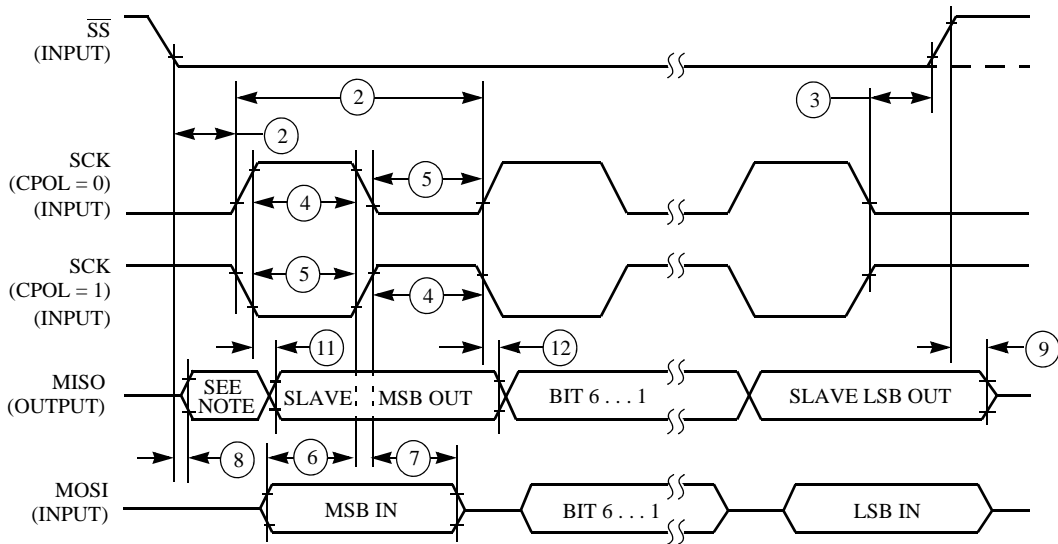
⁴ Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range $-40\text{ }^\circ\text{C}$ to $105\text{ }^\circ\text{C}$.



NOTE:

1. Not defined, but normally MSB of character just received

Figure 17. SPI Slave Timing (CPHA = 0)



NOTE:

1. Not defined, but normally LSB of character just received

Figure 18. SPI Slave Timing (CPHA = 1)

3.14 Flash Specifications

This section provides details about program/erase times and program-erase endurance for the Flash memory.

Program and erase operations do not require any special power sources other than the normal V_{DD} supply. For more detailed information about program/erase operations, see the Memory chapter in the Reference Manual for this device (MCF51JE256RM).

Table 23. Flash Characteristics

#	Characteristic	Symbol	Minimum	Typical	Maximum	Unit	C
1	Supply voltage for program/erase -40°C to 105°C	$V_{\text{prog/erase}}$	1.8	—	3.6	V	D
2	Supply voltage for read operation	V_{Read}	1.8	—	3.6	V	D
3	Internal FCLK frequency ¹	f_{FCLK}	150	—	200	kHz	D
4	Internal FCLK period (1/FCLK)	t_{FcyC}	5	—	6.67	μs	D
5	Byte program time (random location) ²	t_{prog}	9			t_{FcyC}	P
6	Byte program time (burst mode) ²	t_{Burst}	4			t_{FcyC}	P
7	Page erase time ²	t_{Page}	4000			t_{FcyC}	P
8	Mass erase time ²	t_{Mass}	20,000			t_{FcyC}	P
9	Program/erase endurance ³ T_L to T_H = -40°C to +105°C T = 25°C		10,000 —	— 100,000	— —	cycles	C
10	Data retention ⁴	$t_{\text{D_ret}}$	15	100	—	years	C

¹ The frequency of this clock is controlled by a software setting.

² These values are hardware state machine controlled. User code does not need to count cycles. This information supplied for calculating approximate time to program and erase.

³ **Typical endurance for flash** was evaluated for this product family on the HC9S12Dx64. For additional information on how Freescale defines typical endurance, please refer to Engineering Bulletin EB619, *Typical Endurance for Nonvolatile Memory*.

⁴ **Typical data retention** values are based on intrinsic capability of the technology measured at high temperature and de-rated to 25°C using the Arrhenius equation. For additional information on how Freescale defines typical data retention, please refer to Engineering Bulletin EB618, *Typical Data Retention for Nonvolatile Memory*.

3.15 USB Electricals

The USB electricals for the USB On-the-Go module conform to the standards documented by the Universal Serial Bus Implementers Forum. For the most up-to-date standards, visit <http://www.usb.org>.

If the Freescale USB On-the-Go implementation has electrical characteristics that deviate from the standard or require additional information, this space would be used to communicate that information.

Table 24. Internal USB 3.3 V Voltage Regulator Characteristics

#	Characteristic	Symbol	Minimum	Typical	Maximum	Unit	C
1	Regulator operating voltage	V_{regin}	3.9	—	5.5	V	C
2	VREG output	V_{regout}	3	3.3	3.75	V	P

Table 24. Internal USB 3.3 V Voltage Regulator Characteristics (continued)

#	Characteristic	Symbol	Minimum	Typical	Maximum	Unit	C
3	V _{USB33} input with internal VREG disabled	V _{usb33in}	3	3.3	3.6	V	C
4	VREG Quiescent Current	I _{VRQ}	—	0.5	—	mA	C

3.16 VREF Electrical Specifications

Table 25. VREF Electrical Specifications

#	Characteristic	Symbol	Minimum	Maximum	Unit	C
1	Supply voltage	V _{DDA}	1.80	3.6	V	C
2	Temperature	T _A	−40	105	°C	C
3	Output Load Capacitance	C _L	—	100	nf	D
4	Maximum Load	—	—	10	mA	—
5	Voltage Reference Output with Factory Trim. V _{DD} = 3 V.	V _{out}	1.148	1.152	V	P
6	Temperature Drift (V _{min} - V _{max} across the full temperature range)	T _{drift}	—	25	mV ¹	T
7	Aging Coefficient ²	A _c	—	60	μV/year	C
8	Powered down Current (Off Mode, VREFEN = 0, VRSTEN = 0)	I	—	0.10	μA	C
9	Bandgap only (MODE_LV[1:0] = 00)	I	—	75	μA	T
10	Low-Power buffer (MODE_LV[1:0] = 01)	I	—	125	μA	T
11	Tight-Regulation buffer (MODE_LV[1:0] = 10)	I	—	1.1	mA	T
12	Load Regulation (MODE_LV = 10)	—	—	100	μV/mA	C
13	Line Regulation MODE = 1:0, Tight Regulation VDD < 2.3 V, Delta VDDA = 100 mV, VREFH = 1.2 V driven externally with VREFO disabled. (Power Supply Rejection)	DC	70	—	dB	C

¹ See typical chart below.

² Linear reliability model (1008 hours stress at 125°C = 10 years operating life) used to calculate Aging μV/year. Vrefo data recorded per month.

Table 26. VREF Limited Range Operating Behaviors

#	Characteristic	Symbol	Minimum	Maximum	Unit	C
1	Voltage Reference Output with Factory Trim	V_{out}	1.149	1.152	mV	T
2	Temperature Drift ($V_{min} - V_{max}$ Temperature range from 0° C to 50° C)	Tdrift	—	3	mV ¹	T

¹ See typical chart that follows (Figure 19).

Figure 19. Typical VREF Output vs Temperature

Figure 20. Typical VREF Output vs V_{DD}

- Open a browser to the Freescale® website (<http://www.freescale.com>), and enter the appropriate document number (from Table 28) in the “Enter Keyword” search box at the top of the page.

5 Revision History

This section lists major changes between versions of the MCF51JE256 Data Sheet.

Table 29. Revision History

Revision	Date	Description
0	March/April 09	Initial Draft
1	July 2009	<ul style="list-style-type: none"> • Revised to follow standard template. • Removed extraneous headings from the TOC. • Corrected units for Monotonicity to be blank in for the DAC specification. • Updated ADC characteristic tables to include 16-Bit SAR in headings.
2	July 2009	<ul style="list-style-type: none"> • Changed MCG (XOSC) Electricals Table - Row 2, Average Internal Reference Frequency typical value from 32.768 to 31.25
3	April 2010	<ul style="list-style-type: none"> • Updated Thermal Characteristics table. Reinserted the 81 and 104 MapBGA devices. • Revised the ESD and Latch-Up Protection Characteristic description to read: Latch-up Current at $T_A = 125^\circ\text{C}$. • Changed Table 9. DC Characteristics rows 2 and 4, to 1.8 V, $I_{\text{Load}} = -600\text{ mA}$ conditions to 1.8 V, $I_{\text{Load}} = 600\mu\text{A}$ respectively. • Corrected the 16-bit SAR ADC Operating Condition table Ref Voltage High Min value to be 1.13 instead of 1.15. • Updated the ADC electricals. • Inserted the Mini-FlexBus Timing Specifications. • Added a Temp Drift parameter to the VREF Electrical Specifications. • Removed the S08 Naming Convention diagram. • Updated the Orderable Part Number Summary to include the Freescale Part Number suffixes. • Completed the Package Description table values. • Changed the 80LQFP package drawing from 98ARL10530D to 98ASS23174W. • Updated electrical characteristic data.