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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8/300H
Core Size	16-Bit
Speed	18MHz
Connectivity	I²C, SCI
Peripherals	PWM, WDT
Number of I/O	45
Program Memory Size	56KB (56K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df36087fpv

Section 7 ROM

The features of the 56-kbyte flash memories built into the flash memory (F-ZTAT) version are summarized below.

- Programming/erase methods

  The flash memory is programmed 128 bytes at a time. Erase is performed in single-block units. The flash memory is configured as follows: 1 kbyte × 4 blocks, 28 kbytes × 1 block, 16 kbytes × 1 block, and 8 kbytes × 1 block for H8/36087F. To erase the entire flash memory, each block must be erased in turn.
- Reprogramming capability

  The flash memory can be reprogrammed up to 1,000 times.
- On-board programming

  On-board programming/erasing can be done in boot mode, in which the boot program built into the chip is started to erase or program of the entire flash memory. In normal user program mode, individual blocks can be erased or programmed.
- Programmer mode

  Flash memory can be programmed/erased in programmer mode using a PROM programmer, as well as in on-board programming mode.
- Automatic bit rate adjustment

  For data transfer in boot mode, this LSI's bit rate can be automatically adjusted to match the transfer bit rate of the host.
- Programming/erasing protection

  Sets software protection against flash memory programming/erasing.
- Power-down mode

  Operation of the power supply circuit can be partly halted in subactive mode. As a result, flash memory can be read with low power consumption.

7.1 Block Configuration

Figure 7.1 shows the block configuration of flash memory. The thick lines indicate erasing units, the narrow lines indicate programming units, and the values are addresses. The 56-kbyte flash memory is divided into 1 kbyte × 4 blocks, 28 kbytes × 1 block, 16 kbytes × 1 block, and 8 kbytes × 1 block. Erasing is performed in these units. Programming is performed in 128-byte units starting from an address with lower eight bits H'00 or H'80.

Table 7.3 System Clock Frequencies for which Automatic Adjustment of LSI Bit Rate is Possible

Host Bit Rate	System Clock Frequency Range of LSI
19,200 bps	16 to 18 MHz
9,600 bps	8 to 16 MHz
4,800 bps	4 to 16 MHz
2,400 bps	4 to 16 MHz

7.3.2 Programming/Erasing in User Program Mode

On-board programming/erasing of an individual flash memory block can also be performed in user program mode by branching to a user program/erase control program. The user must set branching conditions and provide on-board means of supplying programming data. The flash memory must contain the user program/erase control program or a program that provides the user program/erase control program from external memory. As the flash memory itself cannot be read during programming/erasing, transfer the user program/erase control program to on-chip RAM, as in boot mode. Figure 7.2 shows a sample procedure for programming/erasing in user program mode. Prepare a user program/erase control program in accordance with the description in section 7.4, Flash Memory Programming/Erasing.

7.4 Flash Memory Programming/Erasing

A software method using the CPU is employed to program and erase flash memory in the on-board programming modes. Depending on the FLMCR1 setting, the flash memory operates in one of the following four modes: Program mode, program-verify mode, erase mode, and erase-verify mode. The programming control program in boot mode and the user program/erase control program in user program mode use these operating modes in combination to perform programming/erasing. Flash memory programming and erasing should be performed in accordance with the descriptions in section 7.4.1, Program/Program-Verify and section 7.4.2, Erase/Erase-Verify, respectively.

7.4.1 Program/Program-Verify

When writing data or programs to the flash memory, the program/program-verify flowchart shown in figure 7.3 should be followed. Performing programming operations according to this flowchart will enable data or programs to be written to the flash memory without subjecting the chip to voltage stress or sacrificing program data reliability.

1. Programming must be done to an empty address. Do not reprogram an address to which programming has already been performed.
2. Programming should be carried out 128 bytes at a time. A 128-byte data transfer must be performed even if writing fewer than 128 bytes. In this case, H'FF data must be written to the extra addresses.
3. Prepare the following data storage areas in RAM: A 128-byte programming data area, a 128-byte reprogramming data area, and a 128-byte additional-programming data area. Perform reprogramming data computation according to table 7.4, and additional programming data computation according to table 7.5.
4. Consecutively transfer 128 bytes of data in byte units from the reprogramming data area or additional-programming data area to the flash memory. The program address and 128-byte data are latched in the flash memory. The lower 8 bits of the start address in the flash memory destination area must be H'00 or H'80.
5. The time during which the P bit is set to 1 is the programming time. Table 7.6 shows the allowable programming times.
6. The watchdog timer (WDT) is set to prevent overprogramming due to program runaway, etc. An overflow cycle of approximately 6.6 ms is allowed.
7. For a dummy write to a verify address, write 1-byte data H'FF to an address whose lower 2 bits are B'00. Verify data can be read in words or in longwords from the address to which a dummy write was performed.

- P11/PWM pin

Register	PMR1	PCR1	
Bit Name	**PWM**	**PCR11**	**Pin Function**
Setting value	0	0	P11 input pin
		1	P11 output pin
	1	X	PWM output pin

[Legend]
X: Don't care.

- P10/TMOW pin

Register	PMR1	PCR1	
Bit Name	**TMOW**	**PCR10**	**Pin Function**
Setting value	0	0	P10 input pin
		1	P10 output pin
	1	X	TMOW output pin

[Legend]
X: Don't care.

9.4.1 Port Mode Register 5 (PMR5)

PMR5 switches the functions of pins in port 5.

Bit	Bit Name	Initial Value	R/W	Description
7	POF57	0	R/W	When the bit is set to 1, the corresponding pin is cut off by PMOS and it functions as the NMOS open-drain output. When cleared to 0, the pin functions as the CMOS output.
6	POF56	0	R/W	
5	WKP5	0	R/W	This bit selects the function of pin P55/$\overline{\text{WKP5}}$/$\overline{\text{ADTRG}}$. 0: General I/O port 1: $\overline{\text{WKP5}}$/$\overline{\text{ADTRG}}$ input pin
4	WKP4	0	R/W	This bit selects the function of pin P54/$\overline{\text{WKP4}}$. 0: General I/O port 1: $\overline{\text{WKP4}}$ input pin
3	WKP3	0	R/W	This bit selects the function of pin P53/$\overline{\text{WKP3}}$. 0: General I/O port 1: $\overline{\text{WKP3}}$ input pin
2	WKP2	0	R/W	This bit selects the function of pin P52/$\overline{\text{WKP2}}$. 0: General I/O port 1: $\overline{\text{WKP2}}$ input pin
1	WKP1	0	R/W	This bit selects the function of pin P51/$\overline{\text{WKP1}}$. 0: General I/O port 1: $\overline{\text{WKP1}}$ input pin
0	WKP0	0	R/W	This bit selects the function of pin P50/$\overline{\text{WKP0}}$. 0: General I/O port 1: $\overline{\text{WKP0}}$ input pin

- P74/TMRIV pin

Register	PCR7	
Bit Name	**PCR74**	**Pin Function**
Setting Value	0	P74 input/TMRIV input pin
	1	P74 output/TMRIV input pin

- P72/TXD_2 pin

Register	PMR1	PCR7	
Bit Name	**TXD2**	**PCR72**	**Pin Function**
Setting Value	0	0	P72 input pin
		1	P72 output pin
	1	X	TXD_2 output pin

[Legend]
X: Don't care.

- P71/RXD_2 pin

Register	SCR3_2	PCR7	
Bit Name	**RE**	**PCR71**	**Pin Function**
Setting Value	0	0	P71 input pin
		1	P71 output pin
	1	X	RXD_2 input pin

[Legend]
X: Don't care.

- P70/SCK3_2 pin

Register	SCR3_2		SMR2	PCR7	
Bit Name	**CKE1**	**CKE0**	**COM**	**PCR70**	**Pin Function**
Setting Value	0	0	0	0	P70 input pin
				1	P70 output pin
	0	0	1	X	SCK3_2 output pin
	0	1	X	X	SCK3_2 output pin
	1	X	X	X	SCK3_2 input pin

[Legend]
X: Don't care.

10.5 Interrupt Source

There are five kinds of RTC interrupts: week interrupts, day interrupts, hour interrupts, minute interrupts, and second interrupts.

When using an interrupt, initiate the RTC last after other registers are set. Do not set multiple interrupt enable bits in RTCCR2 simultaneously to 1.

When an interrupt request of the RTC occurs, the IRRTA flag in IRR1 is set to 1. When clearing the flag, write 0.

Table 10.2 Interrupt Source

Interrupt Name	Interrupt Source	Interrupt Enable Bit
Overflow interrupt	Occurs when the free running counter is overflown.	FOIE
Week periodic interrupt	Occurs every week when the day-of-week date register value becomes 0.	WKIE
Day periodic interrupt	Occurs every day when the day-of-week date register is counted.	DYIE
Hour periodic interrupt	Occurs every hour when the hour date register is counted.	HRIE
Minute periodic interrupt	Occurs every minute when the minute date register is counted.	MNIE
Second periodic interrupt	Occurs every second when the second date register is counted.	SCIE

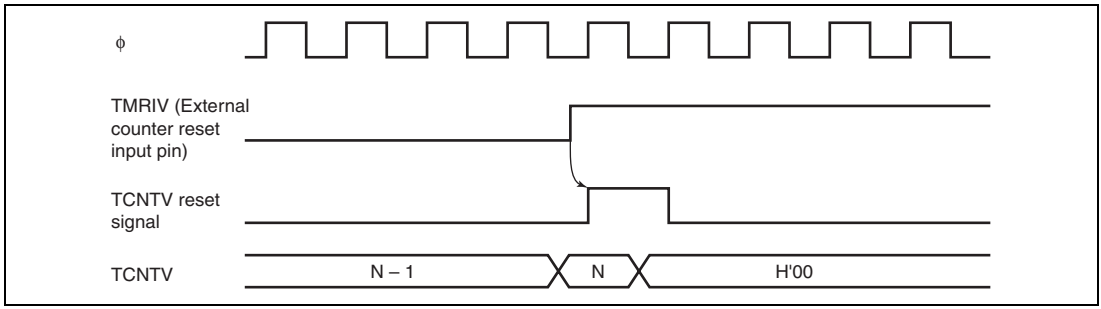

Figure 12.8 Clear Timing by TMRIV Input

12.5 Timer V Application Examples

12.5.1 Pulse Output with Arbitrary Duty Cycle

Figure 12.9 shows an example of output of pulses with an arbitrary duty cycle.

1. Set bits CCLR1 and CCLR0 in TCRV0 so that TCNTV will be cleared by compare match with TCORA.
2. Set bits OS3 to OS0 in TCSRV so that the output will go to 1 at compare match with TCORA and to 0 at compare match with TCORB.
3. Set bits CKS2 to CKS0 in TCRV0 and bit ICKS0 in TCRV1 to select the desired clock source.
4. With these settings, a waveform is output without further software intervention, with a period determined by TCORA and a pulse width determined by TCORB.

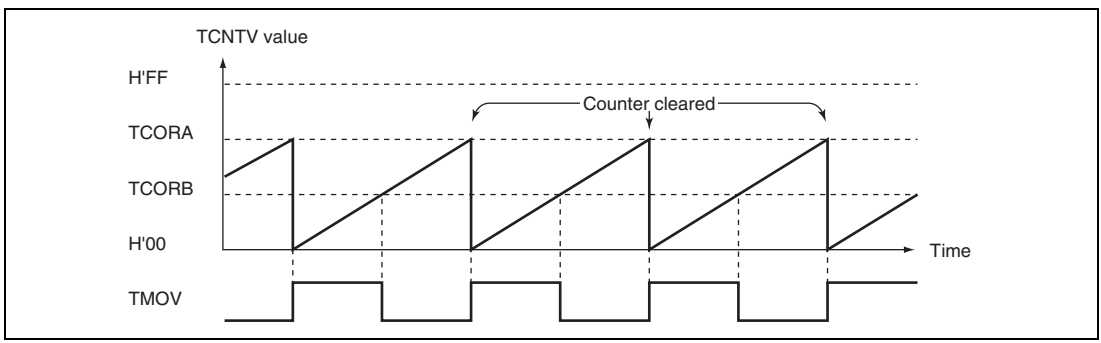

Figure 12.9 Pulse Output Example

Figures 13.27 and 13.28 show examples of operation in reset synchronous PWM mode.

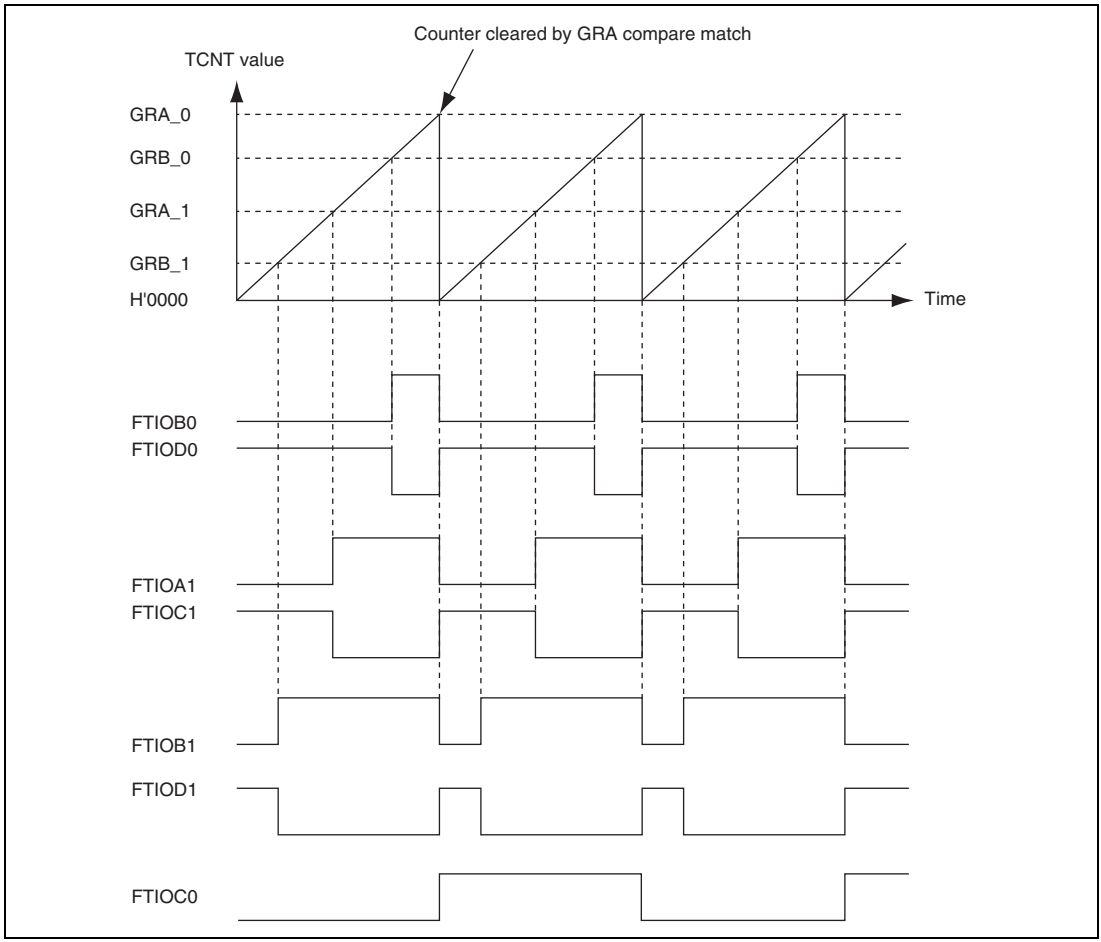

Figure 13.27 Example of Reset Synchronous PWM Mode Operation (OLS0 = OLS1 = 1)

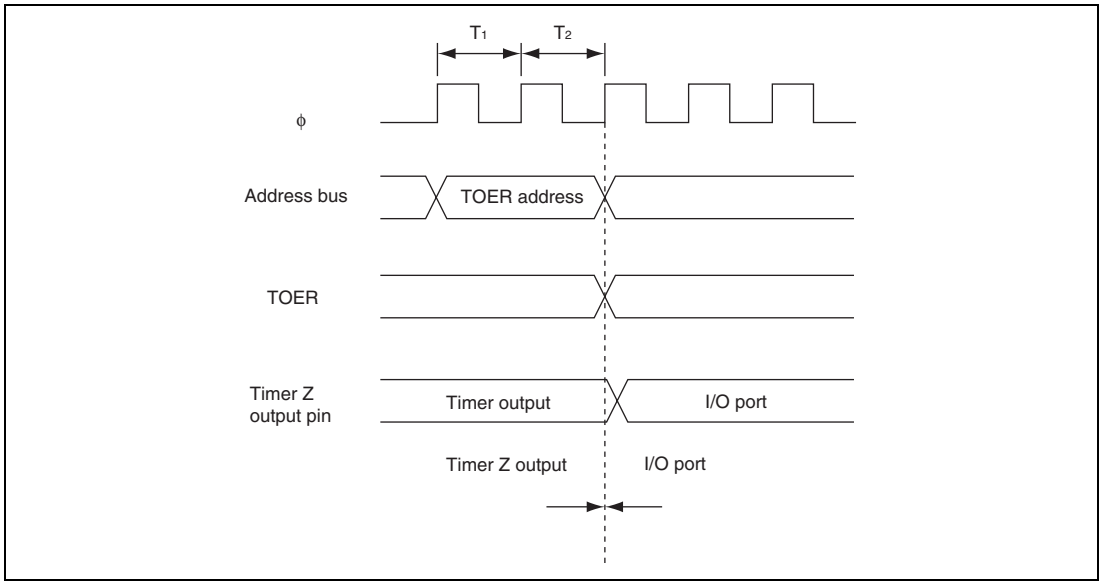

Figure 13.44 Example of Output Disable Timing of Timer Z by Writing to TOER

2. Output Disable Timing of Timer Z by External Trigger: When P54/$\overline{\text{WKP4}}$ is set as a $\overline{\text{WKP4}}$ input pin, and low level is input to $\overline{\text{WKP4}}$, the master enable bit in TOER is set to 1 and the output of timer Z will be disabled.

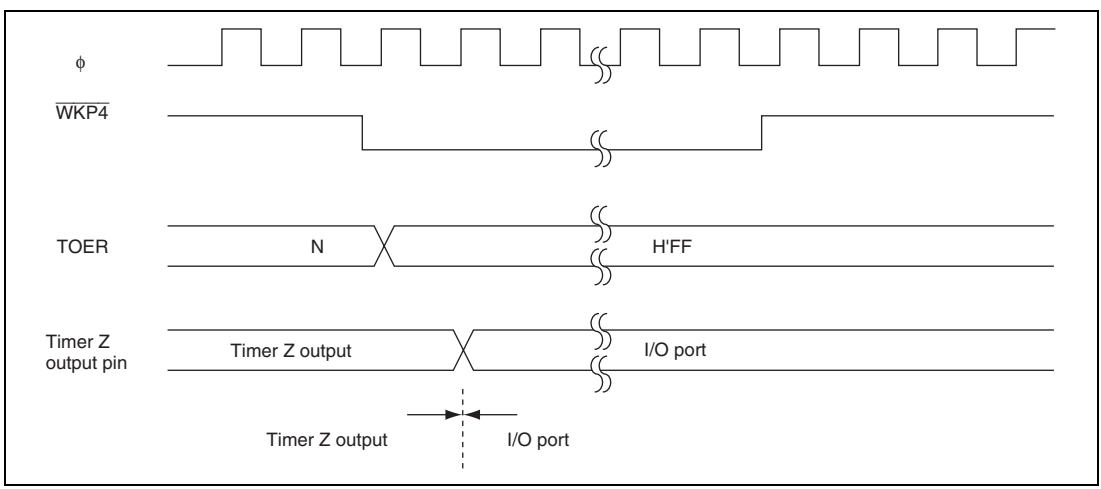

Figure 13.45 Example of Output Disable Timing of Timer Z by External Trigger

13.5.2 Status Flag Clearing Timing

The status flag can be cleared by writing 0 after reading 1 from the CPU. Figure 13.51 shows the timing in this case.

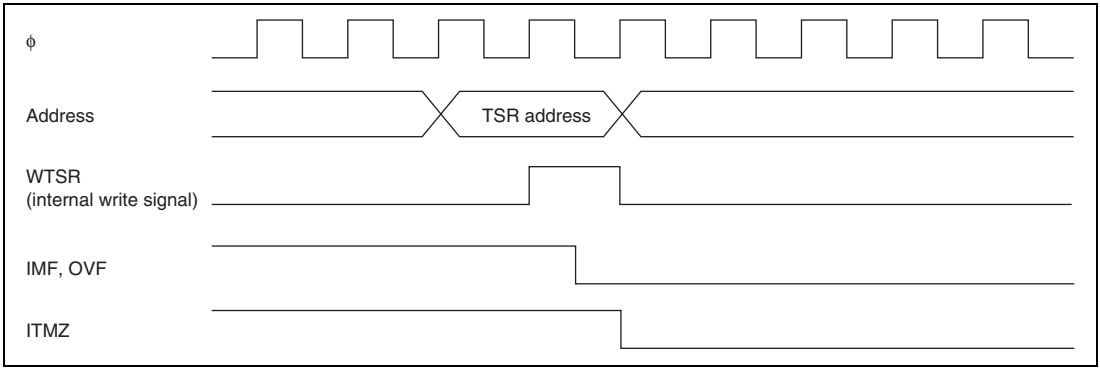

Figure 13.51 Status Flag Clearing Timing

TOCR has been set to H'06. Compare match B0 and compare match C0 are used. The FTIOB0 pin is in the 1 output state, and is set to the toggle output or the 0 output by compare match B0.
When BCLR#2, @TOCR is executed to clear the TOC0 bit (the FTIOC0 signal is low) and compare match B0 occurs at the same timing as shown below, the H'02 writing to TOCR has priority and compare match B0 does not drive the FTIOB0 signal low; the FTIOB0 signal remains high.

Bit	7	6	5	4	3	2	1	0
TOCR	TOD1	TOC1	TOB1	TOA1	TOD0	TOC0	TOB0	TOA0
Set value	0	0	0	0	0	1	1	0

BCLR#2, @TOCR
(1) TOCR read operation: Read H'06
(2) Modify operation: Modify H'06 to H'02
(3) Write operation to TOCR: Write H'02

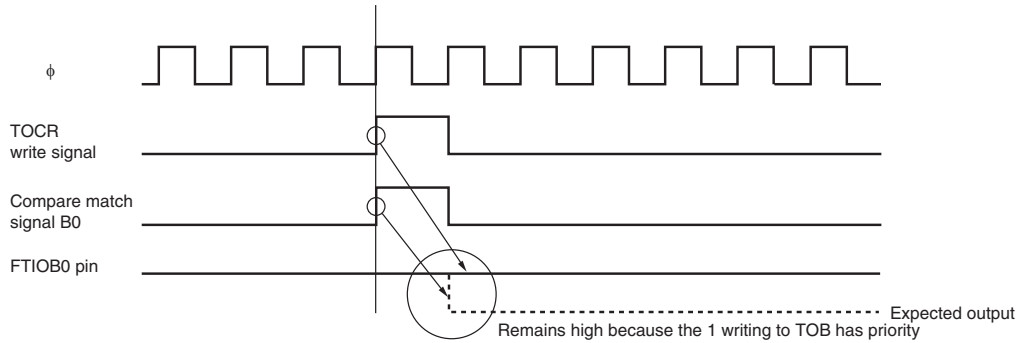

Figure 13.59 When Compare Match and Bit Manipulation Instruction to TOCR Occur at the Same Timing

15.2 Input/Output Pin

Table 15.1 shows the 14-bit PWM pin configuration.

Table 15.1 Pin Configuration

Name	Abbreviation	I/O	Function
14-bit PWM square-wave output	PWM	Output	14-bit PWM square-wave output pin

15.3 Register Descriptions

The 14-bit PWM has the following registers.

- PWM control register (PWCR)
- PWM data register U (PWDRU)
- PWM data register L (PWDRL)

15.3.1 PWM Control Register (PWCR)

PWCR selects the conversion period.

Bit	Bit Name	Initial Value	R/W	Description
7 to 1	—	All 1	—	Reserved These bits are always read as 1, and cannot be modified.
0	PWCR0	0	R/W	Clock Select 0: The input clock is $\phi/2$ ($t\phi = 2/\phi$) — The conversion period is $16384/\phi$, with a minimum modulation width of $1/\phi$ 1: The input clock is $\phi/4$ ($t\phi = 4/\phi$) — The conversion period is $32768/\phi$, with a minimum modulation width of $2/\phi$

[Legend]

$t\phi$: Period of PWM clock input

18.6 Usage Notes

18.6.1 Permissible Signal Source Impedance

This LSI's analog input is designed such that conversion accuracy is guaranteed for an input signal for which the signal source impedance is 5 kΩ or less. This specification is provided to enable the A/D converter's sample-and-hold circuit input capacitance to be charged within the sampling time; if the sensor output impedance exceeds 5 kΩ, charging may be insufficient and it may not be possible to guarantee A/D conversion accuracy. However, for A/D conversion in single mode with a large capacitance provided externally, the input load will essentially comprise only the internal input resistance of 10 kΩ, and the signal source impedance is ignored. However, as a low-pass filter effect is obtained in this case, it may not be possible to follow an analog signal with a large differential coefficient (e.g., 5 mV/µs or greater) (see figure 18.6). When converting a high-speed analog signal or converting in scan mode, a low-impedance buffer should be inserted.

18.6.2 Influences on Absolute Accuracy

Adding capacitance results in coupling with GND, and therefore noise in GND may adversely affect absolute accuracy. Be sure to make the connection to an electrically stable GND.

Care is also required to ensure that filter circuits do not interfere with digital signals or act as antennas on the mounting board.

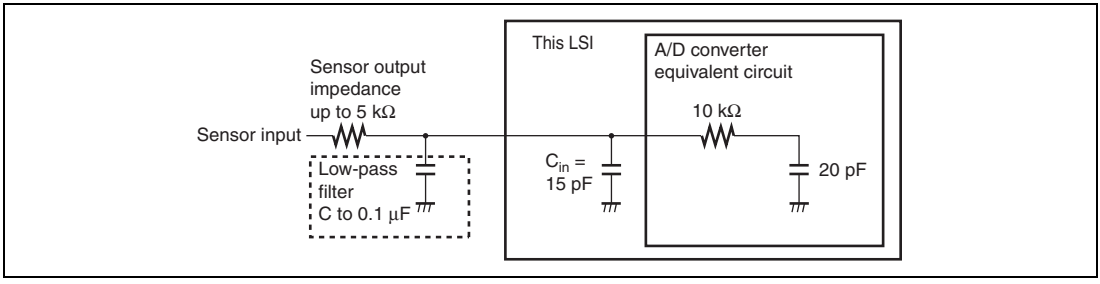

Figure 18.6 Analog Input Circuit Example

Register	Abbre-viation	Bit No	Address	Module Name	Data Bus Width	Access State
System control register 1	SYSCR1	8	H'FFF0	Low power	8	2
System control register 2	SYSCR2	8	H'FFF1	Low power	8	2
Interrupt edge select register 1	IEGR1	8	H'FFF2	Interrupt	8	2
Interrupt edge select register 2	IEGR2	8	H'FFF3	Interrupt	8	2
Interrupt enable register 1	IENR1	8	H'FFF4	Interrupt	8	2
Interrupt enable register 2	IENR2	8	H'FFF5	Interrupt	8	2
Interrupt flag register 1	IRR1	8	H'FFF6	Interrupt	8	2
Interrupt flag register 2	IRR2	8	H'FFF7	Interrupt	8	2
Wakeup interrupt flag register	IWPR	8	H'FFF8	Interrupt	8	2
Module standby control register 1	MSTCR1	8	H'FFF9	Low power	8	2
Module standby control register 2	MSTCR2	8	H'FFFA	Low power	8	2
—	—	—	H'FFFB to H'FFFF	—	—	—

Note: * WDT: Watchdog timer

Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module Name
ADDRC	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	A/D converter
	AD1	AD0	—	—	—	—	—	—	
ADDRD	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	
	AD1	AD0	—	—	—	—	—	—	
ADCSR	ADF	ADIE	ADST	SCAN	CKS	CH2	CH1	CH0	
ADCR	TRGE	—	—	—	—	—	—	—	
—	—	—	—	—	—	—	—	—	—
PWDRL	PWDRL7	PWDRL6	PWDRL5	PWDRL4	PWDRL3	PWDRL2	PWDRL1	PWDRL0	14-bit PWM
PWDRU	—	—	PWDRU5	PWDRU4	PWDRU3	PWDRU2	PWDRU1	PWDRU0	
PWCR	—	—	—	—	—	—	—	PWCR0	
TCSRWD	B6WI	TCWE	B4WI	TCSRWE	B2WI	WDON	B0WI	WRST	WDT*
TCWD	TCWD7	TCWD6	TCWD5	TCWD4	TCWD3	TCWD2	TCWD1	TCWD0	
TMWD	—	—	—	—	CKS3	CKS2	CKS1	CKS0	
—	—	—	—	—	—	—	—	—	—
ABRKCR	RTINTE	CSEL1	CSEL0	ACMP2	ACMP1	ACMP0	DCMP1	DCMP0	Address break
ABRKSR	ABIF	ABIE	—	—	—	—	—	—	
BARH	BARH7	BARH6	BARH5	BARH4	BARH3	BARH2	BARH1	BARH0	
BARL	BARL7	BARL6	BARL5	BARL4	BARL3	BARL2	BARL1	BARL0	
BDRH	BDRH7	BDRH6	BDRH5	BDRH4	BDRH3	BDRH2	BDRH1	BDRH0	
BDRL	BDRL7	BDRL6	BDRL5	BDRL4	BDRL3	BDRL2	BDRL1	BDRL0	
—	—	—	—	—	—	—	—	—	—
PUCR1	PUCR17	PUCR16	PUCR15	PUCR14	—	PUCR12	PUCR11	PUCR10	I/O port
PUCR5	—	—	PUCR55	PUCR54	PUCR53	PUCR52	PUCR51	PUCR50	
PDR1	P17	P16	P15	P14	—	P12	P11	P10	
PDR2	—	—	—	P24	P23	P22	P21	P20	
PDR3	P37	P36	P35	P34	P33	P32	P31	P30	
PDR5	P57	P56	P55	P54	P53	P52	P51	P50	
PDR6	P67	P66	P65	P64	P63	P62	P61	P60	
PDR7	—	P76	P75	P74	—	P72	P71	P70	
PDR8	P87	P86	P85	—	—	—	—	—	
PDRB	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0	

20.2.4 A/D Converter Characteristics

Table 20.6 A/D Converter Characteristics

V_{CC} = 3.0 to 3.6 V, V_{SS} = 0.0 V, T_a = –20 to +75°C, unless otherwise indicated.

Item	Symbol	Applicable Pins	Test Condition	Values			Unit	Reference Figure
				Min.	Typ.	Max.		
Analog power supply voltage	AV_{CC}	AV_{CC}		3.0	V_{CC}	3.6	V	*1
Analog input voltage	AV_{IN}	AN0 to AN7		V_{SS} – 0.3	—	AV_{CC} + 0.3	V	
Analog power supply current	AI_{OPE}	AV_{CC}	AV_{CC} = 3.3 V f_{OSC} = 18 MHz	—	—	2.0	mA	
	AI_{STOP1}	AV_{CC}		—	50	—	µA	*2 Reference value
	AI_{STOP2}	AV_{CC}		—	—	5.0	µA	*3
Analog input capacitance	C_{AIN}	AN0 to AN7		—	—	30.0	pF	
Allowable signal source impedance	R_{AIN}	AN0 to AN7		—	—	5.0	kΩ	
Resolution (data length)				10	10	10	bit	
Conversion time (single mode)			AV_{CC} = 3.0 to 3.6 V	134	—	—	t_{cyc}	
Nonlinearity error				—	—	±5.5	LSB	
Offset error				—	—	±5.5	LSB	
Full-scale error				—	—	±5.5	LSB	
Quantization error				—	—	±0.5	LSB	
Absolute accuracy				—	—	±6.0	LSB	
Conversion time (single mode)			AV_{CC} = 3.0 to 3.6 V	70	—	—	t_{cyc}	
Nonlinearity error				—	—	±7.5	LSB	
Offset error				—	—	±7.5	LSB	
Full-scale error				—	—	±7.5	LSB	
Quantization error				—	—	±0.5	LSB	
Absolute accuracy				—	—	±8.0	LSB	

Instruction	Mnemonic	Instruction Fetch I	Branch Addr. Read J	Stack Operation K	Byte Data Access L	Word Data Access M	Internal Operation N
Bcc	BRA d:8 (BT d:8)	2					
	BRN d:8 (BF d:8)	2					
	BHI d:8	2					
	BLS d:8	2					
	BCC d:8 (BHS d:8)	2					
	BCS d:8 (BLO d:8)	2					
	BNE d:8	2					
	BEQ d:8	2					
	BVC d:8	2					
	BVS d:8	2					
	BPL d:8	2					
	BMI d:8	2					
	BGE d:8	2					
Bcc	BLT d:8	2					
	BGT d:8	2					
	BLE d:8	2					
	BRA d:16(BT d:16)	2					2
	BRN d:16(BF d:16)	2					2
	BHI d:16	2					2
	BLS d:16	2					2
	BCC d:16(BHS d:16)	2					2
	BCS d:16(BLO d:16)	2					2
	BNE d:16	2					2
	BEQ d:16	2					2
	BVC d:16	2					2
	BVS d:16	2					2
	BPL d:16	2					2
	BMI d:16	2					2
	BGE d:16	2					2
	BLT d:16	2					2
	BGT d:16	2					2
	BLE d:16	2					2

Appendix C Product Code Lineup

Product Classification			Product Code	Model Marking	Package Code
H8/36087	Flash memory version	Standard product	HD64F36087H	DF36087H	QFP-64 (FP-64A)
			HD64F36087FP	DF36087FP	LQFP-64 (FP-64E)
	Mask ROM version	Standard product	HD64336087H	D336087(***)H	QFP-64 (FP-64A)
			HD64336087FP	D336087(***)FP	LQFP-64 (FP-64E)
H8/36086	Mask ROM version	Standard product	HD64336086H	D336086(***)H	QFP-64 (FP-64A)
			HD64336086FP	D336086(***)FP	LQFP-64 (FP-64E)
H8/36085	Mask ROM version	Standard product	HD64336085H	D336085(***)H	QFP-64 (FP-64A)
			HD64336085FP	D336085(***)FP	LQFP-64 (FP-64E)
H8/36084	Mask ROM version	Standard product	HD64336084H	D336084(***)H	QFP-64 (FP-64A)
			HD64336084FP	D336084(***)FP	LQFP-64 (FP-64E)
H8/36083	Mask ROM version	Standard product	HD64336083H	D336083(***)H	QFP-64 (FP-64A)
			HD64336083FP	D336083(***)FP	LQFP-64 (FP-64E)
H8/36082	Mask ROM version	Standard product	HD64336082H	D336082(***)H	QFP-64 (FP-64A)
			HD64336082FP	D336082(***)FP	LQFP-64 (FP-64E)

[Legend]

(***): ROM code