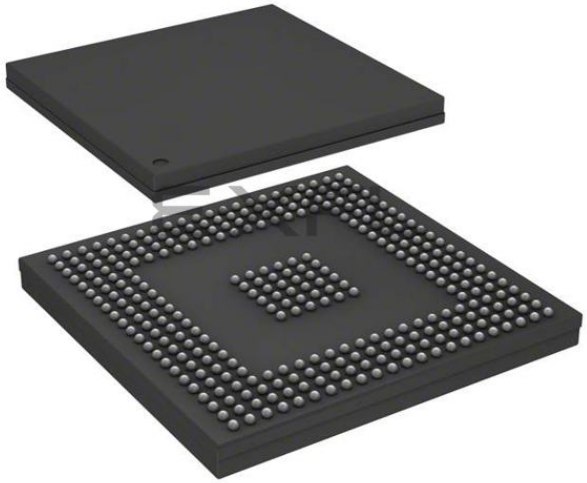

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Details	
Product Status	Active
Core Processor	e200z4
Core Size	32-Bit Single-Core
Speed	150MHz
Connectivity	CANbus, EBI/EMI, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	151
Program Memory Size	3MB (3M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	1.14V ~ 5.25V
Data Converters	A/D 40x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	324-BBGA
Supplier Device Package	324-PBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5643af0mvz1

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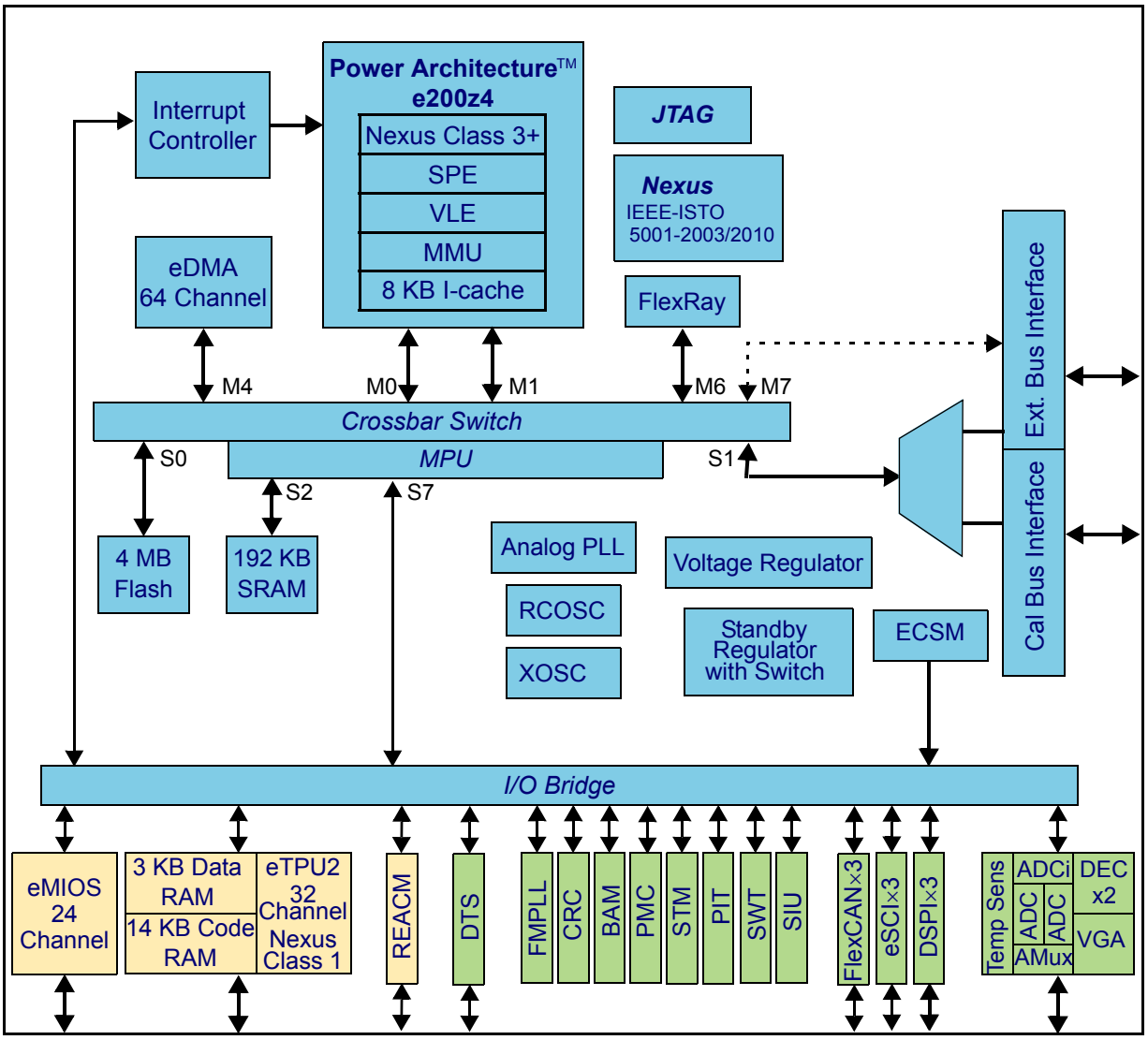

LEGEND

ADC – Analog to Digital Converter
ADCi – ADC interface
AMux – Analog Multiplexer
BAM – Boot Assist Module
CRC – Cyclic Redundancy Check unit
DEC – Decimation Filter
DTS – Development Trigger Semaphore
DSPI – Deserial/Serial Peripheral Interface
EBI – External Bus Interface
ECSM – Error Correction Status Module
eDMA – Enhanced Direct Memory Access
eMIOS – Enhanced Modular Input Output System
eSCI – Enhanced Serial Communications Interface
eTPU2 – Second gen. Enhanced Time Processing Unit
FlexCAN– Controller Area Network (FlexCAN)
FMPLL – Frequency-Modulated Phase Locked Loop
JTAG – IEEE 1149.1 test controller
MMU – Memory Management Unit
MPU – Memory Protection Unit
PMC – Power Management Controller
PIT – Periodic Interrupt Timer
RCOSC – low-speed RC oscillator
REACM – Reaction module
SIU – System Integration Unit
SPE – Signal Processing Extension
SRAM – Static RAM
STM – System Timer Module
SWT – Software Watchdog Timer
VGA – Variable Gain Amplifier
VLE – Variable Length (instruction) Encoding
XOSC – XTAL Oscillator

Figure 1. MPC5644A series block diagram

Table 2. MPC5644A series block summary (continued)

Block	Function
Reaction Module (REACM)	Works in conjunction with the eQADC and eTPU2 to increase system performance by removing the CPU from the current control loop.
System Integration Unit (SIU)	Controls MCU reset configuration, pad configuration, external interrupt, general purpose I/O (GPIO), internal peripheral multiplexing, and the system reset operation.
Static random-access memory (SRAM)	Provides storage for program code, constants, and variables.
System timers	Includes periodic interrupt timer with real-time interrupt; output compare timer and system watchdog timer.
Temperature sensor	Provides the temperature of the device as an analog value.

2.2 208 MAP BGA ballmap

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	VSS	AN9	AN11	VDDA1	VSSA1	AN1	AN5	VRH	VRL	AN27	VSSA0	AN12-SDS	MDO2	MDO0	VRC33	VSS	A
B	VDD	VSS	AN8	AN21	AN0	AN4	REFBYPC	AN22	AN25	AN28	VDDA0	AN13-SDO	MDO3	MDO1	VSS	VDD	B
C	VSTBY	VDD	VSS	AN17	AN34	AN16	AN3	AN7	AN23	AN32	AN33	AN14-SDI	AN15-FCK	VSS	MSEO0	TCK	C
D	VRC33	AN39	VDD	VSS	AN18	AN2	AN6	AN24	AN30	AN31	AN35	VDDEH7	VSS	TMS	EVTO	NC	D
E	ETPUA30	ETPUA31	AN37	VDD									NC	TDI	EVTI	MSEO1	E
F	ETPUA28	ETPUA29	ETPUA26	AN36									VDDEH6AB	TDO	MCKO	JCOMP	F
G	ETPUA24	ETPUA27	ETPUA25	ETPUA21			VSS	VSS	VSS	VSS			DSPI_B_ SOUT	DSPI_B_ PCS3	DSPI_B_ SIN	DSPI_B_ PCS0	G
H	ETPUA23	ETPUA22	ETPUA17	ETPUA18			VSS	VSS	VSS	VSS			GPIO99	DSPI_B_ PCS4	DSPI_B_ PCS2	DSPI_B_ PCS1	H
J	ETPUA20	ETPUA19	ETPUA14	ETPUA13			VSS	VSS	VSS	VSS			DSPI_B_ PCS5	SCI_A_TX	GPIO98	DSPI_B_ SCK	J
K	ETPUA16	ETPUA15	ETPUA7	VDDEH1AB			VSS	VSS	VSS	VSS			CAN_C_TX	SCI_A_RX	RSTOUT	VDDREG	K
L	ETPUA12	ETPUA11	ETPUA6	TCRCLKA									SCI_B_TX	CAN_C_ RX	WKPCFG	RESET	L
M	ETPUA10	ETPUA9	ETPUA1	ETPUA5									SCI_B_RX	PLLREF	BOOTCFG1	VSS	M
N	ETPUA8	ETPUA4	ETPUA0	VSS	VDD	VRC33	EMIOS2	EMIOS10	VDDEH4AB	EMIOS12	MDO7_ ETPUA19_O	VRC33	VSS[1]	VRCCTL	NC	EXTAL	N
P	ETPUA3	ETPUA2	VSS	VDD	GPIO207	NC	EMIOS6	EMIOS8	MDO11_ ETPUA29_O	MDO4_ ETPUA2_O	MDO8_ ETPUA21_O	CAN_A_TX	VDD	VSS	NC	XTAL	P
R	NC	VSS	VDD	GPIO206	EMIOS4	EMIOS3	EMIOS9	EMIOS11	EMIOS14	MDO10_ ETPUA27_O	EMIOS23	CAN_A_RX	CAN_B_RX	VDD	VSS	VDDPLL	R
T	VSS	VDD	NC	EMIOS0	EMIOS1	GPIO219	MDO9_ ETPUA25_O	EMIOS13	EMIOS15	MDO5_ ETPUA4_O	MDO6_ ETPUA13_O	CAN_B_TX	VDDE5	ENGCLK	VDD	VSS	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

[1] This pin (N13) should be tied low.

Figure 3. 208-pin MAPBGA package ballmap (viewed from above)

2.3 324 TEPBGA ballmap

	1	2	3	4	5	6	7	8	9	10	11
A	VSS	VDD	AN16	AN17	AN37	VDDA1	VSSA1	AN23	AN25	VRH	VRL
B	VRC33	VSS	VDD	AN18	AN36	AN21	AN4	AN5	AN24	REFBYPC	AN30
C	AN11	AN9 ANX	VSS	VDD	AN20	AN0	AN1	AN6	AN7	AN27	AN29
D	AN10 ANY	AN39	AN38	VSS	VDD	AN19	AN2	AN3	AN22	AN26	AN28
E	AN8 ANW	VSSA0	VDDA0	VSTBY							
F	MCKO	VRCCTL	MDO0	VDDREG							
G	CS0	MDO1	MDO2	MDO3							
H	CS1	CS2	OE	CS3							
J	WE1	WE0	BDIP	RD_WR					VSS	VSS	VSS
K	ETPUA31	TA	TS	VDDEH1AB					VSS	VSS	VSS
L	ETPUA27	ETPUA26	ETPUA29	ETPUA30					VSS	VSS	VSS

Figure 4. 324-pin TEPBGA package ballmap (northwest, viewed from above)

Table 3. MPC5644A signal properties (continued)

Name	Function[1]	PAG[2]	PCR PA Field[3]	PCR[4]	I/O Type	Voltage[5] / Pad Type[6]	Status[7]		Package pin #		
							During Reset	After Reset	176	208	324
MDO2[16]	Nexus message data out	P	01	222	O	VRC33 Fast	—	MDO[2] / —	19	A13	G3
MDO3[16]	Nexus message data out	P	01	223	O	VRC33 Fast	—	MDO[3] / —	20	B13	G4
MDO4[16] ETPUA2_O[8] GPIO[75]	Nexus message data out eTPU A channel (output only) GPIO[	P A1 G	01 10 00	75	O O I/O	VDDEH7 MultiV[12,14]	—	— / —	126	P10	B19
MDO5[16] ETPUA4_O[8] GPIO[76]	Nexus message data out eTPU A channel (output only) GPIO	P A1 G	01 10 00	76	O O I/O	VDDEH7 MultiV[12,14]	—	— / —	129	T10	B20
MDO6[16] ETPUA13_O[8] GPIO[77]	Nexus message data out eTPU A channel (output only) GPIO	P A1 G	01 10 00	77	O O I/O	VDDEH7 MultiV[12,14]	—	— / —	135	T11	C18
MDO7[16] ETPUA19_O[8] GPIO[78]	Nexus message data out eTPU A channel (output only) GPIO	P A1 G	01 10 00	78	O O I/O	VDDEH7 MultiV[12,14]	—	— / —	136	N11	B18
MDO8[16] ETPUA21_O[8] GPIO[79]	Nexus message data out eTPU A channel (output only) GPIO	P A1 G	01 10 00	79	O O I/O	VDDEH7 MultiV[12,14]	—	— / —	137	P11	A18
MDO9[16] ETPUA25_O[8] GPIO[80]	Nexus message data out eTPU A channel (output only) GPIO	P A1 G	01 10 00	80	O O I/O	VDDEH7 MultiV[12,14]	—	— / —	139	T7	D18
MDO10[16] ETPUA27_O[8] GPIO[81]	Nexus message data out eTPU A channel (output only) GPIO	P A1 G	01 10 00	81	O O I/O	VDDEH7 MultiV[12,14]	—	— / —	134	R10	A19
MDO11[16] ETPUA29_O[8] GPIO[82]	Nexus message data out eTPU A channel (output only) GPIO[82]	P A1 G	01 10 00	82	O O I/O	VDDEH7 MultiV[12,14]	—	— / —	124	P9	C19
$\overline{\text{MSEO}}$[0][16]	Nexus message start/end out	P	01	224	O	VDDEH7 MultiV[12,14]	—	$\overline{\text{MSEO}}$[0] / —	118	C15	G21
$\overline{\text{MSEO}}$[1][16]	Nexus message start/end out	P	01	225	O	VDDEH7 MultiV[12,14]	—	$\overline{\text{MSEO}}$[1] / —	117	E16	G22
$\overline{\text{RDY}}$	Nexus ready output	P	01	226	O	VDDEH7 MultiV[12,14]	—	—	—	—	G19
JTAG											

Table 3. MPC5644A signal properties (continued)

Name	Function[1]	PAG[2]	PCR PA Field[3]	PCR[4]	I/O Type	Voltage[5] / Pad Type[6]	Status[7]		Package pin #		
							During Reset	After Reset	176	208	324
AN14 - SDI MA2 ETPUA27_O[8] SDI	Single-ended Analog Input MUX Address 2 eTPU A channel (output only) eQADC Serial Data In	P A1 A2 G	001 010 100 000	217	I O O I	VDDEH7[19] Medium	I / —	AN[14] / —	146	C12	A13
AN15 - FCK FCK ETPUA29_O[8]	Single-ended Analog Input eQADC Free Running Clock eTPU A channel (output only)	P A1 A2	001 010 100	218	I O O	VDDEH7[19] Medium	I / —	AN[15] / —	145	C13	A14
AN16	Single-ended Analog Input	P	—	—	I	VDDA Analog	I / —	AN[16] / —	3	C6	A3
AN17	Single-ended Analog Input	P	—	—	I	VDDA Analog	I / —	AN[17] / —	2	C4	A4
AN18	Single-ended Analog Input	P	—	—	I	VDDA Analog	I / —	AN[18] / —	1	D5	B4
AN19	Single-ended Analog Input	P	—	—	I	VDDA Analog	I / —	AN[19] / —	—	—	D6
AN20	Single-ended Analog Input	P	—	—	I	VDDA Analog	I / —	AN[20] / —	—	—	C5
AN21	Single-ended Analog Input	P	—	—	I	VDDA Analog	I / —	AN[21] / —	173	B4	B6
AN22	Single-ended Analog Input	P	—	—	I	VDDA Analog	I / —	AN[22] / —	161	B8	D9
AN23	Single-ended Analog Input	P	—	—	I	VDDA Analog	I / —	AN[23] / —	160	C9	A8
AN24	Single-ended Analog Input	P	—	—	I	VDDA Analog	I / —	AN[24] / —	159	D8	B9
AN25	Single-ended Analog Input	P	—	—	I	VDDA Analog	I / —	AN[25] / —	158	B9	A9
AN26	Single-ended Analog Input	P	—	—	I	VDDA Analog	I / —	AN[26] / —	—	—	D10
AN27	Single-ended Analog Input	P	—	—	I	VDDA Analog	I / —	AN[27] / —	157	A10	C10
AN28	Single-ended Analog Input	P	—	—	I	VDDA Analog	I / —	AN[28] / —	156	B10	D11

Table 3. MPC5644A signal properties (continued)

Name	Function[1]	PAG[2]	PCR PA Field[3]	PCR[4]	I/O Type	Voltage[5] / Pad Type[6]	Status[7]		Package pin #		
							During Reset	After Reset	176	208	324
ETPUA8 ETPUA20_O[8] DSPI_B_SOUT_LVDS+ GPIO[122]	eTPU A channel eTPU A channel (output only) LVDS positive DSPI data out GPIO	P A1 A2 G	001 010 100 000	122	I/O O O I/O	VDDEH4 Slow + LVDS	— / WKPCFG	— / WKPCFG	51	N1	Y10
ETPUA9 ETPUA21_O[8] RCH1_B GPIO[123]	eTPU A channel eTPU A channel (output only) Reaction channel 1B GPIO	P A1 A2 G	001 010 100 000	123	I/O O O I/O	VDDEH4 Slow	— / WKPCFG	— / WKPCFG	50	M2	AA9
ETPUA10 ETPUA22_O[8] RCH1_C GPIO[124]	eTPU A channel eTPU A channel (output only) Reaction channel 1C GPIO	P A1 A2 G	001 010 100 000	124	I/O O O I/O	VDDEH1 Slow	— / WKPCFG	— / WKPCFG	49	M1	AA4
ETPUA11 ETPUA23_O[8] RCH4_B GPIO[125]	eTPU A channel eTPU A channel (output only) Reaction channel 4B GPIO	P A1 A2 G	001 010 100 000	125	I/O O O I/O	VDDEH1 Slow	— / WKPCFG	— / WKPCFG	48	L2	AB4
ETPUA12 DSPI_B_PCS[1] RCH4_C GPIO[126]	eTPU A channel DSPI B peripheral chip select Reaction channel 4C GPIO	P A1 A2 G	001 010 100 000	126	I/O O O I/O	VDDEH1 Medium	— / WKPCFG	— / WKPCFG	47	L1	AB3
ETPUA13 DSPI_B_PCS[3] GPIO[127]	eTPU A channel DSPI B peripheral chip select GPIO	P A1 G	01 10 00	127	I/O O I/O	VDDEH1 Medium	— / WKPCFG	— / WKPCFG	46	J4	AB2
ETPUA14 DSPI_B_PCS[4] ETPUA9_O[8] RCH0_A GPIO[128]	eTPU A channel DSPI B peripheral chip select eTPU A channel (output only) Reaction channel 0A GPIO	P A1 A2 A3 G	0001 0010 0100 1000 0000	128	I/O O O O I/O	VDDEH1 Medium	— / WKPCFG	— / WKPCFG	42	J3	AA2
ETPUA15 DSPI_B_PCS[5] RCH1_A GPIO[129]	eTPU A channel DSPI B peripheral chip select Reaction channel 1A GPIO	P A1 A2 G	001 010 100 000	129	I/O O O I/O	VDDEH1 Medium	— / WKPCFG	— / WKPCFG	40	K2	AA1
ETPUA16 DSPI_D_PCS[1] RCH2_A GPIO[130]	eTPU A channel DSPI D peripheral chip select Reaction channel 2A GPIO	P A1 A2 G	001 010 100 000	130	I/O O O I/O	VDDEH1 Slow	— / WKPCFG	— / WKPCFG	39	K1	Y2

Table 3. MPC5644A signal properties (continued)

Name	Function[1]	P A G[2]	PCR PA Field[3]	PCR[4]	I/O Type	Voltage[5] / Pad Type[6]	Status[7]		Package pin #		
							During Reset	After Reset	176	208	324
VDDEH7	I/O Supply Input	—		—	I	3.3 V - 5.0 V	I / —	VDDEH7	—	D12	B22, C21, D15, D20, E19, F19, H19, J14
VDDEH7A	I/O Supply Input	—		—	I	3.3 V - 5.0 V	I / —	VDDEH7A	125	—	—
VDDEH7B	I/O Supply Input	—		—	I	3.3 V - 5.0 V	I / —	VDDEH7B	138	—	—
VSS	Ground	—		—	I	—	I / —	VSS	15, 29, 43, 57, 72, 90, 94, 96, 108, 115, 127, 133, 140	A1, A16, B2, B15, C3, C14, D4, D13, G7, G8, G9, G10, H7, H8, H9, H10, J7, J8, J9, J10, K7, K8, K9, K10, M16, N4, N13, P3, P14, R2, R15, T1, T16	A1, A22, B2, B21, C3, C20, D4, D17, D19, F21, H21, J9, J10, J11, J12, J13, K9, K10, K11, K12, K13, K14, L9, L10, L11, L12, L13, L14, L21, M11, M12, M13, M14, N9, N10, N12, N13, N14, N21, P9, P10, P12, P13, P14, T19, T21, T22, W4, Y3, Y20, AA21, AB1, AB22

1 For each pin in the table, each line in the Function column is a separate function of the pin. For all I/O pins the selection of primary pin function or secondary function or GPIO is done in the SIU except where explicitly noted. See the Signal details table for a description of each signal.

2 The P/A/G column indicates the position a signal occupies in the muxing order for a pin—Primary, Alternate 1, Alternate 2, Alternate 3, or GPIO. Signals are selected by setting the PA field value in the appropriate PCR register in the SIU module. The PA field values are as follows: P - 0b0001, A1 - 0b0010, A2 - 0b0100, A3 - 0b1000, or G - 0b0000. Depending on the register, the PA field size can vary in length. For PA fields having fewer than four bits, remove the appropriate number of leading zeroes from these values.

3 The Pad Configuration Register (PCR) PA field is used by software to select pin function.

4 Values in the PCR No. column refer to registers in the System Integration Unit (SIU). The actual register name is “SIU_PCR” suffixed by the PCR number. For example, PCR[190] refers to the SIU register named SIU_PCR190.

Table 5. Signal details (continued)

Signal	Module or Function	Description
DSPI_C_SOUT_LVDS- DSPI_C_SOUT_LVDS+	DSPI	LVDS pair used for DSPI_C TSB mode transmission
PCS_B[0] PCS_C[0] PCS_D[0]	DSPI_B - DSPI_D	Peripheral chip select when device is in master mode—slave select when used in slave mode
PCS_B[1:5] PCS_C[1:5] PCS_D[1:5]	DSPI_B - DSPI_D	Peripheral chip select when device is in master mode—not used in slave mode
SCK_B SCK_C SCK_D	DSPI_B - DSPI_D	DSPI clock—output when device is in master mode; input when in slave mode
SIN_B SIN_C SIN_D	DSPI_B - DSPI_D	DSPI data in
SOUT_B SOUT_C SOUT_D	DSPI_B - DSPI_D	DSPI data out
ADDR[10:31]	EBI	The ADDR[10:31] signals specify the physical address of the bus transaction. The 26 address lines correspond to bits 3-31 of the EBI's 32-bit internal address bus. ADDR[15:31] can be used as Address and Data signals when configured appropriately for a multiplexed external bus. This allows 32-bit data operations, or 16-bit data operations without using DATA[0:15] signals.
ALE	EBI	The Address Latch Enable (ALE) signal is used to demultiplex the address from the data bus. It is asserted while the least significant 16 bits of the address are present in the multiplexed address/data bus.
$\overline{\text{BDIP}}$	EBI	$\overline{\text{BDIP}}$ is asserted to indicate that the master is requesting another data beat following the current one.
$\overline{\text{CS}}$[0:3]	EBI	$\overline{\text{CS}}$x is asserted by the master to indicate that this transaction is targeted for a particular memory bank on the Primary external bus.
DATA[0:31]	EBI	The DATA[0:31] signals contain the data to be transferred for the current transaction.
$\overline{\text{OE}}$	EBI	$\overline{\text{OE}}$ is used to indicate when an external memory is permitted to drive back read data. External memories must have their data output buffers off when $\overline{\text{OE}}$ is negated. $\overline{\text{OE}}$ is only asserted for chip-select accesses.
RD_$\overline{\text{WR}}$	EBI	RD_$\overline{\text{WR}}$ indicates whether the current transaction is a read access or a write access.

Table 17. MPC5644A External network specification

External Network Parameter	Min	Typ	Max	Comment
Re	0.252Ω	0.280Ω	0.308Ω	+/-10%
Creg		10μF		It depends on external Vreg.
Cc	5μF	10μF	13.5μF	X7R, -50%/+35%
Rc	1.1Ω		5.6Ω	May or may not be required. It depends on the allowable power dissipation of T1.

3.6.3 Recommended power transistors

The following NPN transistors are recommended for use with the on-chip voltage regulator controller: ON Semiconductor™ BCP68T1 or NJD2873 as well as Philips Semiconductor™ BCP68. The collector of the external transistor is preferably connected to the same voltage supply source as the output stage of the regulator.

Table 18. Recommended operating characteristics

Symbol	Parameter	Value	Unit
h_{FE} (β)	DC current gain (Beta)	60 – 550	—
P_D	Absolute minimum power dissipation	>1.0 (1.5 preferred)	W
I_{CMaxDC}	Minimum peak collector current	1.0	A
VCE_{SAT}	Collector-to-emitter saturation voltage	200 – 600[1]	mV
V_{BE}	Base-to-emitter voltage	0.4 – 1.0	V

[1] Adjust resistor at bipolar transistor collector for 3.3 V/5.0 V to avoid VCE < VCE_{SAT}.

3.7 Power up/down sequencing

There is no power sequencing required among power sources during power up and power down, in order to operate within specification.

Although there are no power up/down sequencing requirements to prevent issues such as latch-up or excessive current spikes the state of the I/O pins during power up/down varies according to Table 19 for all pins with fast pads, and Table 20 for all pins with medium, slow, and multi-voltage pads.

Table 19. Power sequence pin states (fast pads)

V_{DDE}	V_{RC33}	V_{DD}	Pad State
LOW	X	X	LOW
V_{DDE}	LOW	X	HIGH
V_{DDE}	V_{RC33}	LOW	HIGH IMPEDANCE
V_{DDE}	V_{RC33}	V_{DD}	FUNCTIONAL

Table 30. eQADC differential ended conversion specifications (operating) (continued)

Symbol		C	Parameter		Value		Unit
					min	max	
GAINVGA2[1]	CC	–	Variable gain amplifier accuracy (gain=2)[2]				
	CC	D	INL	8 MHz ADC	–5	5	Counts
	CC	D		16 MHz ADC	–8	8	Counts
	CC	D	DNL	8 MHz ADC	–3	3	Counts
	CC	D		16 MHz ADC	–3	3	Counts
GAINVGA4[1]	CC	–	Variable gain amplifier accuracy (gain=4)[2]				
	CC	D	INL	8 MHz ADC	–7	7	Counts
	CC	D		16 MHz ADC	–8	8	Counts
	CC	D	DNL	8 MHz ADC	–4	4	Counts
	CC	D		16 MHz ADC	–4	4	Counts
$DIFF_{max}$	CC	C	Maximum differential voltage (DANx+ - DANx-) or (DANx- - DANx+)[5]	PREGAIN set to 1X setting	—	(VRH - VRL)/2	V
$DIFF_{max2}$	CC	C		PREGAIN set to 2X setting	—	(VRH - VRL)/4	V
$DIFF_{max4}$	CC	C		PREGAIN set to 4X setting	—	(VRH - VRL)/8	V
$DIFF_{cmv}$	CC	C	Differential input Common mode voltage (DANx- + DANx+)/2[5]	—	$(V_{RH} + V_{RL})/2$ - 5%	$(V_{RH} + V_{RL})/2$ + 5%	V

1 Applies only to differential channels.

2 Variable gain is controlled by setting the PRE_GAIN bits in the ADC_ACR1-8 registers to select a gain factor of ×1, ×2, or ×4. Settings are for differential input only. Tested at ×1 gain. Values for other settings are guaranteed by as indicated.

3 At $V_{RH} – V_{RL}$ = 5.12 V, one LSB = 1.25 mV.

4 Guaranteed 10-bit mono tonicity.

5 Voltages between VRL and VRH will not cause damage to the pins. However, they may not be converted accurately if the differential voltage is above the maximum differential voltage. In addition, conversion errors may occur if the common mode voltage of the differential signal violates the Differential Input common mode voltage specification.

[2] This parameter is supplied for reference and is not guaranteed by design and not tested.
[3] Delay and rise/fall are measured to 20% or 80% of the respective signal.
[4] This parameter is guaranteed by characterization before qualification rather than 100% tested.
[5] In high swing mode, high/low swing pad Vol and Voh values are the same as those of the slew controlled output pads
[6] Medium Slew-Rate Controlled Output buffer. Contains an input buffer and weak pullup/pulldown.
[7] Output delay is shown in Figure 9. Add a maximum of one system clock to the output delay for delay with respect to system clock.
[8] Can be used on the tester.
[9] This drive select value is not supported. If selected, it will be approximately equal to 11.
[10] Slow Slew-Rate Controlled Output buffer. Contains an input buffer and weak pullup/pulldown.
[11] Selectable high/low swing IO pad with selectable slew in high swing mode only.
[12] Stand alone input buffer. Also has weak pull-up/pull-down.

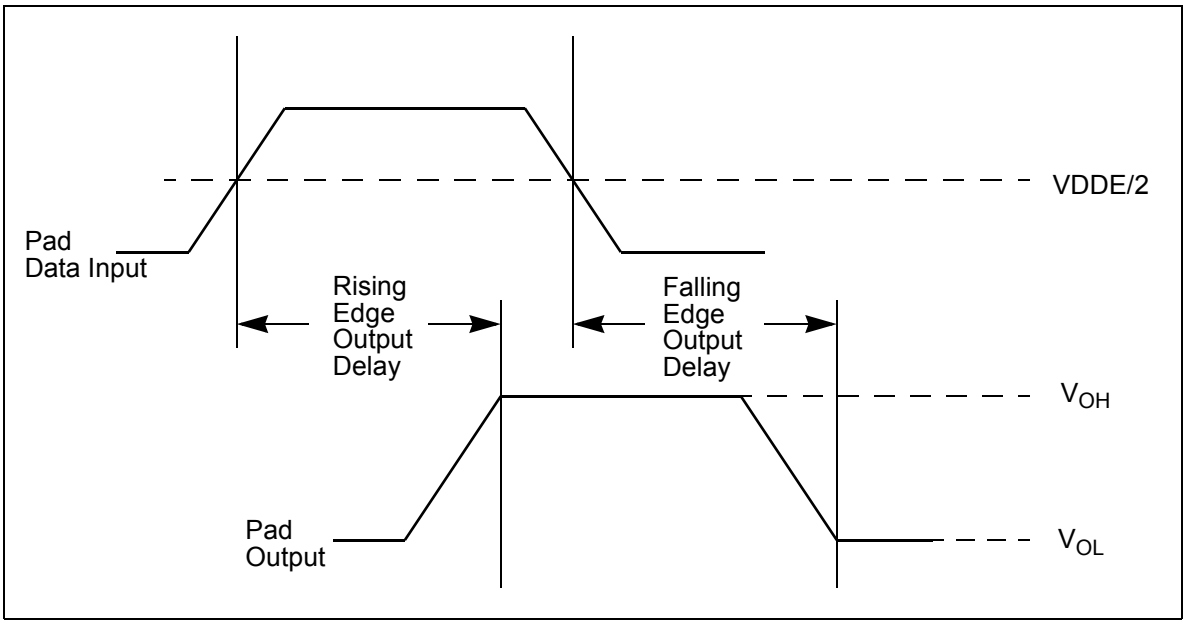

Figure 9. Pad output delay

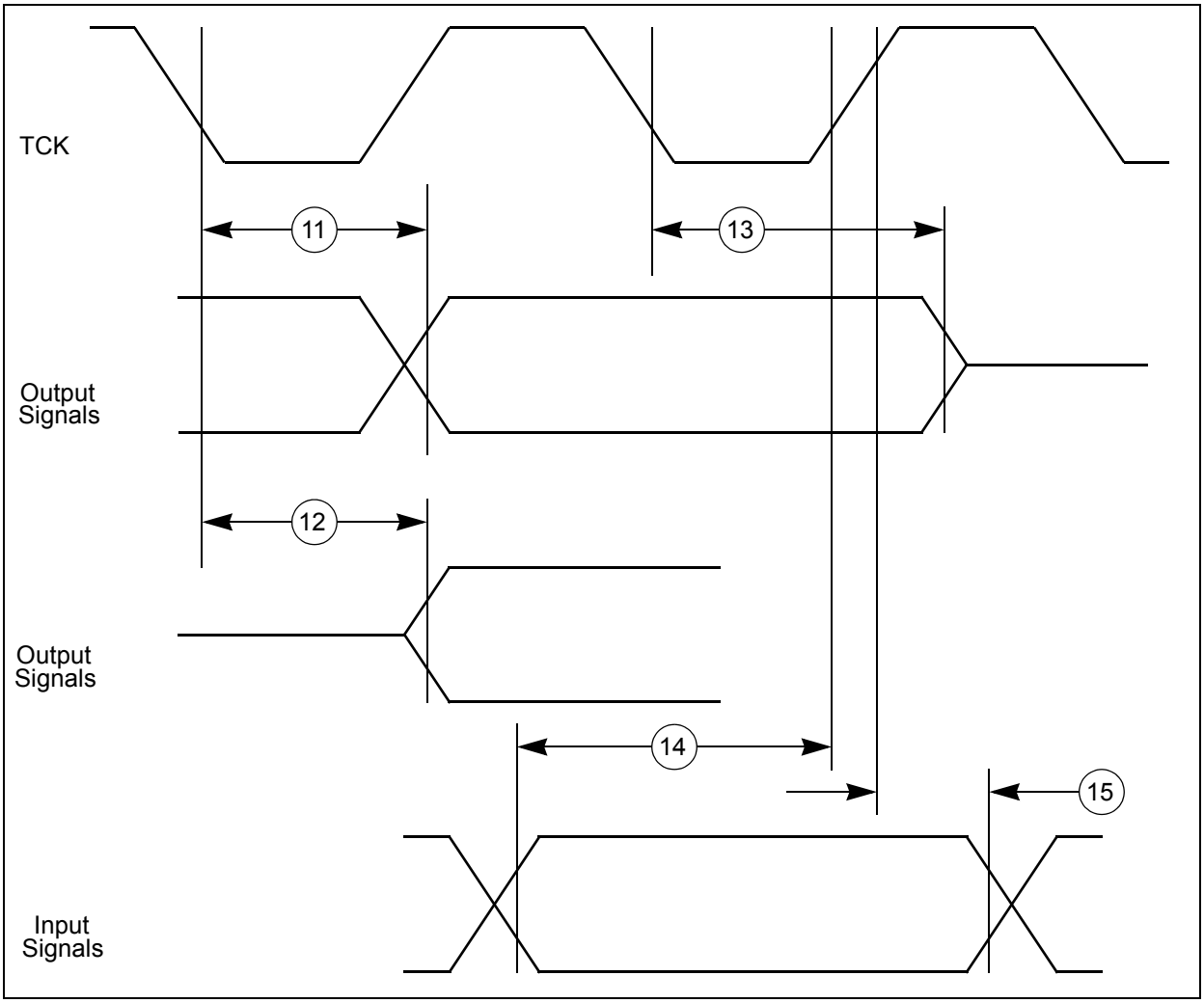

Figure 14. JTAG boundary scan timing

3.17.3 Nexus timing

Table 39. Nexus debug port timing[1]

#	Symbol		C	Characteristic	Min. Value	Max. Value	Unit
1	t_{MCYC}	CC	D	MCKO Cycle Time	2[2,3]	8	t_{CYC}
1a	t_{MCYC}	CC	D	Absolute Minimum MCKO Cycle Time	25[4]	—	ns
2	t_{MDC}	CC	D	MCKO Duty Cycle	40	60	%
3	t_{MDOV}	CC	D	MCKO Low to MDO Data Valid[5]	- 0.1	0.35	t_{MCYC}
4	t_{MSEOV}	CC	D	MCKO Low to $\overline{\text{MSEO}}$ Data Valid[5]	- 0.1	0.35	t_{MCYC}
6	t_{EVTOV}	CC	D	MCKO Low to $\overline{\text{EVTO}}$ Data Valid[5]	- 0.1	0.35	t_{MCYC}
7	t_{EVTIPW}	CC	D	$\overline{\text{EVTI}}$ Pulse Width	4.0	—	t_{TCYC}
8	t_{EVTOPW}	CC	D	$\overline{\text{EVTO}}$ Pulse Width	1	—	t_{MCYC}
9	t_{TCYC}	CC	D	TCK Cycle Time	4[6,7]	—	t_{CYC}
9a	t_{TCYC}	CC	D	Absolute Minimum TCK Cycle Time	100[8]	—	ns
10	t_{TDC}	CC	D	TCK Duty Cycle	40	60	%

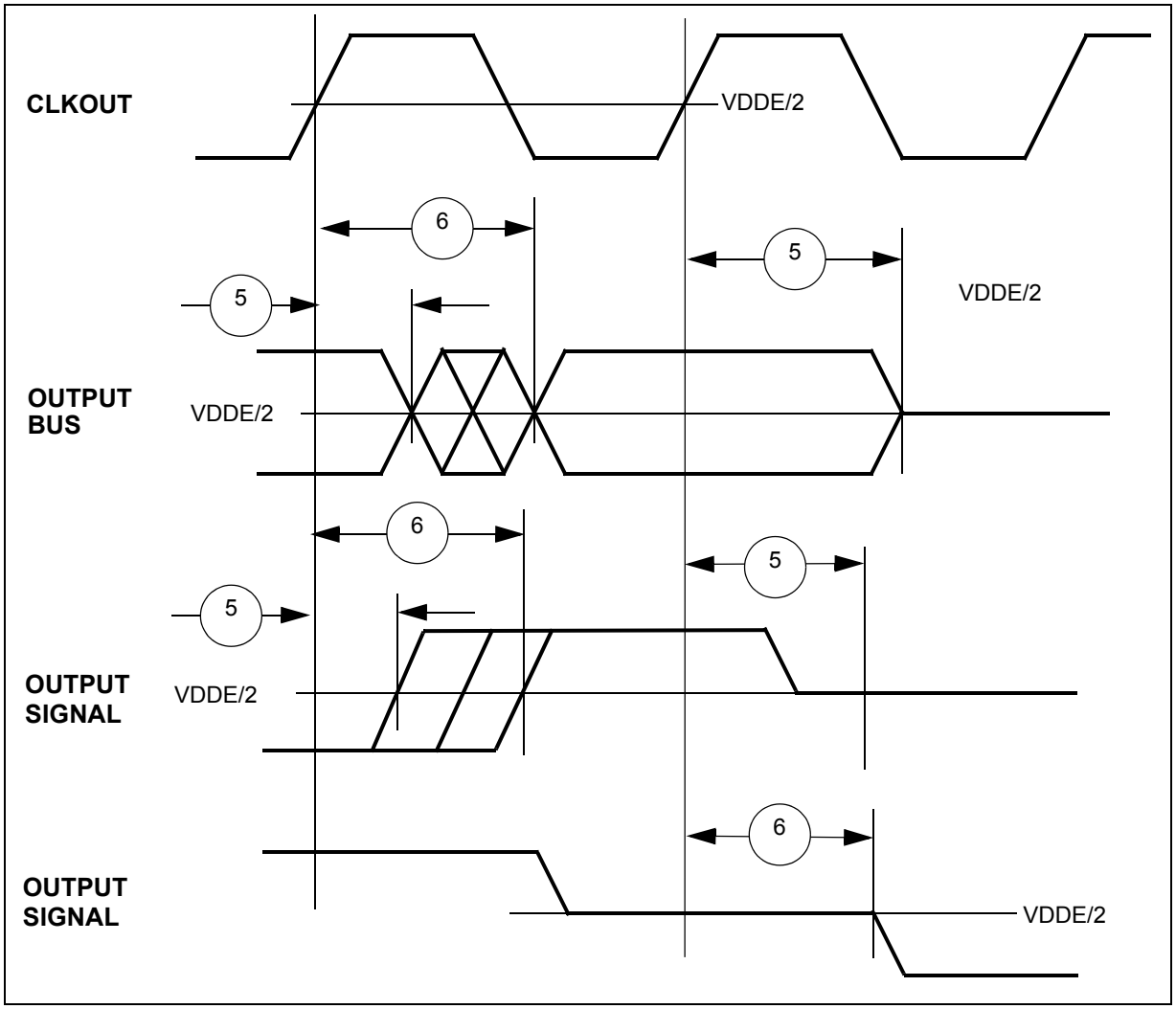

Figure 19. Synchronous output timing

3.17.7 eMIOS timing

Table 46. eMIOS timing[1]

#	Symbol		C	Characteristic	Min. Value	Max. Value	Unit
1	t_{MIPW}	CC	D	eMIOS Input Pulse Width	4	—	t_{CYC}
2	t_{MOPW}	CC	D	eMIOS Output Pulse Width	1	—	t_{CYC}

[1] eMIOS timing specified at f_{SYS} = 80 MHz, V_{DD} = 1.14 V to 1.32 V, V_{DDEH} = 4.5 V to 5.5 V, $T_A = T_L$ to T_H, and C_L = 50 pF with SRC = 0b00.

3.17.8 DSPI timing

DSPI channel frequency support for the MPC5644A MCU is shown in Table 47. Timing specifications are in Table 48.

Table 47. DSPI channel frequency support

System Clock (MHz)	DSPI Use Mode	Max. Usable Frequency (MHz)	Notes
150	LVDS	37.5	Use sysclock /4 divide ratio.
	Non-LVDS	18.75	Use sysclock /8 divide ratio.
120	LVDS	40	Use sysclock /3 divide ratio. Gives 33/66 duty cycle. Use DSPI configuration DBR=0b1 (double baud rate), BR=0b0000 (scaler value 2) and PBR=0b01 (prescaler value 3).
	Non-LVDS	20	Use sysclock /6 divide ratio.
80	LVDS	40	Use sysclock /2 divide ratio.
	Non-LVDS	20	Use sysclock /4 divide ratio.

Table 48. DSPI timing[1,2]

#	Symbol		C	Characteristic	Condition	Min.	Max.	Unit
1	t_{SCK}	CC	D	SCK Cycle Time[3,4,5]		24.4 ns	2.9 ms	—
2	t_{CSC}	CC	D	PCS to SCK Delay[6]		22[7]	—	ns
3	t_{ASC}	CC	D	After SCK Delay[8]		21[9]	—	ns
4	t_{SDC}	CC	D	SCK Duty Cycle		$(½t_{SC})–2$	$(½t_{SC})+2$	ns
5	t_A	CC	D	Slave Access Time ($\overline{SS}$ active to SOUT driven)		—	25	ns
6	t_{DIS}	CC	D	Slave SOUT Disable Time ($\overline{SS}$ inactive to SOUT High-Z or invalid)		—	25	ns
7	t_{PCSC}	CC	D	PCSx to $\overline{PCSS}$ time		4[10]	—	ns
8	t_{PASC}	CC	D	$\overline{PCSS}$ to PCSx time		5[11]	—	ns

3.17.10 FlexCAN system clock source

Table 50. FlexCAN engine system clock divider threshold

#	Symbol	Characteristic	Value	Unit
1	F_{CAN_TH}	FlexCAN engine system clock threshold	100	MHz

Table 51. FlexCAN engine system clock divider

System Frequency	Required SIU_SYSDIV[CAN_SRC] Value
<= F_{CAN_TH}	0[1,2]
> F_{CAN_TH}	1[2,3]

[1] Divides system clock source for FlexCAN engine by 1.
[2] System clock is only selected for FlexCAN when CAN_CR[CLK_SRC] = 1.
[3] Divides system clock source for FlexCAN engine by 2.

5 Ordering information

Table 52 shows the orderable part numbers for the MPC5644A series.

Table 52. Orderable part number summary

Part number	Flash/SRAM	Package	Speed (MHz)
SPC5643AF0MLU3	3 MB/192 KB	176LQFP (Pb free)	80
SPC5643AF0MMG3	3 MB/192 KB	208MAPBGA(Pb free)	80
SPC5643AF0MVZ3	3 MB/192 KB	324PBGA (Pb free)	80
SPC5643AF0MLU2	3 MB/192 KB	176LQFP (Pb free)	120
SPC5643AF0MMG2	3 MB/192 KB	208MAPBGA (Pb free)	120
SPC5643AF0MVZ2	3 MB/192 KB	324PBGA (Pb free)	120
SPC5643AF0MLU1	3 MB/192 KB	176LQFP (Pb free)	150
SPC5643AF0MMG1	3 MB/192 KB	208MAPBGA (Pb free)	150
SPC5643AF0MVZ1	3 MB/192 KB	324PBGA (Pb free)	150
SPC5644AF0MLU3	4 MB/192 KB	176 LQFP (Pb free)	80
SPC5644AF0MMG3	4 MB/192 KB	208 MAPBGA (Pb free)	80
SPC5644AF0MVZ3	4 MB/192 KB	324 TEPBGA (Pb free)	80
SPC5644AF0MLU2	4 MB/192 KB	176 LQFP (Pb free)	120
SPC5644AF0MMG2	4 MB/192 KB	208 MAPBGA (Pb free)	120
SPC5644AF0MVZ2	4 MB/192 KB	324 TEPBGA (Pb free)	120
SPC5644AF0MLU1	4 MB/192 KB	176 LQFP (Pb free)	150
SPC5644AF0MMG1	4 MB/192 KB	208 MAPBGA (Pb free)	150
SPC5644AF0MVZ1	4 MB/192 KB	324 TEPBGA (Pb free)	150

Table 53. Revision history (continued)

Revision	Date	Substantive changes
Rev. 5	2/2011	• Minor editorial updates. • Re-organized the first few subsections of the “Overview” section. • Added ECSM to the block diagram. • Added information on the REACM, SIU, and ECS modules to the “Block summary” section. • Added DATA[0:15] to V_{DDE5} in the “signal properties” table. • Updated VSTBY parameters in the “Power/ground segmentation” table. • Updated the parameter symbols and classifications throughout the document. • Updated footnote instances in the “Absolute maximum ratings” table. • Removed I_{MAXA} footnote in the “Absolute Maximum Ratings” table. • Updated the format of the “EMI (electromagnetic interference) characteristics” table. • Removed the footnote on V_{DDREG} in the “Power management control (PMC) and power on reset (POR) electrical specifications” table. • Updated values for Vbg, Idd3p3, Por3.3V_r, Por3.3V_f, Por5V_r, and Por5V_f in the “PMC electrical characteristics” table. • Updated “Bandgap reference supply voltage variation” in the “PMC Electrical Characteristics” table. • Updated VCE_{SAT} and V_{BE}in the “Recommended power transistors” operating characteristics” table. • Updated V_{IH_LS} in the “DC electrical specifications” table. • Updated the V_{OH_LS} min value in the “DC electrical specifications” table. • Updated I_{DDSTBY} and $I_{DDSTBY150}$ in the “DC electrical specifications” table. • Updated the $I_{DDA}/I_{REF}/I_{DDREG}$ max value in the “DC electrical specifications” table. • Updated I_{ACT_F}, $I_{ACT_MV_PU}$, $I_{ACT_MV_PD}$, R_{PUPD5K}, $R_{PUPDMTCH}$, and footnotes in the “DC electrical specifications” table. • Updated Medium pad type I_{DD33} values in the “I/O pad V_{RC33} average I_{DDE} specifications” table. • Updated values for V_{OD} in the “DSPI LVDS pad specification” table. • Removed the footnotes from the “DSPI LVDS pad specifications” table. • Removed the redundant “XTAL Load Capacitance” parameter instance from the “PLLMRFM electrical specifications” table. • Updated footnotes in the “PLLMRFM electrical specifications” table. • Updated values for OFFNC and GAINNC in the “eQADC conversion specifications (operating)” table. • Added $DIFF_{max}$, $DIFF_{max2}$, $DIFF_{max4}$, and $DIFF_{cmv}$ parameters to the “eQADC conversion specifications (operating)” table. • Added the maximum operating frequency values in the “Cutoff frequency for additional SRAM wait state” table. • Updated multiple entries in the “APC, RWSC, WWSC settings vs. frequency of operation” table. • Removed footnote in the “APC, RWSC, WWSC settings vs. frequency of operation” table. • Changed the voltage in the “Pad AC specifications” table title from 4.5 V to 5.0 V. • Added the maximum LH/HL output delay values for pad type MultiV in the “Pad AC specifications (V_{DDE} = 3.3 V)” table.
Rev. 6	—	• Rev. 6 not published.

Table 53. Revision history (continued)

Revision	Date	Substantive changes
Rev. 7 (cont.)	01/12	• Added Table 17MPC5644A External network specification. • Updated Figure 8. • Changed External Network Parameter Ce min value to “3*2.35μF+5μF” from “2*2.35μF+5μF” in Table 17MPC5644A External network specification. • Changed Trans. Line (differential Zo) unit to Ω from W in Table 25DSPI LVDS pad specification.