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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	e200z4
Core Size	32-Bit Single-Core
Speed	150MHz
Connectivity	CANbus, EBI/EMI, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	84
Program Memory Size	4MB (4M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	1.14V ~ 5.25V
Data Converters	A/D 40x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=spc5644af0mlu1

Table 1. MPC5644A, MPC5634M and MPC5642A comparison (continued)

Feature		MPC5644A	MPC5634M	MPC5642A
	Micro Second Channel (MSC) bus downlink	Yes		
	DSPI_A	No		
	DSPI_B	Yes (with LVDS)		
	DSPI_C	Yes (with LVDS)		
	DSPI_D	Yes	No	Yes
FlexRay		Yes	No	Yes
System timers		5 PIT channels 4 STM channels 1 Software Watchdog		
eMIOS		24 ch.	16 ch.	24 ch.
eTPU		32 ch. eTPU2		
	Code memory	14 KB		
	Data memory	3 KB		
Interrupt controller		486 ch. ¹	307 ch.	486 ch. ¹
ADC		40 ch.	34 ch.	40 ch.
	ADC_A	Yes		
	ADC_B	Yes		
	Temp sensor	Yes		
	Variable gain amp.	Yes		
	Decimation filter	2	1	2
	Sensor diagnostics	Yes		
CRC		Yes	No	Yes
FMPLL		Yes		
VRC		Yes		
Supplies		5 V, 3.3 V ²	5 V, 3.3 V ³	5 V, 3.3 V ²
Low-power modes		Stop Mode Slow Mode		
Packages		176 LQFP ⁴ 208 MAPBGA ^{4,5} 324 TEPBGA324 ⁶ 496-pin CSP ⁷	144 LQFP 176 LQFP 208 MAPBGA 496-pin CSP ⁷	176 LQFP ⁴ 208 MAPBGA ^{4,5} 324 TEPBGA324 ⁶ 496-pin CSP ⁷

¹ 199 interrupt vectors are reserved.

² 5 V single supply only for 176 LQFP.

³ 5 V single supply only for 144 LQFP.

⁴ Pinout compatible with Freescale's MPC5634M devices.

⁵ Pinout compatible with Freescale's MPC5534.

⁶ Ballmap upwardly compatible with the standardized package ballmap used for various Freescale MPC5xxx family members, including MPC5554, MPC5567 and MPC5666.

⁷ For Freescale VertiCal Calibration System only.

1.4 Feature details

1.4.1 e200z4 core

MPC5644A devices have a high performance e200z448n3 core processor:

- Dual issue, 32-bit Power Architecture embedded category CPU
- Variable Length Encoding Enhancements
- 8 KB instruction cache: 2- or 4- way set associative instruction cache
- Thirty-two 64-bit general purpose registers (GPRs)
- Memory management unit (MMU) with 24-entry fully-associative translation look-aside buffer (TLB)
- Harvard Architecture: Separate instruction bus and load/store bus
- Vectored interrupt support
- Non-maskable interrupt input
- Critical Interrupt input
- New ‘Wait for Interrupt’ instruction, to be used with new low power modes
- Reservation instructions for implementing read-modify-write accesses
- Signal processing extension (SPE) APU
- Single Precision Floating point (scalar and vector)
- Nexus Class 3+ debug
- Process ID manipulation for the MMU using an external tool

1.4.2 Crossbar Switch (XBAR)

The XBAR multiport crossbar switch supports simultaneous connections between five master ports and four slave ports. The crossbar supports a 32-bit address bus width and a 64-bit data bus width.

The crossbar allows three concurrent transactions to occur from the master ports to any slave port but each master must access a different slave. If a slave port is simultaneously requested by more than one master port, arbitration logic selects the higher priority master and grants it ownership of the slave port. All other masters requesting that slave port are stalled until the higher priority master completes its transactions. Requesting masters are treated with equal priority and are granted access to a slave port in round-robin fashion, based upon the ID of the last master to be granted access. The crossbar provides the following features:

- 5 master ports
 - CPU instruction bus
 - CPU data bus
 - eDMA
 - FlexRay
 - External Bus Interface
- 4 slave ports
 - Flash
 - Calibration and EBI bus
 - SRAM
 - Peripheral bridge
- 32-bit internal address, 64-bit internal data paths

- Supports serial bootloading via FlexCAN bus and eSCI with auto baud rate sensing
- Supports serial bootloading of either Power Architecture code (default) or Freescale VLE code
- Supports booting from calibration bus interface
- Supports censorship protection for internal flash memory
- Provides an option to enable the core watchdog timer
- Provides an option to disable the system watchdog timer

1.4.10 eMIOS

The eMIOS timer module provides the capability to generate or measure events in hardware.

The eMIOS module features include:

- Twenty-four 24-bit wide channels
- 3 channels' internal timebases can be shared between channels
- 1 Timebase from eTPU2 can be imported and used by the channels
- Global enable feature for all eMIOS and eTPU timebases
- Dedicated pin for each channel (not available on all package types)

Each channel (0–23) supports the following functions:

- General-purpose input/output (GPIO)
- Single-action input capture (SAIC)
- Single-action output compare (SAOC)
- Output pulse-width modulation buffered (OPWMB)
- Input period measurement (IPM)
- Input pulse-width measurement (IPWM)
- Double-action output compare (DAOC)
- Modulus counter buffered (MCB)
- Output pulse width and frequency modulation buffered (OPWFMB)

1.4.11 eTPU2

The eTPU2 is an enhanced co-processor designed for timing control. Operating in parallel with the host CPU, the eTPU2 processes instructions and real-time input events, performs output waveform generation, and accesses shared data without host intervention. Consequently, for each timer event, the host CPU setup and service times are minimized or eliminated. A powerful timer subsystem is formed by combining the eTPU2 with its own instruction and data RAM. High-level assembler/compiler and documentation allows customers to develop their own functions on the eTPU2.

MPC5644A devices feature the second generation of the eTPU, called eTPU2. Enhancements of the eTPU2 over the standard eTPU include:

- The Timer Counter (TCR1), channel logic and digital filters (both channel and the external timer clock input [TCRCLK]) now have an option to run at full system clock speed or system clock / 2.
- Channels support unordered transitions: transition 2 can now be detected before transition 1. Related to this enhancement, the transition detection latches (TDL1 and TDL2) can now be independently negated by microcode.
- A new User Programmable Channel Mode has been added: the blocking, enabling, service request and capture characteristics of this channel mode can be programmed via microcode.
- Microinstructions now provide an option to issue Interrupt and Data Transfer requests selected by channel. They can also be requested simultaneously at the same instruction.
- Channel Flags 0 and 1 can now be tested for branching, in addition to selecting the entry point.
- Channel digital filters can be bypassed.

be used primarily as a vehicle serial data bus, meeting the specific requirements of this field: real-time processing, reliable operation in the EMI environment of a vehicle, cost-effectiveness and required bandwidth. Each FlexCAN module contains 64 message buffers.

The FlexCAN modules provide the following features:

- Based on and including all existing features of the Freescale TouCAN module
- Full Implementation of the CAN protocol specification, Version 2.0B
 - Standard data and remote frames
 - Extended data and remote frames
 - Zero to eight bytes data length
 - Programmable bit rate up to 1 Mbit/s
- Content-related addressing
- 64 message buffers of zero to eight bytes data length
- Individual Rx Mask Register per message buffer
- Each message buffer configurable as Rx or Tx, all supporting standard and extended messages
- Includes 1088 bytes of embedded memory for message buffer storage
- Includes 256-byte memory for storing individual Rx mask registers
- Full featured Rx FIFO with storage capacity for six frames and internal pointer handling
- Powerful Rx FIFO ID filtering, capable of matching incoming IDs against 8 extended, 16 standard or 32 partial (8 bits) IDs, with individual masking capability
- Selectable backwards compatibility with previous FlexCAN versions
- Programmable clock source to the CAN Protocol Interface, either system clock or oscillator clock
- Listen only mode capability
- Programmable loop-back mode supporting self-test operation
- 3 programmable Mask Registers
- Programmable transmit-first scheme: lowest ID, lowest buffer number or highest priority
- Time Stamp based on 16-bit free-running timer
- Global network time, synchronized by a specific message
- Maskable interrupts
- Warning interrupts when the Rx and Tx Error Counters reach 96
- Independent of the transmission medium (an external transceiver is assumed)
- Multi-master concept
- High immunity to EMI
- Short latency time due to an arbitration scheme for high-priority messages
- Low power mode, with programmable wake-up on bus activity

1.4.17 FlexRay

The MPC5644A includes one dual-channel FlexRay module that implements the FlexRay Communications System Protocol Specification, Version 2.1 Rev A. Features include:

- Single channel support
- FlexRay bus data rates of 10 Mbit/s, 8 Mbit/s, 5 Mbit/s, and 2.5 Mbit/s supported
- 128 message buffers, each configurable as:
 - Receive message buffer
 - Single buffered transmit message buffer
 - Double buffered transmit message buffer (combines two single buffered message buffer)
- 2 independent receive FIFOs

1.4.23 Calibration EBI

The Calibration EBI controls data transfer across the crossbar switch to/from memories or peripherals attached to the VertiCal connector in the calibration address space. The Calibration EBI is only available in the VertiCal Calibration System.

Features include:

- 1.8 V to 3.3 V \pm 10% I/O (1.6 V to 3.6 V)
- Memory controller supports various memory types
- 16-bit data bus, up to 22-bit address bus
- Pin muxing supports 32-bit muxed bus
- Selectable drive strength
- Configurable bus speed modes
- Bus monitor
- Configurable wait states

1.4.24 Power management controller (PMC)

The power management controller contains circuitry to generate the internal 3.3 V supply and to control the regulation of 1.2 V supply with an external NPN ballast transistor. It also contains low voltage inhibit (LVI) and power-on reset (POR) circuits for the 1.2 V supply, the 3.3 V supply, the 3.3 V/5 V supply of the closest I/O segment (VDDEH1) and the 5 V supply of the regulators (VDDREG).

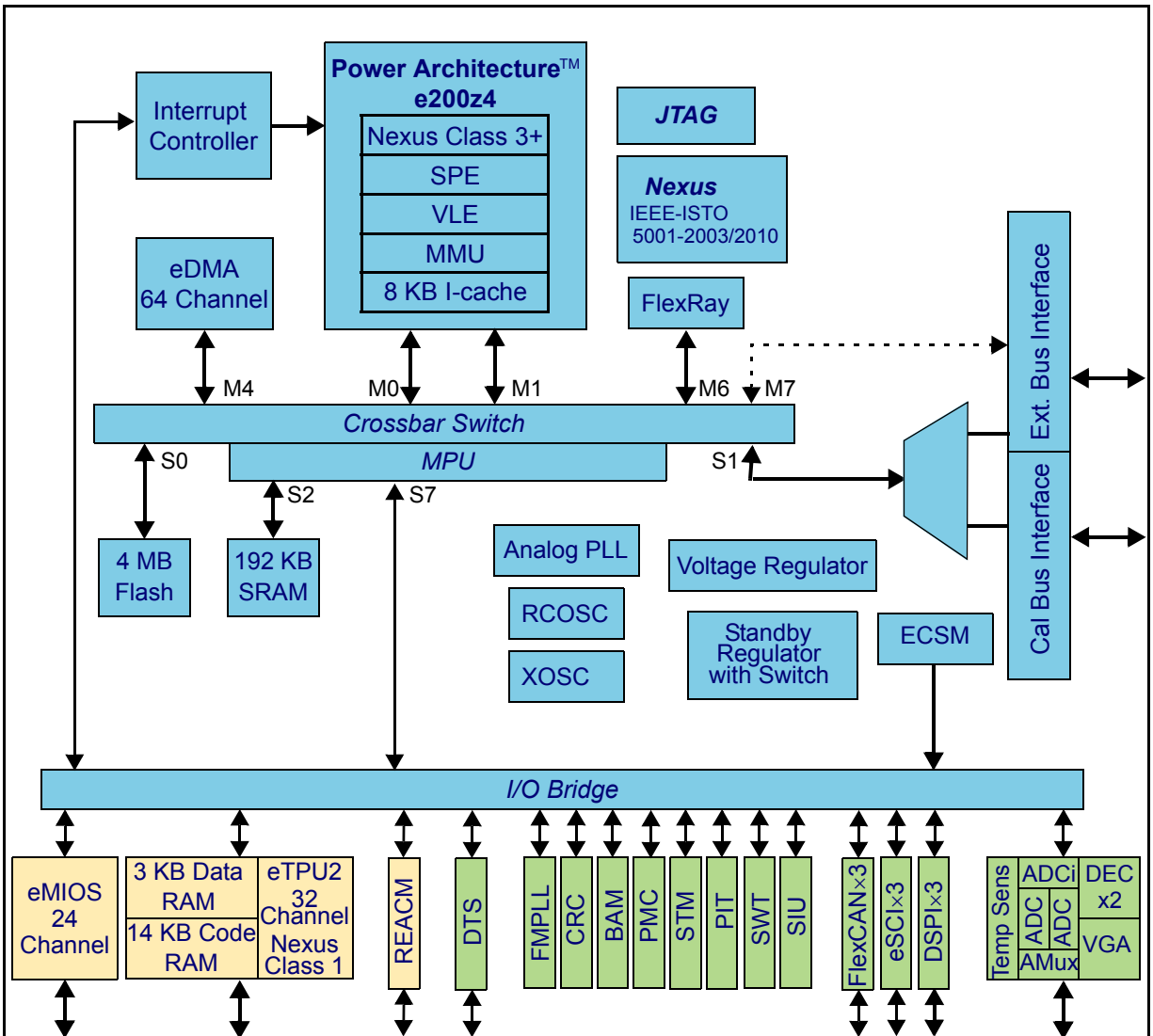
1.4.25 Nexus port controller

The NPC (Nexus Port Controller) block provides real-time Nexus Class3+ development support capabilities for the MPC5644A Power Architecture-based MCU in compliance with the IEEE-ISTO 5001-2003 and 2010 standards. MDO port widths of 4 pins and 12 pins are available in all packages.

1.4.26 JTAG

The JTAGC (JTAG Controller) block provides the means to test chip functionality and connectivity while remaining transparent to system logic when not in test mode. Testing is performed via a boundary scan technique, as defined in the IEEE 1149.1-2001 standard. All data input to and output from the JTAGC block is communicated in serial format. The JTAGC block is compliant with the IEEE 1149.1-2001 standard and supports the following features:

- IEEE 1149.1-2001 Test Access Port (TAP) interface 4 pins (TDI, TMS, TCK, and TDO)
- A 5-bit instruction register that supports the following IEEE 1149.1-2001 defined instructions:
 - BYPASS, IDCODE, EXTEST, SAMPLE, SAMPLE/PRELOAD, HIGHZ, CLAMP
- A 5-bit instruction register that supports the additional following public instructions:
 - ACCESS_AUX_TAP_NPC
 - ACCESS_AUX_TAP_ONCE
 - ACCESS_AUX_TAP_eTPU
 - ACCESS_CENSOR
- 3 test data registers to support JTAG Boundary Scan mode
 - Bypass register
 - Boundary scan register
 - Device identification register
- A TAP controller state machine that controls the operation of the data registers, instruction register and associated circuitry
- Censorship Inhibit Register



LEGEND

ADC	– Analog to Digital Converter	JTAG	– IEEE 1149.1 test controller
ADCi	– ADC interface	MMU	– Memory Management Unit
AMux	– Analog Multiplexer	MPU	– Memory Protection Unit
BAM	– Boot Assist Module	PMC	– Power Management Controller
CRC	– Cyclic Redundancy Check unit	PIT	– Periodic Interrupt Timer
DEC	– Decimation Filter	RCOSC	– low-speed RC oscillator
DTS	– Development Trigger Semaphore	REACM	– Reaction module
DSPI	– Deserial/Serial Peripheral Interface	SIU	– System Integration Unit
EBI	– External Bus Interface	SPE	– Signal Processing Extension
ECSM	– Error Correction Status Module	SRAM	– Static RAM
eDMA	– Enhanced Direct Memory Access	STM	– System Timer Module
eMIOS	– Enhanced Modular Input Output System	SWT	– Software Watchdog Timer
eSCI	– Enhanced Serial Communications Interface	VGA	– Variable Gain Amplifier
eTPU2	– Second gen. Enhanced Time Processing Unit	VLE	– Variable Length (instruction) Encoding
FlexCAN	– Controller Area Network (FlexCAN)	XOSC	– XTAL Oscillator
FMPLL	– Frequency-Modulated Phase Locked Loop		

Figure 1. MPC5644A series block diagram

Table 3. MPC5644A signal properties (continued)

Name	Function ¹	P A G ²	PCR PA Field ³	PCR ⁴	I/O Type	Voltage ⁵ / Pad Type ⁶	Status ⁷		Package pin #		
							During Reset	After Reset	176	208	324
ADDR16 FR_A_TX DATA16 GPIO[12]	External address bus Flexray TX data channel A External data bus GPIO	P A1 A2 G	001 010 100 000	12	I/O O I/O I/O	VDDE-EH Medium	— / Up	— / Up	—	—	P3
ADDR17 FR_A_TX_EN DATA17 GPIO[13]	External address bus FlexRay ch. A TX data enable External data bus GPIO	P A1 A2 G	001 010 100 000	13	I/O O I/O I/O	VDDE-EH Medium	— / Up	— / Up	—	—	P4
ADDR18 FR_A_RX DATA18 GPIO[14]	External address bus Flexray RX data ch. A External data bus GPIO	P A1 A2 G	001 010 100 000	14	I/O I I/O I/O	VDDE-EH Medium	— / Up	— / Up	—	—	R1
ADDR19 FR_B_TX DATA19 GPIO[15]	External address bus Flexray TX data ch. B External data bus GPIO	P A1 A2 G	001 010 100 000	15	I/O O I/O I/O	VDDE-EH Medium	— / Up	— / Up	—	—	R2
ADDR20 FR_B_TX_EN DATA20 GPIO[16]	External address bus Flexray TX data enable for ch. B External data bus GPIO	P A1 A2 G	001 010 100 000	16	I/O O I/O I/O	VDDE-EH Medium	— / Up	— / Up	—	—	R4
ADDR21 FR_B_RX DATA21 GPIO[17]	External address bus Flexray RX data channel B External data bus GPIO	P A1 A2 G	001 010 100 000	17	I/O I I/O I/O	VDDE-EH Medium	— / Up	— / Up	—	—	T1
ADDR22 DATA22 GPIO[18]	External address bus External data bus GPIO	P A2 G	001 100 000	18	I/O I/O I/O	VDDE-EH Medium	— / Up	— / Up	—	—	T2
ADDR23 DATA23 GPIO[19]	External address bus External data bus GPIO	P A2 G	001 100 000	19	I/O I/O I/O	VDDE-EH Medium	— / Up	— / Up	—	—	T3
ADDR24 DATA24 GPIO[20]	External address bus External data bus GPIO	P A2 G	001 100 000	20	I/O I/O I/O	VDDE-EH Medium	— / Up	— / Up	—	—	T4
ADDR25 DATA25 GPIO[21]	External address bus External data bus GPIO	P A2 G	001 100 000	21	I/O I/O I/O	VDDE-EH Medium	— / Up	— / Up	—	—	U1

Table 3. MPC5644A signal properties (continued)

Name	Function ¹	P A G ²	PCR PA Field ³	PCR ⁴	I/O Type	Voltage ⁵ / Pad Type ⁶	Status ⁷		Package pin #		
							During Reset	After Reset	176	208	324
AN29	Single-ended Analog Input	P	—	—	I	VDDA Analog	I / —	AN[29] / —	—	—	C11
AN30	Single-ended Analog Input	P	—	—	I	VDDA Analog	I / —	AN[30] / —	155	D9	B11
AN31	Single-ended Analog Input	P	—	—	I	VDDA Analog	I / —	AN[31] / —	154	D10	D12
AN32	Single-ended Analog Input	P	—	—	I	VDDA Analog	I / —	AN[32] / —	153	C10	C12
AN33	Single-ended Analog Input	P	—	—	I	VDDA Analog	I / —	AN[33] / —	152	C11	B12
AN34	Single-ended Analog Input	P	—	—	I	VDDA Analog	I / —	AN[34] / —	151	C5	A12
AN35	Single-ended Analog Input	P	—	—	I	VDDA Analog	I / —	AN[35] / —	150	D11	D13
AN36	Single-ended Analog Input	P	—	—	I	VDDA Analog	I / —	AN[36] / —	174	F4	B5
AN37	Single-ended Analog Input	P	—	—	I	VDDA Analog	I / —	AN[37] / —	175	E3	A5
AN38	Single-ended Analog Input	P	—	—	I	VDDA Analog	I / —	AN[38] / —	—	—	D3
AN39	Single-ended Analog Input	P	—	—	I	VDDA Analog	I / —	AN[39] / —	8	D2	D2
VRH	Voltage Reference High	P	—	—	I	VDDA —	I / —	VRH	163	A8	A10
VRL	Voltage Reference Low	P	—	—	I	VDDA —	I / —	VRL	162	A9	A11
REFBYBC	Reference Bypass Capacitor Input	P	—	—	I	VDDA Analog	I / —	REFBYPC	164	B7	B10
eTPU2											
TCRCLKA IRQ[7] GPIO[113]	eTPU A TCR clock External interrupt request GPIO	P A1 G	01 10 00	113	I I I/O	VDDEH4 Slow	— / Up	— / Up	—	L4	AB12

MPC5644A Microcontroller Data Sheet, Rev. 7

Name	Function ¹	P A G²	PCR PA Field³	PCR⁴	I/O Type	Voltage⁵ / Pad Type⁶	Status⁷		Package pin #		
							During Reset	After Reset	176	208	324
EMIOS11 DSPI_D_PCS[4] RCH3_C GPIO[190]	eMIOS channel DSPI D peripheral chip select Reaction channel 3C GPIO	P A1 A2 G	001 010 100 000	190	I/O O O I/O	VDDEH4 Medium	— / WKPCFG	— / WKPCFG	75	R8	AB15
EMIOS12 DSPI_C_SOUT ETPUA27_O ⁸ GPIO[191]	eMIOS channel DSPI C data output eTPU A channel (output only) GPIO	P A1 A2 G	001 010 100 000	191	I/O O O I/O	VDDEH4 Medium	— / WKPCFG	— / WKPCFG	76	N10	AB16
EMIOS13 DSPI_D_SOUT GPIO[192]	eMIOS channel DSPI D data output GPIO	P A1 G	01 10 00	192	I/O O I/O	VDDEH4 Medium	— / WKPCFG	— / WKPCFG	77	T8	AA16
EMIOS14 IRQ[0] ETPUA29_O ⁸ GPIO[193]	eMIOS channel External interrupt request eTPU A channel (output only) GPIO	P A1 A2 G	001 010 100 000	193	I/O I O I/O	VDDEH4 Slow	— / Down	— / Down	78	R9	Y16
EMIOS15 IRQ[1] GPIO[194]	eMIOS channel External interrupt request GPIO	P A1 G	01 10 00	194	I/O I I/O	VDDEH4 Slow	— / Down	— / Down	79	T9	W16
EMIOS16 GPIO[195]	eMIOS channel GPIO	P G	01 00	195	I/O I/O	VDDEH4 Slow	— / Up	— / Up	—	—	W17
EMIOS17 GPIO[196]	eMIOS channel GPIO	P G	01 00	196	I/O I/O	VDDEH4 Slow	— / Up	— / Up	—	—	Y17
EMIOS18 GPIO[197]	eMIOS channel GPIO	P G	01 00	197	I/O I/O	VDDEH4 Slow	— / Up	— / Up	—	—	AA17
EMIOS19 GPIO[198]	eMIOS channel GPIO	P G	01 00	198	I/O I/O	VDDEH4 Slow	— / WKPCFG	— / WKPCFG	—	—	AB17
EMIOS20 GPIO[199]	eMIOS channel GPIO	P G	01 00	199	I/O I/O	VDDEH4 Slow	— / WKPCFG	— / WKPCFG	—	—	AB18
EMIOS21 GPIO[200]	eMIOS channel GPIO	P G	01 00	200	I/O I/O	VDDEH4 Slow	— / WKPCFG	— / WKPCFG	—	—	AA18
EMIOS22 GPIO[201]	eMIOS channel GPIO	P G	01 00	201	I/O I/O	VDDEH4 Slow	— / Down	— / Down	—	—	Y18
EMIOS23 GPIO[202]	eMIOS channel GPIO	P G	01 00	202	I/O I/O	VDDEH4 Slow	— / Down	— / Down	80	R11	W18

Clock Synthesizer

Table 3. MPC5644A signal properties (continued)

Name	Function ¹	P A G ²	PCR PA Field ³	PCR ⁴	I/O Type	Voltage ⁵ / Pad Type ⁶	Status ⁷		Package pin #		
							During Reset	After Reset	176	208	324
VDDE12	External supply input for calibration bus interfaces	—		—	I	1.8 V - 3.3 V	I / —	VDDE12	—	—	—
VDDE2 ²³	External supply input for EBI interfaces	—		—	I	1.8 V - 3.3 V	I / —	VDDE2 ²⁴	—	—	M9, M10
VDDE5	External supply input for ENGCLK, CLKOUT and EBI signals DATA[0:15]	—		—	I	1.8 V - 3.3 V	I / —	VDDE5	—	T13	N11, W5, W8
VDDE-EH	External supply for EBI interfaces	—		—	I	3.0 V - 5 V	I / —	VDDE-EH	—	—	R3, V2
VDDEH1A ²⁵	I/O Supply Input	—		—	I	3.3 V - 5.0 V	I / —	VDDEH1A ²⁵	31	—	—
VDDEH1B ²⁵	I/O Supply Input	—		—	I	3.3 V - 5.0 V	I / —	VDDEH1B ²⁵	41	—	—
VDDEH1AB ²⁵	I/O Supply Input	—		—	I	3.3 V - 5.0 V	I / —	VDDEH1AB ²⁵	—	K4	K4
VDDEH4 ²⁶	I/O Supply Input	—		—	I	3.3 V - 5.0 V	I / —	VDDEH4 ²⁶	—	—	—
VDDEH4A ²⁶	I/O Supply Input	—		—	I	3.3 V - 5.0 V	I / —	VDDEH4A ²⁶	55	—	—
VDDEH4B ²⁶	I/O Supply Input	—		—	I	3.3 V - 5.0 V	I / —	VDDEH4B ²⁶	74	—	—
VDDEH4AB ²⁶	I/O Supply Input	—		—	I	3.3 V - 5.0 V	I / —	VDDEH4AB ²⁶	—	N9	W14, AA19
VDDEH6 ²⁷	I/O Supply Input	—		—	I	3.3 V - 5.0 V	I / —	VDDEH6 ²⁷	—	—	—
VDDEH6A ²⁷	I/O Supply Input	—		—	I	3.3 V - 5.0 V	I / —	VDDEH6A ²⁷	95	—	—
VDDEH6B ²⁷	I/O Supply Input	—		—	I	3.3 V - 5.0 V	I / —	VDDEH6B ²⁷	110	—	—
VDDEH6AB ²⁷	I/O Supply Input	—		—	I	3.3 V - 5.0 V	I / —	VDDEH6AB ²⁷	—	F13	M22, U19

- ⁴ V_{FLASH} is only available in the calibration package.
- ⁵ Power supply for multi-voltage pads cannot be below 4.5 V when in low-swing mode.
- ⁶ The slew rate (SRC) setting must be 0b11 when in low-swing mode.
- ⁷ While in low-swing mode there are no restrictions in transitioning to high-swing mode.
- ⁸ Pin in low-swing mode can accept a 5 V input.
- ⁹ All V_{OL}/V_{OH} values 100% tested with ± 2 mA load except where noted.
- ¹⁰ Bypass mode, system clock at 1 MHz (using system clock divider), PLL shut down, CPU running simple executive code, 4 x ADC conversion every 10 ms, 2 x PWM channels 1 kHz, all other modules stopped.
- ¹¹ Bypass mode, system clock at 1 MHz (using system clock divider), CPU stopped, PIT running, all other modules stopped.
- ¹² This current will be consumed for external regulation and internal regulation, when 3.3V regulator is switched off by shadow flash
- ¹³ If 1.2V and 3.3V internal regulators are on, then $iddreg=70mA$
If supply is external that is 3.3V internal regulator is off, then $iddreg=15mA$
- ¹⁴ Power requirements for each I/O segment are dependent on the frequency of operation and load of the I/O pins on a particular I/O segment, and the voltage of the I/O segment. See [Table 22](#) for values to calculate power dissipation for specific operation. The total power consumption of an I/O segment is the sum of the individual power consumptions for each pin on the segment.
- ¹⁵ Absolute value of current, measured at V_{IL} and V_{IH} .
- ¹⁶ Weak pull up/down inactive. Measured at $V_{DDE} = 3.6$ V and $V_{DDEH} = 5.25$ V. Applies to fast, slow, and medium pads.
- ¹⁷ Maximum leakage occurs at maximum operating temperature. Leakage current decreases by approximately one-half for each 8 to 12 °C, in the ambient temperature range of 50 to 125 °C. Applies to analog pads.
- ¹⁸ Applies to CLKOUT, external bus pins, and Nexus pins.
- ¹⁹ Applies to the FCK, SDI, SDO, and \overline{SDS} pins.
- ²⁰ This programmable option applies only to eQADC differential input channels and is used for biasing and sensor diagnostics.

3.9 I/O pad current specifications

The power consumption of an I/O segment depends on the usage of the pins on a particular segment. The power consumption is the sum of all output pin currents for a particular segment. The output pin current can be calculated from Table 22 based on the voltage, frequency, and load on the pin. Use linear scaling to calculate pin currents for voltage, frequency, and load parameters that fall outside the values given in Table 22.

Table 22. I/O pad average I_{DDE} specifications¹

Pad Type	Symbol	C		Period (ns)	Load ² (pF)	V _{DDE} (V)	Drive/Slew Rate Select	I _{DDE} Avg (mA) ³	I _{DDE} RMS (mA)
Slow	I _{DRV_SSR_HV}	CC	D	37	50	5.5	11	9	—
		CC	D	130	50	5.5	01	2.5	—
		CC	D	650	50	5.5	00	0.5	—
		CC	D	840	200	5.5	00	1.5	—
Medium	I _{DRV_MSR_HV}	CC	D	24	50	5.5	11	14	—
		CC	D	62	50	5.5	01	5.3	—
		CC	D	317	50	5.5	00	1.1	—
		CC	D	425	200	5.5	00	3	—
Fast	I _{DRV_FC}	CC	D	10	50	3.6	11	22.7	68.3
		CC	D	10	30	3.6	10	12.1	41.1
		CC	D	10	20	3.6	01	8.3	27.7
		CC	D	10	10	3.6	00	4.44	14.3
		CC	D	10	50	1.98	11	12.5	31
		CC	D	10	30	1.98	10	7.3	18.6
		CC	D	10	20	1.98	01	5.42	12.6
		CC	D	10	10	1.98	00	2.84	6.4
MultiV (High Swing Mode)	I _{DRV_MULTV_HV}	CC	D	20	50	5.5	11	9	—
		CC	D	30	50	5.5	01	6.1	—
		CC	D	117	50	5.5	00	2.3	—
		CC	D	212	200	5.5	00	5.8	—
MultiV (Low Swing Mode)	I _{DRV_MULTV_HV}	CC	D	30	30	5.5	11	3.4	—

¹ Numbers from simulations at best case process, 150 °C.

² All loads are lumped.

³ Average current is for pad configured as output only.

Table 24. V_{RC33} pad average DC current¹

Pad Type	Symbol		C	Period (ns)	Load ² (pF)	V _{RC33} (V)	V _{DDE} (V)	Drive Select	I _{DD33} Avg (μA)	I _{DD33} RMS (μA)
Fast	I _{DRV_FC}	CC	D	10	50	3.6	3.6	11	2.35	6.12
		CC	D	10	30	3.6	3.6	10	1.75	4.3
		CC	D	10	20	3.6	3.6	01	1.41	3.43
		CC	D	10	10	3.6	3.6	00	1.06	2.9
		CC	D	10	50	3.6	1.98	11	1.75	4.56
		CC	D	10	30	3.6	1.98	10	1.32	3.44
		CC	D	10	20	3.6	1.98	01	1.14	2.95
		CC	D	10	10	3.6	1.98	00	0.95	2.62

¹ These are typical values that are estimated from simulation and not tested. Currents apply to output pins only.

² All loads are lumped.

3.9.2 LVDS pad specifications

LVDS pads are implemented to support the MSC (Microsecond Channel) protocol which is an enhanced feature of the DSPI module. The LVDS pads are compliant with LVDS specifications and support data rates up to 50 MHz.

Table 25. DSPI LVDS pad specification

#	Characteristic	Symbol	C	Condition	Min. Value	Typ. Value	Max. Value	Unit	
Data Rate									
4	Data Frequency	f _{LVDSCLK}	CC	D	—		50		MHz
Driver Specs									
5	Differential output voltage	V _{OD}	CC	P	SRC=0b00 or 0b11	150		400	mV
			CC	P	SRC=0b01	90		320	
			CC	P	SRC=0b10	160		480	
6	Common mode voltage (LVDS), VOS	V _{OD}	CC	P		1.06	1.2	1.39	V
7	Rise/Fall time	T _R /T _F	CC	D	—		2		ns
8	Propagation delay (Low to High)	T _{PLH}	CC	D			4		ns
9	Propagation delay (High to Low)	T _{PHL}	CC	D	—		4		ns
10	Delay (H/L), sync Mode	t _{PDSYNC}	CC	D			4		ns

¹³ Stand alone input buffer. Also has weak pull-up/pull-down.

Table 36. Pad AC specifications ($V_{DDE} = 3.3 \text{ V}$)¹

Pad Type		C	Output Delay (ns) ^{2,3} Low-to-High / High-to-Low		Rise/Fall Edge (ns) ^{3,4}		Drive Load (pF)	SRC/DSC
			Min	Max	Min	Max		MSB,LSB
Medium ^{5,6,7}	CC	D	5.8/4.4	18/17	2.7/2.1	10/10	50	11 ⁸
	CC	D	16/13	46/49	11.2/8.6	34/34	200	
	N/A							10 ⁹
	CC	D	14/16	37/45	6.5/6.7	19/19	50	01
	CC	D	27/27	69/82	15/13	43/43	200	
	CC	D	83/86	200/210	38/38	86/86	50	00
	CC	D	113/109	270/285	53/46	120/120	200	
Slow ^{7,10}	CC	D	9.2/6.9	27/28	5.5/4.1	20/20	50	11
	CC	D	30/23	81/87	21/16	63/63	200	
	N/A							10 ⁹
	CC	D	31/31	80/90	15.4/15.4	42/42	50	01
	CC	D	58/52	144/155	32/26	82/85	200	
	CC	D	162/168	415/415	80/82	190/190	50	00
	CC	D	216/205	533/540	106/95	250/250	200	
MultiV ^{7,11} (High Swing Mode)	CC	D		3.7/3.1		10/10	30	11 ⁸
	CC	D		46/49		37/37	200	
	N/A							10 ⁹
	CC	D		32		15/15	50	01
	CC	D		72		46/46	200	
	CC	D		210		100/100	50	00
	CC	D		295		134/134	200	
MultiV (Low Swing Mode)	Not a valid operational mode							
Fast	CC	D		2.5/2.5		1.2/1.2	10	00
	CC	D		2.5/2.5		1.2/1.2	20	01
	CC	D		2.5/2.5		1.2/1.2	30	10
	CC	D		2.5/2.5		1.2/1.2	50	11 ⁸
pad_i_hv ¹²	CC	D	0.5/0.5	3/3	0.4/0.4	±1.5/1.5	0.5	N/A
pull_hv	CC	D	NA	6000		5000/5000	50	N/A

¹ These are worst case values that are estimated from simulation and not tested. The values in the table are simulated at $V_{DD} = 1.14 \text{ V}$ to 1.32 V , $V_{DDE} = 3 \text{ V}$ to 3.6 V , $V_{DDEH} = 3 \text{ V}$ to 3.6 V , $T_A = T_L$ to T_H .

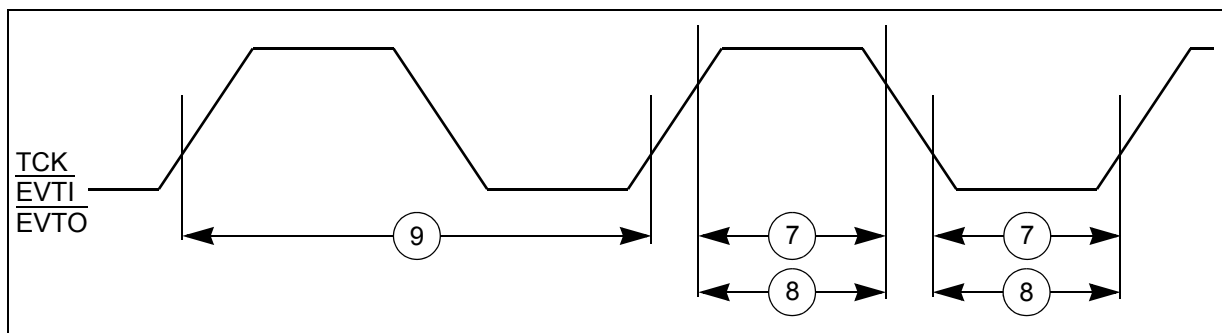


Figure 16. Nexus event trigger and test clock timings

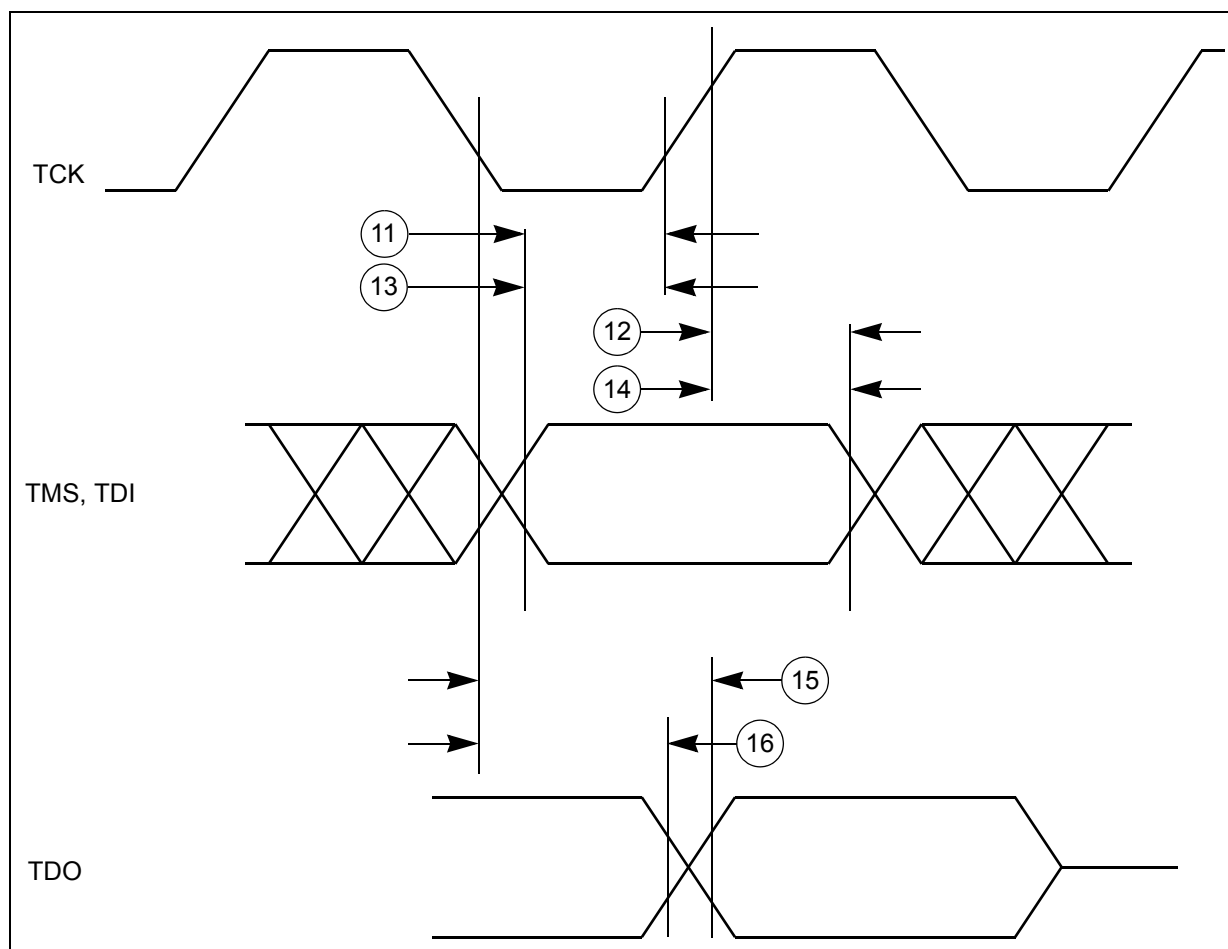


Figure 17. Nexus TDI, TMS, TDO timing

3.17.7 eMIOS timing

Table 46. eMIOS timing¹

#	Symbol	C	Characteristic	Min. Value	Max. Value	Unit	
1	t _{MIPW}	CC	D	eMIOS Input Pulse Width	4	—	t _{CYC}
2	t _{MOPW}	CC	D	eMIOS Output Pulse Width	1	—	t _{CYC}

¹ eMIOS timing specified at f_{sys} = 80 MHz, V_{DD} = 1.14 V to 1.32 V, V_{DDEH} = 4.5 V to 5.5 V, T_A = T_L to T_H, and C_L = 50 pF with SRC = 0b00.

3.17.8 DSPI timing

DSPI channel frequency support for the MPC5644A MCU is shown in Table 47. Timing specifications are in Table 48.

Table 47. DSPI channel frequency support

System Clock (MHz)	DSPI Use Mode	Max. Usable Frequency (MHz)	Notes
150	LVDS	37.5	Use sysclock /4 divide ratio.
	Non-LVDS	18.75	Use sysclock /8 divide ratio.
120	LVDS	40	Use sysclock /3 divide ratio. Gives 33/66 duty cycle. Use DSPI configuration DBR=0b1 (double baud rate), BR=0b0000 (scaler value 2) and PBR=0b01 (prescaler value 3).
	Non-LVDS	20	Use sysclock /6 divide ratio.
80	LVDS	40	Use sysclock /2 divide ratio.
	Non-LVDS	20	Use sysclock /4 divide ratio.

Table 48. DSPI timing^{1,2}

#	Symbol	C	Characteristic	Condition	Min.	Max.	Unit
1	t _{SCK}	CC	D	SCK Cycle Time ^{3,4,5}	24.4 ns	2.9 ms	—
2	t _{CSC}	CC	D	PCS to SCK Delay ⁶	22 ⁷	—	ns
3	t _{ASC}	CC	D	After SCK Delay ⁸	21 ⁹	—	ns
4	t _{SDC}	CC	D	SCK Duty Cycle	(1/2t _{SC})–2	(1/2t _{SC})+2	ns
5	t _A	CC	D	Slave Access Time (\overline{SS} active to SOUT driven)	—	25	ns
6	t _{DIS}	CC	D	Slave SOUT Disable Time (\overline{SS} inactive to SOUT High-Z or invalid)	—	25	ns
7	t _{PCSC}	CC	D	PCSx to \overline{PCSS} time	4 ¹⁰	—	ns
8	t _{PASC}	CC	D	\overline{PCSS} to PCSx time	5 ¹¹	—	ns

3.17.10 FlexCAN system clock source

Table 50. FlexCAN engine system clock divider threshold

#	Symbol	Characteristic	Value	Unit
1	F _{CAN_TH}	FlexCAN engine system clock threshold	100	MHz

Table 51. FlexCAN engine system clock divider

System Frequency	Required SIU_SYSDIV[CAN_SRC] Value
$\leq F_{CAN_TH}$	0 ^{1,2}
$> F_{CAN_TH}$	1 ^{2,3}

¹ Divides system clock source for FlexCAN engine by 1.

² System clock is only selected for FlexCAN when CAN_CR[CLK_SRC] = 1.

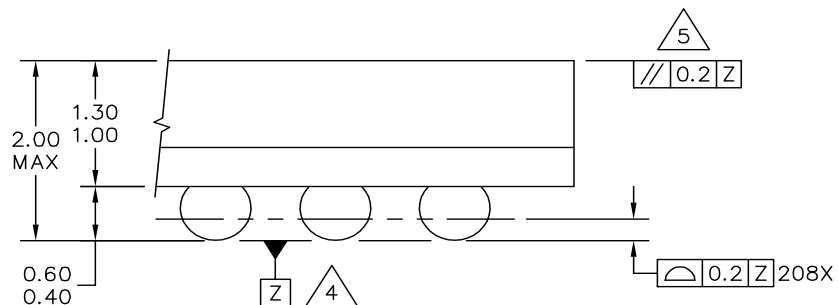
³ Divides system clock source for FlexCAN engine by 2.

NOTES:

1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25MM PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE DATUM H.
2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THEN 0.08MM. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07MM FOR 0.4MM AND 0.5MM PITCH PACKAGES.

DIM	MIN	NOM	MAX	DIM	MIN	NOM	MAX	DIM	MIN	NOM	MAX
A	---		1.6	L1		1 REF					
A1	0.05		0.15	R1	0.08		---				
A2	1.35	1.4	1.45	R2	0.08		0.2				
b	0.17	0.22	0.27	S		0.2 REF					
b1	0.17	0.2	0.23	θ	0°	3.5°	7°				
c	0.09		0.2	θ1	0°		---				
c1	0.09		0.16	θ2	11°	12°	13°				
D		26 BSC		θ3	11°	12°	13°				
D1		24 BSC									
e		0.5 BSC									
E		26 BSC									
E1		24 BSC									
L	0.45	0.6	0.75	UNIT		DIMENSION AND TOLERANCES			REFERENCE DOCUMENT		
				MM		ASME Y14.5M			64-06-280-1392		
TITLE: LQFP 176LD 24X24X1.4 PKG 0.5 PITCH POD 2mm FOOTPRINT											
						SHEET			3		

Figure 35. 176 LQFP package mechanical drawing (part 3)



DETAIL K
(ROTATED 90° CLOCKWISE)

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE Z.
4. DATUM Z (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

TITLE: 208 I/O MAP BGA, 17 X 17 PKG, 1-MM PITCH	CASE NUMBER: 1159A-01	
	STANDARD: JEDEC MO-151 AAF-1	
	PACKAGE CODE: 5253	SHEET: 2

Figure 37. 208 MAPBGA package mechanical drawing (part 2)

Table 53. Revision history (continued)

Revision	Date	Substantive changes
Rev. 4 (cont)	08/2010	<p>Change in signal name notation for DSPI, CAN and SCI signals:</p> <p>DSPI: PCS_x[n] is now DSPI_x_PCS[n] SOUT_x is now DSPI_x_SOUT SIN_x is now DSPI_x_SIN SCK_x is now DSPI_x_SCK</p> <p>CAN: CNTXx is now CAN_x_TX CNRXx is now CAN_x_RX</p> <p>SCI: RDXx is now SCI_x_RX TXDx is now SCI_x_TX</p> <p>Updates to DC electrical specifications:</p> <ul style="list-style-type: none"> • Slew rate on power supply pins specification changed to 25 V/ms (was 50 V/ms) <p>V_{OH_LS} min spec changed to 2.0 V at 0.5 mA (was 2.7 V at 0.5 mA)</p> <p>Updated I/O pad current specifications</p> <p>Updated I/O pad V_{RC33} current specifications</p> <p>Corrections to Nexus timing:</p> <ul style="list-style-type: none"> • Maximum Nexus debug port operating frequency is 40 MHz in all configurations • To route Nexus to MDO, clear NPC_PCR[NEXCFG] (formerly this was documented as NPC_PCR[CAL]) • To route Nexus to CAL_MDO, set NPC_PCR[NEXCFG]=1 (formerly this was documented as NPC_PCR[CAL])