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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	84
Program Memory Size	4MB (4M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	1.14V ~ 5.25V
Data Converters	A/D 40x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=spc5644af0mlu2

— 1 receive FIFO per channel
— Up to 255 entries for each FIFO
- ECC support

1.4.18 System timers

The system timers include two distinct types of system timer:

- Periodic interrupts/triggers using the Periodic Interrupt Timer (PIT)
- Operating system task monitors using the System Timer Module (STM)

1.4.18.1 Periodic interrupt timer (PIT)

The PIT provides five independent timer channels, capable of producing periodic interrupts and periodic triggers. The PIT has no external input or output pins and is intended to provide system 'tick' signals to the operating system, as well as periodic triggers for eQADC queues. Of the five channels in the PIT, four are clocked by the system clock and one is clocked by the crystal clock. This one channel is also referred to as Real-Time Interrupt (RTI) and is used to wake up the device from low power stop mode.

The following features are implemented in the PIT:

- 5 independent timer channels
- Each channel includes 32-bit wide down counter with automatic reload
- 4 channels clocked from system clock
- 1 channel clocked from crystal clock (wake-up timer)
- Wake-up timer remains active when System STOP mode is entered; used to restart system clock after predefined time-out period
- Each channel optionally able to generate an interrupt request or a trigger event (to trigger eQADC queues) when timer reaches zero

1.4.18.2 System timer module (STM)

The System Timer Module (STM) is designed to implement the software task monitor as defined by AUTOSAR[1]. It consists of a single 32-bit counter, clocked by the system clock, and four independent timer comparators. These comparators produce a CPU interrupt when the timer exceeds the programmed value.

The following features are implemented in the STM:

- One 32-bit up counter with 8-bit prescaler
- Four 32-bit compare channels
- Independent interrupt source for each channel
- Counter can be stopped in debug mode

1.4.19 Software watchdog timer (SWT)

The Software Watchdog Timer (SWT) is a second watchdog module to complement the standard Power Architecture watchdog integrated in the CPU core. The SWT is a 32-bit modulus counter, clocked by the system clock or the crystal clock, that can provide a system reset or interrupt request when the correct software key is not written within the required time window.

The following features are implemented:

- 32-bit modulus counter
- Clocked by system clock or crystal clock

1.AUTOSAR: AUTomotive Open System ARchitecture (see http://www.autosar.org)

Table 3. MPC5644A signal properties (continued)

Name	Function[1]	PAG[2]	PCR PA Field[3]	PCR[4]	I/O Type	Voltage[5] / Pad Type[6]	Status[7]		Package pin #		
							During Reset	After Reset	176	208	324
CAL_DATA[2]	Calibration data bus	P	01	341	I/O	VDDE12 Fast	— / Up	— / Up	—	—	—
CAL_DATA[3]	Calibration data bus	P	01	341	I/O	VDDE12 Fast	— / Up	— / Up	—	—	—
CAL_DATA[4]	Calibration data bus	P	01	341	I/O	VDDE12 Fast	— / Up	— / Up	—	—	—
CAL_DATA[5]	Calibration data bus	P	01	341	I/O	VDDE12 Fast	— / Up	— / Up	—	—	—
CAL_DATA[6]	Calibration data bus	P	01	341	I/O	VDDE12 Fast	— / Up	— / Up	—	—	—
CAL_DATA[7]	Calibration data bus	P	01	341	I/O	VDDE12 Fast	— / Up	— / Up	—	—	—
CAL_DATA[8]	Calibration data bus	P	01	341	I/O	VDDE12 Fast	— / Up	— / Up	—	—	—
CAL_DATA[9]	Calibration data bus	P	01	341	I/O	VDDE12 Fast	— / Up	— / Up	—	—	—
CAL_DATA[10]	Calibration data bus	P	01	341	I/O	VDDE12 Fast	— / Up	— / Up	—	—	—
CAL_DATA[11]	Calibration data bus	P	01	341	I/O	VDDE12 Fast	— / Up	— / Up	—	—	—
CAL_DATA[12]	Calibration data bus	P	01	341	I/O	VDDE12 Fast	— / Up	— / Up	—	—	—
CAL_DATA[13]	Calibration data bus	P	01	341	I/O	VDDE12 Fast	— / Up	— / Up	—	—	—
CAL_DATA[14]	Calibration data bus	P	01	341	I/O	VDDE12 Fast	— / Up	— / Up	—	—	—
CAL_DATA[15]	Calibration data bus	P	01	341	I/O	VDDE12 Fast	— / Up	— / Up	—	—	—
CAL_RD_WR	Calibration read/write enable	P	01	342	O	VDDE12 Fast		— / —	—	—	—
CAL_$\overline{WE}$[0]/$\overline{BE}$[0]	Calibration write/byte enable	P	01	342	O	VDDE12 Fast		— / —	—	—	—

Table 3. MPC5644A signal properties (continued)

Name	Function[1]	PAG[2]	PCR PA Field[3]	PCR[4]	I/O Type	Voltage[5] / Pad Type[6]	Status[7]		Package pin #		
							During Reset	After Reset	176	208	324
SCI_A_TX EMIOS13[8] GPIO[89]	eSCI A TX eMIOS channel GPIO	P A1 G	01 10 00	89	O O I/O	VDDEH6 Medium	— / Up	— / Up	100	J14	N20
SCI_A_RX EMIOS15[8] GPIO[90]	eSCI A RX eMIOS channel GPIO	P A1 G	01 10 00	90	I O I/O	VDDEH6 Medium	— / Up	— / Up	99	K14	P20
SCI_B_TX DSPI_D_PCS[1] GPIO[91]	eSCI B TX DSPI D peripheral chip select GPIO	P A1 G	01 10 00	91	O O I/O	VDDEH6 Medium	— / Up	— / Up	87	L13	AB21
SCI_B_RX DSPI_D_PCS[5] GPIO[92]	eSCI B RX DSPI D peripheral chip select GPIO	P A1 G	01 10 00	92	I O I/O	VDDEH6 Medium	— / Up	— / Up	84	M13	AB20
SCI_C_TX GPIO[244]	eSCI C TX GPIO	P G	01 00	244	O I/O	VDDEH6 Medium	— / Up	— / Up	—	—	W19
SCI_C_RX GPIO[245]	eSCI C RX GPIO	P G	01 00	245	I I/O	VDDEH6 Medium	— / Up	— / Up	—	—	V19
DSPI											
DSPI_A_SCK[17] DSPI_C_PCS[1] GPIO[93]	— DSPI C peripheral chip select GPIO	— A1 G	— 10 00	93	— O I/O	VDDEH7 Medium	— / Up	— / Up	—	—	C17
DSPI_A_SIN[17] DSPI_C_PCS[2] GPIO[94]	— DSPI C peripheral chip select GPIO	— A1 G	— 10 00	94	— O I/O	VDDEH7 Medium	— / Up	— / Up	—	—	B17
DSPI_A_SOUT[17] DSPI_C_PCS[5] GPIO[95]	— DSPI C peripheral chip select GPIO	— A1 G	— 10 00	95	— O I/O	VDDEH7 Medium	— / Up	— / Up	—	—	A17
DSPI_A_PCS[0][17] DSPI_D_PCS[2] GPIO[96]	— DSPI D peripheral chip select GPIO	— A1 G	— 10 00	96	— O I/O	VDDEH7 Medium	— / Up	— / Up	—	—	D16
DSPI_A_PCS[1][17] DSPI_B_PCS[2] GPIO[97]	— DSPI B peripheral chip select GPIO	— A1 G	— 10 00	97	— O I/O	VDDEH7 Medium	— / Up	— / Up	—	—	C16
CS[2] DSPI_D_SCK GPIO[98]	— SPI clock pin for DSPI module GPIO	— A1 G	— 10 00	98	— I/O I/O	VDDEH7 Medium	— / Up	— / Up	141	J15	C15

Table 3. MPC5644A signal properties (continued)

Name	Function[1]	PAG[2]	PCR PA Field[3]	PCR[4]	I/O Type	Voltage[5] / Pad Type[6]	Status[7]		Package pin #		
							During Reset	After Reset	176	208	324
ETPUA17 DSPI_D_PCS[2] RCH3_A GPIO[131]	eTPU A channel DSPI D peripheral chip select Reaction channel 3A GPIO	P A1 A2 G	001 010 100 000	131	I/O O O I/O	VDDEH1 Slow	— / WKPCFG	— / WKPCFG	38	H3	Y1
ETPUA18 DSPI_D_PCS[3] RCH4_A GPIO[132]	eTPU A channel DSPI D peripheral chip select Reaction channel 4A GPIO	P A1 A2 G	001 010 100 000	132	I/O O O I/O	VDDEH1 Slow	— / WKPCFG	— / WKPCFG	37	H4	W3
ETPUA19 DSPI_D_PCS[4] RCH5_A GPIO[133]	eTPU A channel DSPI D peripheral chip select Reaction channel 5A GPIO	P A1 A2 G	001 010 100 000	133	I/O O O I/O	VDDEH1 Slow	— / WKPCFG	— / WKPCFG	36	J2	W2
ETPUA20 IRQ[8] RCH0_B FR_A_TX GPIO[134]	eTPU A channel External interrupt request Reaction channel 0B Flexray TX data channel A GPIO	P A1 A2 A3 G	0001 0010 0100 1000 0000	134	I/O I O O I/O	VDDEH1 Slow	— / WKPCFG	— / WKPCFG	35	J1	W1
ETPUA21 IRQ[9] RCH0_C FR_A_RX GPIO[135]	eTPU A channel External interrupt request Reaction channel 0C Flexray RX channel A GPIO	P A1 A2 A3 G	0001 0010 0100 1000 0000	135	I/O I O I I/O	VDDEH1 Slow	— / WKPCFG	— / WKPCFG	34	G4	N4
ETPUA22 IRQ[10] ETPUA17_O[8] GPIO[136]	eTPU A channel External interrupt request eTPU A channel (output only) GPIO	P A1 A2 G	001 010 100 000	136	I/O I O I/O	VDDEH1 Slow	— / WKPCFG	— / WKPCFG	32	H2	N3
ETPUA23 IRQ[11] ETPUA21_O[8] FR_A_TX_EN GPIO[137]	eTPU A channel External interrupt request eTPU A channel (output only) Flexray ch. A TX enable GPIO	P A1 A2 A3 G	0001 0010 0100 1000 0000	137	I/O I O O I/O	VDDEH1 Slow	— / WKPCFG	— / WKPCFG	30	H1	M1
ETPUA24 IRQ[12] DSPI_C_SCK_LV DS- GPIO[138]	eTPU A channel External interrupt request LVDS negative DSPI clock GPIO	P A1 A2 G	001 010 100 000	138	I/O I O I/O	VDDEH1 Slow + LVDS	— / WKPCFG	— / WKPCFG	28	G1	M2

Table 3. MPC5644A signal properties (continued)

Name	Function[1]	PAG[2]	PCR PA Field[3]	PCR[4]	I/O Type	Voltage[5] / Pad Type[6]	Status[7]		Package pin #		
							During Reset	After Reset	176	208	324
ETPUA25 IRQ[13] DSPI_C_SCK_LVDS+ GPIO[139]	eTPU A channel External interrupt request LVDS positive DSPI clock GPIO	P A1 A2 G	001 010 100 000	139	I/O I O I/O	VDDEH1 Medium + LVDS	— / WKPCFG	— / WKPCFG	27	G3	M3
ETPUA26 IRQ[14] DSPI_C_SOUT_LVDS- GPIO[140]	eTPU A channel External interrupt request LVDS negative DSPI data out GPIO	P A1 A2 G	001 010 100 000	140	I/O I O I/O	VDDEH1 Slow + LVDS	— / WKPCFG	— / WKPCFG	26	F3	L2
ETPUA27 IRQ[15] DSPI_C_SOUT_LVDS+ DSPI_B_SOUT GPIO[141]	eTPU A channel External interrupt request LVDS positive DSPI data out DSPI data out GPIO	P A1 A2 A3 G	0001 0010 0100 1000 0000	141	I/O I O O I/O	VDDEH1 Slow + LVDS	— / WKPCFG	— / WKPCFG	25	G2	L1
ETPUA28 DSPI_C_PCS[1] RCH5_B GPIO[142]	eTPU A channel DSPI C peripheral chip select Reaction channel 5B GPIO	P A1 A2 G	001 010 100 000	142	I/O O O I/O	VDDEH1 Medium	— / WKPCFG	— / WKPCFG	24	F1	M4
ETPUA29 DSPI_C_PCS[2] RCH5_C GPIO[143]	eTPU A channel DSPI C peripheral chip select Reaction channel 5C GPIO	P A1 A2 G	001 010 100 000	143	I/O O O I/O	VDDEH1 Medium	— / WKPCFG	— / WKPCFG	23	F2	L3
ETPUA30 DSPI_C_PCS[3] ETPUA11_O[8] GPIO[144]	eTPU A channel DSPI C peripheral chip select eTPU A channel (output only) GPIO	P A1 A2 G	001 010 100 000	144	I/O O O I/O	VDDEH1 Medium	— / WKPCFG	— / WKPCFG	22	E1	L4
ETPUA31 DSPI_C_PCS[4] ETPUA13_O[8] GPIO[145]	eTPU A channel DSPI C peripheral chip select eTPU A channel (output only) GPIO	P A1 A2 G	001 010 100 000	145	I/O O O I/O	VDDEH1 Medium	— / WKPCFG	— / WKPCFG	21	E2	K1
eMIOS											
EMIOS0 ETPUA0_O[8] ETPUA25_O[8] GPIO[179]	eMIOS channel eTPU A channel (output only) eTPU A channel (output only) GPIO	P A1 A2 G	001 010 100 000	179	I/O O O I/O	VDDEH4 Slow	— / Up	— / Up	63	T4	AA12

Table 3. MPC5644A signal properties (continued)

Name	Function[1]	PAG[2]	PCR PA Field[3]	PCR[4]	I/O Type	Voltage[5] / Pad Type[6]	Status[7]		Package pin #		
							During Reset	After Reset	176	208	324
EMIOS1 ETPUA1_O[8] GPIO[180]	eMIOS channel eTPU A channel (output only) GPIO	P A1 G	01 10 00	180	I/O O I/O	VDDEH4 Slow	— / Up	— / Up	64	T5	W13
EMIOS2 ETPUA2_O[8] RCH2_B GPIO[181]	eMIOS channel eTPU A channel (output only) Reaction channel 2B GPIO	P A1 A2 G	001 010 100 000	181	I/O O O I/O	VDDEH4 Slow	— / Up	— / Up	65	N7	Y13
EMIOS3 ETPUA3_O[8] GPIO[182]	eMIOS channel eTPU A channel (output only) GPIO	P A1 G	01 10 00	182	I/O O I/O	VDDEH4 Slow	— / WKPCFG	— / WKPCFG	66	R6	AA13
EMIOS4 ETPUA4_O[8] RCH2_C GPIO[183]	eMIOS channel eTPU A channel (output only) Reaction channel 2C GPIO	P A1 A2 G	001 010 100 000	183	I/O O O I/O	VDDEH4 Slow	— / WKPCFG	— / WKPCFG	67	R5	AB13
EMIOS5 ETPUA5_O[8] GPIO[184]	eMIOS channel eTPU A channel (output only) GPIO	P A1 G	01 10 00	184	I/O O I/O	VDDEH4 Slow	— / WKPCFG	— / WKPCFG	—	—	Y14
EMIOS6 ETPUA6_O[8] GPIO[185]	eMIOS channel eTPU A channel (output only) GPIO	P A1 G	01 10 00	185	I/O O I/O	VDDEH4 Slow	— / Down	— / Down	68	P7	AA14
EMIOS7 ETPUA7_O[8] GPIO[186]	eMIOS channel eTPU A channel (output only) GPIO	P A1 G	01 10 00	186	I/O O I/O	VDDEH4 Slow	— / Down	— / Down	69	—	AB14
EMIOS8 ETPUA8_O[8] SCI_B_TX GPIO[187]	eMIOS channel eTPU A channel (output only) eSCI B TX GPIO	P A1 A2 G	001 010 100 000	187	I/O O O I/O	VDDEH4 Slow	— / Up	— / Up	70	P8	W15
EMIOS9 ETPUA9_O[8] SCI_B_RX GPIO[188]	eMIOS channel eTPU A channel (output only) eSCI B RX GPIO	P A1 A2 G	001 010 100 000	188	I/O O I I/O	VDDEH4 Slow	— / Up	— / Up	71	R7	Y15
EMIOS10 DSPI_D_PCS[3] RCH3_B GPIO[189]	eMIOS channel DSPI D peripheral chip select Reaction channel 3B GPIO	P A1 A2 G	001 010 100 000	189	I/O O O I/O	VDDEH4 Medium	— / WKPCFG	— / WKPCFG	73	N8	AA15

Table 5. Signal details (continued)

Signal	Module or Function	Description
GPIO[0:3] GPIO[8:43] GPIO[62:65] GPIO[68:70] GPIO[75:145] GPIO[179:204] GPIO[208:213] GPIO[219] GPIO[244:245]	SIU - GPIO	Configurable general purpose I/O pins. Each GPIO input and output is separately controlled by an 8-bit input (GPDI) or output (GPDO) register. Additionally, each GPIO pins is configured using a dedicated SIU_PCR register. The GPIO pins are generally multiplexed with other I/O pin functions. See The *MPC5644A Microcontroller Reference Manual* for more information. •
$\overline{\text{RESET}}$	SIU - Reset	The $\overline{\text{RESET}}$ pin is an active low input. The $\overline{\text{RESET}}$ pin is asserted by an external device during a power-on or external reset. The internal reset signal asserts only if the $\overline{\text{RESET}}$ pin asserts for 10 clock cycles. Assertion of the $\overline{\text{RESET}}$ pin while the device is in reset causes the reset cycle to start over. The $\overline{\text{RESET}}$ pin has a glitch detector which detects spikes greater than two clock cycles in duration that fall below the switch point of the input buffer logic of the VDDEH input pins. The switch point lies between the maximum VIL and minimum VIH specifications for the VDDEH input pins.
RSTCFG	SIU - Reset	Used to enable or disable the PLLREF and the BOOTCFG[0:1] configuration signals. 0: Get configuration information from BOOTCFG[0:1] and PLLREF 1: Use default configuration of booting from internal flash with crystal clock source **Note:** For the 176-pin QFP and 208-ball BGA packages RSTCFG is always 0, so PLLREF and BOOTCFG signals are used.
$\overline{\text{RSTOUT}}$	SIU - Reset	The $\overline{\text{RSTOUT}}$ pin is an active low output that uses a push/pull configuration. The $\overline{\text{RSTOUT}}$ pin is driven to the low state by the MCU for all internal and external reset sources. There is a delay between initiation of the reset and the assertion of the RSTOUT pin.

[1] Do not connect pin directly to a power supply or ground.

Table 6. Power/ground segmentation

Power Segment	Voltage	I/O Pins Powered by Segment
VDDA	5 V	AN0, AN1, AN2, AN3, AN4, AN5, AN6, AN7, AN8, AN9, AN10, AN11, AN16, AN17, AN18, AN19, AN20, AN21, AN22, AN23, AN24, AN25, AN26, AN27, AN28, AN29, AN30, AN31, AN32, AN33, AN34, AN35, AN36, AN37, AN38, AN39, VRH, VRL, REFBYBC
VRC33[1]	3.3 V	MCKO, MDO0, MDO1, MDO2, MDO3
Other Power Segments		
VDDREG	5 V	—
VRCCTL	—	—
VDDPLL	1.2 V	—
VSTBY	0.95–1.2 V (unregulated mode)	—
	2.0–5.5 V (regulated mode)	—
VSS	—	—

[1] Do not use VRC33 to drive external circuits.

[2] Device failure is defined as: “If after exposure to ESD pulses, the device does not meet the device specification requirements, which includes the complete DC parametric and functional testing at room temperature and hot temperature.”

3.6 Power management control (PMC) and power on reset (POR) electrical specifications

Table 14. PMC Operating Conditions and External Regulators Supply Voltage

ID	Name			Parameter	Min	Typ	Max	Unit
1	Jtemp	SR	—	Junction temperature	–40	27	150	°C
2	Vddreg	SR	—	PMC 5 V supply voltage V_{DDREG}	4.75	5	5.25	V
3	Vdd	SR	—	Core supply voltage 1.2 V V_{DD} when external regulator is used without disabling the internal regulator (PMC unit turned on, LVI monitor active)[1]	1.26[2]	1.3	1.32	V
3a	—	SR	—	Core supply voltage 1.2 V V_{DD} when external regulator is used with a disabled internal regulator (PMC unit turned-off, LVI monitor disabled)	1.14	1.2	1.32	V
4	Ivdd	SR	—	Voltage regulator core supply maximum required DC output current	400	—	—	mA
5	Vdd33	SR	—	Regulated 3.3 V supply voltage when external regulator is used without disabling the internal regulator (PMC unit turned-on, internal 3.3V regulator enabled, LVI monitor active)[3]	3.3	3.45	3.6	V
5a	—	SR	—	Regulated 3.3 V supply voltage when external regulator is used with a disabled internal regulator (PMC unit turned-off, LVI monitor disabled)	3	3.3	3.6	V
6	—	SR	—	Voltage regulator 3.3 V supply maximum required DC output current	80	—	—	mA

[1] An internal regulator controller can be used to regulate core supply.

[2] The minimum supply required for the part to exit reset and enter in normal run mode is 1.28 V.

[3] An internal regulator can be used to regulate 3.3 V supply.

Table 15. PMC Electrical Characteristics (continued)

ID	Name			Parameter	Min	Typ	Max	Unit	Notes
5	Vdd33	CC	C	Nominal 3.3 V supply internal regulator DC output voltage	—	3.39	—	V	
5a	—	CC	P	Nominal 3.3 V supply internal regulator DC output voltage variation at power-on reset	Vdd33 - 8.5%	Vdd33	Vdd3 + 7%	V	See note [5]
5b	—	CC	P	Nominal 3.3 V supply internal regulator DC output voltage variation power-on reset	Vdd33 - 7.5%	Vdd33	Vdd33 + 7%	V	With internal load up to Idd3p3
5c	—	CC	D	Voltage regulator 3.3 V output impedance at maximum DC load	—	—	2	Ω	
5d	Idd3p3	CC	P	Voltage regulator 3.3 V maximum DC output current (internal regulator enabled)[6]	80[7]	—	—	mA	
5e	Vdd33 ILim	CC	C	Voltage regulator 3.3 V DC current limit	—	130	—	mA	
6	Lvi3p3	CC	C	Nominal LVI for rising 3.3 V supply	—	3.090	—	V	The Lvi3p3 specs are also valid for the Vddeh LVI
6a	—	CC	C	Variation of LVI for rising 3.3 V supply at power-on reset	Lvi3p3 - 6%	Lvi3p3	Lvi3p3 + 6%	V	See note [8]
6b	—	CC	C	Variation of LVI for rising 3.3 V supply after power-on reset	Lvi3p3 - 3%	Lvi3p3	Lvi3p3 + 3%	V	See note 8
6c	—	CC	C	Trimming step LVI 3.3 V	—	20	—	mV	
6d	Lvi3p3_h	CC	C	LVI 3.3 V hysteresis	—	60	—	mV	
7	Por3.3V_r	CC	C	Nominal POR for rising 3.3 V supply	—	2.07	—	V	The 3.3V POR specs are also valid for the V_{DDEH} POR
7a	—	CC	C	Variation of POR for rising 3.3 V supply	Por3.3V_r-35%	Por3.3V_r	Por3.3V_r + 35%	V	
7b	Por3.3V_f	CC	C	Nominal POR for falling 3.3 V supply	—	1.95	—	V	
7c	—	CC	C	Variation of POR for falling 3.3 V supply	Por3.3V_f-35%	Por3.3V_f	Por3.3V_f+35%	V	
8	Lvi5p0	CC	C	Nominal LVI for rising 5 V V_{DDREG} supply	—	4.290	—	V	

Table 17. MPC5644A External network specification

External Network Parameter	Min	Typ	Max	Comment
Re	0.252Ω	0.280Ω	0.308Ω	+/-10%
Creg		10μF		It depends on external Vreg.
Cc	5μF	10μF	13.5μF	X7R, -50%/+35%
Rc	1.1Ω		5.6Ω	May or may not be required. It depends on the allowable power dissipation of T1.

3.6.3 Recommended power transistors

The following NPN transistors are recommended for use with the on-chip voltage regulator controller: ON Semiconductor™ BCP68T1 or NJD2873 as well as Philips Semiconductor™ BCP68. The collector of the external transistor is preferably connected to the same voltage supply source as the output stage of the regulator.

Table 18. Recommended operating characteristics

Symbol	Parameter	Value	Unit
h_{FE} (β)	DC current gain (Beta)	60 – 550	—
P_D	Absolute minimum power dissipation	>1.0 (1.5 preferred)	W
I_{CMaxDC}	Minimum peak collector current	1.0	A
VCE_{SAT}	Collector-to-emitter saturation voltage	200 – 600[1]	mV
V_{BE}	Base-to-emitter voltage	0.4 – 1.0	V

[1] Adjust resistor at bipolar transistor collector for 3.3 V/5.0 V to avoid VCE < VCE_{SAT}.

3.7 Power up/down sequencing

There is no power sequencing required among power sources during power up and power down, in order to operate within specification.

Although there are no power up/down sequencing requirements to prevent issues such as latch-up or excessive current spikes the state of the I/O pins during power up/down varies according to Table 19 for all pins with fast pads, and Table 20 for all pins with medium, slow, and multi-voltage pads.

Table 19. Power sequence pin states (fast pads)

V_{DDE}	V_{RC33}	V_{DD}	Pad State
LOW	X	X	LOW
V_{DDE}	LOW	X	HIGH
V_{DDE}	V_{RC33}	LOW	HIGH IMPEDANCE
V_{DDE}	V_{RC33}	V_{DD}	FUNCTIONAL

Table 21. DC electrical specifications (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					min	typ	max	
I_{ACT_S}	CC	C	Slow/medium I/O weak pull up/down current[15]	3.0 V – 3.6 V	15	—	95	µA
		P		4.75 V – 5.5 V	35	—	200	
I_{ACT_F}	CC	D	Fast I/O weak pull up/down current[15]	1.62 V – 1.98 V	36	—	120	µA
		D		2.25 V – 2.75 V	34	—	139	
		D		3.0 V – 3.6 V	42	—	158	
$I_{ACT\_MV\_PU}$	CC	C	Multi-voltage pad weak pullup current	V_{DDE}= 3.0–3.6 V[5], MultiV pad, high swing mode only	10	—	75	µA
		P		4.75 V – 5.25 V	25	—	200	
$I_{ACT\_MV\_PD}$	CC	C	Multivoltage pad weak pulldown current	V_{DDE}= 3.0–3.6 V[5], MultiV pad, high swing mode only	10	—	60	µA
		P		4.75 V – 5.25 V	25	—	200	
I_{INACT_D}	CC	P	I/O input leakage current[16]	—	–2.5	—	2.5	µA
I_{IC}	SR	T	DC injection current (per pin)	—	–1.0	—	1.0	mA
I_{INACT_A}	SR	P	Analog input current, channel off, AN[0:7][17]	—	–250	—	250	nA
		P	Analog input current, channel off, all other analog pins[17]	—	–150	—	150	

Table 26. PLLMRFM electrical specifications

(V_{DDPLL} = 1.08 V to 3.6 V, V_{SS} = V_{SSPLL} = 0 V, T_A = T_L to T_H) (continued)

Symbol		C	Parameter	Conditions	Value		Unit
					min	max	
V_{IHEXT}	CC	T	EXTAL input high voltage	Crystal Mode[12]	Vxtal + 0.4	—	V
		T		External Reference[12, 13]	V_{RC33} /2 + 0.4	V_{RC33}	
V_{ILEXT}	CC	T	EXTAL input low voltage	Crystal Mode[12]	—	Vxtal - 0.4	V
		T		External Reference[12, 13]	0	V_{RC33} /2 - 0.4	
—	CC	T	XTAL load capacitance[10]	4 MHz	5	30	pF
				8 MHz	5	26	
				12 MHz	5	23	
				16 MHz	5	19	
				20 MHz	5	16	
				40 MHz	5	8	
t_{lpll}	CC	P	PLL lock time [10, 14]	—	—	200	µs
t_{dc}	CC	T	Duty cycle of reference	—	40	60	%
f_{LCK}	CC	T	Frequency LOCK range	—	–6	6	% f_{sys}
f_{UL}	CC	T	Frequency un-LOCK range	—	–18	18	% f_{sys}
f_{CS} f_{DS}	CC	D	Modulation Depth	Center spread	±0.25	±4.0	% f_{sys}
		D		Down Spread	–0.5	–8.0	
f_{MOD}	CC	D	Modulation frequency[15]	—	—	100	kHz

1 Considering operation with PLL not bypassed.

2 All internal registers retain data at 0 Hz.

3 “Loss of Reference Frequency” window is the reference frequency range outside of which the PLL is in self clocked mode.

4 Self clocked mode frequency is the frequency that the PLL operates at when the reference frequency falls outside the f_{LOR} window.

5 f_{VCO} self clock range is 20–150 MHz. f_{SCM} represents f_{SYS} after PLL output divider (ERFD) of 2 through 16 in enhanced mode.

6 This value is determined by the crystal manufacturer and board design.

7 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{SYS}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via V_{DDPLL} and V_{SSPLL} and variation in crystal oscillator frequency increase the C_{JITTER} percentage for a given interval.

Table 30. eQADC differential ended conversion specifications (operating) (continued)

Symbol		C	Parameter		Value		Unit
					min	max	
GAINVGA2[1]	CC	–	Variable gain amplifier accuracy (gain=2)[2]				
	CC	D	INL	8 MHz ADC	–5	5	Counts
	CC	D		16 MHz ADC	–8	8	Counts
	CC	D	DNL	8 MHz ADC	–3	3	Counts
	CC	D		16 MHz ADC	–3	3	Counts
GAINVGA4[1]	CC	–	Variable gain amplifier accuracy (gain=4)[2]				
	CC	D	INL	8 MHz ADC	–7	7	Counts
	CC	D		16 MHz ADC	–8	8	Counts
	CC	D	DNL	8 MHz ADC	–4	4	Counts
	CC	D		16 MHz ADC	–4	4	Counts
$DIFF_{max}$	CC	C	Maximum differential voltage (DANx+ - DANx-) or (DANx- - DANx+)[5]	PREGAIN set to 1X setting	—	(VRH - VRL)/2	V
$DIFF_{max2}$	CC	C		PREGAIN set to 2X setting	—	(VRH - VRL)/4	V
$DIFF_{max4}$	CC	C		PREGAIN set to 4X setting	—	(VRH - VRL)/8	V
$DIFF_{cmv}$	CC	C	Differential input Common mode voltage (DANx- + DANx+)/2[5]	—	$(V_{RH} + V_{RL})/2$ - 5%	$(V_{RH} + V_{RL})/2$ + 5%	V

1 Applies only to differential channels.

2 Variable gain is controlled by setting the PRE_GAIN bits in the ADC_ACR1-8 registers to select a gain factor of ×1, ×2, or ×4. Settings are for differential input only. Tested at ×1 gain. Values for other settings are guaranteed by as indicated.

3 At $V_{RH} – V_{RL}$ = 5.12 V, one LSB = 1.25 mV.

4 Guaranteed 10-bit mono tonicity.

5 Voltages between VRL and VRH will not cause damage to the pins. However, they may not be converted accurately if the differential voltage is above the maximum differential voltage. In addition, conversion errors may occur if the common mode voltage of the differential signal violates the Differential Input common mode voltage specification.

3.17.5 External interrupt timing (IRQ pin)

Table 44. External interrupt timing[1]

#	Characteristic	Symbol	Min	Max	Unit
1	IRQ Pulse Width Low	t_{IPWL}	3	—	t_{cyc}
2	IRQ Pulse Width High	t_{IPWH}	3	—	t_{cyc}
3	IRQ Edge to Edge Time[2]	t_{ICYC}	6	—	t_{cyc}

1 IRQ timing specified at V_{DD} = 1.14 V to 1.32 V, V_{DDEH} = 3.0 V to 5.5 V, V_{DD33} and V_{DDSYN} = 3.0 V to 3.6 V, $T_A = T_L$ to T_H.

2 Applies when IRQ pins are configured for rising edge or falling edge events, but not both.

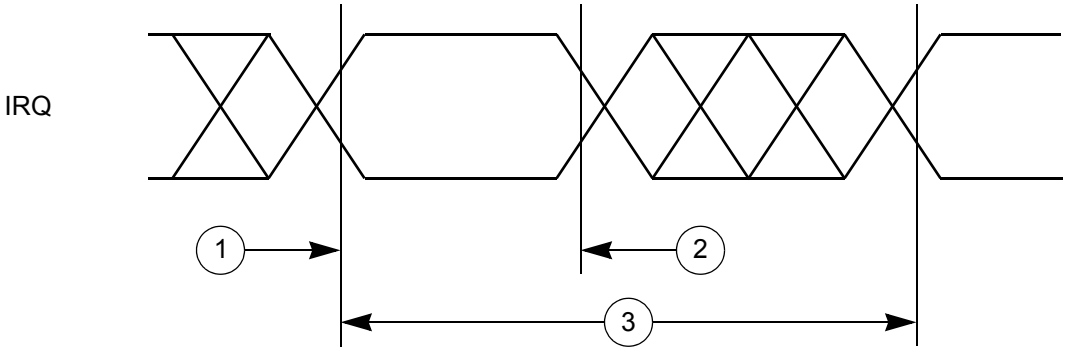


Figure 22. External Interrupt Timing

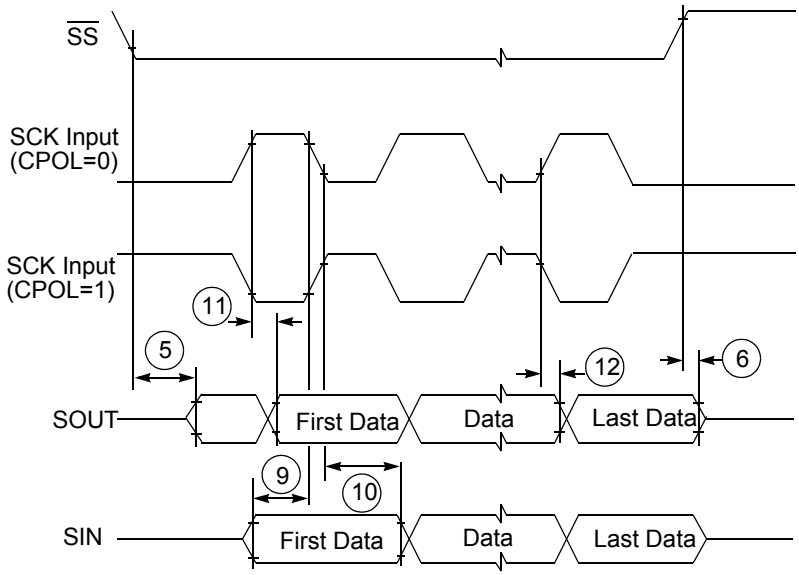
3.17.6 eTPU timing

Table 45. eTPU timing[1]

#	Characteristic	Symbol	Min	Max	Unit
1	eTPU Input Channel Pulse Width	t_{ICPW}	4	—	t_{cyc}
2	eTPU Output Channel Pulse Width	t_{OCPW}	2^2	—	t_{cyc}

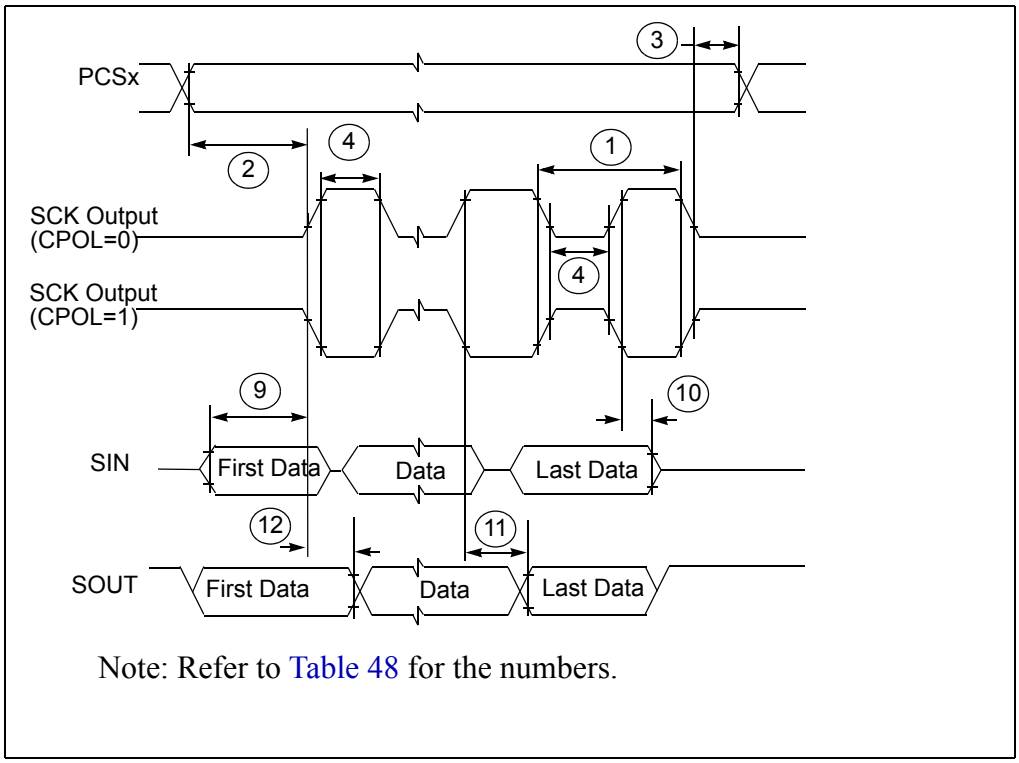
1 eTPU timing specified at V_{DD} = 1.08 V to 1.32 V, V_{DDEH} = 3.0 V to 5.5 V, V_{DD33} and V_{DDSYN} = 3.0 V to 3.6 V, $T_A = T_L$ to T_H, and C_L = 200 pF with SRC = 0b00.

2 This specification does not include the rise and fall times. When calculating the minimum eTPU pulse width, include the rise and fall times defined in the slew rate control fields (SRC) of the pad configuration registers (PCR).



Note: Refer to Table 48 for the numbers.

Figure 26. DSPI classic SPI timing — slave, CPHA = 1



Note: Refer to Table 48 for the numbers.

Figure 27. DSPI modified transfer format timing — master, CPHA = 0

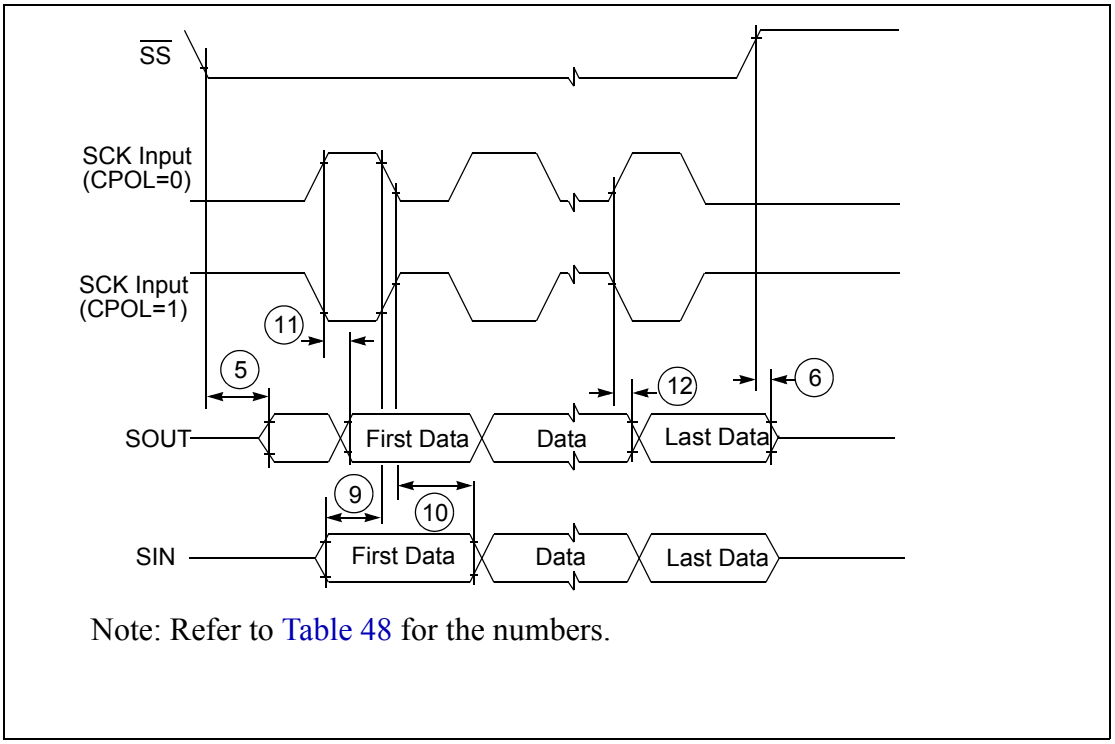


Figure 30. DSPI modified transfer format timing — slave, CPHA =1

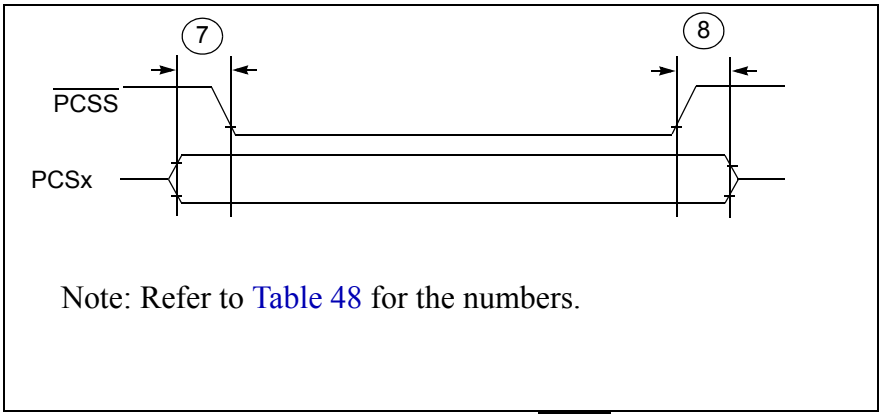


Figure 31. DSPI PCS strobe (PCSS) timing

3.17.9 eQADC SSI timing

Table 49. eQADC SSI timing characteristics (pads at 3.3 V or at 5.0 V)[1]

CLOAD = 25 pF on all outputs. Pad drive strength set to maximum.								
#	**Symbol**		**C**	**Rating**	**Min**	**Typ**	**Max**	**Unit**
1	f_{FCK}	CC	D	FCK Frequency [2, 3]	1/17		1/2	f_{SYS_CLK}
1	t_{FCK}	CC	D	FCK Period (t_{FCK} = 1/ f_{FCK})	2		17	t_{SYS_CLK}
2	t_{FCKHT}	CC	D	Clock (FCK) High Time	t_{SYS_CLK} − 6.5		$_{9*}$ t_{SYS_CLK} + 6.5	ns
3	t_{FCKLT}	CC	D	Clock (FCK) Low Time	t_{SYS_CLK} − 6.5		$_{8*}$ t_{SYS_CLK} + 6.5	ns
4	t_{SDS_LL}	CC	D	SDS Lead/Lag Time	-7.5		7.5	ns
5	t_{SDO_LL}	CC	D	SDO Lead/Lag Time	-7.5		7.5	ns
6	t_{DVFE}	CC	D	Data Valid from FCK Falling Edge (t_{FCKLT}+t_{SDO_LL})	1			ns
7	t_{EQ_SU}	CC	D	eQADC Data Setup Time (Inputs)	22			ns
8	t_{EQ_HO}	CC	D	eQADC Data Hold Time (Inputs)	1			ns

1 SS timing specified at f_{SYS} = 80 MHz, V_{DD} = 1.14 V to 1.32 V, V_{DDEH} = 4.5 V to 5.5 V, T_A = T_L to T_H, and C_L = 50 pF with SRC = 0b00.

2 Maximum operating frequency is highly dependent on track delays, master pad delays, and slave pad delays.

3 FCK duty is not 50% when it is generated through the division of the system clock by an odd number.

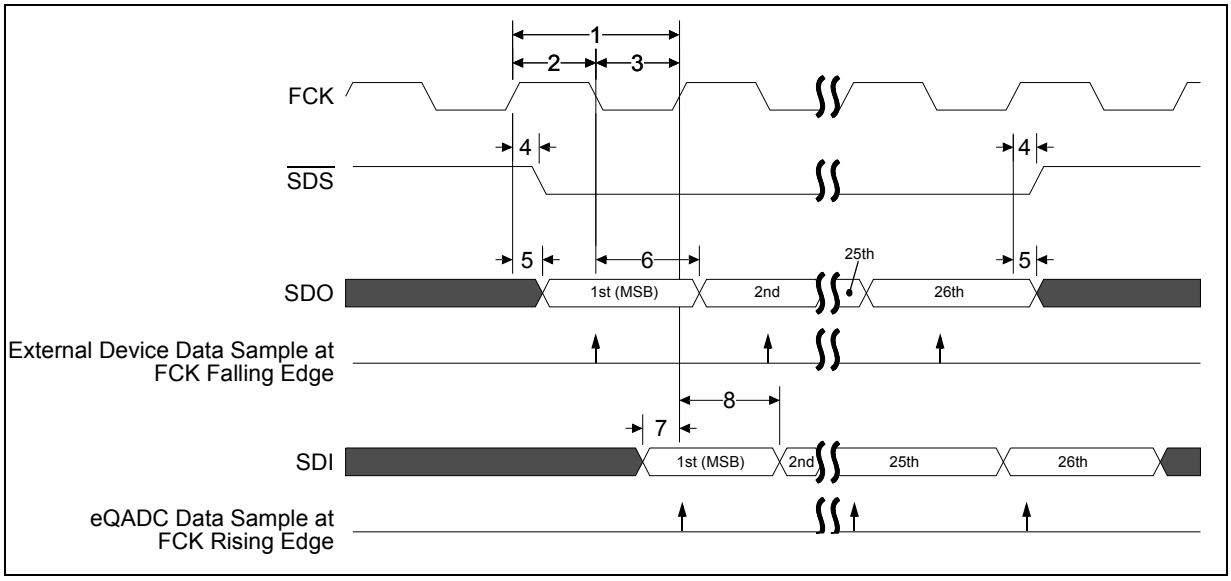
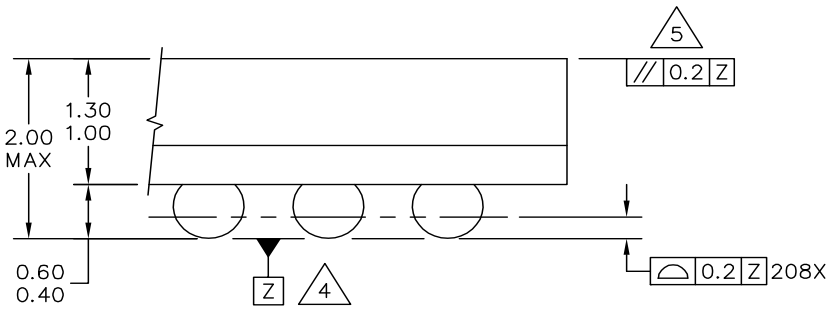


Figure 32. eQADC SSI timing



DETAIL K
(ROTATED 90° CLOCKWISE)

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE Z.
4. DATUM Z (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

TITLE: 208 I/O MAP BGA, 17 X 17 PKG, 1–MM PITCH	CASE NUMBER: 1159A–01	
	STANDARD: JEDEC MO–151 AAF–1	
	PACKAGE CODE: 5253	SHEET: 2

Figure 37. 208 MAPBGA package mechanical drawing (part 2)

Table 53. Revision history (continued)

Revision	Date	Substantive changes
Rev. 3	04/2010	Changes to Signal Properties table (changes apply to Revision 2 and later devices: EBI changes: • WE_BE[2] (A2) and CAL_WE_BE[2] (A3) signals added to CS[2] (PCR 2) • WE_BE[3] (A2) and CAL_WE_BE[3] (A3) signals added to CS[3] (PCR 3) Calibration bus changes: • CAL_WE[2]/BE[2] (A2) signal added to CAL_CS[2] (PCR 338) • CAL_WE[3]/BE[3] (A2) signal added to CAL_CS[3] (PCR 339) • CAL_ALE (A1) added to CAL_ADDR[15] (PCR 340) eQADC changes: • AN[8] and AN[38] pins swapped. AN[8] Is now on pins 9 (176-pin), B3 (208-ball) and E1 (324-ball). AN[8] was on D3 (324-ball) on previous devices. AN[38] Is now on D3 (324-ball). AN[38] was on pins 9 (176-pin), B3 (208-ball) and E1 (324-ball) on previous devices. • ANZ function added to AN11 pin Reaction channels added to eTPU2: • RCH0_A (A3) added to ETPU_A[14] (PCR 128) • RCH0_B (A2) added to ETPU_A[20] (PCR 134) • RCH0_C (A2) added to ETPU_A[21] (PCR 135) • RCH1_A (A2) added to ETPU_A[15] (PCR 129) • RCH1_B (A2) added to ETPU_A[9] (PCR 123) • RCH1_C (A2) added to ETPU_A[10] (PCR 124) • RCH2_A (A2) added to ETPU_A[16] (PCR 130) • RCH3_A (A2) added to ETPU_A[17] (PCR 131 • RCH4_A (A2) added to ETPU_A[18] (PCR 132)) • RCH4_B (A2) added to ETPU_A[11] (PCR 125) • RCH4_C (A2) added to ETPU_A[12] (PCR 126) • RCH5_A (A2) added to ETPU_A[19] (PCR 133) • RCH5_B (A2) added to ETPU_A[28] (PCR 142) • RCH5_C (A2) added to ETPU_A[29] (PCR 143) Reaction channels added to eMIOS: • RCH2_B (A2) added to EMIOS[2] (PCR 181) • RCH2_C (A2) added to EMIOS[4] (PCR 183) • RCH3_B (A2) added to EMIOS[10] (PCR 189) • RCH3_C (A2) added to EMIOS[11] (PCR 190) Pad changes: • ETPUA16 (PCR 130) has Medium (was Slow) pad • ETPUA17 (PCR 131) has Medium (was Slow) pad • ETPUA18 (PCR 132) has Medium (was Slow) pad • ETPUA19 (PCR 133) has Medium (was Slow) pad • ETPUA25 (PCR 139) has Slow+LVDS (was Medium+LVDS) pads Signal Details table updated: • Added eTPU2 reaction channels • Changed IRQ[0:15] to two ranges, excluding IRQ6, which does not exist on this device • Changed TCR_A to TCRCLKA (TCR_A is the pin name, not the signal name) • Changed WE_BE[0:1] to WE_BE[0:3] (2 new signals added to Rev. 2). Also changed notation from “WE_BE[n]” to “WE[n]/BE[n]” to be consistent.