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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, EBI/EMI, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	84
Program Memory Size	4MB (4M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	1.14V ~ 5.25V
Data Converters	A/D 40x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5644af0mlu3

1.4 Feature details

1.4.1 e200z4 core

MPC5644A devices have a high performance e200z448n3 core processor:

- Dual issue, 32-bit Power Architecture embedded category CPU
- Variable Length Encoding Enhancements
- 8 KB instruction cache: 2- or 4- way set associative instruction cache
- Thirty-two 64-bit general purpose registers (GPRs)
- Memory management unit (MMU) with 24-entry fully-associative translation look-aside buffer (TLB)
- Harvard Architecture: Separate instruction bus and load/store bus
- Vectored interrupt support
- Non-maskable interrupt input
- Critical Interrupt input
- New ‘Wait for Interrupt’ instruction, to be used with new low power modes
- Reservation instructions for implementing read-modify-write accesses
- Signal processing extension (SPE) APU
- Single Precision Floating point (scalar and vector)
- Nexus Class 3+ debug
- Process ID manipulation for the MMU using an external tool

1.4.2 Crossbar Switch (XBAR)

The XBAR multiport crossbar switch supports simultaneous connections between five master ports and four slave ports. The crossbar supports a 32-bit address bus width and a 64-bit data bus width.

The crossbar allows three concurrent transactions to occur from the master ports to any slave port but each master must access a different slave. If a slave port is simultaneously requested by more than one master port, arbitration logic selects the higher priority master and grants it ownership of the slave port. All other masters requesting that slave port are stalled until the higher priority master completes its transactions. Requesting masters are treated with equal priority and are granted access to a slave port in round-robin fashion, based upon the ID of the last master to be granted access. The crossbar provides the following features:

- 5 master ports
  - CPU instruction bus
  - CPU data bus
  - eDMA
  - FlexRay
  - External Bus Interface
- 4 slave ports
  - Flash
  - Calibration and EBI bus
  - SRAM
  - Peripheral bridge
- 32-bit internal address, 64-bit internal data paths

- Lock detect circuitry reports when the PLL has achieved frequency lock and continuously monitors lock status to report loss of lock conditions
- Clock Quality Module
  - Detects the quality of the crystal clock and causes interrupt request or system reset if error is detected
  - Detects the quality of the PLL output clock; if error detected, causes system reset or switches system clock to crystal clock and causes interrupt request
- Programmable interrupt request or system reset on loss of lock
- Self-clocked mode (SCM) operation

1.4.7 SIU

The MPC5644A SIU controls MCU reset configuration, pad configuration, external interrupt, general purpose I/O (GPIO), internal peripheral multiplexing, and the system reset operation. The reset configuration block contains the external pin boot configuration logic. The pad configuration block controls the static electrical characteristics of I/O pins. The GPIO block provides uniform and discrete input/output control of the I/O pins of the MCU. The reset controller performs reset monitoring of internal and external reset sources, and drives the $\overline{\text{RSTOUT}}$ pin. Communication between the SIU and the e200z4 CPU core is via the crossbar switch. The SIU provides the following features:

- System configuration
  - MCU reset configuration via external pins
  - Pad configuration control for each pad
  - Pad configuration control for virtual I/O via DSPI serialization
- System reset monitoring and generation
  - Power-on reset support
  - Reset status register provides last reset source to software
  - Glitch detection on reset input
  - Software controlled reset assertion
- External interrupt
  - Rising or falling edge event detection
  - Programmable digital filter for glitch rejection
  - Critical Interrupt request
  - Non-Maskable Interrupt request
- GPIO
  - Centralized control of I/O and bus pins
  - Virtual GPIO via DSPI serialization (requires external deserialization device)
  - Dedicated input and output registers for setting each GPIO and Virtual GPIO pin
- Internal multiplexing
  - Allows serial and parallel chaining of DSPIs
  - Allows flexible selection of eQADC trigger inputs
  - Allows selection of interrupt requests between external pins and DSPI

1.4.8 Flash memory

The MPC5644A provides up to 4 MB of programmable, non-volatile, flash memory. The non-volatile memory (NVM) can be used to store instructions or data, or both. The flash module includes a Fetch Accelerator that optimizes the performance of the flash array to match the CPU architecture. The flash module interfaces the system bus to a dedicated flash memory array controller. For CPU ‘loads’, DMA transfers and CPU instruction fetch, it supports a 64-bit data bus width at the system bus port,

2.4 Signal summary

Table 3. MPC5644A signal properties

Name	Function[1]	PAG[2]	PCR PA Field[3]	PCR[4]	I/O Type	Voltage[5] / Pad Type[6]	Status[7]		Package pin #		
							During Reset	After Reset	176	208	324
GPIO											
EMIOS14[8] GPIO[203]	eMIOS channel GPIO	P G	01 00	203	O I/O	VDDEH7 Slow	— / Up	— / Up	—	—	A15
EMIOS15[8] GPIO[204]	eMIOS channel GPIO	P G	01 00	204	O I/O	VDDEH7 Slow	— / Up	—/ Up	—	—	D14
GPIO[206] ETRIG0	GPIO / eQADC Trigger Input	G	00	206	I/O[9]	VDDEH7 Slow[10]	— / Up	— / Up	143	R4	C14
GPIO[207] ETRIG1	GPIO / eQADC Trigger Input	G	00	207	I/O[9]	VDDEH7 Slow	— / Up	— / Up	144	P5	B14
GPIO[219]	GPIO	G	—	219[11]	I/O	VDDEH7 MultiV[12]	— / Up	— / Up	122	T6	—
Reset / Configuration											
$\overline{\text{RESET}}$	External Reset Input	P	—	—	I	VDDEH6 Slow	$\overline{\text{RESET}}$ / Up	$\overline{\text{RESET}}$ / Up	97	L16	R22
$\overline{\text{RSTOUT}}$	External Reset Output	P	01	230	O	VDDEH6 Slow	$\overline{\text{RSTOUT}}$ / Down	$\overline{\text{RSTOUT}}$ / Down	102	K15	P21
PLLREF $\overline{\text{IRQ}}$[4] ETRIG2 GPIO[208]	FMPLL Mode Selection External Interrupt Request eQADC Trigger Input GPIO	P A1 A2 G	001 010 100 000	208	I I I I/O	VDDEH6 Slow	— / Up	PLLREF / Up	83	M14	V21
PLLCFG1[13] $\overline{\text{IRQ}}$[5] DSPI_D_SOUT GPIO[209]	— External interrupt request DSPI D data output GPIO	— A1 A2 G	— 010 100 000	209	— I O I/O	VDDEH6 Medium	— / Up	— / Up	—	—	U20
RSTCFG GPIO[210]	RSTCFG GPIO	P G	01 00	210	I I/O	VDDEH6 Slow	— / Down	—	—	—	P22
BOOTCFG[0] $\overline{\text{IRQ}}$[2] GPIO[211]	Boot Config. Input External Interrupt Request GPIO	P A1 G	01 10 00	211	I I I/O	VDDEH6 Slow	— / Down	BOOTCFG[0] / Down	—	—	T20

Table 3. MPC5644A signal properties (continued)

Name	Function[1]	PAG[2]	PCR PA Field[3]	PCR[4]	I/O Type	Voltage[5] / Pad Type[6]	Status[7]		Package pin #		
							During Reset	After Reset	176	208	324
ADDR16 FR_A_TX DATA16 GPIO[12]	External address bus Flexray TX data channel A External data bus GPIO	P A1 A2 G	001 010 100 000	12	I/O O I/O I/O	VDDE-EH Medium	— / Up	— / Up	—	—	P3
ADDR17 FR_A_TX_EN DATA17 GPIO[13]	External address bus FlexRay ch. A TX data enable External data bus GPIO	P A1 A2 G	001 010 100 000	13	I/O O I/O I/O	VDDE-EH Medium	— / Up	— / Up	—	—	P4
ADDR18 FR_A_RX DATA18 GPIO[14]	External address bus Flexray RX data ch. A External data bus GPIO	P A1 A2 G	001 010 100 000	14	I/O I I/O I/O	VDDE-EH Medium	— / Up	— / Up	—	—	R1
ADDR19 FR_B_TX DATA19 GPIO[15]	External address bus Flexray TX data ch. B External data bus GPIO	P A1 A2 G	001 010 100 000	15	I/O O I/O I/O	VDDE-EH Medium	— / Up	— / Up	—	—	R2
ADDR20 FR_B_TX_EN DATA20 GPIO[16]	External address bus Flexray TX data enable for ch. B External data bus GPIO	P A1 A2 G	001 010 100 000	16	I/O O I/O I/O	VDDE-EH Medium	— / Up	— / Up	—	—	R4
ADDR21 FR_B_RX DATA21 GPIO[17]	External address bus Flexray RX data channel B External data bus GPIO	P A1 A2 G	001 010 100 000	17	I/O I I/O I/O	VDDE-EH Medium	— / Up	— / Up	—	—	T1
ADDR22 DATA22 GPIO[18]	External address bus External data bus GPIO	P A2 G	001 100 000	18	I/O I/O I/O	VDDE-EH Medium	— / Up	— / Up	—	—	T2
ADDR23 DATA23 GPIO[19]	External address bus External data bus GPIO	P A2 G	001 100 000	19	I/O I/O I/O	VDDE-EH Medium	— / Up	— / Up	—	—	T3
ADDR24 DATA24 GPIO[20]	External address bus External data bus GPIO	P A2 G	001 100 000	20	I/O I/O I/O	VDDE-EH Medium	— / Up	— / Up	—	—	T4
ADDR25 DATA25 GPIO[21]	External address bus External data bus GPIO	P A2 G	001 100 000	21	I/O I/O I/O	VDDE-EH Medium	— / Up	— / Up	—	—	U1

Table 3. MPC5644A signal properties (continued)

Name	Function[1]	PAG[2]	PCR PA Field[3]	PCR[4]	I/O Type	Voltage[5] / Pad Type[6]	Status[7]		Package pin #		
							During Reset	After Reset	176	208	324
CAL_$\overline{WE}$[1]/$\overline{BE}$[1]	Calibration write/byte enable	P	01	342	O	VDDE12 Fast		— / —	—	—	—
CAL_OE	Calibration output enable	P	01	342	O	VDDE12 Fast		— / —	—	—	—
CAL_TS CAL_ALE	Calibration transfer start Address Latch Enable	P A	01 10	343	O O	VDDE12 Fast		— / —	—	—	—
CAL_MDO[4]	Calibration Nexus Message Data Out	P	01	—	O	VDDE12 Fast	—	CAL_MDO[4] / —	—	—	—
CAL_MDO[5]	Calibration Nexus Message Data Out	P	01	—	O	VDDE12 Fast	—	CAL_MDO[5] / —	—	—	—
CAL_MDO[6]	Calibration Nexus Message Data Out	P	01	—	O	VDDE12 Fast	—	CAL_MDO[6] / —	—	—	—
CAL_MDO[7]	Calibration Nexus Message Data Out	P	01	—	O	VDDE12 Fast	—	CAL_MDO[7] / —	—	—	—
CAL_MDO[8]	Calibration Nexus Message Data Out	P	01	—	O	VDDE12 Fast	—	CAL_MDO[8] / —	—	—	—
CAL_MDO[9]	Calibration Nexus Message Data Out	P	01	—	O	VDDE12 Fast	—	CAL_MDO[9] / —	—	—	—
CAL_MDO[10]	Calibration Nexus Message Data Out	P	01	—	O	VDDE12 Fast	—	CAL_MDO[10] / —	—	—	—
CAL_MDO[11]	Calibration Nexus Message Data Out	P	01	—	O	VDDE12 Fast	—	CAL_MDO[11] / —	—	—	—
NEXUS											
$\overline{EVTI}$	Nexus event in	P	01	231	I	VDDEH7 MultiV[12,14]	— / Up	$\overline{EVTI}$ / Up	116	E15	H20
$\overline{EVTO}$	Nexus event out	P	01	227	O	VDDEH7 MultiV[12,14,15]	—	$\overline{EVTO}$ / —	120	D15	G20
MCKO	Nexus message clock out	P	—	219[11]	O	VRC33 Fast	—	MCKO / —	14	F15	F1
MDO0[16]	Nexus message data out	P	01	220	O	VRC33 Fast	—	MDO[0] / —	17	A14	F3
MDO1[16]	Nexus message data out	P	01	221	O	VRC33 Fast	—	MDO[1] / —	18	B14	G2

Table 3. MPC5644A signal properties (continued)

Name	Function[1]	PAG[2]	PCR PA Field[3]	PCR[4]	I/O Type	Voltage[5] / Pad Type[6]	Status[7]		Package pin #		
							During Reset	After Reset	176	208	324
TCK	JTAG test clock input	P	01	—	I	VDDEH7 MultiV[12]	TCK / Down	TCK / Down	128	C16	D21
TDI	JTAG test data input	P	01	232	I	VDDEH7 MultiV[12]	TDI / Up	TDI / Up	130	E14	D22
TDO	JTAG test data output	P	01	228	O	VDDEH7 MultiV[12]	TDO / Up	TDO / Up	123	F14	E21
TMS	JTAG test mode select input	P	01	—	I	VDDEH7 MultiV[12]	TMS / Up	TMS / Up	131	D14	E20
JCOMP	JTAG TAP controller enable	P	01	—	I	VDDEH7 MultiV[12]	JCOMP / Down	JCOMP / Down	121	F16	F20
FlexCAN											
CAN_A_TX SCI_A_TX GPIO[83]	FlexCAN A TX eSCI A TX GPIO	P A1 G	01 10 00	83	O O I/O	VDDEH6 Slow	— / Up	— / Up	81	P12	AB19
CAN_A_RX SCI_A_RX GPIO[84]	FlexCAN A RX eSCI A RX GPIO	P A1 G	01 10 00	84	I I I/O	VDDEH6 Slow	— / Up	— / Up	82	R12	Y19
CAN_B_TX DSPI_C_PCS[3] SCI_C_TX GPIO[85]	FlexCAN B TX DSPI C peripheral chip select eSCI C TX GPIO	P A1 A2 G	001 010 100 000	85	O O O I/O	VDDEH6 Slow	— / Up	— / Up	88	T12	Y22
CAN_B_RX DSPI_C_PCS[4] SCI_C_RX GPIO[86]	FlexCAN B RX DSPI C peripheral chip select eSCI C RX GPIO	P A1 A2 G	001 010 100 000	86	I O I I/O	VDDEH6 Slow	— / Up	— / Up	89	R13	W21
CAN_C_TX DSPI_D_PCS[3] GPIO[87]	FlexCAN C TX DSPI D peripheral chip select GPIO	P A1 G	01 10 00	87	O O I/O	VDDEH6 Medium	— / Up	— / Up	101	K13	P19
CAN_C_RX DSPI_D_PCS[4] GPIO[88]	FlexCAN C RX DSPI D peripheral chip select GPIO	P A1 G	01 10 00	88	I O I/O	VDDEH6 Slow	— / Up	— / Up	98	L14	V20
eSCI											

Table 3. MPC5644A signal properties (continued)

Name	Function[1]	PAG[2]	PCR PA Field[3]	PCR[4]	I/O Type	Voltage[5] / Pad Type[6]	Status[7]		Package pin #		
							During Reset	After Reset	176	208	324
EMIOS11 DSPI_D_PCS[4] RCH3_C GPIO[190]	eMIOS channel DSPI D peripheral chip select Reaction channel 3C GPIO	P A1 A2 G	001 010 100 000	190	I/O O O I/O	VDDEH4 Medium	— / WKPCFG	— / WKPCFG	75	R8	AB15
EMIOS12 DSPI_C_SOUT ETPUA27_O[8] GPIO[191]	eMIOS channel DSPI C data output eTPU A channel (output only) GPIO	P A1 A2 G	001 010 100 000	191	I/O O O I/O	VDDEH4 Medium	— / WKPCFG	— / WKPCFG	76	N10	AB16
EMIOS13 DSPI_D_SOUT GPIO[192]	eMIOS channel DSPI D data output GPIO	P A1 G	01 10 00	192	I/O O I/O	VDDEH4 Medium	— / WKPCFG	— / WKPCFG	77	T8	AA16
EMIOS14 IRQ[0] ETPUA29_O[8] GPIO[193]	eMIOS channel External interrupt request eTPU A channel (output only) GPIO	P A1 A2 G	001 010 100 000	193	I/O I O I/O	VDDEH4 Slow	— / Down	— / Down	78	R9	Y16
EMIOS15 IRQ[1] GPIO[194]	eMIOS channel External interrupt request GPIO	P A1 G	01 10 00	194	I/O I I/O	VDDEH4 Slow	— / Down	— / Down	79	T9	W16
EMIOS16 GPIO[195]	eMIOS channel GPIO	P G	01 00	195	I/O I/O	VDDEH4 Slow	— / Up	— / Up	—	—	W17
EMIOS17 GPIO[196]	eMIOS channel GPIO	P G	01 00	196	I/O I/O	VDDEH4 Slow	— / Up	— / Up	—	—	Y17
EMIOS18 GPIO[197]	eMIOS channel GPIO	P G	01 00	197	I/O I/O	VDDEH4 Slow	— / Up	— / Up	—	—	AA17
EMIOS19 GPIO[198]	eMIOS channel GPIO	P G	01 00	198	I/O I/O	VDDEH4 Slow	— / WKPCFG	— / WKPCFG	—	—	AB17
EMIOS20 GPIO[199]	eMIOS channel GPIO	P G	01 00	199	I/O I/O	VDDEH4 Slow	— / WKPCFG	— / WKPCFG	—	—	AB18
EMIOS21 GPIO[200]	eMIOS channel GPIO	P G	01 00	200	I/O I/O	VDDEH4 Slow	— / WKPCFG	— / WKPCFG	—	—	AA18
EMIOS22 GPIO[201]	eMIOS channel GPIO	P G	01 00	201	I/O I/O	VDDEH4 Slow	— / Down	— / Down	—	—	Y18
EMIOS23 GPIO[202]	eMIOS channel GPIO	P G	01 00	202	I/O I/O	VDDEH4 Slow	— / Down	— / Down	80	R11	W18
Clock Synthesizer											

Table 6. Power/ground segmentation

Power Segment	Voltage	I/O Pins Powered by Segment
VDDA	5 V	AN0, AN1, AN2, AN3, AN4, AN5, AN6, AN7, AN8, AN9, AN10, AN11, AN16, AN17, AN18, AN19, AN20, AN21, AN22, AN23, AN24, AN25, AN26, AN27, AN28, AN29, AN30, AN31, AN32, AN33, AN34, AN35, AN36, AN37, AN38, AN39, VRH, VRL, REFBYBC
VRC33[1]	3.3 V	MCKO, MDO0, MDO1, MDO2, MDO3
Other Power Segments		
VDDREG	5 V	—
VRCCTL	—	—
VDDPLL	1.2 V	—
VSTBY	0.95–1.2 V (unregulated mode)	—
	2.0–5.5 V (regulated mode)	—
VSS	—	—

[1] Do not use VRC33 to drive external circuits.

- B. Joiner and V. Adams, “Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling,” Proceedings of SemiTherm, San Diego, 1999, pp. 212-220.

3.4 EMI (electromagnetic interference) characteristics

Table 12. EMI Testing Specifications[1]

Symbol	Parameter	Conditions	Clocks	Frequency Range	Level (Max)	Unit
Radiated emissions, electric field	V_{RE_TEM}	V_{DDREG} = 5.25 V; T_A = 25 °C 150 kHz – 30 MHz RBW 9 kHz, Step Size 5 kHz 30 MHz – 1 GHz - RBW 120 kHz, Step Size 80 kHz	16 MHz crystal 40 MHz bus No PLL frequency modulation	150 kHz – 50 MHz	20	dBμV
				50 – 150 MHz	20	
				150 – 500 MHz	26	
				500 – 1000 MHz	26	
				IEC Level	K	—
				SAE Level	3	—
			16 MHz crystal 40 MHz bus ±2% PLL frequency modulation	150 kHz– 50 MHz	13	dBμV
				50 – 150 MHz	13	
				150 – 500 MHz	11	
				500 – 1000 MHz	13	
				IEC Level	L	—
				SAE Level	2	—

1 EMI testing and I/O port waveforms per SAE J1752/3 issued 1995-03 and IEC 61967-2.

3.5 Electrostatic discharge (ESD) characteristics

Table 13. ESD ratings[1,2]

Symbol		Parameter	Conditions	Value	Unit
—	SR	ESD for Human Body Model (HBM)	—	2000	V
R1	SR	HBM circuit description	—	1500	Ω
C	SR		—	100	pF
—	SR	ESD for field induced charge Model (FDCM)	All pins	500	V
			Corner pins	750	
—	SR	Number of pulses per pin	Positive pulses (HBM)	1	—
			Negative pulses (HBM)	1	—
—	SR	Number of pulses	—	1	—

1 All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

Table 15. PMC Electrical Characteristics (continued)

ID	Name			Parameter	Min	Typ	Max	Unit	Notes
5	Vdd33	CC	C	Nominal 3.3 V supply internal regulator DC output voltage	—	3.39	—	V	
5a	—	CC	P	Nominal 3.3 V supply internal regulator DC output voltage variation at power-on reset	Vdd33 - 8.5%	Vdd33	Vdd3 + 7%	V	See note [5]
5b	—	CC	P	Nominal 3.3 V supply internal regulator DC output voltage variation power-on reset	Vdd33 - 7.5%	Vdd33	Vdd33 + 7%	V	With internal load up to Idd3p3
5c	—	CC	D	Voltage regulator 3.3 V output impedance at maximum DC load	—	—	2	Ω	
5d	Idd3p3	CC	P	Voltage regulator 3.3 V maximum DC output current (internal regulator enabled)[6]	80[7]	—	—	mA	
5e	Vdd33 ILim	CC	C	Voltage regulator 3.3 V DC current limit	—	130	—	mA	
6	Lvi3p3	CC	C	Nominal LVI for rising 3.3 V supply	—	3.090	—	V	The Lvi3p3 specs are also valid for the Vddeh LVI
6a	—	CC	C	Variation of LVI for rising 3.3 V supply at power-on reset	Lvi3p3 - 6%	Lvi3p3	Lvi3p3 + 6%	V	See note [8]
6b	—	CC	C	Variation of LVI for rising 3.3 V supply after power-on reset	Lvi3p3 - 3%	Lvi3p3	Lvi3p3 + 3%	V	See note 8
6c	—	CC	C	Trimming step LVI 3.3 V	—	20	—	mV	
6d	Lvi3p3_h	CC	C	LVI 3.3 V hysteresis	—	60	—	mV	
7	Por3.3V_r	CC	C	Nominal POR for rising 3.3 V supply	—	2.07	—	V	The 3.3V POR specs are also valid for the V_{DDEH} POR
7a	—	CC	C	Variation of POR for rising 3.3 V supply	Por3.3V_r-35%	Por3.3V_r	Por3.3V_r + 35%	V	
7b	Por3.3V_f	CC	C	Nominal POR for falling 3.3 V supply	—	1.95	—	V	
7c	—	CC	C	Variation of POR for falling 3.3 V supply	Por3.3V_f-35%	Por3.3V_f	Por3.3V_f+35%	V	
8	Lvi5p0	CC	C	Nominal LVI for rising 5 V V_{DDREG} supply	—	4.290	—	V	

3.9.1 I/O pad V_{RC33} current specifications

The power consumption of the V_{RC33} supply is dependent on the usage of the pins on all I/O segments. The power consumption is the sum of all input and output pin V_{RC33} currents for all I/O segments. The output pin V_{RC33} current can be calculated from Table 23 based on the voltage, frequency, and load on all fast pad pins. The input pin V_{RC33} current can be calculated from Table 23 based on the voltage, frequency, and load on all medium-speed pads. Use linear scaling to calculate pin currents for voltage, frequency, and load parameters that fall outside the values given in Table 23.

Table 23. I/O pad V_{RC33} average I_{DDE} specifications[1]

Pad Type	Symbol		C	Period (ns)	Load[2] (pF)	Drive Select	I_{DD33} Avg (µA)	I_{DD33} RMS (µA)
Slow	$I_{DRV\_SSR\_HV}$	CC	D	100	50	11	0.8	235.7
		CC	D	200	50	01	0.04	87.4
		CC	D	800	50	00	0.06	47.4
		CC	D	800	200	00	0.009	47
Medium	$I_{DRV\_MSR\_HV}$	CC	D	40	50	11	2.75	258
		CC	D	100	50	01	0.11	76.5
		CC	D	500	50	00	0.02	56.2
		CC	D	500	200	00	0.01	56.2
MultiV[3] (High Swing Mode)	$I_{DRV\_MULTV\_HV}$	CC	D	20	50	11	33.4	35.4
		CC	D	30	50	01	33.4	34.8
		CC	D	117	50	00	33.4	33.8
		CC	D	212	200	00	33.4	33.7
MultiV[4] (Low Swing Mode)	$I_{DRV\_MULTV\_HV}$	CC	D	30	30	11	33.4	34.9

1 These are typical values that are estimated from simulation and not tested. Currents apply to output pins only.

2 All loads are lumped.

3 Average current is for pad configured as output only.

4 In low swing mode, multi-voltage pads must operate in highest slew rate setting.

Table 43. External bus interface (EBI) and calibration bus operation timing [1] (continued)

#	Symbol		C	Characteristic	66 MHz (ext. bus)[2]		Unit	Notes
					Min	Max		
6	t_{COV}	CC	D	CLKOUT Posedge to Output Signal Valid (Output Delay) ADDR[8:31] CS[0:3] DATA[0:31] OE RD_WR TS WE[0:3]/BE[0:3]	—	9	ns	
7	t_{CIS}	CC	D	Input Signal Valid to CLKOUT Posedge (Setup Time) DATA[0:31]	6.0	—	ns	
8	t_{CIH}	CC	D	CLKOUT Posedge to Input Signal Invalid (Hold Time) DATA[0:31]	1.0	—	ns	
9	t_{APW}	CC	D	ALE Pulse Width[4]	6.5	—	ns	
10	t_{AAI}	CC	D	ALE Negated to Address Invalid[4]	1.5[5]	—	ns	

1 External Bus and Calibration bus timing specified at f_{SYS} = 150 MHz and 100 MHz, V_{DD} = 1.14 V to 1.32 V, V_{DDE} = 3 V to 3.6 V (unless stated otherwise), $T_A = T_L$ to T_H, and C_L = 30 pF with DSC = 0b10.

2 The external bus is limited to half the speed of the internal bus. The maximum external bus frequency is 66 MHz for 16-bit muxed mode and 33 MHz for non-muxed mode. For The EBI division factor should be set accordingly based on the internal frequency being used.

3 Refer to Fast Pad timing in Table 35 and Table 36 (different values for 1.8 V vs. 3.3 V).

4 Measured at 50% of ALE.

5 When CAL_TS pad is used for CAL_ALE function the hold time is 1 ns instead of 1.5 ns.

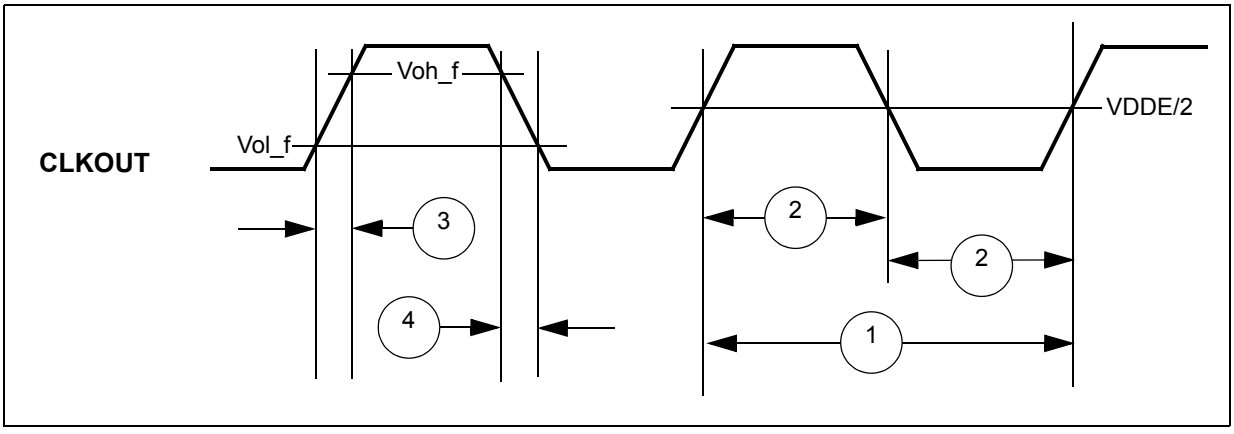


Figure 18. CLKOUT timing

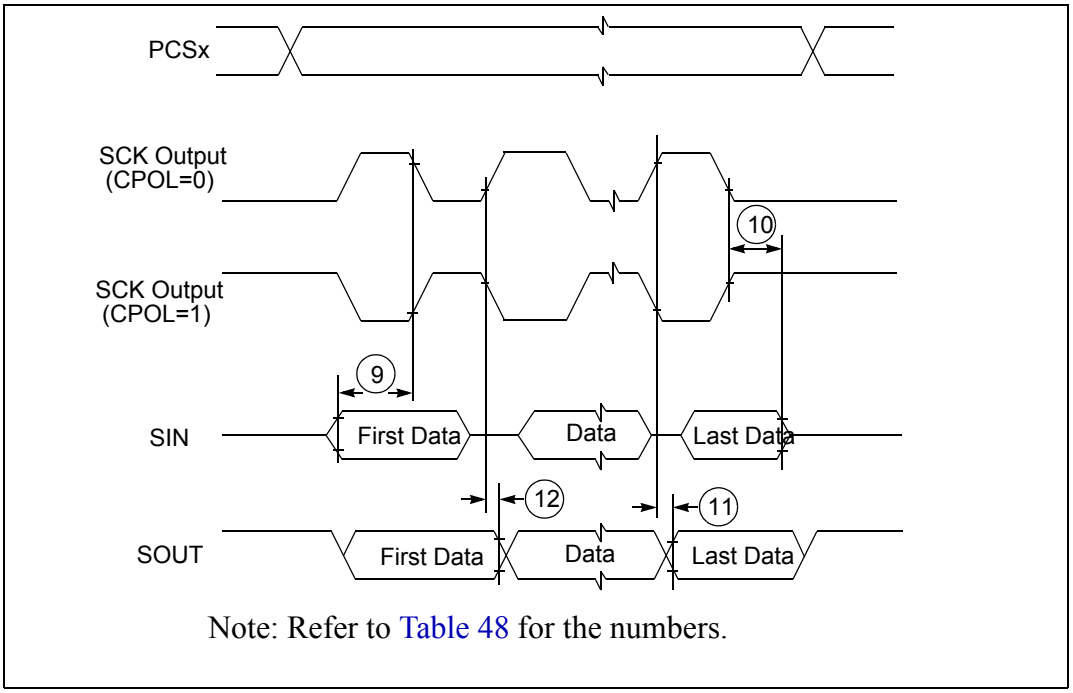


Figure 24. DSPI classic SPI timing — master, CPHA = 1

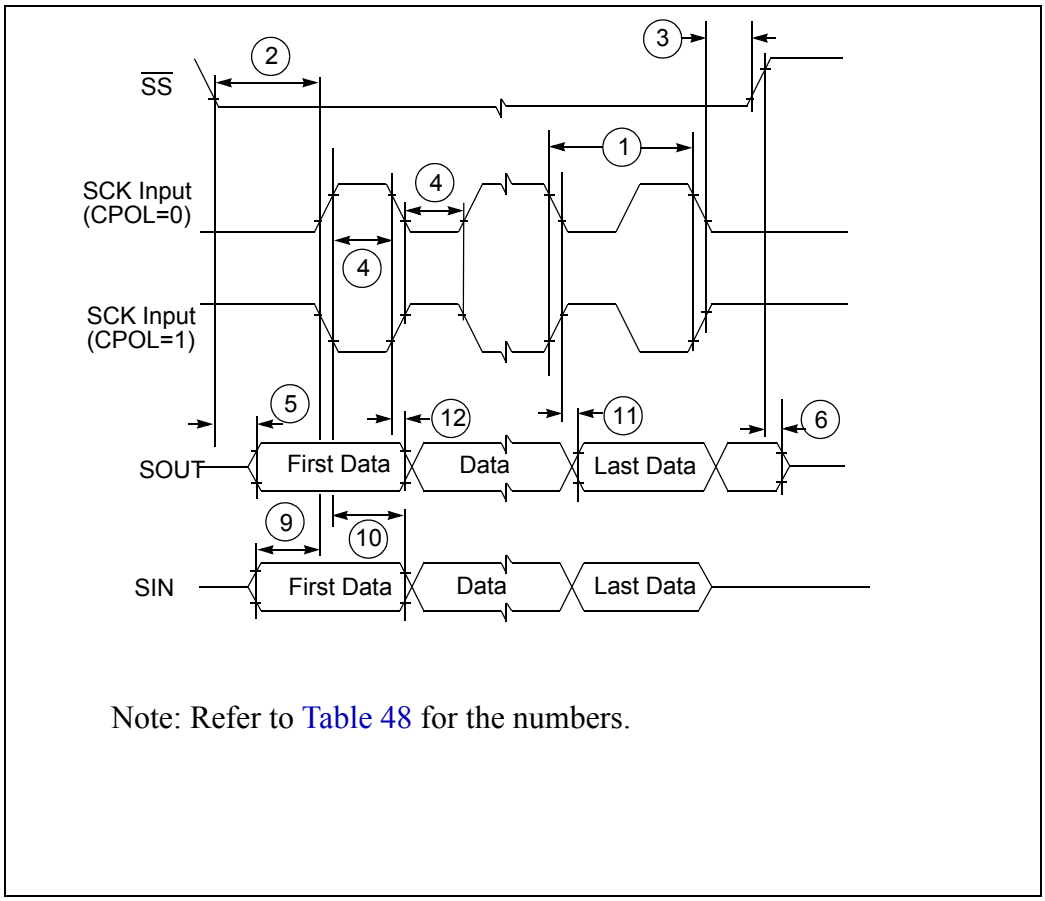
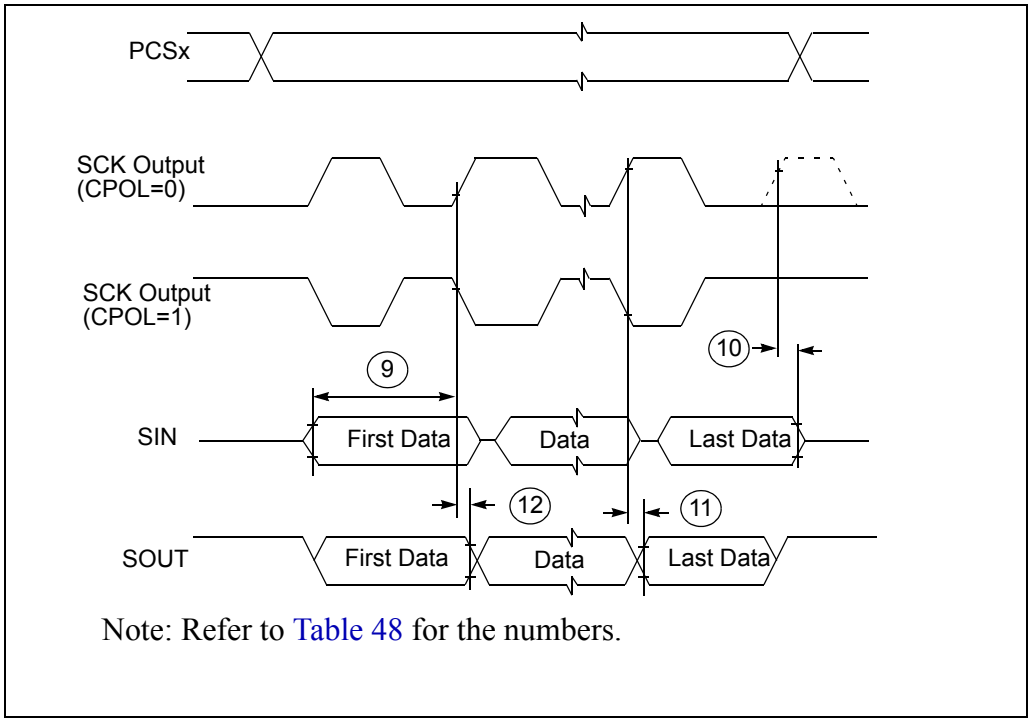
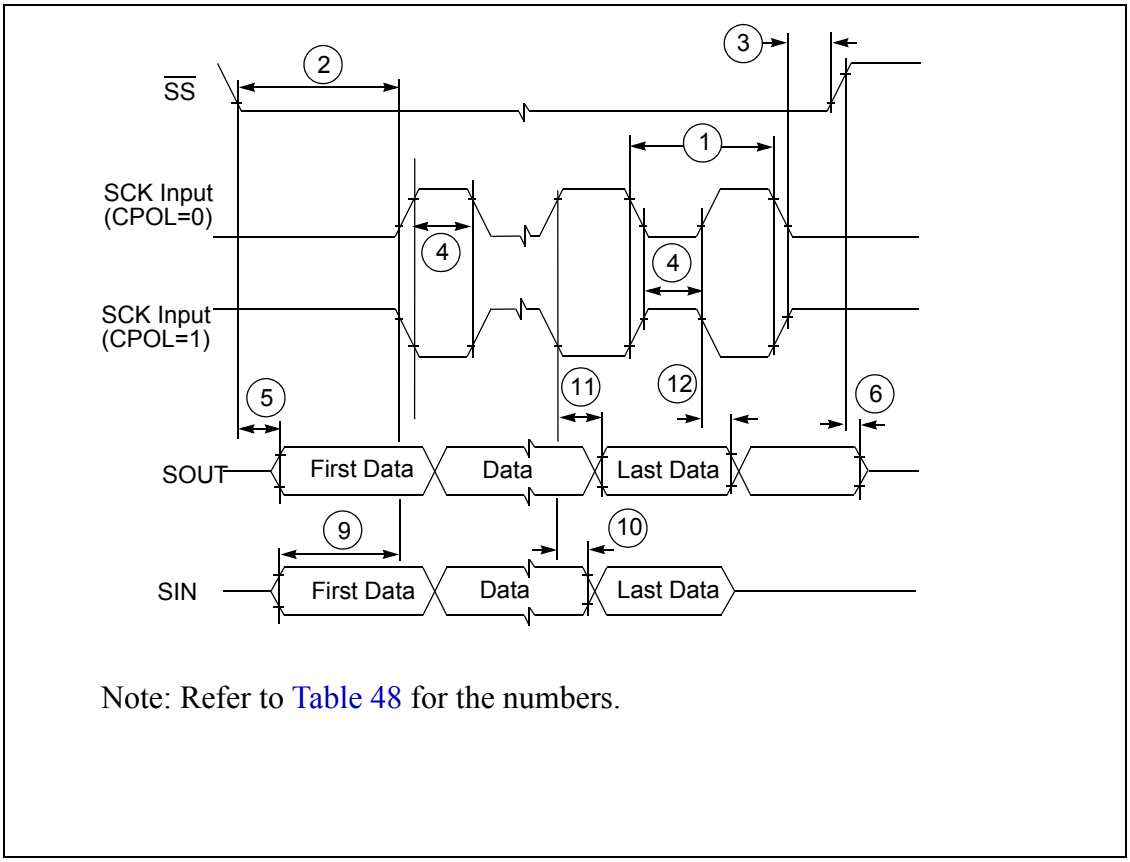


Figure 25. DSPI classic SPI timing — slave, CPHA = 0



Note: Refer to Table 48 for the numbers.

Figure 28. DSPI modified transfer format timing — master, CPHA = 1



Note: Refer to Table 48 for the numbers.

Figure 29. DSPI modified transfer format timing — slave, CPHA =0

Figure 33. 176 LQFP package mechanical drawing (part 1)

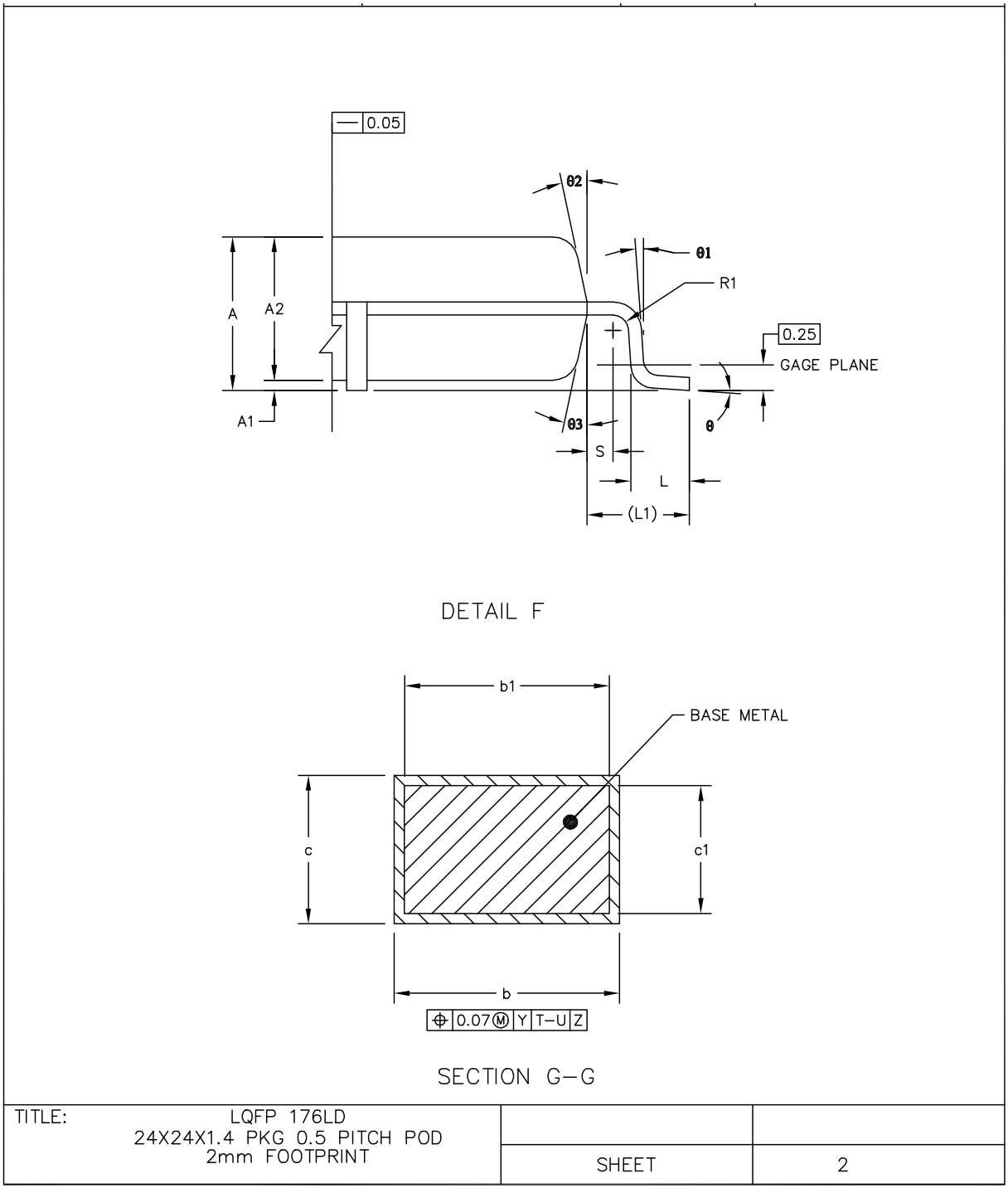


Figure 34. 176 LQFP package mechanical drawing (part 2)

4.1.3 324 TEPBGA

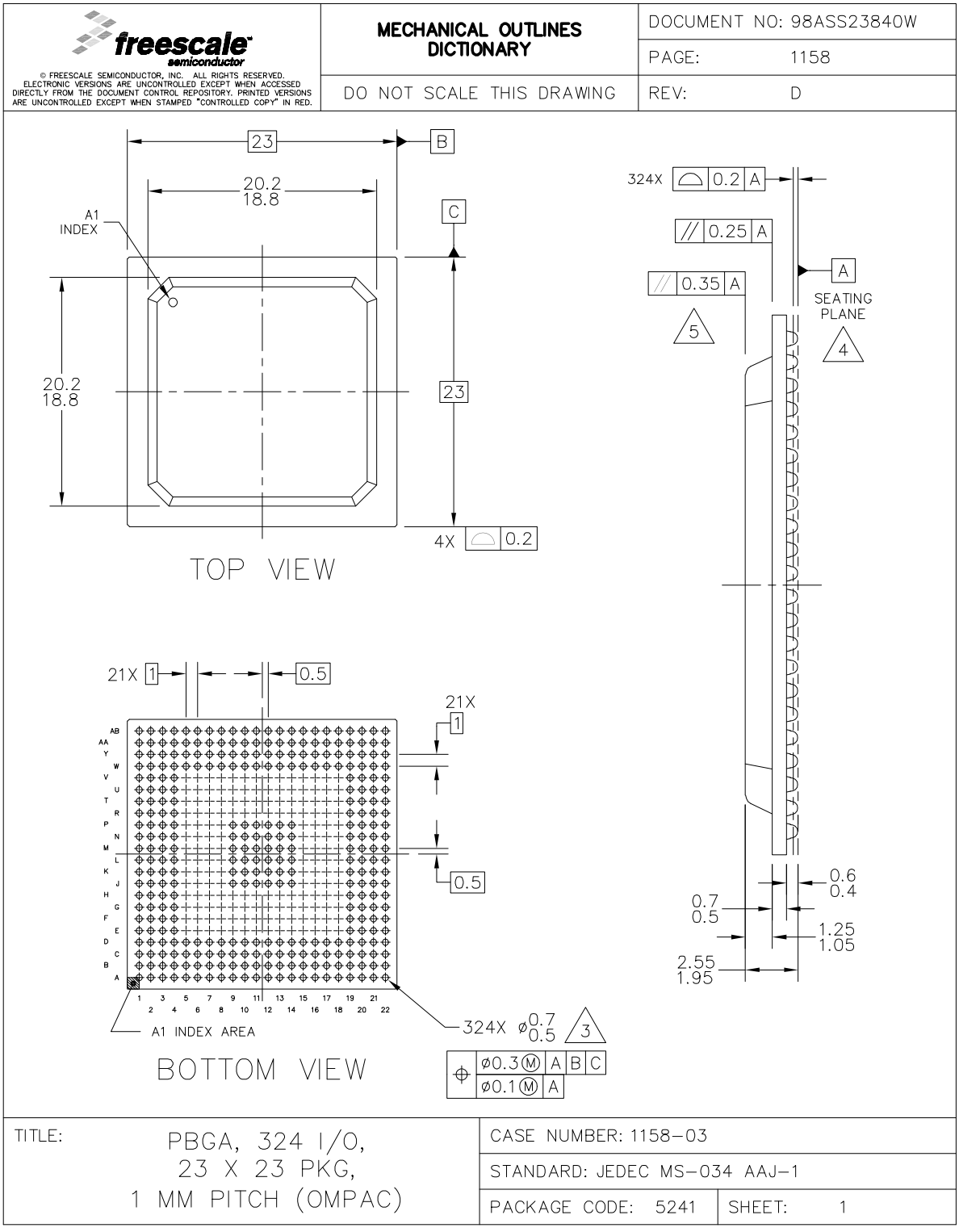


Figure 38. 324 BGA package mechanical drawing (part 1)

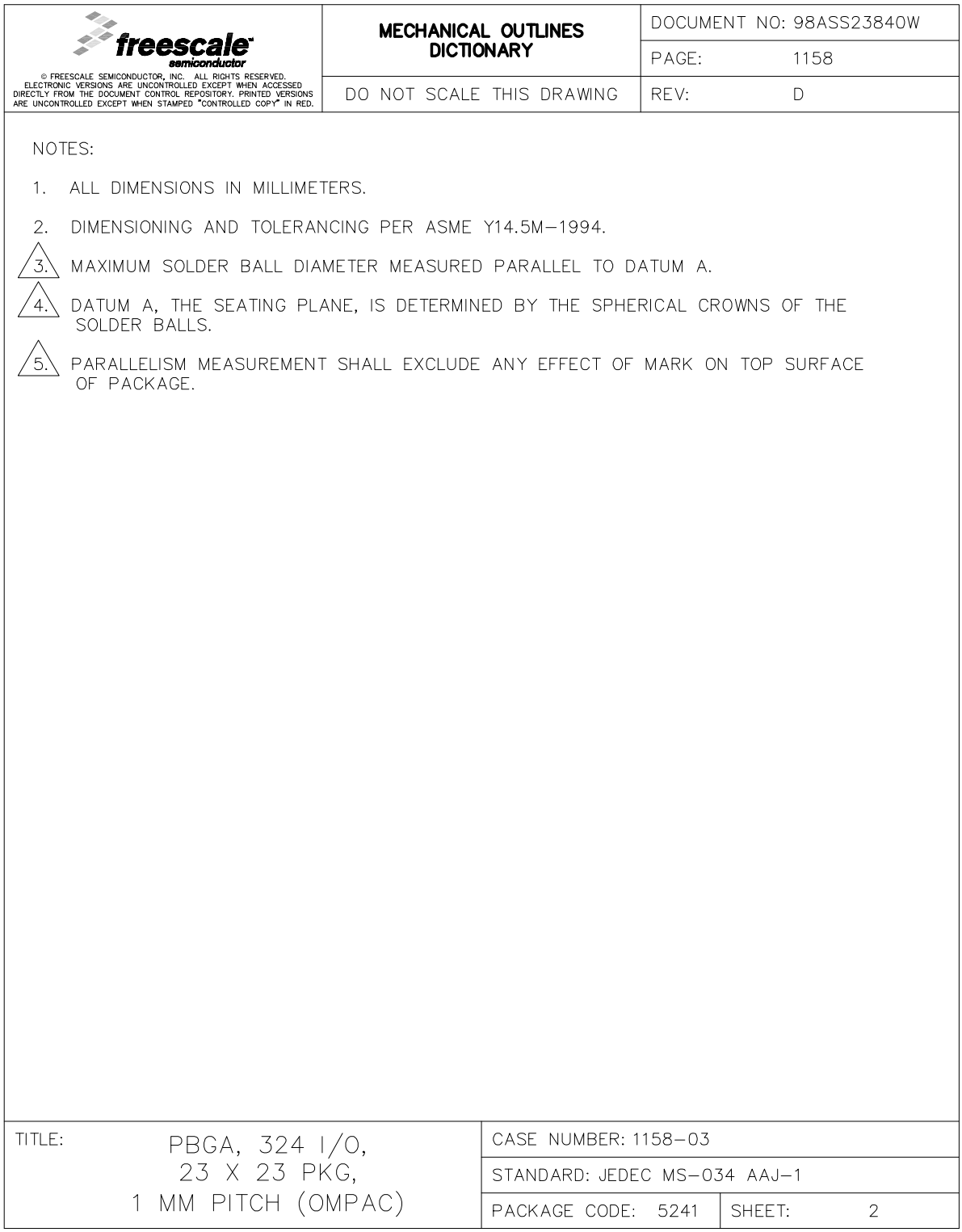


Figure 39. 324 BGA package mechanical drawing (part 2)

5 Ordering information

Table 52 shows the orderable part numbers for the MPC5644A series.

Table 52. Orderable part number summary

Part number	Flash/SRAM	Package	Speed (MHz)
SPC5643AF0MLU3	3 MB/192 KB	176LQFP (Pb free)	80
SPC5643AF0MMG3	3 MB/192 KB	208MAPBGA(Pb free)	80
SPC5643AF0MVZ3	3 MB/192 KB	324PBGA (Pb free)	80
SPC5643AF0MLU2	3 MB/192 KB	176LQFP (Pb free)	120
SPC5643AF0MMG2	3 MB/192 KB	208MAPBGA (Pb free)	120
SPC5643AF0MVZ2	3 MB/192 KB	324PBGA (Pb free)	120
SPC5643AF0MLU1	3 MB/192 KB	176LQFP (Pb free)	150
SPC5643AF0MMG1	3 MB/192 KB	208MAPBGA (Pb free)	150
SPC5643AF0MVZ1	3 MB/192 KB	324PBGA (Pb free)	150
SPC5644AF0MLU3	4 MB/192 KB	176 LQFP (Pb free)	80
SPC5644AF0MMG3	4 MB/192 KB	208 MAPBGA (Pb free)	80
SPC5644AF0MVZ3	4 MB/192 KB	324 TEPBGA (Pb free)	80
SPC5644AF0MLU2	4 MB/192 KB	176 LQFP (Pb free)	120
SPC5644AF0MMG2	4 MB/192 KB	208 MAPBGA (Pb free)	120
SPC5644AF0MVZ2	4 MB/192 KB	324 TEPBGA (Pb free)	120
SPC5644AF0MLU1	4 MB/192 KB	176 LQFP (Pb free)	150
SPC5644AF0MMG1	4 MB/192 KB	208 MAPBGA (Pb free)	150
SPC5644AF0MVZ1	4 MB/192 KB	324 TEPBGA (Pb free)	150

Table 53. Revision history (continued)

Revision	Date	Substantive changes
Rev. 3 (cont)	04/2010	Changes to Power/ground segmentation table: • ADDR[20:21] removed from VDDE2 segment; they are in VDDE-EH • CAL_CS1 removed from VDDE12 segment (there is no CAL_CS1 on this device) • CAL_EVTO and CAL_MCKO removed from VDDE12 segment. Those pins do not exist • VDDE-VDDEH renamed to VDDE-EH • EMIOS24 removed from VDDEH segment. That pin does not exist. • ETPUA[0:9] added to VDDEH4 segment • Renamed TCR_A in VDDEH4 segment to TCRCLKA. • EXTAL and XTAL added to VDDEH6 segment • AN15-FCK added to VDDEH7 segment • GPIO98, GPIO99, GPIO206, GPIO207 and GPIO219 added to VDDEH7 segment. • MSEO1 added to VDDEH7 segment • Power segment VDDEH1A renamed to VDDEH1 Changes to 176-pin package pinout: • Changed pin 9 from AN38 to AN8. • Added note that pin 96 (VSS) should be tied low. Changes to 208-ball package ballmap: • Changed ball B3 from AN38 to AN8. • Added note that ball N13 (VSS) should be tied low. 324-ball package ballmap updated for Rev. 2 silicon: • AN8 was on ball D3; it is now on E1 • AN38 was on ball E1; it is now on D3 Changes to features list: • Correction: there are 6 reaction channels (was noted as 5) • Development Trigger Semaphore (DTS) added to features list and feature details • FlexRay module now has 128 message buffers (was 64) and ECC support Added note after JTAG pin AC electrical characteristics table detailing JTAG EVTI and RDY signal clocking with TCK. This affects debuggers. Part numbers and part number decoder updated.

Table 53. Revision history (continued)

Revision	Date	Substantive changes
Rev. 7 (cont.)	01/12	• Added Table 17MPC5644A External network specification. • Updated Figure 8. • Changed External Network Parameter Ce min value to “3*2.35μF+5μF” from “2*2.35μF+5μF” in Table 17MPC5644A External network specification. • Changed Trans. Line (differential Zo) unit to Ω from W in Table 25DSPI LVDS pad specification.