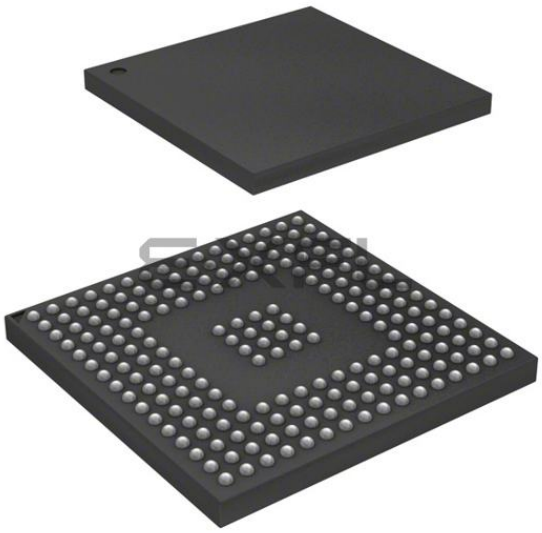


**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | e200z4 |
| Core Size | 32-Bit Single-Core |
| Speed | 150MHz |
| Connectivity | CANbus, EBI/EMI, LINbus, SCI, SPI |
| Peripherals | DMA, POR, PWM, WDT |
| Number of I/O | 120 |
| Program Memory Size | 4MB (4M x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 192K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.14V ~ 5.25V |
| Data Converters | A/D 40x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 208-BGA |
| Supplier Device Package | 208-BGA (17x17) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5644af0mmg1r |

## 1.4.23 Calibration EBI

The Calibration EBI controls data transfer across the crossbar switch to/from memories or peripherals attached to the VertiCal connector in the calibration address space. The Calibration EBI is only available in the VertiCal Calibration System.

Features include:

- 1.8 V to 3.3 V ± 10% I/O (1.6 V to 3.6 V)
- Memory controller supports various memory types
- 16-bit data bus, up to 22-bit address bus
- Pin muxing supports 32-bit muxed bus
- Selectable drive strength
- Configurable bus speed modes
- Bus monitor
- Configurable wait states

## 1.4.24 Power management controller (PMC)

The power management controller contains circuitry to generate the internal 3.3 V supply and to control the regulation of 1.2 V supply with an external NPN ballast transistor. It also contains low voltage inhibit (LVI) and power-on reset (POR) circuits for the 1.2 V supply, the 3.3 V supply, the 3.3 V/5 V supply of the closest I/O segment (VDDEH1) and the 5 V supply of the regulators (VDDREG).

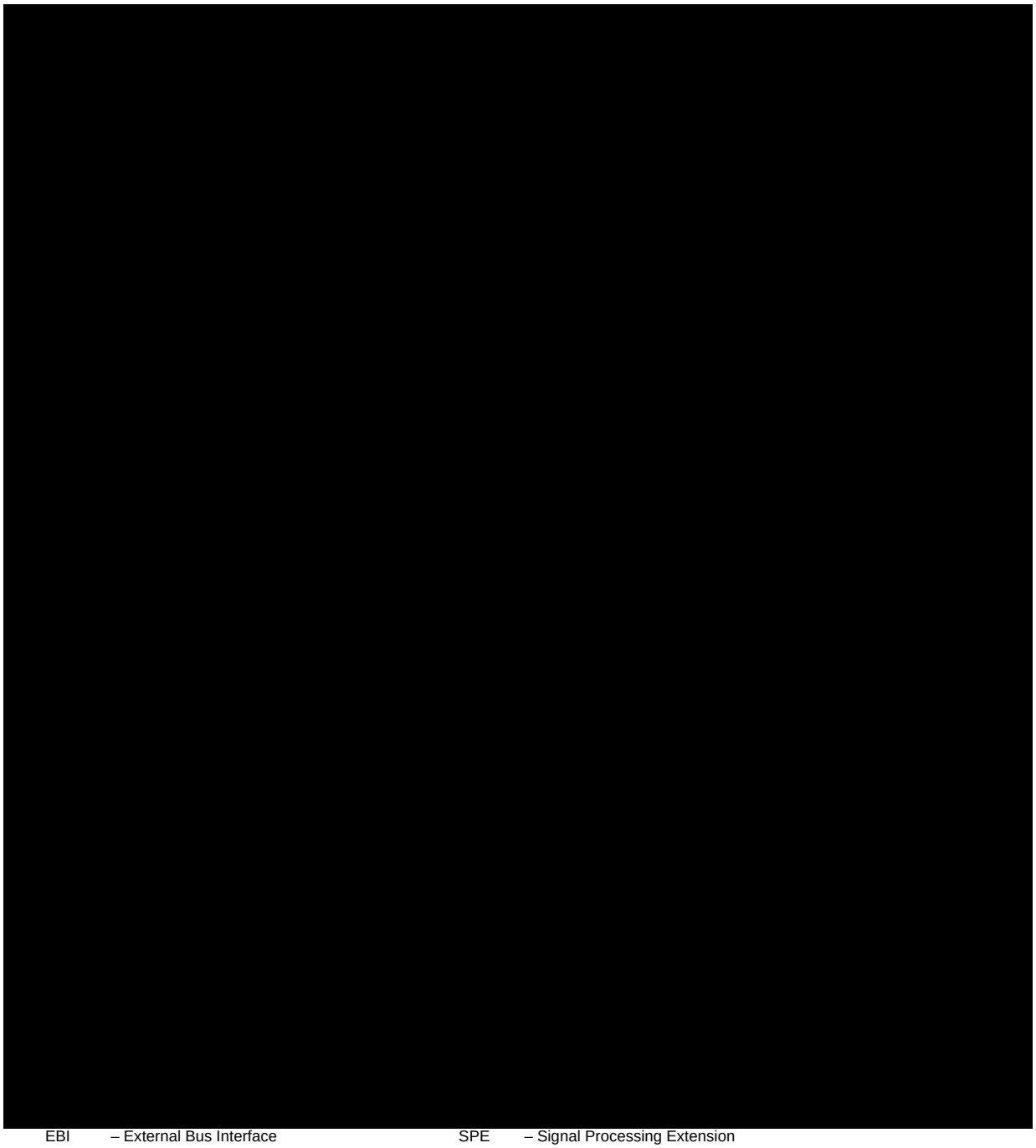
## 1.4.25 Nexus port controller

The NPC (Nexus Port Controller) block provides real-time Nexus Class3+ development support capabilities for the MPC5644A Power Architecture-based MCU in compliance with the IEEE-ISTO 5001-2003 and 2010 standards. MDO port widths of 4 pins and 12 pins are available in all packages.

## 1.4.26 JTAG

The JTAGC (JTAG Controller) block provides the means to test chip functionality and connectivity while remaining transparent to system logic when not in test mode. Testing is performed via a boundary scan technique, as defined in the IEEE 1149.1-2001 standard. All data input to and output from the JTAGC block is communicated in serial format. The JTAGC block is compliant with the IEEE 1149.1-2001 standard and supports the following features:

- IEEE 1149.1-2001 Test Access Port (TAP) interface 4 pins (TDI, TMS, TCK, and TDO)
- A 5-bit instruction register that supports the following IEEE 1149.1-2001 defined instructions:
  - BYPASS, IDCODE, EXTEST, SAMPLE, SAMPLE/PRELOAD, HIGHZ, CLAMP
- A 5-bit instruction register that supports the additional following public instructions:
  - ACCESS_AUX_TAP_NPC
  - ACCESS_AUX_TAP_ONCE
  - ACCESS_AUX_TAP_eTPU
  - ACCESS_CENSOR
- 3 test data registers to support JTAG Boundary Scan mode
  - Bypass register
  - Boundary scan register
  - Device identification register
- A TAP controller state machine that controls the operation of the data registers, instruction register and associated circuitry
- Censorship Inhibit Register



EBI – External Bus Interface
ECSM – Error Correction Status Module
eDMA – Enhanced Direct Memory Access
eMIOS – Enhanced Modular Input Output System
eSCI – Enhanced Serial Communications Interface
eTPU2 – Second gen. Enhanced Time Processing Unit
FlexCAN – Controller Area Network (FlexCAN)
FMPLL – Frequency-Modulated Phase Locked Loop
SPE – Signal Processing Extension
SRAM – Static RAM
STM – System Timer Module
SWT – Software Watchdog Timer
VGA – Variable Gain Amplifier
VLE – Variable Length (instruction) Encoding
XOSC – XTAL Oscillator

Figure 1. MPC5644A series block diagram

NOTES:

1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25MM PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE DATUM H.

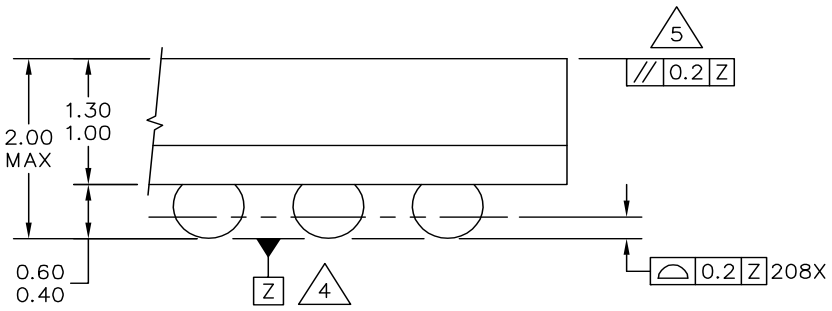
2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THEN 0.08MM. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07MM FOR 0.4MM AND 0.5MM PITCH PACKAGES.

| DIM | MIN | NOM | MAX | DIM | MIN | NOM | MAX | DIM | MIN | NOM | MAX |
|---|---|---|---|---|---|---|---|---|---|---|---|
| A | --- | | 1.6 | L1 | | 1 REF | | | | | |
| A1 | 0.05 | | 0.15 | R1 | 0.08 | | --- | | | | |
| A2 | 1.35 | 1.4 | 1.45 | R2 | 0.08 | | 0.2 | | | | |
| b | 0.17 | 0.22 | 0.27 | S | | 0.2 REF | | | | | |
| b1 | 0.17 | 0.2 | 0.23 | θ | 0° | 3.5° | 7° | | | | |
| c | 0.09 | | 0.2 | θ1 | 0° | | --- | | | | |
| c1 | 0.09 | | 0.16 | θ2 | 11° | 12° | 13° | | | | |
| D | | 26 BSC | | θ3 | 11° | 12° | 13° | | | | |
| D1 | | 24 BSC | | | | | | | | | |
| e | | 0.5 BSC | | | | | | | | | |
| E | | 26 BSC | | | | | | | | | |
| E1 | | 24 BSC | | | | | | | | | |
| L | 0.45 | 0.6 | 0.75 | | | | | | | | |

| UNIT | DIMENSION AND TOLERANCES | REFERANCE DOCUMENT |
|---|---|---|
| MM | ASME Y14.5M | 64-06-280-1392 |

| TITLE: | | |
|---|---|---|
| LQFP 176LD<br>24X24X1.4 PKG 0.5 PITCH POD<br>2mm FOOTPRINT | | |
| | SHEET | 3 |

**Figure 35. 176 LQFP package mechanical drawing (part 3)**




DETAIL K
(ROTATED 90° CLOCKWISE)

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE Z.
4. DATUM Z (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

| TITLE: 208 I/O MAP BGA, 17 X 17 PKG, 1–MM PITCH | CASE NUMBER: 1159A–01 | |
|---|---|---|
| | STANDARD: JEDEC MO–151 AAF–1 | |
| | PACKAGE CODE: 5253 | SHEET: 2 |

**Figure 37. 208 MAPBGA package mechanical drawing (part 2)**

## 4.1.3 324 TEPBGA

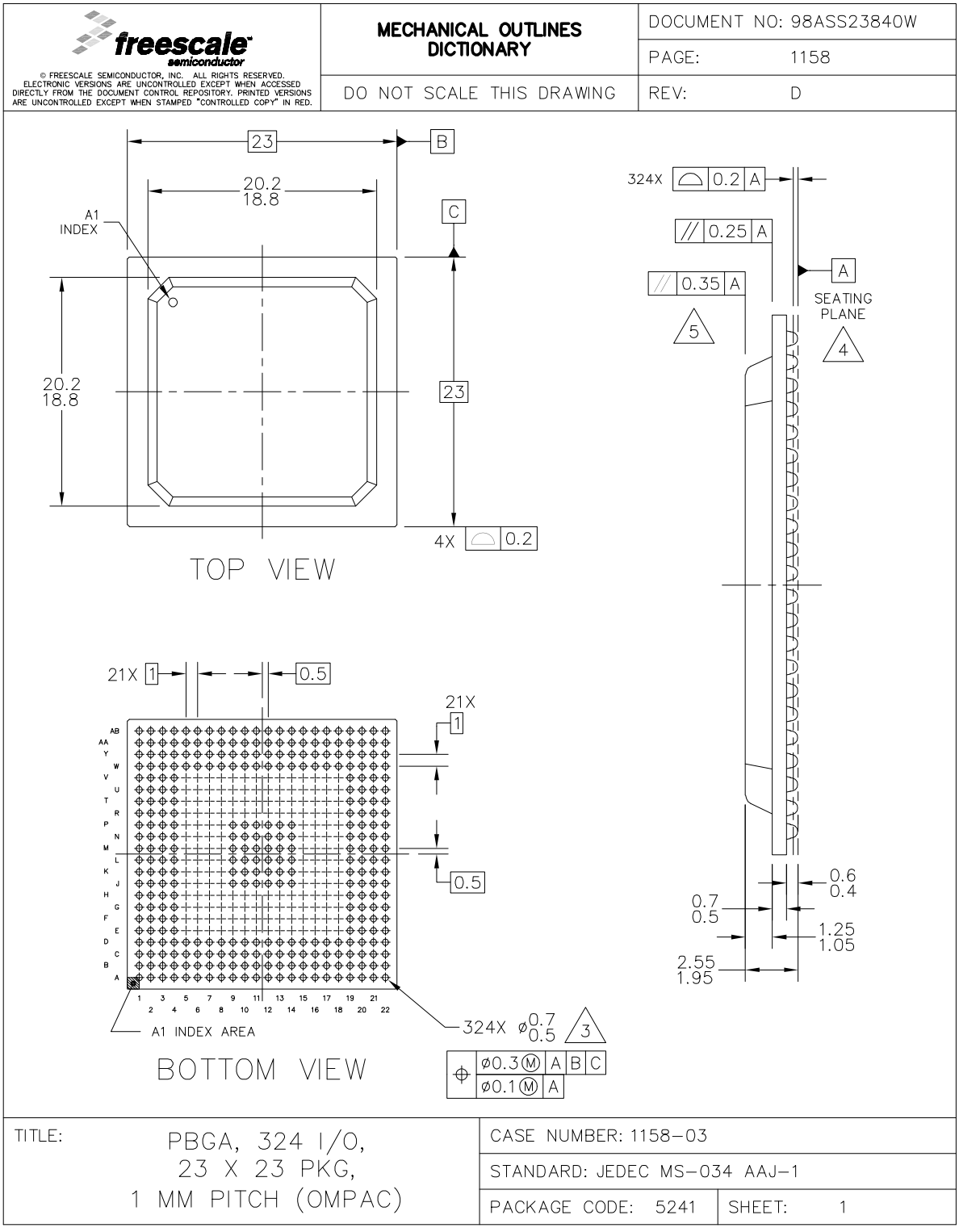



**Figure 38. 324 BGA package mechanical drawing (part 1)**