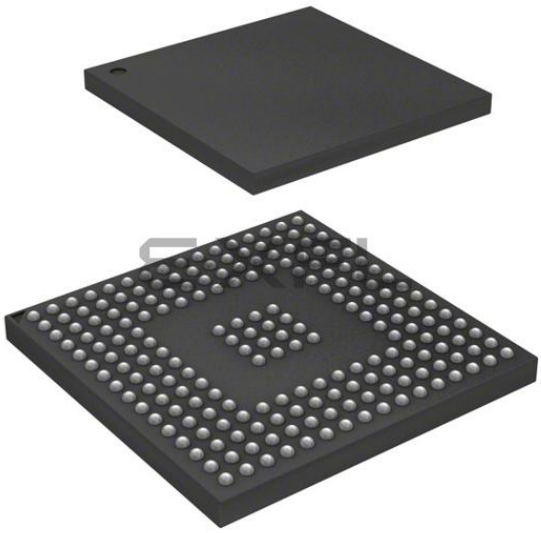

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	e200z4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	120
Program Memory Size	4MB (4M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	1.14V ~ 5.25V
Data Converters	A/D 40x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	208-BGA
Supplier Device Package	208-BGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5644af0mmg2

1.3 Device comparison

Table 1 summarizes the MPC5644A and compares it to the MPC5634M.

Table 1. MPC5644A, MPC5634M and MPC5642A comparison

Feature		MPC5644A	MPC5634M	MPC5642A
Process		90 nm		
Core		e200z4	e200z3	e200z4
	SIMD	Yes		
	VLE	Yes		
	Cache	8 KB instruction	No	8 KB instruction
	Non-Maskable Interrupt (NMI)	NMI & Critical Interrupt		
	MMU	24 entry	16 entry	24 entry
	MPU	16 entry	No	16 entry
	Crossbar switch	5 × 4	3 × 4	4 × 4
	Core performance	0–150 MHz	0–80 MHz	0–150 MHz
Windowing software watchdog		Yes		
Core Nexus		Class 3+	Class 2+	Class 3+
SRAM		192 KB	94 KB	128 KB
Flash		4 MB	1.5 MB	2 MB
Flash fetch accelerator		4 × 256-bit	4 × 128-bit	
External bus		16-bit (incl 32-bit muxed)	None	
Calibration bus		16-bit (incl 32-bit muxed)	16-bit	16-bit (incl 32-bit muxed)
DMA		64 ch.	32 ch.	64 ch.
DMA Nexus		None		
Serial		3	2	3
	eSCI_A	Yes (MSC Uplink)		
	eSCI_B	Yes (MSC Uplink)		
	eSCI_C	Yes	No	Yes
CAN		3	2	3
	CAN_A	64 buf		
	CAN_B	64 buf	No	64 buf
	CAN_C	64 buf	32 buf	64 buf
SPI		3	2	3

The eTPU2 includes these distinctive features:

- 32 channels; each channel associated with one input and one output signal
  - Enhanced input digital filters on the input pins for improved noise immunity
  - Identical, orthogonal channels: each channel can perform any time function. Each time function can be assigned to more than one channel at a given time, so each signal can have any functionality.
  - Each channel has an event mechanism which supports single and double action functionality in various combinations. It includes two 24-bit capture registers, two 24-bit match registers, 24-bit greater-equal and equal-only comparators.
  - Input and output signal states visible from the host
- 2 independent 24-bit time bases for channel synchronization:
  - First time base clocked by system clock with programmable prescale division from 2 to 512 (in steps of 2), or by output of second time base prescaler
  - Second time base counter can work as a continuous angle counter, enabling angle based applications to match angle instead of time
  - Both time bases can be exported to the eMIOS timer module
  - Both time bases visible from the host
- Event-triggered microengine:
  - Fixed-length instruction execution in two-system-clock microcycle
  - 14 KB of code memory (SCM)
  - 3 KB of parameter (data) RAM (SPRAM)
  - Parallel execution of data memory, ALU, channel control and flow control sub-instructions in selected combinations
  - 32-bit microengine registers and 24-bit wide ALU, with 1 microcycle addition and subtraction, absolute value, bitwise logical operations on 24-bit, 16-bit, or byte operands, single-bit manipulation, shift operations, sign extension and conditional execution
  - Additional 24-bit Multiply/MAC/Divide unit which supports all signed/unsigned Multiply/MAC combinations, and unsigned 24-bit divide. The MAC/Divide unit works in parallel with the regular microcode commands.
- Resource sharing features support channel use of common channel registers, memory and microengine time:
  - Hardware scheduler works as a “task management” unit, dispatching event service routines by predefined, host-configured priority
  - Automatic channel context switch when a “task switch” occurs, that is, one function thread ends and another begins to service a request from other channel: channel-specific registers, flags and parameter base address are automatically loaded for the next serviced channel
  - SPRAM shared between host CPU and eTPU2, supporting communication either between channels and host or inter-channel
  - Hardware implementation of four semaphores support coherent parameter sharing between both eTPU engines
  - Dual-parameter coherency hardware support allows atomic access to two parameters by host
- Test and development support features:
  - Nexus Class 1 debug, supporting single-step execution, arbitrary microinstruction execution, hardware breakpoints and watchpoints on several conditions
  - Software breakpoints
  - SCM continuous signature-check built-in self test (MISC - multiple input signature calculator), runs concurrently with eTPU2 normal operation

1.4.12 Reaction module

The reaction module provides the ability to modulate output signals to manage closed loop control without CPU assistance. It works in conjunction with the eQADC and eTPU2 to increase system performance by removing the CPU from the current control loop.

The reaction module has the following features:

- Six reaction channels
- Each channel output is a bus of three signals, providing ability to control 3 inputs.
- Each channel can implement a peak and hold waveform, making it possible to implement up to six independent peak and hold control channels

Target applications include solenoid control for direct injection systems and valve control in automatic transmissions

1.4.13 eQADC

The enhanced queued analog to digital converter (eQADC) block provides accurate and fast conversions for a wide range of applications. The eQADC provides a parallel interface to two on-chip analog to digital converters (ADC), and a single master to single slave serial interface to an off-chip external device. Both on-chip ADCs have access to all the analog channels.

The eQADC prioritizes and transfers commands from six command conversion command ‘queues’ to the on-chip ADCs or to the external device. The block can also receive data from the on-chip ADCs or from an off-chip external device into the six result queues, in parallel, independently of the command queues. The six command queues are prioritized with Queue_0 having the highest priority and Queue_5 the lowest. Queue_0 also has the added ability to bypass all buffering and queuing and abort a currently running conversion on either ADC and start a Queue_0 conversion. This means that Queue_0 will always have a deterministic time from trigger to start of conversion, irrespective of what tasks the ADCs were performing when the trigger occurred. The eQADC supports software and external hardware triggers from other blocks to initiate transfers of commands from the queues to the on-chip ADCs or to the external device. It also monitors the fullness of command queues and result queues, and accordingly generates DMA or interrupt requests to control data movement between the queues and the system memory, which is external to the eQADC.

The ADCs also support features designed to allow the direct connection of high impedance acoustic sensors that might be used in a system for detecting engine knock. These features include differential inputs; integrated variable gain amplifiers for increasing the dynamic range; programmable pull-up and pull-down resistors for biasing and sensor diagnostics.

The eQADC also integrates a programmable decimation filter capable of taking in ADC conversion results at a high rate, passing them through a hardware low pass filter, then down-sampling the output of the filter and feeding the lower sample rate results to the result FIFOs. This allows the ADCs to sample the sensor at a rate high enough to avoid aliasing of out-of-band noise; while providing a reduced sample rate output to minimize the amount DSP processing bandwidth required to fully process the digitized waveform.

The eQADC provides the following features:

- Dual on-chip ADCs
  - 2 × 12-bit ADC resolution
  - Programmable resolution for increased conversion speed (12-bit, 10-bit, 8-bit)
    - 12-bit conversion time: 938 ns (1 M sample/sec)
    - 10-bit conversion time: 813 ns (1.2 M sample/second)
    - 8-bit conversion time: 688 ns (1.4 M sample/second)
  - Up to 10-bit accuracy at 500 KSample/s and 8-bit accuracy at 1 MSample/s
  - Differential conversions
  - Single-ended signal range from 0 to 5 V
  - Variable gain amplifiers on differential inputs (×1, ×2, ×4)
  - Sample times of 2 (default), 8, 64 or 128 ADC clock cycles

Table 3. MPC5644A signal properties (continued)

Name	Function[1]	PAG[2]	PCR PA Field[3]	PCR[4]	I/O Type	Voltage[5] / Pad Type[6]	Status[7]		Package pin #		
							During Reset	After Reset	176	208	324
BOOTCFG[1] IRQ[3] ETRIG3 GPIO[212]	Boot Config. Input External Interrupt Request eQADC Trigger Input GPIO	P A1 A2 G	001 010 100 000	212	I I I I/O	VDDEH6 Slow	— / Down	BOOTCFG[1] / Down	85	M15	U21
WKPCFG NMI DSPI_B_SOUT GPIO[213]	Weak Pull Config. Input Non-Maskable Interrupt DSPI D data output GPIO	P A1 A2 G	001 010 100 000	213	I I O I/O	VDDEH6 Medium	— / Up	WKPCFG / Up	86	L15	AA20
External Bus Interface											
CS[0] ADDR[8] GPIO[0]	External chip selects External address bus GPIO	P A1 G	01 10 00	0	O I/O I/O	VDDE2 Fast	— / Up	— / Up	—	—	G1
CS[1] ADDR9 GPIO[1]	External chip selects External address bus GPIO	P A1 G	01 10 00	1	O I/O I/O	VDDE2 Fast	— / Up	— / Up	—	—	H1
CS[2] ADDR10 WE[2]/BE[2] CAL_WE[2]/BE[2] GPIO[2]	External chip selects External address bus Write/byte enable Cal. bus write/byte enable GPIO	P A1 A2 A3 G	0001 0010 0100 1000 0000	2	O I/O O O I/O	VDDE2 Fast	— / Up	— / Up	—	—	H2
CS[3] ADDR11 WE[3]/BE[3] CAL_WE[3]/BE[3] GPIO[3]	External chip selects External address bus Write/byte enable Cal bus write/byte enable GPIO	P A1 A2 A3 G	0001 0010 0100 1000 0000	3	O I/O O O I/O	VDDE2 Fast	— / Up	— / Up	—	—	H4
ADDR12 GPIO[8]	External address bus GPIO	P G	01 00	8	I/O I/O	VDDE3 Fast	— / Up	— / Up	—	—	N2
ADDR13 WE[2] GPIO[9]	External address bus Write/byte enable GPIO	P A2 G	001 100 000	9	I/O O I/O	VDDE3 Fast	— / Up	— / Up	—	—	N1
ADDR14 WE[3] GPIO[10]	External address bus Write/byte enables GPIO	P A2 G	001 100 000	10	I/O O I/O	VDDE3 Fast	— / Up	— / Up	—	—	P1
ADDR15 GPIO[11]	External address bus GPIO	P G	01 00	11	I/O I/O	VDDE3 Fast	— / Up	— / Up	—	—	P2

Table 10. Thermal characteristics for 208-pin MAPBGA[1]

Symbol		C	Parameter	Conditions	Value	Unit
$R_{\theta JA}$	CC	D	Junction-to-Ambient, Natural Convection[2,3]	One layer board - 1s	39	°C/W
$R_{\theta JA}$	CC	D	Junction-to-Ambient, Natural Convection[2,4]	Four layer board - 2s2p	24	°C/W
$R_{\theta JMA}$	CC	D	Junction-to-Moving-Air, Ambient[2,4]	at 200 ft./min., one layer board	31	°C/W
$R_{\theta JMA}$	CC	D	Junction-to-Moving-Air, Ambient[2,4]	at 200 ft./min., four layer board 2s2p	20	°C/W
$R_{\theta JB}$	CC	D	Junction-to-board[5]	Four layer board - 2s2p	13	°C/W
$R_{\theta JC}$	CC	D	Junction-to-case[6]		6	°C/W
Ψ_{JT}	CC	D	Junction-to-package top natural convection[7]		2	°C/W

1 Thermal characteristics are targets based on simulation that are subject to change per device characterization.

2 Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

3 Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board horizontal.

4 Per JEDEC JESD51-6 with the board horizontal.

5 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

6 Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature.

7 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

Table 11. Thermal characteristics for 324-pin TEPBGA[1]

Symbol		C	Parameter	Conditions	Value	Unit
$R_{\theta JA}$	CC	D	Junction-to-Ambient, Natural Convection[2]	Single layer board - 1s	29	°C/W
$R_{\theta JA}$	CC	D	Junction-to-Ambient, Natural Convection[2]	Four layer board - 2s2p	19	°C/W
$R_{\theta JMA}$	CC	D	Junction-to-Moving-Air, Ambient[2]	at 200 ft./min., single layer board	23	°C/W
$R_{\theta JMA}$	CC	D	Junction-to-Moving-Air, Ambient[2]	at 200 ft./min., four layer board 2s2p	16	°C/W
$R_{\theta JB}$	CC	D	Junction-to-Board[3]		10	°C/W
$R_{\theta JCtop}$	CC	D	Junction-to-Case[4]		7	°C/W
Ψ_{JT}	CC	D	Junction-to-Package Top, Natural Convection[5]		2	°C/W

1 Thermal characteristics are targets based on simulation that are subject to change per device characterization.

2 Junction-to-Ambient Thermal Resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.

3 Junction-to-Board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.

4 Junction-to-Case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

[5] Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

3.3.1 General notes for specifications at maximum junction temperature

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} * P_D) \quad \textit{Eqn. 1}$$

where:

T_A = ambient temperature for the package (^oC)
$R_{\theta JA}$ = junction-to-ambient thermal resistance ($^oC/W$)
P_D = power dissipation in the package (W)

The thermal resistance values used are based on the JEDEC JESD51 series of standards to provide consistent values for estimations and comparisons. The difference between the values determined for the single-layer (1s) board compared to a four-layer board that has two signal layers, a power and a ground plane (2s2p), demonstrate that the effective thermal resistance is not a constant. The thermal resistance depends on the:

- Construction of the application board (number of planes)
- Effective size of the board which cools the component
- Quality of the thermal and electrical connections to the planes
- Power dissipated by adjacent components

Connect all the ground and power balls to the respective planes with one via per ball. Using fewer vias to connect the package to the planes reduces the thermal performance. Thinner planes also reduce the thermal performance. When the clearance between the vias leave the planes virtually disconnected, the thermal performance is also greatly reduced.

As a general rule, the value obtained on a single-layer board is within the normal range for the tightly packed printed circuit board. The value obtained on a board with the internal planes is usually within the normal range if the application board has:

- One oz. (35 micron nominal thickness) internal planes
- Components are well separated
- Overall power dissipation on the board is less than 0.02 W/cm^2

The thermal performance of any component depends on the power dissipation of the surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter (edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using the following equation:

$$T_J = T_B + (R_{\theta JB} * P_D) \quad \textit{Eqn. 2}$$

where:

T_B = board temperature for the package perimeter (^oC)
$R_{\theta JB}$ = junction-to-board thermal resistance ($^oC/W$) per JESD51-8S
P_D = power dissipation in the package (W)

When the heat loss from the package case to the air does not factor into the calculation, an acceptable value for the junction temperature is predictable. Ensure the application board is similar to the thermal test condition, with the component soldered to a board with internal planes.

Table 15. PMC Electrical Characteristics

ID	Name			Parameter	Min	Typ	Max	Unit	Notes
1	VBG	CC	C	Nominal bandgap voltage reference	—	1.219	—	V	
1a	—	CC	P	Untrimmed bandgap reference voltage	VBG - 7%	VBG	Vbg + 6%	V	
1b	—	CC	P	Trimmed bandgap reference voltage (5 V, 27 °C)	VBG -10mV	VBG	VBG + 10mV	V	
1c	—	CC	C	Bandgap reference temperature variation	—	100	—	ppm /°C	
1d	—	CC	C	Bandgap reference supply voltage variation	—	3000	—	ppm /V	
2	Vdd	CC	C	Nominal V_{DD} core supply internal regulator target DC output voltage[1]	—	1.28	—	V	
2a	—	CC	P	Nominal V_{DD} core supply internal regulator target DC output voltage variation at power-on reset	Vdd - 6%	Vdd	Vdd + 10%	V	
2b	—	CC	P	Nominal V_{DD} core supply internal regulator target DC output voltage variation after power-on reset	Vdd - 10%[2]	Vdd	Vdd + 3%	V	
2c	—	CC	C	Trimming step Vdd	—	20	—	mV	
2d	Ivrcctl	CC	C	Voltage regulator controller for core supply maximum DC output current	20	—	—	mA	
3	Lvi1p2	CC	C	Nominal LVI for rising core supply[3]	—	1.160	—	V	
3a	—	CC	C	Variation of LVI for rising core supply at power-on reset	1.120	1.200	1.280	V	See note [4]
3b	—	CC	C	Variation of LVI for rising core supply after power-on reset	Lvi1p2 - 3%	Lvi1p2	Lvi1p2 + 3%	V	See note 4
3c	—	CC	C	Trimming step LVI core supply	—	20	—	mV	
3d	Lvi1p2_h	CC	C	LVI core supply hysteresis	—	40	—	mV	
4	Por1.2V_r	CC	C	POR 1.2 V rising	—	0.709	—	V	
4a	—	CC	C	POR 1.2 V rising variation	Por1.2V_r - 35%	Por1.2V_r	Por1.2V_r + 35%	V	
4b	Por1.2V_f	CC	C	POR 1.2 V falling	—	0.638	—	V	
4c	—	CC	C	POR 1.2 V falling variation	Por1.2V_f - 35%	Por1.2V_f	Por1.2V_f+ 35%	V	

Table 21. DC electrical specifications (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					min	typ	max	
I_{DDSTBY}	CC	T	Operating current 0.95-1.2 V	V_{STBY} at 55 °C	—	35	100	µA
		T	Operating current 2–5.5 V	V_{STBY} at 55 °C	—	45	110	µA
$I_{DDSTBY27}$	CC	P	Operating current 0.95-1.2 V	V_{STBY} 27 °C		25	90	µA
		P	Operating current 2-5.5 V	V_{STBY} 27 °C		35	100	µA
$I_{DDSTBY150}$	CC	P	Operating current 0.95-1.2 V	V_{STBY} 150 °C	—	790	2000	µA
		P	Operating current 2–5.5 V	V_{STBY} at 150 °C	—	760	2000	µA
I_{DDPLL}	CC	P	Operating current 1.2 V supplies	V_{DDPLL}, 80 MHz, V_{DD}=1.2 V	—		15	mA
I_{DDSLOW} I_{DDSTOP}	CC	P	V_{DD} low-power mode operating current at 1.32 V	Slow mode[10]	—		90	mA
		P		Stop mode[11]	—		75	
I_{DD33}	CC	C	Operating current 3.3 V supplies	V_{RC33}[1,12]	—		60	mA
I_{DDA} I_{REF} I_{DDREG}	CC	P	Operating current 5.0 V supplies	V_{DDA}	—	—	30.0	mA
		P		Analog reference supply current (transient)	—	—	1.0	
		C		V_{DDREG}	—	—	70[13]	
I_{DDH1} I_{DDH4} I_{DDH6} I_{DDH7} I_{DD7} I_{DDH9} I_{DD12}	CC	D	Operating current V_{DDE}[14] supplies	V_{DDEH1}	—	—	See note [14]	mA
		D		V_{DDEH4}	—	—		
		D		V_{DDEH6}	—	—		
		D		V_{DDEH7}	—	—		
		D		V_{DDE7}	—	—		
		D		V_{DDEH9}	—	—		
		D		V_{DDE12}	—	—		

[4] V_{FLASH} is only available in the calibration package.

[5] Power supply for multi-voltage pads cannot be below 4.5 V when in low-swing mode.

[6] The slew rate (SRC) setting must be 0b11 when in low-swing mode.

[7] While in low-swing mode there are no restrictions in transitioning to high-swing mode.

[8] Pin in low-swing mode can accept a 5 V input.

[9] All V_{OL}/V_{OH} values 100% tested with ± 2 mA load except where noted.

[10] Bypass mode, system clock at 1 MHz (using system clock divider), PLL shut down, CPU running simple executive code, 4 x ADC conversion every 10 ms, 2 x PWM channels 1 kHz, all other modules stopped.

[11] Bypass mode, system clock at 1 MHz (using system clock divider), CPU stopped, PIT running, all other modules stopped.

[12] This current will be consumed for external regulation and internal regulation, when 3.3V regulator is switched off by shadow flash

[13] If 1.2V and 3.3V internal regulators are on,then iddreg=70mA

If supply is external that is 3.3V internal regulator is off, then iddreg=15mA

[14] Power requirements for each I/O segment are dependent on the frequency of operation and load of the I/O pins on a particular I/O segment, and the voltage of the I/O segment. See Table 22 for values to calculate power dissipation for specific operation. The total power consumption of an I/O segment is the sum of the individual power consumptions for each pin on the segment.

[15] Absolute value of current, measured at V_{IL} and V_{IH}.

[16] Weak pull up/down inactive. Measured at V_{DDE} = 3.6 V and V_{DDEH} = 5.25 V. Applies to fast, slow, and medium pads.

[17] Maximum leakage occurs at maximum operating temperature. Leakage current decreases by approximately one-half for each 8 to 12 ^{o}C, in the ambient temperature range of 50 to 125 ^{o}C. Applies to analog pads.

[18] Applies to CLKOUT, external bus pins, and Nexus pins.

[19] Applies to the FCK, SDI, SDO, and $\overline{SDS}$ pins.

[20] This programmable option applies only to eQADC differential input channels and is used for biasing and sensor diagnostics.

Table 30. eQADC differential ended conversion specifications (operating) (continued)

Symbol		C	Parameter		Value		Unit
					min	max	
GAINVGA2[1]	CC	–	Variable gain amplifier accuracy (gain=2)[2]				
	CC	D	INL	8 MHz ADC	–5	5	Counts
	CC	D		16 MHz ADC	–8	8	Counts
	CC	D	DNL	8 MHz ADC	–3	3	Counts
	CC	D		16 MHz ADC	–3	3	Counts
GAINVGA4[1]	CC	–	Variable gain amplifier accuracy (gain=4)[2]				
	CC	D	INL	8 MHz ADC	–7	7	Counts
	CC	D		16 MHz ADC	–8	8	Counts
	CC	D	DNL	8 MHz ADC	–4	4	Counts
	CC	D		16 MHz ADC	–4	4	Counts
$DIFF_{max}$	CC	C	Maximum differential voltage (DANx+ - DANx-) or (DANx- - DANx+)[5]	PREGAIN set to 1X setting	—	(VRH - VRL)/2	V
$DIFF_{max2}$	CC	C		PREGAIN set to 2X setting	—	(VRH - VRL)/4	V
$DIFF_{max4}$	CC	C		PREGAIN set to 4X setting	—	(VRH - VRL)/8	V
$DIFF_{cmv}$	CC	C	Differential input Common mode voltage (DANx- + DANx+)/2[5]	—	$(V_{RH} + V_{RL})/2$ - 5%	$(V_{RH} + V_{RL})/2$ + 5%	V

1 Applies only to differential channels.

2 Variable gain is controlled by setting the PRE_GAIN bits in the ADC_ACR1-8 registers to select a gain factor of ×1, ×2, or ×4. Settings are for differential input only. Tested at ×1 gain. Values for other settings are guaranteed by as indicated.

3 At $V_{RH} – V_{RL}$ = 5.12 V, one LSB = 1.25 mV.

4 Guaranteed 10-bit mono tonicity.

5 Voltages between VRL and VRH will not cause damage to the pins. However, they may not be converted accurately if the differential voltage is above the maximum differential voltage. In addition, conversion errors may occur if the common mode voltage of the differential signal violates the Differential Input common mode voltage specification.

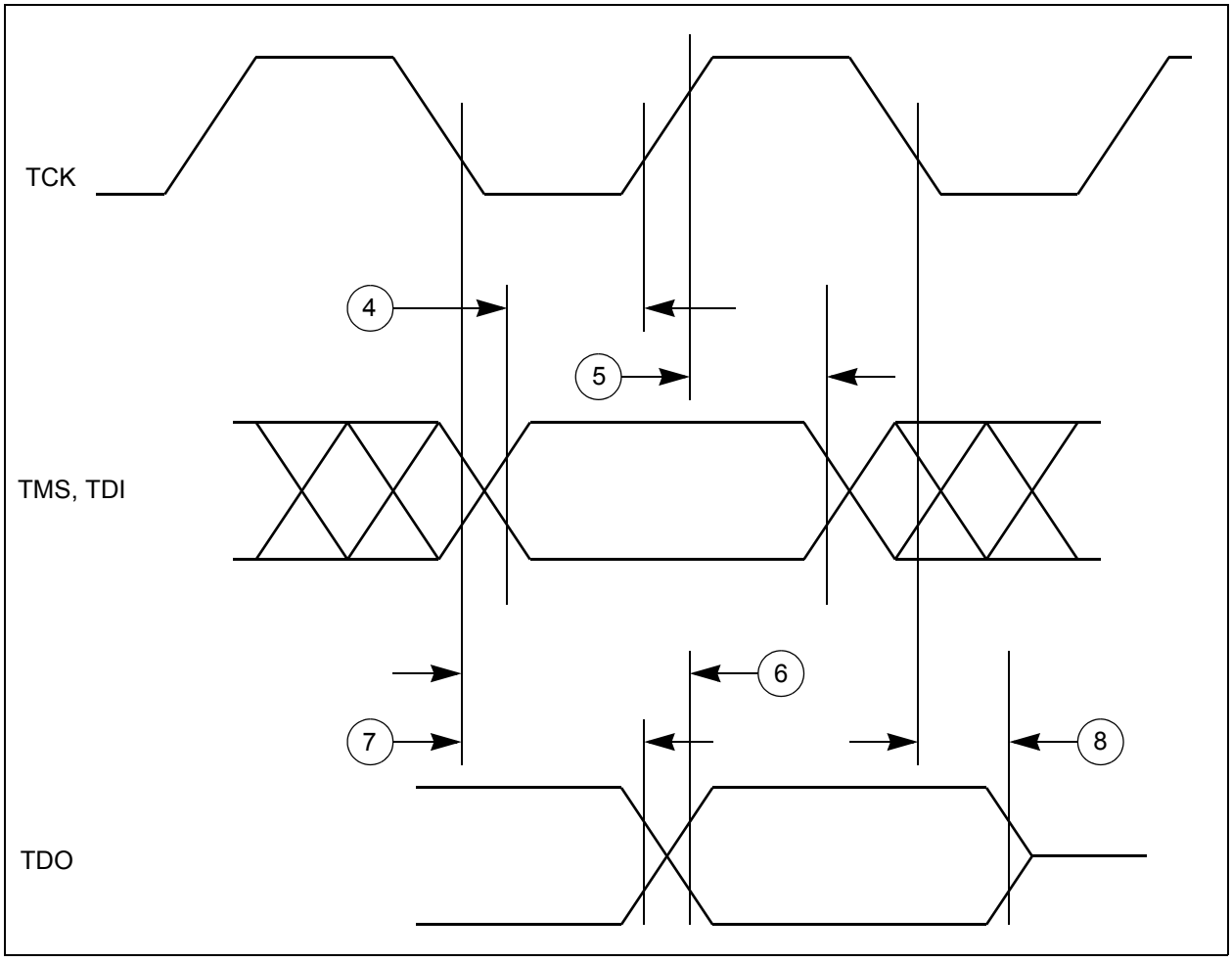


Figure 12. JTAG test access port timing

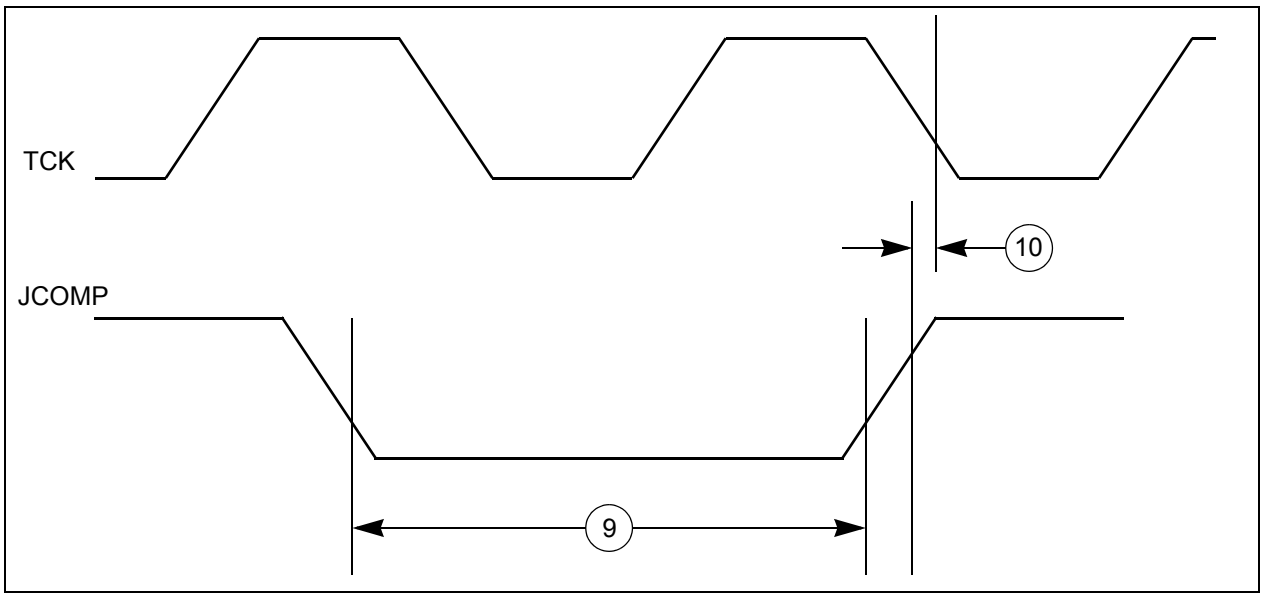


Figure 13. JTAG JCOMP timing

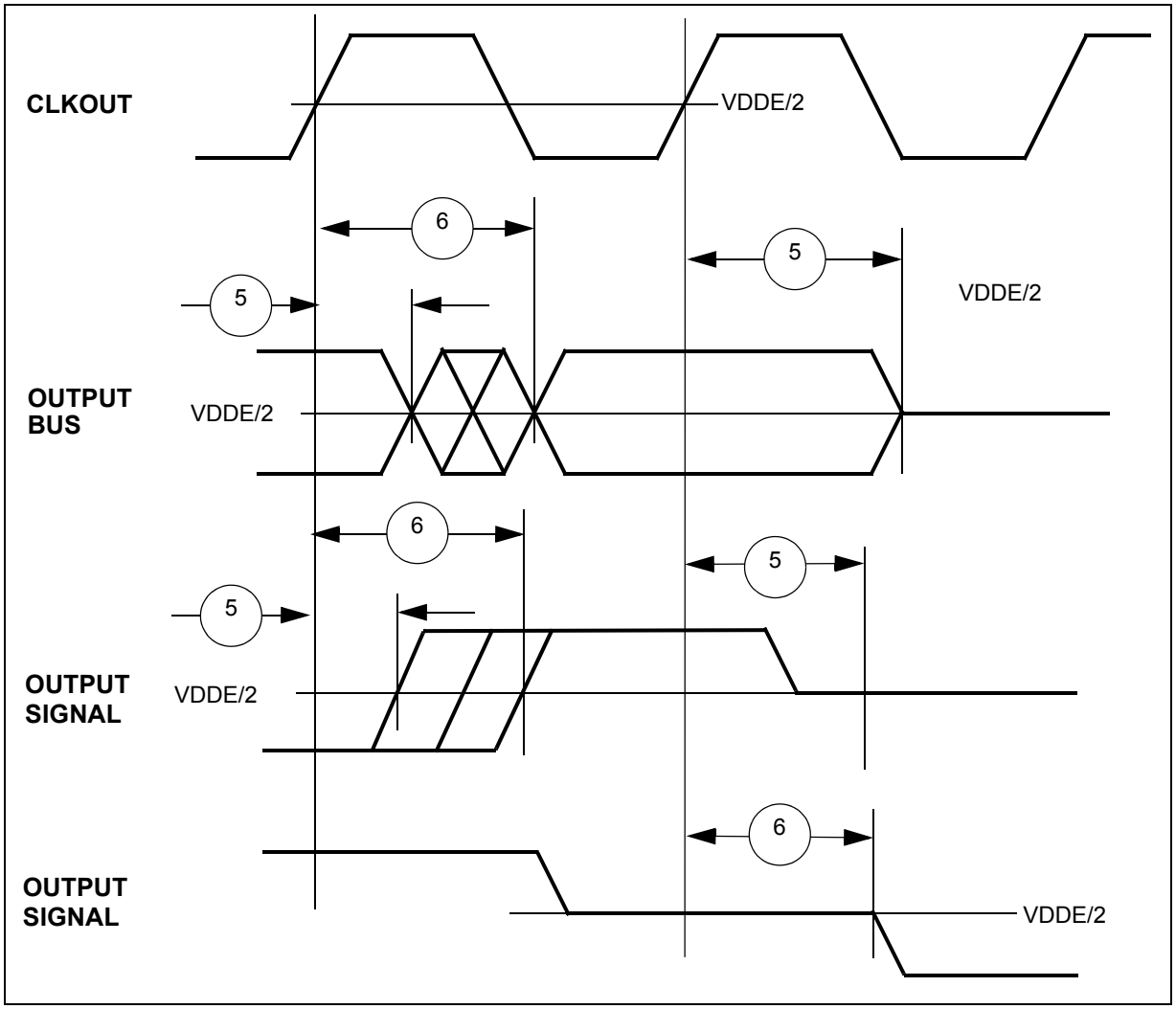
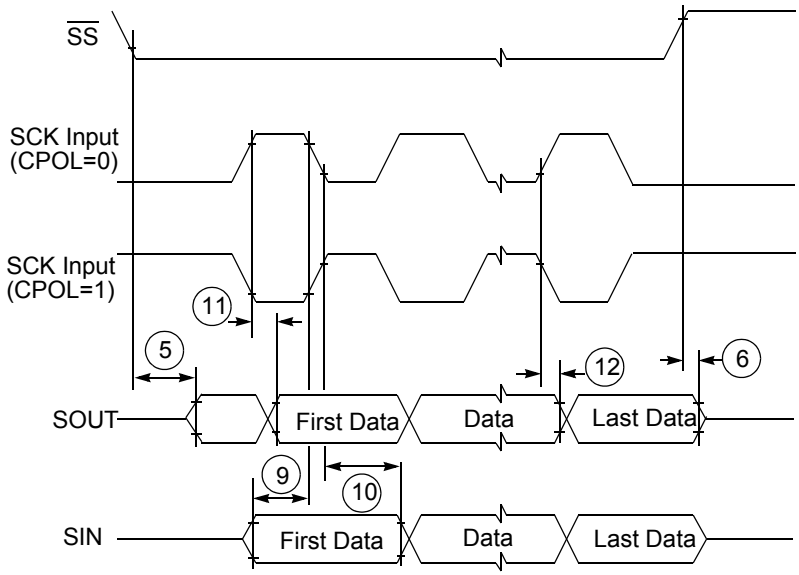
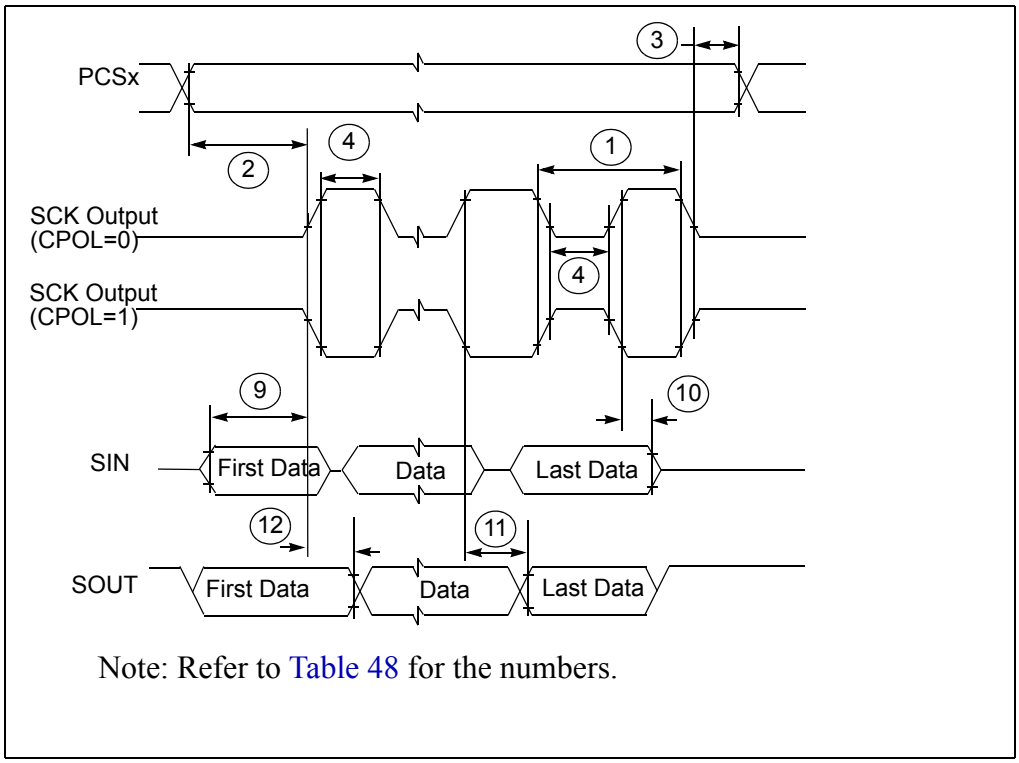


Figure 19. Synchronous output timing



Note: Refer to Table 48 for the numbers.

Figure 26. DSPI classic SPI timing — slave, CPHA = 1



Note: Refer to Table 48 for the numbers.

Figure 27. DSPI modified transfer format timing — master, CPHA = 0

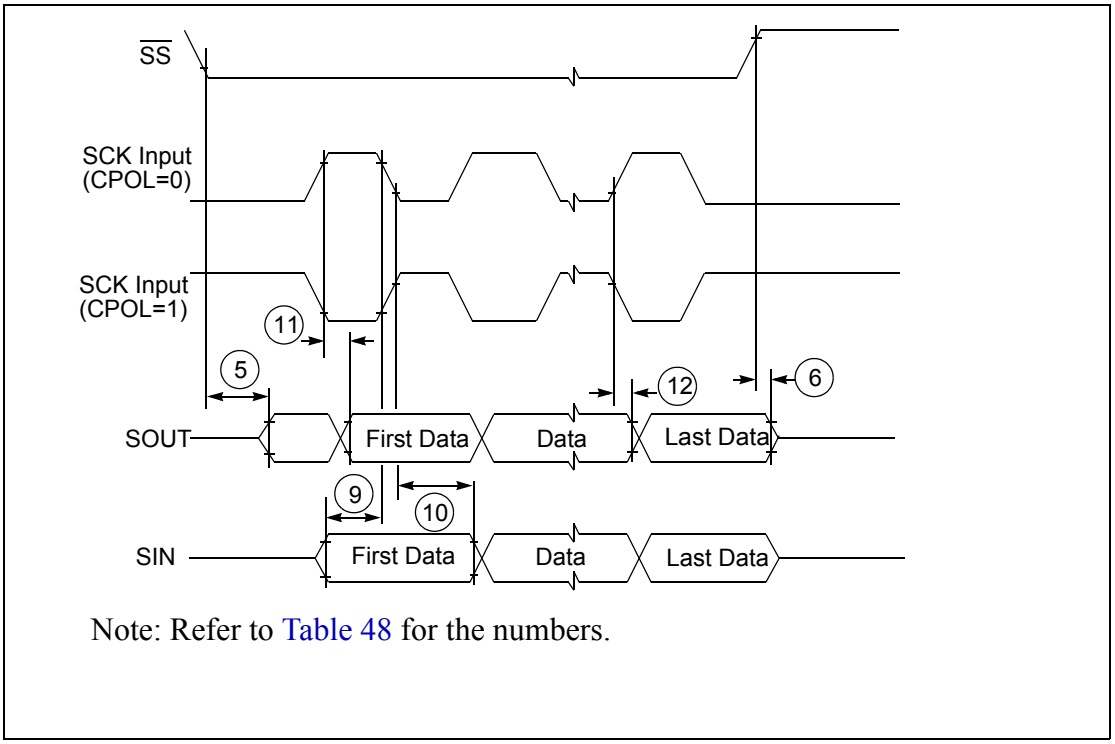


Figure 30. DSPI modified transfer format timing — slave, CPHA =1

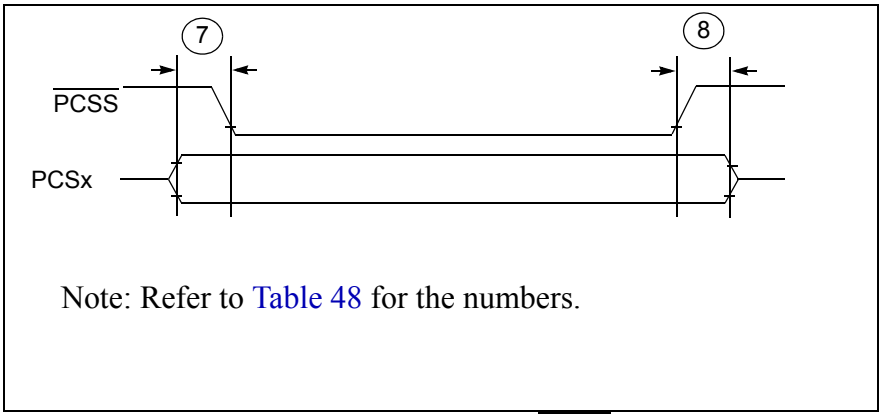


Figure 31. DSPI PCS strobe (PCSS) timing

Figure 33. 176 LQFP package mechanical drawing (part 1)

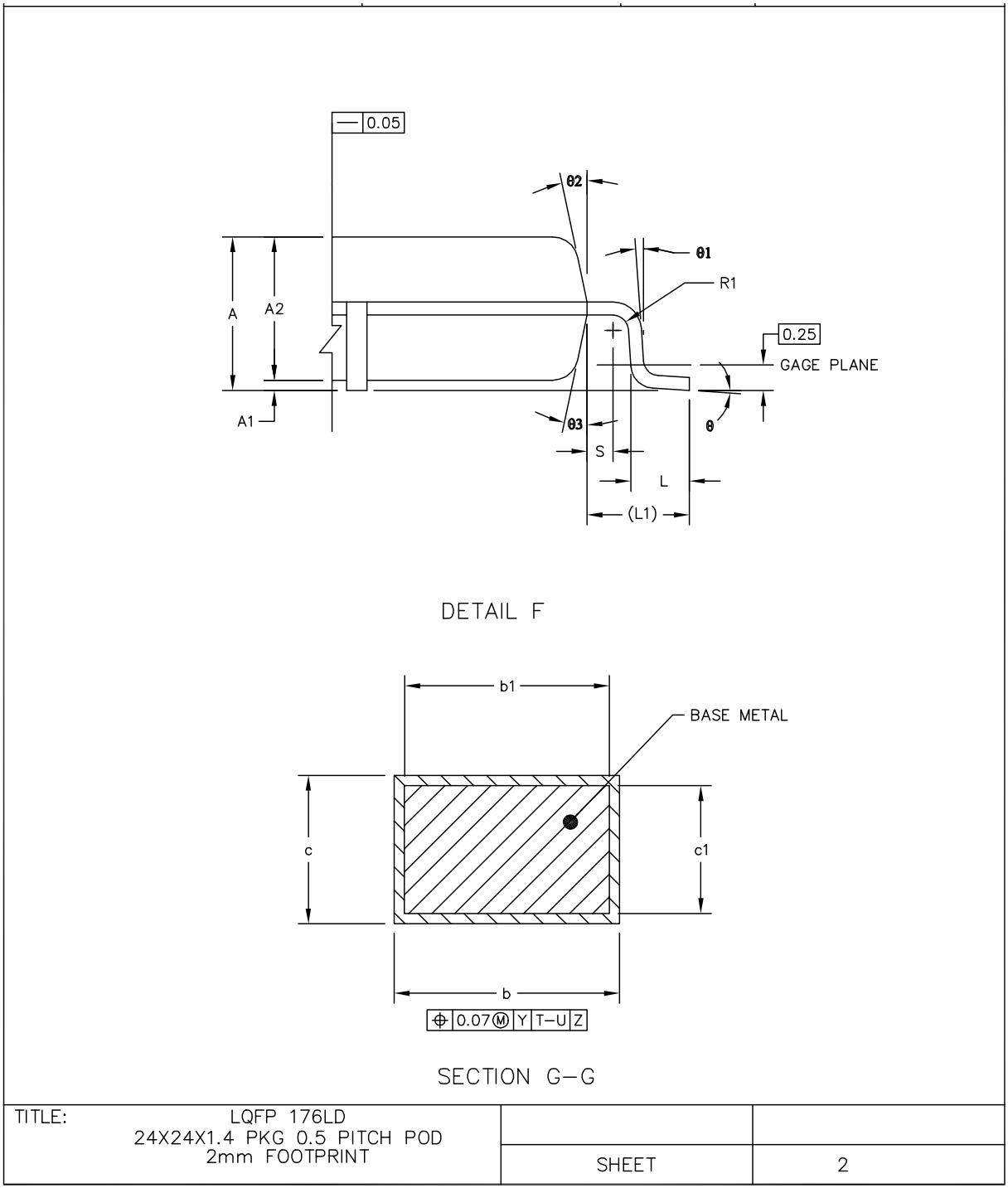


Figure 34. 176 LQFP package mechanical drawing (part 2)

4.1.2 208 MAPBGA

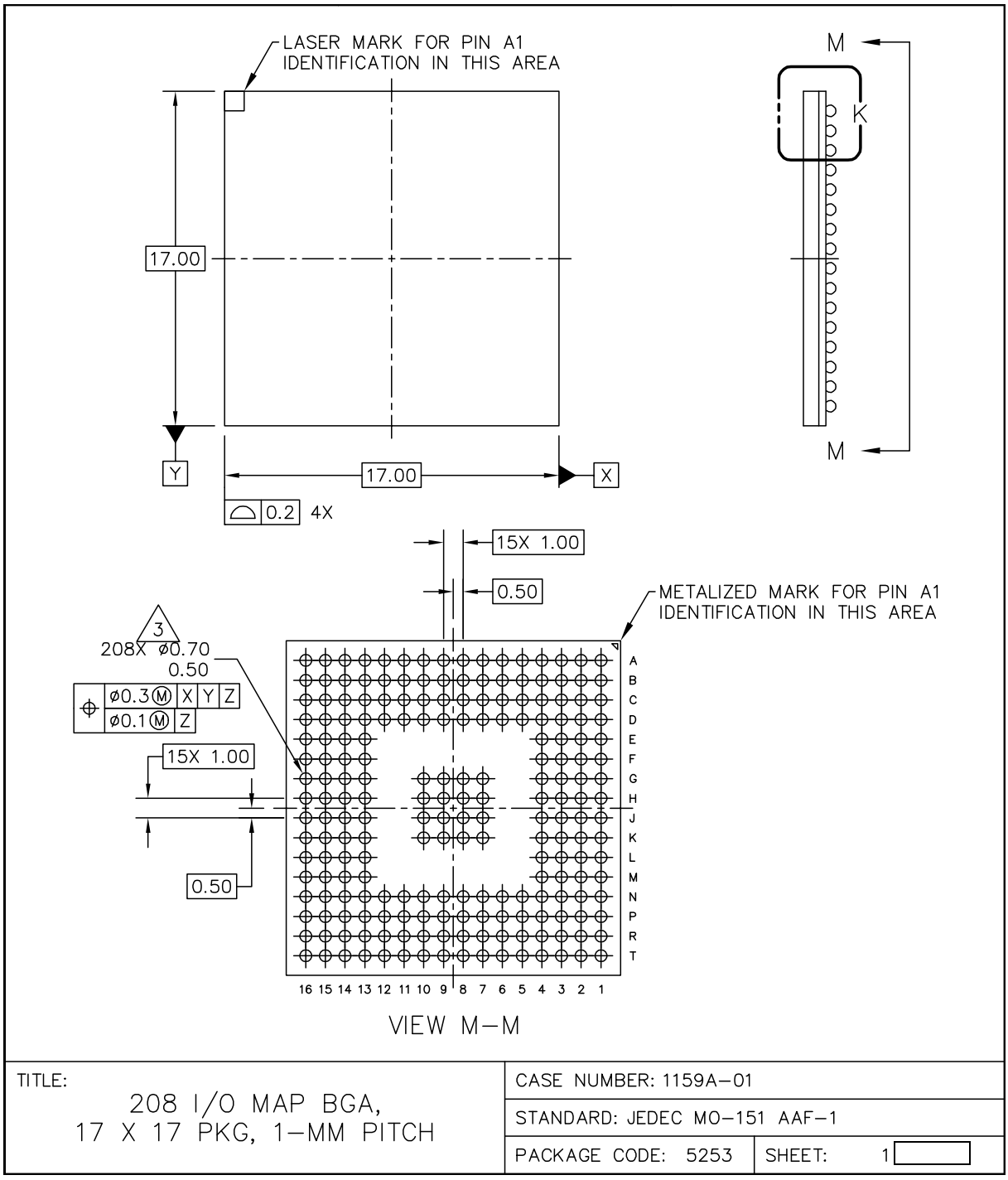
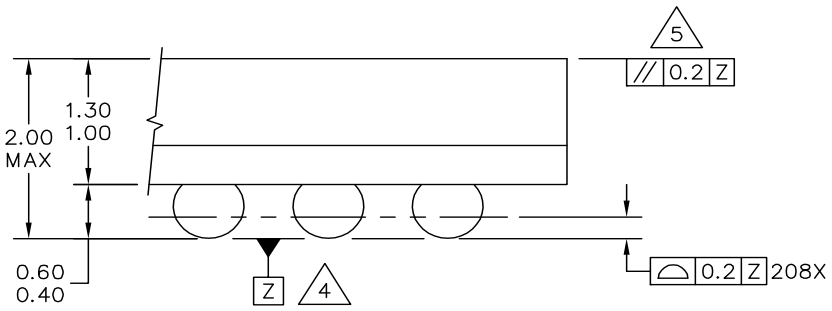


Figure 36. 208 MAPBGA package mechanical drawing (part 1)



DETAIL K
(ROTATED 90° CLOCKWISE)

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE Z.
4. DATUM Z (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

TITLE: 208 I/O MAP BGA, 17 X 17 PKG, 1–MM PITCH	CASE NUMBER: 1159A–01	
	STANDARD: JEDEC MO–151 AAF–1	
	PACKAGE CODE: 5253	SHEET: 2

Figure 37. 208 MAPBGA package mechanical drawing (part 2)

4.1.3 324 TEPBGA

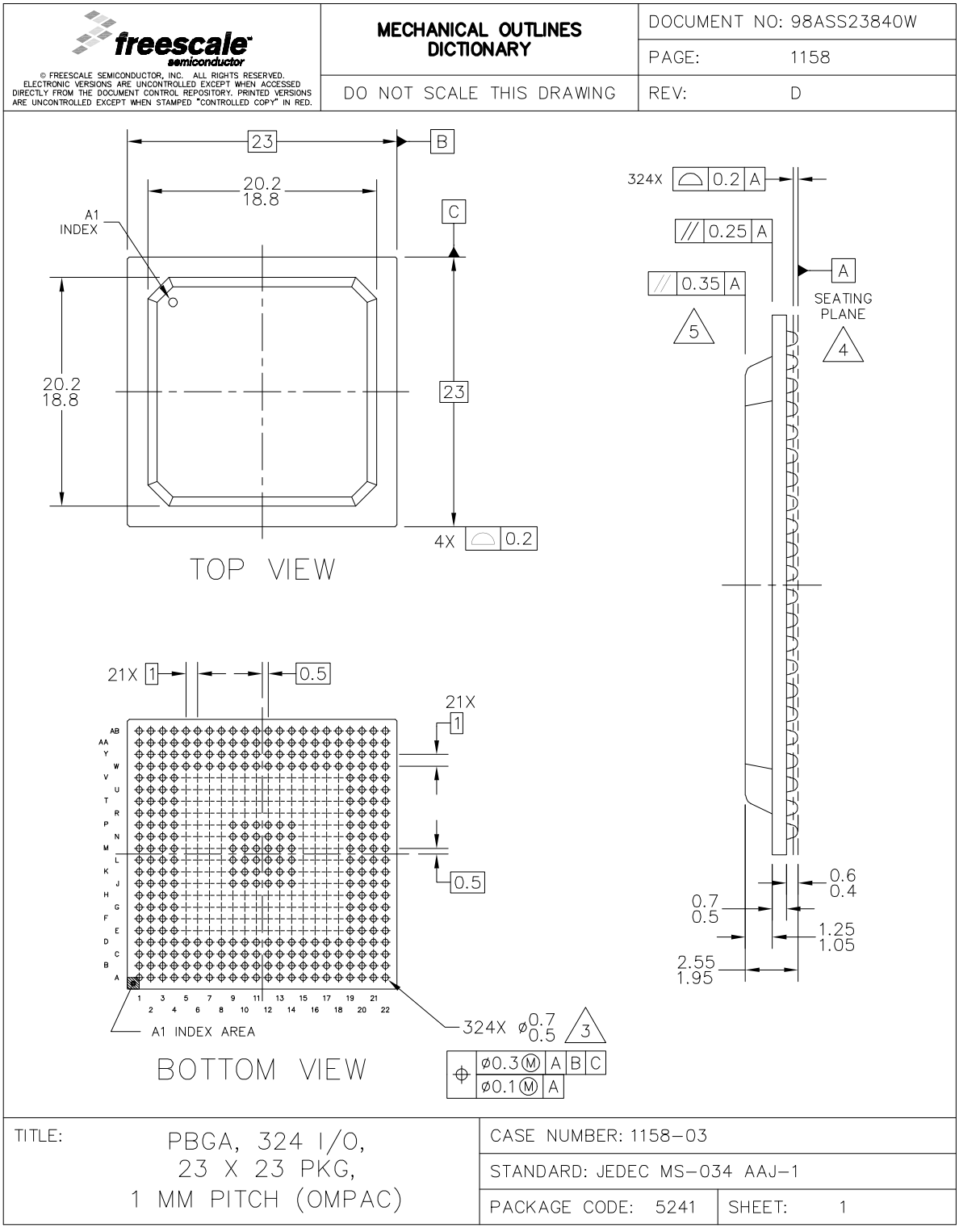


Figure 38. 324 BGA package mechanical drawing (part 1)

5 Ordering information

Table 52 shows the orderable part numbers for the MPC5644A series.

Table 52. Orderable part number summary

Part number	Flash/SRAM	Package	Speed (MHz)
SPC5643AF0MLU3	3 MB/192 KB	176LQFP (Pb free)	80
SPC5643AF0MMG3	3 MB/192 KB	208MAPBGA(Pb free)	80
SPC5643AF0MVZ3	3 MB/192 KB	324PBGA (Pb free)	80
SPC5643AF0MLU2	3 MB/192 KB	176LQFP (Pb free)	120
SPC5643AF0MMG2	3 MB/192 KB	208MAPBGA (Pb free)	120
SPC5643AF0MVZ2	3 MB/192 KB	324PBGA (Pb free)	120
SPC5643AF0MLU1	3 MB/192 KB	176LQFP (Pb free)	150
SPC5643AF0MMG1	3 MB/192 KB	208MAPBGA (Pb free)	150
SPC5643AF0MVZ1	3 MB/192 KB	324PBGA (Pb free)	150
SPC5644AF0MLU3	4 MB/192 KB	176 LQFP (Pb free)	80
SPC5644AF0MMG3	4 MB/192 KB	208 MAPBGA (Pb free)	80
SPC5644AF0MVZ3	4 MB/192 KB	324 TEPBGA (Pb free)	80
SPC5644AF0MLU2	4 MB/192 KB	176 LQFP (Pb free)	120
SPC5644AF0MMG2	4 MB/192 KB	208 MAPBGA (Pb free)	120
SPC5644AF0MVZ2	4 MB/192 KB	324 TEPBGA (Pb free)	120
SPC5644AF0MLU1	4 MB/192 KB	176 LQFP (Pb free)	150
SPC5644AF0MMG1	4 MB/192 KB	208 MAPBGA (Pb free)	150
SPC5644AF0MVZ1	4 MB/192 KB	324 TEPBGA (Pb free)	150

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