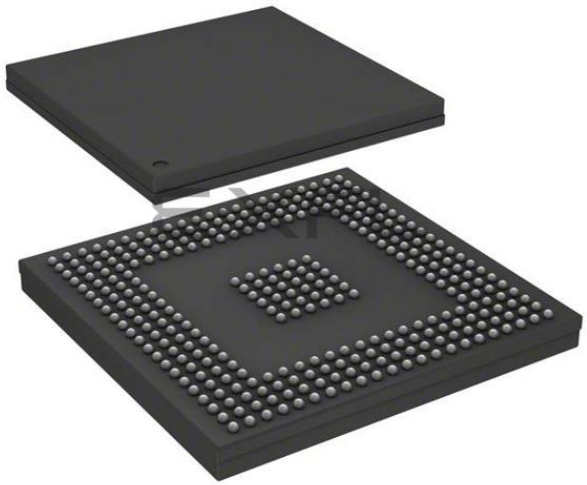

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	151
Program Memory Size	4MB (4M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	1.14V ~ 5.25V
Data Converters	A/D 40x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	324-BBGA
Supplier Device Package	324-PBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5644af0mvz2

- Supports serial bootloading via FlexCAN bus and eSCI with auto baud rate sensing
- Supports serial bootloading of either Power Architecture code (default) or Freescale VLE code
- Supports booting from calibration bus interface
- Supports censorship protection for internal flash memory
- Provides an option to enable the core watchdog timer
- Provides an option to disable the system watchdog timer

1.4.10 eMIOS

The eMIOS timer module provides the capability to generate or measure events in hardware.

The eMIOS module features include:

- Twenty-four 24-bit wide channels
- 3 channels' internal timebases can be shared between channels
- 1 Timebase from eTPU2 can be imported and used by the channels
- Global enable feature for all eMIOS and eTPU timebases
- Dedicated pin for each channel (not available on all package types)

Each channel (0–23) supports the following functions:

- General-purpose input/output (GPIO)
- Single-action input capture (SAIC)
- Single-action output compare (SAOC)
- Output pulse-width modulation buffered (OPWMB)
- Input period measurement (IPM)
- Input pulse-width measurement (IPWM)
- Double-action output compare (DAOC)
- Modulus counter buffered (MCB)
- Output pulse width and frequency modulation buffered (OPWFMB)

1.4.11 eTPU2

The eTPU2 is an enhanced co-processor designed for timing control. Operating in parallel with the host CPU, the eTPU2 processes instructions and real-time input events, performs output waveform generation, and accesses shared data without host intervention. Consequently, for each timer event, the host CPU setup and service times are minimized or eliminated. A powerful timer subsystem is formed by combining the eTPU2 with its own instruction and data RAM. High-level assembler/compiler and documentation allows customers to develop their own functions on the eTPU2.

MPC5644A devices feature the second generation of the eTPU, called eTPU2. Enhancements of the eTPU2 over the standard eTPU include:

- The Timer Counter (TCR1), channel logic and digital filters (both channel and the external timer clock input [TCRCLK]) now have an option to run at full system clock speed or system clock / 2.
- Channels support unordered transitions: transition 2 can now be detected before transition 1. Related to this enhancement, the transition detection latches (TDL1 and TDL2) can now be independently negated by microcode.
- A new User Programmable Channel Mode has been added: the blocking, enabling, service request and capture characteristics of this channel mode can be programmed via microcode.
- Microinstructions now provide an option to issue Interrupt and Data Transfer requests selected by channel. They can also be requested simultaneously at the same instruction.
- Channel Flags 0 and 1 can now be tested for branching, in addition to selecting the entry point.
- Channel digital filters can be bypassed.

  - Provides time stamp information when requested
  - Allows time stamp information relative to eTPU clock sources, such as an angle clock
  - Parallel interface to eQADC CFIFOs and RFIFOs
  - Supports both right-justified unsigned and signed formats for conversion results
- 40 single-ended input channels, expandable to 56 channels with external multiplexers (supports four external 8-to-1 muxes)
- 8 channels can be used as 4 pairs of differential analog input channels
- Differential channels include variable gain amplifier for improved dynamic range
- Differential channels include programmable pull-up and pull-down resistors for biasing and sensor diagnostics (200 kΩ, 100 kΩ, 5 kΩ)
- Additional internal channels for monitoring voltages (such as core voltage, I/O voltage, LVI voltages, etc.) inside the device
- An internal bandgap reference to allow absolute voltage measurements
- Silicon die temperature sensor
  - Provides temperature of silicon as an analog value
  - Read using an internal ADC analog channel
  - May be read with either ADC
- 2 Decimation Filters
  - Programmable decimation factor (1 to 16)
  - Selectable IIR or FIR filter
  - Up to 4th order IIR or 8th order FIR
  - Programmable coefficients
  - Saturated or non-saturated modes
  - Programmable Rounding (Convergent; Two's Complement; Truncated)
  - Prefill mode to precondition the filter before the sample window opens
  - Supports Multiple Cascading Decimation Filters to implement more complex filter designs
  - Optional Absolute Integrators on the output of Decimation Filters
- Full duplex synchronous serial interface to an external device
  - Free-running clock for use by an external device
  - Supports a 26-bit message length
- Priority based queues
  - Supports six queues with fixed priority. When commands of distinct queues are bound for the same ADC, the higher priority queue is always served first
  - Queue_0 can bypass all prioritization, buffering and abort current conversions to start a Queue_0 conversion a deterministic time after the queue trigger
  - Supports software and hardware trigger modes to arm a particular queue
  - Generates interrupt when command coherency is not achieved
- External hardware triggers
  - Supports rising edge, falling edge, high level and low level triggers
  - Supports configurable digital filter

1.4.14 DSPI

The deserial serial peripheral interface (DSPI) block provides a synchronous serial interface for communication between the MPC5644A MCU and external devices. The DSPI supports pin count reduction through serialization and deserialization of eTPU and eMIOS channels and memory-mapped registers. The channels and register content are transmitted using a SPI-like protocol. This SPI-like protocol is completely configurable for baud rate, polarity and phase, frame length, chip select assertion,

Table 3. MPC5644A signal properties (continued)

Name	Function[1]	PAG[2]	PCR PA Field[3]	PCR[4]	I/O Type	Voltage[5] / Pad Type[6]	Status[7]		Package pin #		
							During Reset	After Reset	176	208	324
CS[3] DSPI_D_SIN GPIO[99]	— DSPI D data input GPIO	— A1 G	— 10 00	99	— I I/O	VDDEH7 Medium	— / Up	— / Up	142	H13	B15
DSPI_A_PCS[4][17] DSPI_D_SOUT GPIO[100]	— DSPI D data output GPIO	— A1 G	— 10 00	100	O I/O	VDDEH7 Medium	— / Up	— / Up	—	—	B16
DSPI_A_PCS[5][17] DSPI_B_PCS[3] GPIO[101]	— DSPI B peripheral chip select GPIO	— A1 G	— 10 00	101	O I/O	VDDEH7 Medium	— / Up	— / Up	—	—	A16
DSPI_B_SCK DSPI_C_PCS[1] GPIO[102]	SPI clock pin for DSPI module DSPI C peripheral chip select GPIO	P A1 G	01 10 00	102	I/O O I/O	VDDEH6 Medium	— / Up	— / Up	106	J16	K21
DSPI_B_SIN DSPI_C_PCS[2] GPIO[103]	DSPI B data input DSPI C peripheral chip select GPIO	P A1 G	01 10 00	103	I O I/O	VDDEH6 Medium	— / Up	— / Up	112	G15	H22
DSPI_B_SOUT DSPI_C_PCS[5] GPIO[104]	DSPI B data output DSPI C peripheral chip select GPIO	P A1 G	01 10 00	104	O O I/O	VDDEH6 Medium	— / Up	— / Up	113	G13	J19
DSPI_B_PCS[0] DSPI_D_PCS[2] GPIO[105]	DSPI B peripheral chip select DSPI D peripheral chip select GPIO	P A1 G	01 10 00	105	I/O O I/O	VDDEH6 Medium	— / Up	— / Up	111	G16	J21
DSPI_B_PCS[1] DSPI_D_PCS[0] GPIO[106]	DSPI B peripheral chip select DSPI D peripheral chip select GPIO	P A1 G	01 10 00	106	O I/O I/O	VDDEH6 Medium	— / Up	— / Up	109	H16	J22
DSPI_B_PCS[2] DSPI_C_SOUT GPIO[107]	DSPI B peripheral chip select DSPI C data output GPIO	P A1 G	01 10 00	107	O O I/O	VDDEH6 Medium	— / Up	— / Up	107	H15	K22
DSPI_B_PCS[3] DSPI_C_SIN GPIO[108]	DSPI B peripheral chip select DSPI C data input GPIO	P A1 G	01 10 00	108	O I I/O	VDDEH6 Medium	— / Up	— / Up	114	G14	J20
DSPI_B_PCS[4] DSPI_C_SCK GPIO[109]	DSPI B peripheral chip select SPI clock pin for DSPI module GPIO	P A1 G	01 10 00	109	O I/O I/O	VDDEH6 Medium	— / Up	— / Up	105	H14	K20
DSPI_B_PCS[5] DSPI_C_PCS[0] GPIO[110]	DSPI B peripheral chip select DSPI C peripheral chip select GPIO	P A1 G	01 10 00	110	O I/O I/O	VDDEH6 Medium	— / Up	— / Up	104	J13	L19

Table 3. MPC5644A signal properties (continued)

Name	Function[1]	PAG[2]	PCR PA Field[3]	PCR[4]	I/O Type	Voltage[5] / Pad Type[6]	Status[7]		Package pin #		
							During Reset	After Reset	176	208	324
ETPUA17 DSPI_D_PCS[2] RCH3_A GPIO[131]	eTPU A channel DSPI D peripheral chip select Reaction channel 3A GPIO	P A1 A2 G	001 010 100 000	131	I/O O O I/O	VDDEH1 Slow	— / WKPCFG	— / WKPCFG	38	H3	Y1
ETPUA18 DSPI_D_PCS[3] RCH4_A GPIO[132]	eTPU A channel DSPI D peripheral chip select Reaction channel 4A GPIO	P A1 A2 G	001 010 100 000	132	I/O O O I/O	VDDEH1 Slow	— / WKPCFG	— / WKPCFG	37	H4	W3
ETPUA19 DSPI_D_PCS[4] RCH5_A GPIO[133]	eTPU A channel DSPI D peripheral chip select Reaction channel 5A GPIO	P A1 A2 G	001 010 100 000	133	I/O O O I/O	VDDEH1 Slow	— / WKPCFG	— / WKPCFG	36	J2	W2
ETPUA20 IRQ[8] RCH0_B FR_A_TX GPIO[134]	eTPU A channel External interrupt request Reaction channel 0B Flexray TX data channel A GPIO	P A1 A2 A3 G	0001 0010 0100 1000 0000	134	I/O I O O I/O	VDDEH1 Slow	— / WKPCFG	— / WKPCFG	35	J1	W1
ETPUA21 IRQ[9] RCH0_C FR_A_RX GPIO[135]	eTPU A channel External interrupt request Reaction channel 0C Flexray RX channel A GPIO	P A1 A2 A3 G	0001 0010 0100 1000 0000	135	I/O I O I I/O	VDDEH1 Slow	— / WKPCFG	— / WKPCFG	34	G4	N4
ETPUA22 IRQ[10] ETPUA17_O[8] GPIO[136]	eTPU A channel External interrupt request eTPU A channel (output only) GPIO	P A1 A2 G	001 010 100 000	136	I/O I O I/O	VDDEH1 Slow	— / WKPCFG	— / WKPCFG	32	H2	N3
ETPUA23 IRQ[11] ETPUA21_O[8] FR_A_TX_EN GPIO[137]	eTPU A channel External interrupt request eTPU A channel (output only) Flexray ch. A TX enable GPIO	P A1 A2 A3 G	0001 0010 0100 1000 0000	137	I/O I O O I/O	VDDEH1 Slow	— / WKPCFG	— / WKPCFG	30	H1	M1
ETPUA24 IRQ[12] DSPI_C_SCK_LV DS- GPIO[138]	eTPU A channel External interrupt request LVDS negative DSPI clock GPIO	P A1 A2 G	001 010 100 000	138	I/O I O I/O	VDDEH1 Slow + LVDS	— / WKPCFG	— / WKPCFG	28	G1	M2

Table 3. MPC5644A signal properties (continued)

Name	Function[1]	PAG[2]	PCR PA Field[3]	PCR[4]	I/O Type	Voltage[5] / Pad Type[6]	Status[7]		Package pin #		
							During Reset	After Reset	176	208	324
EMIOS11 DSPI_D_PCS[4] RCH3_C GPIO[190]	eMIOS channel DSPI D peripheral chip select Reaction channel 3C GPIO	P A1 A2 G	001 010 100 000	190	I/O O O I/O	VDDEH4 Medium	— / WKPCFG	— / WKPCFG	75	R8	AB15
EMIOS12 DSPI_C_SOUT ETPUA27_O[8] GPIO[191]	eMIOS channel DSPI C data output eTPU A channel (output only) GPIO	P A1 A2 G	001 010 100 000	191	I/O O O I/O	VDDEH4 Medium	— / WKPCFG	— / WKPCFG	76	N10	AB16
EMIOS13 DSPI_D_SOUT GPIO[192]	eMIOS channel DSPI D data output GPIO	P A1 G	01 10 00	192	I/O O I/O	VDDEH4 Medium	— / WKPCFG	— / WKPCFG	77	T8	AA16
EMIOS14 IRQ[0] ETPUA29_O[8] GPIO[193]	eMIOS channel External interrupt request eTPU A channel (output only) GPIO	P A1 A2 G	001 010 100 000	193	I/O I O I/O	VDDEH4 Slow	— / Down	— / Down	78	R9	Y16
EMIOS15 IRQ[1] GPIO[194]	eMIOS channel External interrupt request GPIO	P A1 G	01 10 00	194	I/O I I/O	VDDEH4 Slow	— / Down	— / Down	79	T9	W16
EMIOS16 GPIO[195]	eMIOS channel GPIO	P G	01 00	195	I/O I/O	VDDEH4 Slow	— / Up	— / Up	—	—	W17
EMIOS17 GPIO[196]	eMIOS channel GPIO	P G	01 00	196	I/O I/O	VDDEH4 Slow	— / Up	— / Up	—	—	Y17
EMIOS18 GPIO[197]	eMIOS channel GPIO	P G	01 00	197	I/O I/O	VDDEH4 Slow	— / Up	— / Up	—	—	AA17
EMIOS19 GPIO[198]	eMIOS channel GPIO	P G	01 00	198	I/O I/O	VDDEH4 Slow	— / WKPCFG	— / WKPCFG	—	—	AB17
EMIOS20 GPIO[199]	eMIOS channel GPIO	P G	01 00	199	I/O I/O	VDDEH4 Slow	— / WKPCFG	— / WKPCFG	—	—	AB18
EMIOS21 GPIO[200]	eMIOS channel GPIO	P G	01 00	200	I/O I/O	VDDEH4 Slow	— / WKPCFG	— / WKPCFG	—	—	AA18
EMIOS22 GPIO[201]	eMIOS channel GPIO	P G	01 00	201	I/O I/O	VDDEH4 Slow	— / Down	— / Down	—	—	Y18
EMIOS23 GPIO[202]	eMIOS channel GPIO	P G	01 00	202	I/O I/O	VDDEH4 Slow	— / Down	— / Down	80	R11	W18
Clock Synthesizer											

Table 5. Signal details (continued)

Signal	Module or Function	Description
BOOTCFG[0:1]	SIU - Configuration	Two BOOTCFG signals are implemented in MPC5644A MCUs. The BAM program uses the BOOTCFG0 bit to determine where to read the reset configuration word, and whether to initiate a FlexCAN or eSCI boot. The BOOTCFG1 pin is sampled during the assertion of the RSTOUT signal, and the value is used to update the RSR and the BAM boot mode See the *MPC5644A Microcontroller Reference Manual* for more information. The following values are for BOOTCFG[0:1}: 00:Boot from internal flash memory 01:FlexCAN/eSCI boot 10:Boot from external memory using EBI 11:Reserved Note: For the 176-pin QFP and 208-ball BGA packages BOOTCFG[0] is always 0 since the EBI interface is not available.
WKPCFG	SIU - Configuration	The WKPCFG pin is applied at the assertion of the internal reset signal (assertion of $\overline{\text{RSTOUT}}$), and is sampled 4 clock cycles before the negation of the $\overline{\text{RSTOUT}}$ pin. The value is used to configure whether the eTPU and eMIOS pins are connected to internal weak pull up or weak pull down devices after reset. The value latched on the WKPCFG pin at reset is stored in the Reset Status Register (RSR), and is updated for all reset sources except the Debug Port Reset and Software External Reset. 0: Weak pulldown applied to eTPU and eMIOS pins at reset 1: Weak pullup applied to eTPU and eMIOS pins at reset.
ETRIG[2:3]	SIU - eQADC Triggers	External signal eTRIGx triggers eQADC CFIFOx
GPIO[206] ETRIG0 (Input)	SIU - eQADC Triggers	External signal eTRIGx triggers eQADC CFIFOx
GPIO[207] ETRIG1 (Input)	SIU - eQADC Triggers	External signal eTRIGx triggers eQADC CFIFOx
$\overline{\text{IRQ}}$[0:5] $\overline{\text{IRQ}}$[7:15]	SIU - External Interrupts	The $\overline{\text{IRQ}}$[0:15] pins connect to the SIU IRQ inputs. IMUX Select Register 1 is used to select the $\overline{\text{IRQ}}$[0:15] pins as inputs to the IRQs. See the *MPC5644A Microcontroller Reference Manual* for more information.
$\overline{\text{NMI}}$	SIU - External Interrupts	Non-Maskable Interrupt

Table 6. Power/ground segmentation

Power Segment	Voltage	I/O Pins Powered by Segment
VDDA	5 V	AN0, AN1, AN2, AN3, AN4, AN5, AN6, AN7, AN8, AN9, AN10, AN11, AN16, AN17, AN18, AN19, AN20, AN21, AN22, AN23, AN24, AN25, AN26, AN27, AN28, AN29, AN30, AN31, AN32, AN33, AN34, AN35, AN36, AN37, AN38, AN39, VRH, VRL, REFBYBC
VRC33[1]	3.3 V	MCKO, MDO0, MDO1, MDO2, MDO3
Other Power Segments		
VDDREG	5 V	—
VRCCTL	—	—
VDDPLL	1.2 V	—
VSTBY	0.95–1.2 V (unregulated mode)	—
	2.0–5.5 V (regulated mode)	—
VSS	—	—

[1] Do not use VRC33 to drive external circuits.

Table 8. Absolute maximum ratings[1] (continued)

Symbol		Parameter	Conditions	Value		Unit
				min	max	
V_{DDA}	SR	Analog supply voltage[5]	Reference to V_{SSA}	–0.3	5.5	V
V_{DDE}	SR	I/O supply voltage[4,6]		–0.3	3.6	V
V_{DDEH}	SR	I/O supply voltage[5]		–0.3	5.5	V
V_{IN}	SR	DC input voltage[7]	V_{DDEH} powered I/O pads	–1.0[8]	V_{DDEH} + 0.3 V[9]	V
			V_{DDE} powered I/O pads	–1.0[10]	V_{DDE} + 0.3 V[10]	
			V_{DDA} powered I/O pads	–1.0	5.5	
V_{DDREG}	SR	Voltage regulator supply voltage		–0.3	5.5	V
V_{RH}	SR	Analog reference high voltage	Reference to VRL	–0.3	5.5	V
$V_{SS} – V_{SSA}$	SR	V_{SS} differential voltage		–0.1	0.1	V
$V_{RH} – V_{RL}$	SR	V_{REF} differential voltage		–0.3	5.5	V
$V_{RL} – V_{SSA}$	SR	VRL to V_{SSA} differential voltage		–0.3	0.3	V
$V_{SSPLL} – V_{SS}$	SR	V_{SSPLL} to V_{SS} differential voltage		–0.1	0.1	V
I_{MAXD}	SR	Maximum DC digital input current[11]	Per pin, applies to all digital pins	–3	3	mA
I_{MAXA}	SR	Maximum DC analog input current[12]	Per pin, applies to all analog pins	—	5	mA
T_J	SR	Maximum operating temperature range - die junction temperature		–40.0	150.0	°C
T_{STG}	SR	Storage temperature range		–55.0	150.0	°C
T_{SDR}	SR	Maximum solder temperature[13]		—	260.0	°C
MSL	SR	Moisture sensitivity level[14]		—	3	

1 Functional operating conditions are given in the DC electrical specifications. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the listed maxima may affect device reliability or cause permanent damage to the device.

2 Allowed 2 V for 10 hours cumulative time, remaining time at 1.2 V +10%.

3 The V_{FLASH} supply is connected to V_{RC33} in the package substrate. This specification applies to calibration package devices only.

4 Allowed 5.3 V for 10 hours cumulative time, remaining time at 3.3 V +10%.

5 Allowed 5.9 V for 10 hours cumulative time, remaining time at 5 V +10%.

[6] All functional non-supply I/O pins are clamped to V_{SS} and V_{DDE}, or V_{DDEH}.

[7] AC signal overshoot and undershoot of up to 2.0 V of the input voltages is permitted for an accumulative duration of 60 hours over the complete lifetime of the device (injection current not limited for this duration).

[8] Internal structures hold the voltage greater than –1.0 V if the injection current limit of 2 mA is met.

[9] Internal structures hold the input voltage less than the maximum voltage on all pads powered by V_{DDEH} supplies, if the maximum injection current specification is met (2 mA for all pins) and V_{DDEH} is within the operating voltage specifications.

[10] Internal structures hold the input voltage less than the maximum voltage on all pads powered by V_{DDE} supplies, if the maximum injection current specification is met (2 mA for all pins) and V_{DDE} is within the operating voltage specifications.

[11] Total injection current for all pins (including both digital and analog) must not exceed 25 mA.

[12] Total injection current for all analog input pins must not exceed 15 mA.

[13] Solder profile per IPC/JEDEC J-STD-020D.

[14] Moisture sensitivity per JEDEC test method A112.

3.3 Thermal characteristics

Table 9. Thermal characteristics for 176-pin QFP[1]

Symbol		C	Parameter	Conditions	Value	Unit
$R_{\theta JA}$	CC	D	Junction-to-Ambient, Natural Convection[2]	Single layer board - 1s	38	°C/W
$R_{\theta JA}$	CC	D	Junction-to-Ambient, Natural Convection[2]	Four layer board - 2s2p	31	°C/W
$R_{\theta JMA}$	CC	D	Junction-to-Moving-Air, Ambient[2]	200 ft./min., single layer board - 1s	30	°C/W
$R_{\theta JMA}$	CC	D	Junction-to-Moving-Air, Ambient[2]	at 200 ft./min., four layer board - 2s2p	25	°C/W
$R_{\theta JB}$	CC	D	Junction-to-Board[3]		20	°C/W
$R_{\theta JCtop}$	CC	D	Junction-to-Case[4]		5	°C/W
Ψ_{JT}	CC	D	Junction-to-Package Top, Natural Convection[5]		2	°C/W

[1] Thermal characteristics are targets based on simulation that are subject to change per device characterization.

[2] Junction-to-Ambient Thermal Resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.

[3] Junction-to-Board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.

[4] Junction-to-Case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

[5] Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

The thermal resistance is expressed as the sum of a junction-to-case thermal resistance plus a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA} \quad \textit{Eqn. 3}$$

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance ($^oC/W$)
$R_{\theta JC}$ = junction-to-case thermal resistance ($^oC/W$)
$R_{\theta CA}$ = case to ambient thermal resistance ($^oC/W$)

$R_{\theta JC}$ is device related and is not affected by other factors. The thermal environment can be controlled to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For example, change the air flow around the device, add a heat sink, change the mounting arrangement on the printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device. This description is most useful for packages with heat sinks where 90% of the heat flow is through the case to heat sink to ambient. For most packages, a better model is required.

A more accurate two-resistor thermal model can be constructed from the junction-to-board thermal resistance and the junction-to-case thermal resistance. The junction-to-case thermal resistance describes when using a heat sink or where a substantial amount of heat is dissipated from the top of the package. The junction-to-board thermal resistance describes the thermal performance when most of the heat is conducted to the printed circuit board. This model can be used to generate simple estimations and for computational fluid dynamics (CFD) thermal models.

To determine the junction temperature of the device in the application on a prototype board, use the thermal characterization parameter (Ψ_{JT}) to determine the junction temperature by measuring the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D) \quad \textit{Eqn. 4}$$

where:

T_T = thermocouple temperature on top of the package (^oC)
Ψ_{JT} = thermal characterization parameter ($^oC/W$)
P_D = power dissipation in the package (W)

The thermal characterization parameter is measured in compliance with the JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. Position the thermocouple so that the thermocouple junction rests on the package. Place a small amount of epoxy on the thermocouple junction and approximately 1 mm of wire extending from the junction. Place the thermocouple wire flat against the package case to avoid measurement errors caused by the cooling effects of the thermocouple wire.

References:

Semiconductor Equipment and Materials International

3081 Zanker Road
San Jose, CA 95134
USA
(408) 943-6900

MIL-SPEC and EIA/JESD (JEDEC) specifications are available from Global Engineering Documents at 800-854-7179 or 303-397-7956.

JEDEC specifications are available on the WEB at http://www.jedec.org.

- C.E. Triplett and B. Joiner, “An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module,” Proceedings of SemiTherm, San Diego, 1998, pp. 47-54.
- G. Kromann, S. Shidore, and S. Addison, “Thermal Modeling of a PBGA for Air-Cooled Applications”, Electronic Packaging and Production, pp. 53-58, March 1998.

[2] Device failure is defined as: “If after exposure to ESD pulses, the device does not meet the device specification requirements, which includes the complete DC parametric and functional testing at room temperature and hot temperature.”

3.6 Power management control (PMC) and power on reset (POR) electrical specifications

Table 14. PMC Operating Conditions and External Regulators Supply Voltage

ID	Name			Parameter	Min	Typ	Max	Unit
1	Jtemp	SR	—	Junction temperature	–40	27	150	°C
2	Vddreg	SR	—	PMC 5 V supply voltage V_{DDREG}	4.75	5	5.25	V
3	Vdd	SR	—	Core supply voltage 1.2 V V_{DD} when external regulator is used without disabling the internal regulator (PMC unit turned on, LVI monitor active)[1]	1.26[2]	1.3	1.32	V
3a	—	SR	—	Core supply voltage 1.2 V V_{DD} when external regulator is used with a disabled internal regulator (PMC unit turned-off, LVI monitor disabled)	1.14	1.2	1.32	V
4	Ivdd	SR	—	Voltage regulator core supply maximum required DC output current	400	—	—	mA
5	Vdd33	SR	—	Regulated 3.3 V supply voltage when external regulator is used without disabling the internal regulator (PMC unit turned-on, internal 3.3V regulator enabled, LVI monitor active)[3]	3.3	3.45	3.6	V
5a	—	SR	—	Regulated 3.3 V supply voltage when external regulator is used with a disabled internal regulator (PMC unit turned-off, LVI monitor disabled)	3	3.3	3.6	V
6	—	SR	—	Voltage regulator 3.3 V supply maximum required DC output current	80	—	—	mA

[1] An internal regulator controller can be used to regulate core supply.

[2] The minimum supply required for the part to exit reset and enter in normal run mode is 1.28 V.

[3] An internal regulator can be used to regulate 3.3 V supply.

Table 20. Power sequence pin states (medium, slow, and multi-voltage pads)

V_{DDEH}	V_{DD}	Pad State
LOW	X	LOW
V_{DDEH}	LOW	HIGH IMPEDANCE
V_{DDEH}	V_{DD}	FUNCTIONAL

3.8 DC electrical specifications

Table 21. DC electrical specifications

Symbol		C	Parameter	Conditions	Value			Unit
					min	typ	max	
V_{DD}	SR	—	Core supply voltage	—	1.14		1.32	V
V_{DDE}	SR	—	I/O supply voltage	—	1.62		3.6	V
V_{DDEH}	SR	—	I/O supply voltage	—	3.0		5.25	V
V_{DDE-EH}	SR	—	I/O supply voltage	—	3.0		5.25	V
V_{RC33}	SR	—	3.3 V regulated voltage[1]	—	3.0	—	3.6	V
V_{DDA}	SR	—	Analog supply voltage	—	4.75[2]	—	5.25	V
V_{INDC}	SR	—	Analog input voltage	—	V_{SSA}-0.3	—	V_{DDA}+0.3	V
$V_{SS} – V_{SSA}$	SR	—	V_{SS} differential voltage	—	–100	—	100	mV
V_{RL}	SR	—	Analog reference low voltage	—	V_{SSA}	—	V_{SSA}+0.1	V
$V_{RL} – V_{SSA}$	SR	—	VRL differential voltage	—	–100	—	100	mV
V_{RH}	SR	—	Analog reference high voltage	—	V_{DDA}-0.1	—	V_{DDA}	V
$V_{RH} – V_{RL}$	SR	—	V_{REF} differential voltage	—	4.75	—	5.25	V
V_{DDF}	SR	—	Flash operating voltage[3]	—	1.14	—	1.32	V
V_{FLASH}[4]	SR	—	Flash read voltage	—	3.0	—	3.6	V
V_{STBY}	SR	—	SRAM standby voltage	Unregulated mode	0.95	—	1.2	V
			Keep-out Range: 1.2V–2V	Regulated mode	2.0	—	5.5	

Table 21. DC electrical specifications (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					min	typ	max	
V_{DDREG}	SR	—	Voltage regulator supply voltage	—	4.75	—	5.25	V
V_{DDPLL}	SR	—	Clock synthesizer operating voltage	—	1.14	—	1.32	V
V_{SSPLL} – V_{SS}	SR	—	V_{SSPLL} to V_{SS} differential voltage	—	–100	—	100	mV
V_{IL_S}	CC	C	Slow/medium I/O pad input low voltage	Hysteresis enabled	V_{SS}-0.3	—	0.35*V_{DDEH}	V
		P		Hysteresis disabled	V_{SS}-0.3	—	0.40*V_{DDEH}	
V_{IL_F}	CC	C	Fast pad I/O input low voltage	Hysteresis enabled	V_{SS}-0.3	—	0.35*V_{DDE}	V
		P		Hysteresis disabled	V_{SS}-0.3	—	0.40*V_{DDE}	
V_{IL_LS}	CC	C	Multi-voltage I/O pad input low voltage in Low-swing-mode[5,6,7,8]	Hysteresis enabled	V_{SS}-0.3	—	0.8	V
		P		Hysteresis disabled	V_{SS}-0.3	—	1.1	
V_{IL_HS}	CC	C	Multi-voltage pad I/O input low voltage in high-swing-mode	Hysteresis enabled	V_{SS}-0.3	—	0.35 V_{DDEH}	V
		P		Hysteresis disabled	V_{SS}-0.3	—	0.4 V_{DDEH}	
V_{IH_S}	CC	C	Slow/medium pad I/O input high voltage[9]	Hysteresis enabled	0.65 V_{DDEH}	—	V_{DDEH}+0.3	V
		P		Hysteresis disabled	0.55 V_{DDEH}	—	V_{DDEH}+0.3	
V_{IH_F}	CC	C	Fast I/O input high voltage	Hysteresis enabled	0.65 V_{DDE}	—	V_{DDE}+0.3	V
		P		Hysteresis disabled	0.58 V_{DDE}	—	V_{DDE}+0.3	
V_{IH_LS}	CC	C	Multi-voltage pad I/O input high voltage in low-swing-mode[5,6,7,8]	Hysteresis enabled	2.5	—	V_{DDEH}+0.3	V
		P		Hysteresis disabled	2.2	—	V_{DDEH}+0.3	
V_{IH_HS}	CC	C	Multi-voltage I/O input high voltage in high-swing-mode	Hysteresis enabled	0.65 V_{DDEH}	—	V_{DDEH}+0.3	V
		P		Hysteresis disabled	0.55 V_{DDEH}	—	V_{DDEH}+0.3	

Table 21. DC electrical specifications (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					min	typ	max	
I_{DDSTBY}	CC	T	Operating current 0.95-1.2 V	V_{STBY} at 55 °C	—	35	100	µA
		T	Operating current 2–5.5 V	V_{STBY} at 55 °C	—	45	110	µA
$I_{DDSTBY27}$	CC	P	Operating current 0.95-1.2 V	V_{STBY} 27 °C		25	90	µA
		P	Operating current 2-5.5 V	V_{STBY} 27 °C		35	100	µA
$I_{DDSTBY150}$	CC	P	Operating current 0.95-1.2 V	V_{STBY} 150 °C	—	790	2000	µA
		P	Operating current 2–5.5 V	V_{STBY} at 150 °C	—	760	2000	µA
I_{DDPLL}	CC	P	Operating current 1.2 V supplies	V_{DDPLL}, 80 MHz, V_{DD}=1.2 V	—		15	mA
I_{DDSLOW} I_{DDSTOP}	CC	P	V_{DD} low-power mode operating current at 1.32 V	Slow mode[10]	—		90	mA
		P		Stop mode[11]	—		75	
I_{DD33}	CC	C	Operating current 3.3 V supplies	V_{RC33}[1,12]	—		60	mA
I_{DDA} I_{REF} I_{DDREG}	CC	P	Operating current 5.0 V supplies	V_{DDA}	—	—	30.0	mA
		P		Analog reference supply current (transient)	—	—	1.0	
		C		V_{DDREG}	—	—	70[13]	
I_{DDH1} I_{DDH4} I_{DDH6} I_{DDH7} I_{DD7} I_{DDH9} I_{DD12}	CC	D	Operating current V_{DDE}[14] supplies	V_{DDEH1}	—	—	See note [14]	mA
		D		V_{DDEH4}	—	—		
		D		V_{DDEH6}	—	—		
		D		V_{DDEH7}	—	—		
		D		V_{DDE7}	—	—		
		D		V_{DDEH9}	—	—		
		D		V_{DDE12}	—	—		

Table 21. DC electrical specifications (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					min	typ	max	
I_{ACT_S}	CC	C	Slow/medium I/O weak pull up/down current[15]	3.0 V – 3.6 V	15	—	95	µA
		P		4.75 V – 5.5 V	35	—	200	
I_{ACT_F}	CC	D	Fast I/O weak pull up/down current[15]	1.62 V – 1.98 V	36	—	120	µA
		D		2.25 V – 2.75 V	34	—	139	
		D		3.0 V – 3.6 V	42	—	158	
$I_{ACT\_MV\_PU}$	CC	C	Multi-voltage pad weak pullup current	V_{DDE}= 3.0–3.6 V[5], MultiV pad, high swing mode only	10	—	75	µA
		P		4.75 V – 5.25 V	25	—	200	
$I_{ACT\_MV\_PD}$	CC	C	Multivoltage pad weak pulldown current	V_{DDE}= 3.0–3.6 V[5], MultiV pad, high swing mode only	10	—	60	µA
		P		4.75 V – 5.25 V	25	—	200	
I_{INACT_D}	CC	P	I/O input leakage current[16]	—	–2.5	—	2.5	µA
I_{IC}	SR	T	DC injection current (per pin)	—	–1.0	—	1.0	mA
I_{INACT_A}	SR	P	Analog input current, channel off, AN[0:7][17]	—	–250	—	250	nA
		P	Analog input current, channel off, all other analog pins[17]	—	–150	—	150	

Table 24. V_{RC33} pad average DC current[1]

Pad Type	Symbol		C	Period (ns)	Load[2] (pF)	V_{RC33} (V)	V_{DDE} (V)	Drive Select	I_{DD33} Avg (µA)	I_{DD33} RMS (µA)
Fast	I_{DRV_FC}	CC	D	10	50	3.6	3.6	11	2.35	6.12
		CC	D	10	30	3.6	3.6	10	1.75	4.3
		CC	D	10	20	3.6	3.6	01	1.41	3.43
		CC	D	10	10	3.6	3.6	00	1.06	2.9
		CC	D	10	50	3.6	1.98	11	1.75	4.56
		CC	D	10	30	3.6	1.98	10	1.32	3.44
		CC	D	10	20	3.6	1.98	01	1.14	2.95
		CC	D	10	10	3.6	1.98	00	0.95	2.62

1 These are typical values that are estimated from simulation and not tested. Currents apply to output pins only.

2 All loads are lumped.

3.9.2 LVDS pad specifications

LVDS pads are implemented to support the MSC (Microsecond Channel) protocol which is an enhanced feature of the DSPI module. The LVDS pads are compliant with LVDS specifications and support data rates up to 50 MHz.

Table 25. DSPI LVDS pad specification

#	Characteristic	Symbol	C		Condition	Min. Value	Typ. Value	Max. Value	Unit
Data Rate									
4	Data Frequency	$f_{LVDSCLK}$	CC	D	—		50		MHz
Driver Specs									
5	Differential output voltage	V_{OD}	CC	P	SRC=0b00 or 0b11	150		400	mV
			CC	P	SRC=0b01	90		320	
			CC	P	SRC=0b10	160		480	
6	Common mode voltage (LVDS), VOS	V_{OD}	CC	P		1.06	1.2	1.39	V
7	Rise/Fall time	T_R/T_F	CC	D	—		2		ns
8	Propagation delay (Low to High)	T_{PLH}	CC	D			4		ns
9	Propagation delay (High to Low)	T_{PHL}	CC	D	—		4		ns
10	Delay (H/L), sync Mode	t_{PDSYNC}	CC	D			4		ns

3.13 Configuring SRAM wait states

Use the SWSC field in the ECSM_MUDCR register to specify an additional wait state for the device SRAM. By default, no wait state is added.

Table 31. Cutoff frequency for additional SRAM wait state

[1]	SWSC Value
98	0
153	1

[1] Max frequencies including 2% PLL FM.

Please see the device reference manual for details.

3.14 Platform flash controller electrical characteristics

Table 32. APC, RWSC, WWSC settings vs. frequency of operation[1,2]

Max. Flash Operating Frequency (MHz)[3]	APC[4]	RWSC[4]	WWSC
20 MHz	0b000	0b000	0b11
61 MHz	0b001	0b001	0b11
90 MHz	0b010	0b010	0b11
123 MHz	0b011	0b011	0b11
153 MHz	0b100	0b100	0b11

[1] APC, RWSC and WWSC are fields in the flash memory BIUCR register used to specify wait states for address pipelining and read/write accesses. Illegal combinations exist—all entries must be taken from the same row.

[2] TBD: To Be Defined.

[3] Max frequencies including 2% PLL FM.

[4] APC must be equal to RWSC.

3.15 Flash memory electrical characteristics

Table 33. Flash program and erase specifications[1]

#	Symbol		C	Parameter	Min. Value	Typical Value	Initial Max[2]	Max[3]	Unit
1	$T_{dwprogram}$	CC	P	Double Word (64 bits) Program Time	—	38	—	500	µs
2	$T_{pprogram}$	CC	P	Page Program Time	—	45	160[4]	500	µs
3	$T_{16kpperase}$	CC	P	16 KB Block Pre-program and Erase Time	—	270	1000	5000	ms
5	$T_{64kpperase}$	CC	P	64 KB Block Pre-program and Erase Time	—	800	1800	5000	ms

[4] The actual minimum SCK cycle time is limited by pad performance.

[5] For DSPI channels using LVDS output operation, up to 40 MHz SCK cycle time is supported. For non-LVDS output, maximum SCK frequency is 20 MHz. Appropriate clock division must be applied.

[6] The maximum value is programmable in DSPI_CTARx[PSSCK] and DSPI_CTARx[CSSCK].

[7] Timing met when pcssck = 3(01), and cssck =2 (0000).

[8] The maximum value is programmable in DSPI_CTARx[PASC] and DSPI_CTARx[ASC].

[9] Timing met when ASC = 2 (0000), and PASC = 3 (01).

[10] Timing met when pcssck = 3.

[11] Timing met when ASC = 3.

[12] This number is calculated assuming the SMPL_PT bitfield in DSPI_MCR is set to 0b10.

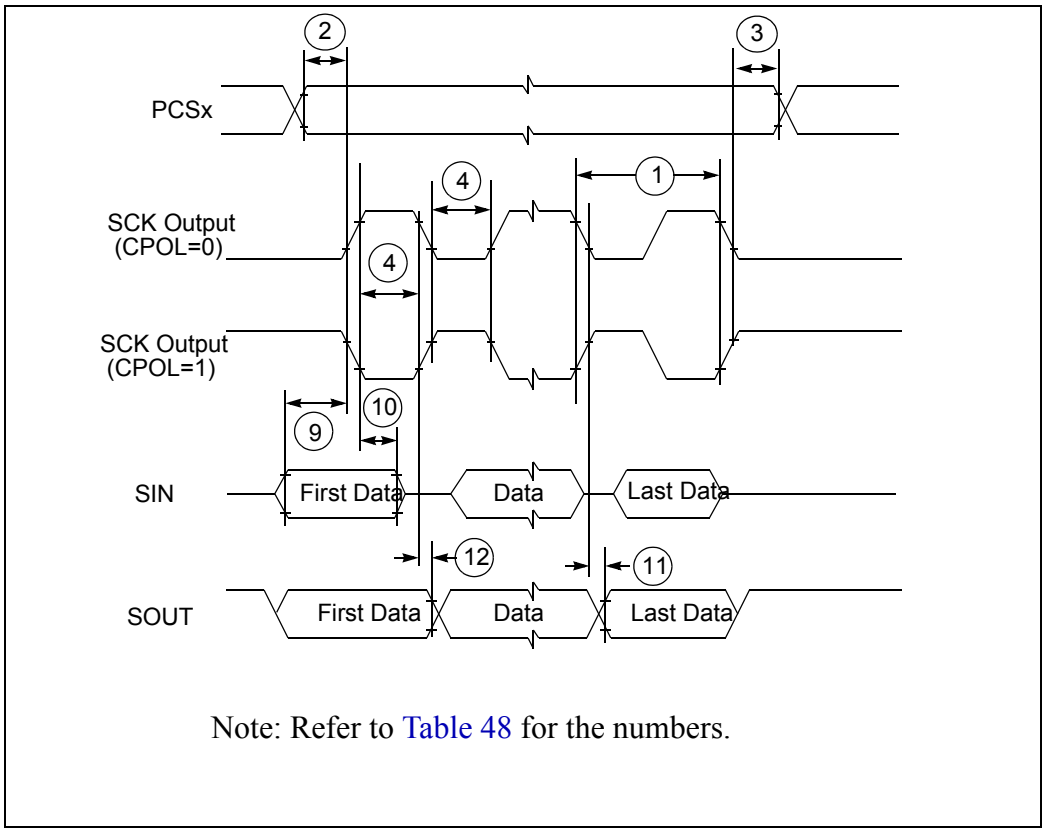

Figure 23. DSPI classic SPI timing — master, CPHA = 0

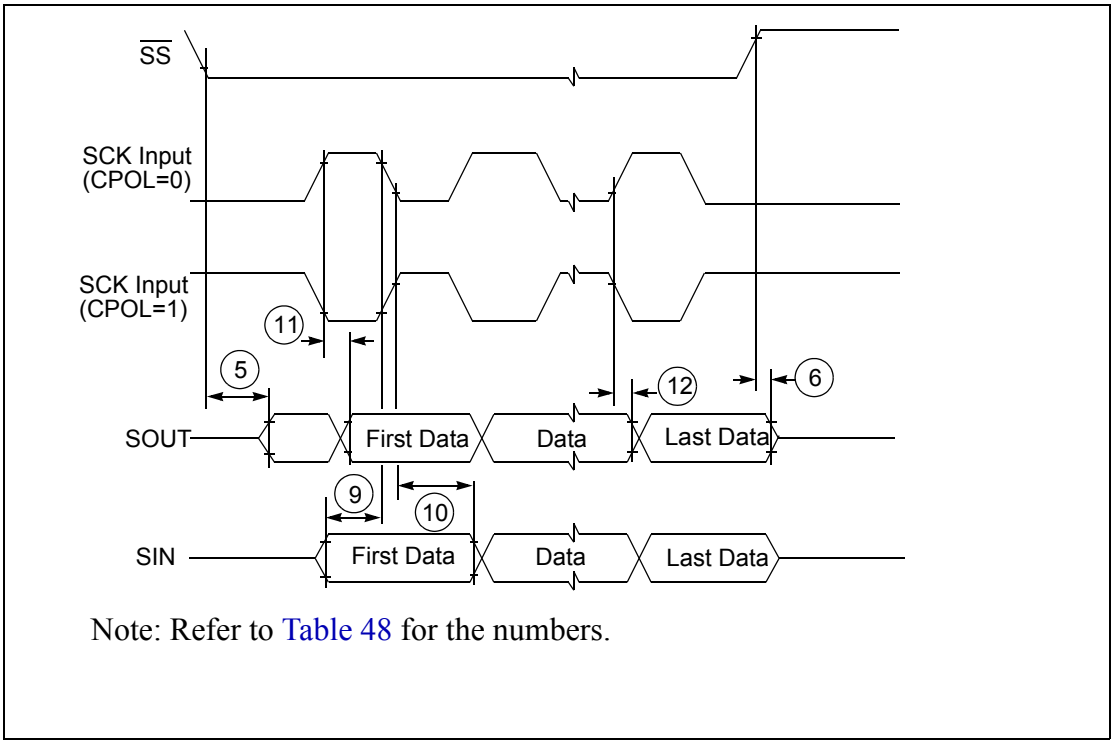

Figure 30. DSPI modified transfer format timing — slave, CPHA =1

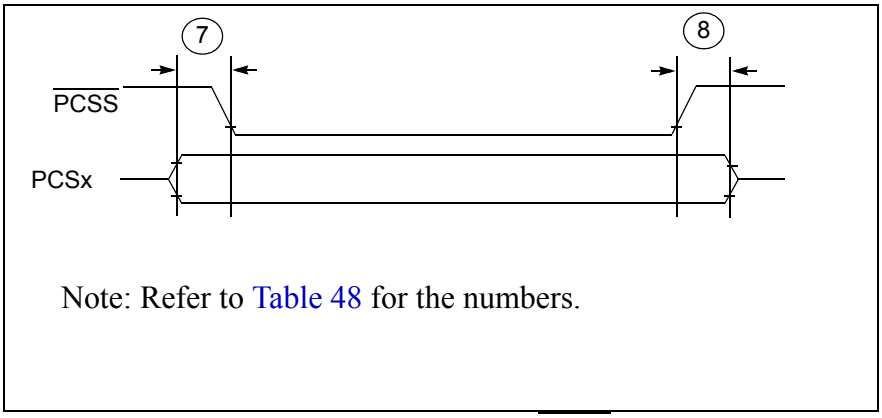

Figure 31. DSPI PCS strobe (PCSS) timing

3.17.9 eQADC SSI timing

Table 49. eQADC SSI timing characteristics (pads at 3.3 V or at 5.0 V)[1]

CLOAD = 25 pF on all outputs. Pad drive strength set to maximum.								
#	**Symbol**		**C**	**Rating**	**Min**	**Typ**	**Max**	**Unit**
1	f_{FCK}	CC	D	FCK Frequency [2, 3]	1/17		1/2	f_{SYS_CLK}
1	t_{FCK}	CC	D	FCK Period (t_{FCK} = 1/ f_{FCK})	2		17	t_{SYS_CLK}
2	t_{FCKHT}	CC	D	Clock (FCK) High Time	t_{SYS_CLK} − 6.5		$_{9*}$ t_{SYS_CLK} + 6.5	ns
3	t_{FCKLT}	CC	D	Clock (FCK) Low Time	t_{SYS_CLK} − 6.5		$_{8*}$ t_{SYS_CLK} + 6.5	ns
4	t_{SDS_LL}	CC	D	SDS Lead/Lag Time	-7.5		7.5	ns
5	t_{SDO_LL}	CC	D	SDO Lead/Lag Time	-7.5		7.5	ns
6	t_{DVFE}	CC	D	Data Valid from FCK Falling Edge (t_{FCKLT}+t_{SDO_LL})	1			ns
7	t_{EQ_SU}	CC	D	eQADC Data Setup Time (Inputs)	22			ns
8	t_{EQ_HO}	CC	D	eQADC Data Hold Time (Inputs)	1			ns

1 SS timing specified at f_{SYS} = 80 MHz, V_{DD} = 1.14 V to 1.32 V, V_{DDEH} = 4.5 V to 5.5 V, T_A = T_L to T_H, and C_L = 50 pF with SRC = 0b00.

2 Maximum operating frequency is highly dependent on track delays, master pad delays, and slave pad delays.

3 FCK duty is not 50% when it is generated through the division of the system clock by an odd number.

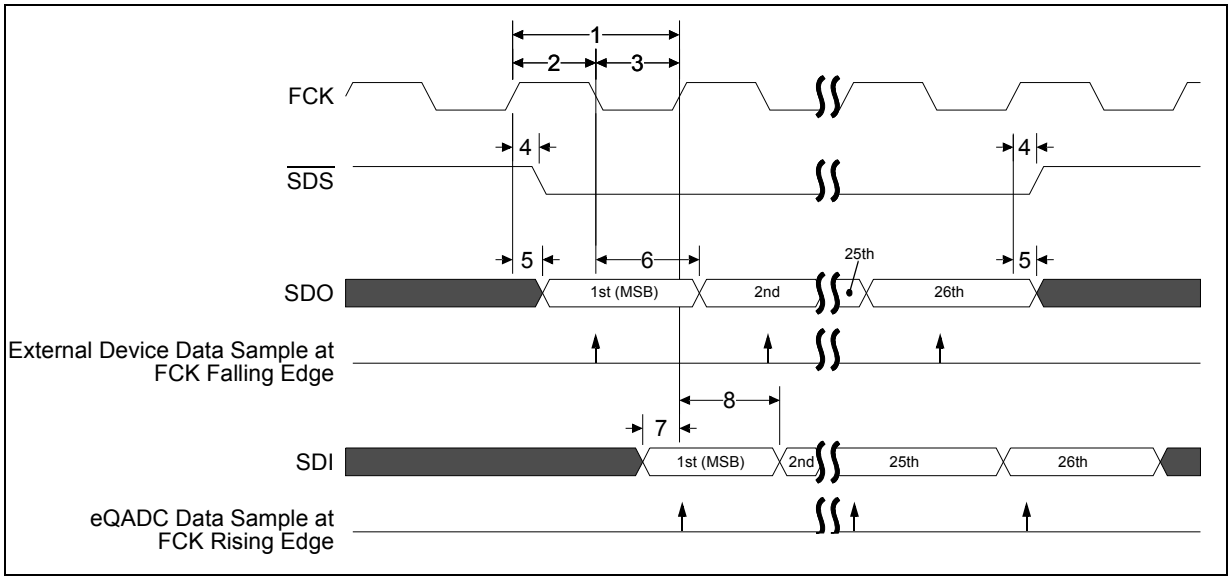

Figure 32. eQADC SSI timing