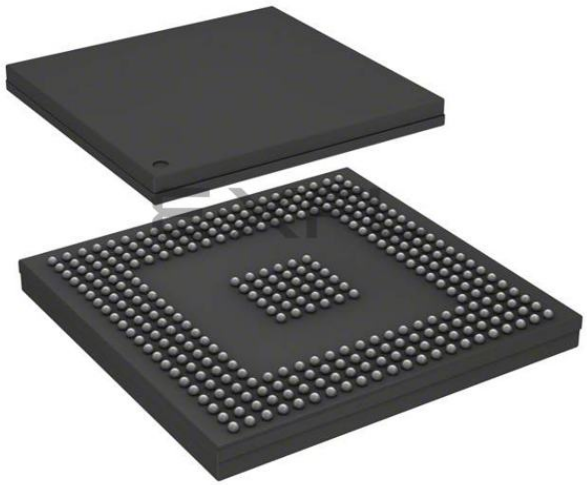

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	151
Program Memory Size	4MB (4M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	1.14V ~ 5.25V
Data Converters	A/D 40x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	324-BBGA
Supplier Device Package	324-PBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5644af0mvz2r

Table of Contents

Table 1. MPC5644A, MPC5634M and MPC5642A comparison (continued)

Feature		MPC5644A	MPC5634M	MPC5642A
	Micro Second Channel (MSC) bus downlink	Yes		
	DSPI_A	No		
	DSPI_B	Yes (with LVDS)		
	DSPI_C	Yes (with LVDS)		
	DSPI_D	Yes	No	Yes
FlexRay		Yes	No	Yes
System timers		5 PIT channels 4 STM channels 1 Software Watchdog		
eMIOS		24 ch.	16 ch.	24 ch.
eTPU		32 ch. eTPU2		
	Code memory	14 KB		
	Data memory	3 KB		
Interrupt controller		486 ch.[1]	307 ch.	486 ch.[1]
ADC		40 ch.	34 ch.	40 ch.
	ADC_A	Yes		
	ADC_B	Yes		
	Temp sensor	Yes		
	Variable gain amp.	Yes		
	Decimation filter	2	1	2
	Sensor diagnostics	Yes		
CRC		Yes	No	Yes
FMPLL		Yes		
VRC		Yes		
Supplies		5 V, 3.3 V[2]	5 V, 3.3 V[3]	5 V, 3.3 V[2]
Low-power modes		Stop Mode Slow Mode		
Packages		176 LQFP[4] 208 MAPBGA[4,5] 324 TEPBGA324[6] 496-pin CSP[7]	144 LQFP 176 LQFP 208 MAPBGA 496-pin CSP[7]	176 LQFP[4] 208 MAPBGA[4,5] 324 TEPBGA324[6] 496-pin CSP[7]

1 199 interrupt vectors are reserved.

2 5 V single supply only for 176 LQFP.

3 5 V single supply only for 144 LQFP.

4 Pinout compatible with Freescale's MPC5634M devices.

5 Pinout compatible with Freescale's MPC5534.

6 Ballmap upwardly compatible with the standardized package ballmap used for various Freescale MPC5xxx family members, including MPC5554, MPC5567 and MPC5666.

7 For Freescale VertiCal Calibration System only.

1.4.5 Memory protection unit (MPU)

The Memory Protection Unit (MPU) provides hardware access control for all memory references generated in a device. Using preprogrammed region descriptors, which define memory spaces and their associated access rights, the MPU concurrently monitors all system bus transactions and evaluates the appropriateness of each transfer. Memory references with sufficient access control rights are allowed to complete; references that are not mapped to any region descriptor or have insufficient rights are terminated with a protection error response.

The MPU has these major features:

- Support for 16 memory region descriptors, each 128 bits in size
  - Specification of start and end addresses provide granularity for region sizes from 32 bytes to 4 GB
  - MPU is invalid at reset, thus no access restrictions are enforced
  - Two types of access control definitions: processor core bus master supports the traditional {read, write, execute} permissions with independent definitions for supervisor and user mode accesses; the remaining non-core bus masters (eDMA, FlexRay, and EBI[1]) support {read, write} attributes
  - Automatic hardware maintenance of the region descriptor valid bit removes issues associated with maintaining a coherent image of the descriptor
  - Alternate memory view of the access control word for each descriptor provides an efficient mechanism to dynamically alter the access rights of a descriptor only[1]
  - For overlapping region descriptors, priority is given to permission granting over access denying as this approach provides more flexibility to system software
- Support for two XBAR slave port connections (SRAM and PBRIDGE)
  - For each connected XBAR slave port (SRAM and PBRIDGE), MPU hardware monitors every port access using the pre-programmed memory region descriptors
  - An access protection error is detected if a memory reference does not hit in any memory region or the reference is flagged as illegal in all memory regions where it does hit. In the event of an access error, the XBAR reference is terminated with an error response and the MPU inhibits the bus cycle being sent to the targeted slave device
  - 64-bit error registers, one for each XBAR slave port, capture the last faulting address, attributes, and detail information

1.4.6 FMPLL

The FMPLL allows the user to generate high speed system clocks from a 4 MHz to 40 MHz crystal oscillator or external clock generator. Further, the FMPLL supports programmable frequency modulation of the system clock. The PLL multiplication factor, output clock divider ratio are all software configurable. The PLL has the following major features:

- Input clock frequency from 4 MHz to 40 MHz
- Reduced frequency divider (RFD) for reduced frequency operation without forcing the PLL to relock
- Three modes of operation
  - Bypass mode with PLL off
  - Bypass mode with PLL running (default mode out of reset)
  - PLL normal mode
- Each of the three modes may be run with a crystal oscillator or an external clock reference
- Programmable frequency modulation
  - Modulation enabled/disabled through software
  - Triangle wave modulation up to 100 kHz modulation frequency
  - Programmable modulation depth (0% to 2% modulation depth)
  - Programmable modulation frequency dependent on reference frequency

1. EBI not available on all packages and is not available, as a master, for customer.

Table 3. MPC5644A signal properties (continued)

Name	Function[1]	PAG[2]	PCR PA Field[3]	PCR[4]	I/O Type	Voltage[5] / Pad Type[6]	Status[7]		Package pin #		
							During Reset	After Reset	176	208	324
ETPUA25 IRQ[13] DSPI_C_SCK_LVDS+ GPIO[139]	eTPU A channel External interrupt request LVDS positive DSPI clock GPIO	P A1 A2 G	001 010 100 000	139	I/O I O I/O	VDDEH1 Medium + LVDS	— / WKPCFG	— / WKPCFG	27	G3	M3
ETPUA26 IRQ[14] DSPI_C_SOUT_LVDS- GPIO[140]	eTPU A channel External interrupt request LVDS negative DSPI data out GPIO	P A1 A2 G	001 010 100 000	140	I/O I O I/O	VDDEH1 Slow + LVDS	— / WKPCFG	— / WKPCFG	26	F3	L2
ETPUA27 IRQ[15] DSPI_C_SOUT_LVDS+ DSPI_B_SOUT GPIO[141]	eTPU A channel External interrupt request LVDS positive DSPI data out DSPI data out GPIO	P A1 A2 A3 G	0001 0010 0100 1000 0000	141	I/O I O O I/O	VDDEH1 Slow + LVDS	— / WKPCFG	— / WKPCFG	25	G2	L1
ETPUA28 DSPI_C_PCS[1] RCH5_B GPIO[142]	eTPU A channel DSPI C peripheral chip select Reaction channel 5B GPIO	P A1 A2 G	001 010 100 000	142	I/O O O I/O	VDDEH1 Medium	— / WKPCFG	— / WKPCFG	24	F1	M4
ETPUA29 DSPI_C_PCS[2] RCH5_C GPIO[143]	eTPU A channel DSPI C peripheral chip select Reaction channel 5C GPIO	P A1 A2 G	001 010 100 000	143	I/O O O I/O	VDDEH1 Medium	— / WKPCFG	— / WKPCFG	23	F2	L3
ETPUA30 DSPI_C_PCS[3] ETPUA11_O[8] GPIO[144]	eTPU A channel DSPI C peripheral chip select eTPU A channel (output only) GPIO	P A1 A2 G	001 010 100 000	144	I/O O O I/O	VDDEH1 Medium	— / WKPCFG	— / WKPCFG	22	E1	L4
ETPUA31 DSPI_C_PCS[4] ETPUA13_O[8] GPIO[145]	eTPU A channel DSPI C peripheral chip select eTPU A channel (output only) GPIO	P A1 A2 G	001 010 100 000	145	I/O O O I/O	VDDEH1 Medium	— / WKPCFG	— / WKPCFG	21	E2	K1
eMIOS											
EMIOS0 ETPUA0_O[8] ETPUA25_O[8] GPIO[179]	eMIOS channel eTPU A channel (output only) eTPU A channel (output only) GPIO	P A1 A2 G	001 010 100 000	179	I/O O O I/O	VDDEH4 Slow	— / Up	— / Up	63	T4	AA12

Table 5. Signal details (continued)

Signal	Module or Function	Description
DSPI_C_SOUT_LVDS- DSPI_C_SOUT_LVDS+	DSPI	LVDS pair used for DSPI_C TSB mode transmission
PCS_B[0] PCS_C[0] PCS_D[0]	DSPI_B - DSPI_D	Peripheral chip select when device is in master mode—slave select when used in slave mode
PCS_B[1:5] PCS_C[1:5] PCS_D[1:5]	DSPI_B - DSPI_D	Peripheral chip select when device is in master mode—not used in slave mode
SCK_B SCK_C SCK_D	DSPI_B - DSPI_D	DSPI clock—output when device is in master mode; input when in slave mode
SIN_B SIN_C SIN_D	DSPI_B - DSPI_D	DSPI data in
SOUT_B SOUT_C SOUT_D	DSPI_B - DSPI_D	DSPI data out
ADDR[10:31]	EBI	The ADDR[10:31] signals specify the physical address of the bus transaction. The 26 address lines correspond to bits 3-31 of the EBI's 32-bit internal address bus. ADDR[15:31] can be used as Address and Data signals when configured appropriately for a multiplexed external bus. This allows 32-bit data operations, or 16-bit data operations without using DATA[0:15] signals.
ALE	EBI	The Address Latch Enable (ALE) signal is used to demultiplex the address from the data bus. It is asserted while the least significant 16 bits of the address are present in the multiplexed address/data bus.
$\overline{\text{BDIP}}$	EBI	$\overline{\text{BDIP}}$ is asserted to indicate that the master is requesting another data beat following the current one.
$\overline{\text{CS}}$[0:3]	EBI	$\overline{\text{CS}}$x is asserted by the master to indicate that this transaction is targeted for a particular memory bank on the Primary external bus.
DATA[0:31]	EBI	The DATA[0:31] signals contain the data to be transferred for the current transaction.
$\overline{\text{OE}}$	EBI	$\overline{\text{OE}}$ is used to indicate when an external memory is permitted to drive back read data. External memories must have their data output buffers off when $\overline{\text{OE}}$ is negated. $\overline{\text{OE}}$ is only asserted for chip-select accesses.
RD_$\overline{\text{WR}}$	EBI	RD_$\overline{\text{WR}}$ indicates whether the current transaction is a read access or a write access.

Table 5. Signal details (continued)

Signal	Module or Function	Description
$\overline{TA}$	EBI	$\overline{TA}$ is asserted to indicate that the slave has received the data (and completed the access) for a write cycle, or returned data for a read cycle. If the transaction is a burst read, $\overline{TA}$ is asserted for each one of the transaction beats. For write transactions, $\overline{TA}$ is only asserted once at access completion, even if more than one write data beat is transferred.
$\overline{TS}$	EBI	The Transfer Start signal ($\overline{TS}$) is asserted by the MPC5644A to indicate the start of a transfer.
$\overline{WE}$[2:3]	EBI	Write enables are used to enable program operations to a particular memory. $\overline{WE}$[2:3] are only asserted for write accesses
$\overline{WE}$[0:3]/$\overline{BE}$[0:3]	EBI	Write enables are used to enable program operations to a particular memory. These signals can also be used as byte enables for read and write operation by setting the WEBS bit in the appropriate EBI Base Register (EBI_BR*n*). $\overline{WE}$[0:3] are only asserted for write accesses. $\overline{BE}$[0:3] are asserted for both read and write accesses
eMIOS[0:23]	eMIOS	eMIOS I/O channels
AN[0:39]	eQADC	Single-ended analog inputs for analog-to-digital converter
FCK	eQADC	eQADC free running clock for eQADC SSI.
MA[0:2]	eQADC	These three control bits are output to enable the selection for an external Analog Mux for expansion channels.
REFBYPC	eQADC	Bypass capacitor input
SDI	eQADC	Serial data in
SDO	eQADC	Serial data out
SDS	eQADC	Serial data select
VRH	eQADC	Voltage reference high input
VRL	eQADC	Voltage reference low input
SCI_A_RX SCI_B_RX SCI_C_RX	eSCI_A - eSCI_C	eSCI receive
SCI_A_TX SCI_B_TX SCI_C_TX	eSCI_A - eSCI_C	eSCI transmit
ETPU_A[0:31]	eTPU	eTPU I/O channel
RCH0_[A:C] RCH1_[A:C] RCH2_[A:C] RCH3_[A:C] RCH4_[A:C] RCH5_[A:C]	eTPU2 Reaction Module	eTPU2 reaction channels. Used to control external actuators, e.g., solenoid control for direct injection systems and valve control in automatic transmissions
TCRCLKA	eTPU2	Input clock for TCR time base

Table 5. Signal details (continued)

Signal	Module or Function	Description
BOOTCFG[0:1]	SIU - Configuration	Two BOOTCFG signals are implemented in MPC5644A MCUs. The BAM program uses the BOOTCFG0 bit to determine where to read the reset configuration word, and whether to initiate a FlexCAN or eSCI boot. The BOOTCFG1 pin is sampled during the assertion of the RSTOUT signal, and the value is used to update the RSR and the BAM boot mode See the *MPC5644A Microcontroller Reference Manual* for more information. The following values are for BOOTCFG[0:1}: 00:Boot from internal flash memory 01:FlexCAN/eSCI boot 10:Boot from external memory using EBI 11:Reserved Note: For the 176-pin QFP and 208-ball BGA packages BOOTCFG[0] is always 0 since the EBI interface is not available.
WKPCFG	SIU - Configuration	The WKPCFG pin is applied at the assertion of the internal reset signal (assertion of $\overline{\text{RSTOUT}}$), and is sampled 4 clock cycles before the negation of the $\overline{\text{RSTOUT}}$ pin. The value is used to configure whether the eTPU and eMIOS pins are connected to internal weak pull up or weak pull down devices after reset. The value latched on the WKPCFG pin at reset is stored in the Reset Status Register (RSR), and is updated for all reset sources except the Debug Port Reset and Software External Reset. 0: Weak pulldown applied to eTPU and eMIOS pins at reset 1: Weak pullup applied to eTPU and eMIOS pins at reset.
ETRIG[2:3]	SIU - eQADC Triggers	External signal eTRIGx triggers eQADC CFIFOx
GPIO[206] ETRIG0 (Input)	SIU - eQADC Triggers	External signal eTRIGx triggers eQADC CFIFOx
GPIO[207] ETRIG1 (Input)	SIU - eQADC Triggers	External signal eTRIGx triggers eQADC CFIFOx
$\overline{\text{IRQ}}$[0:5] $\overline{\text{IRQ}}$[7:15]	SIU - External Interrupts	The $\overline{\text{IRQ}}$[0:15] pins connect to the SIU IRQ inputs. IMUX Select Register 1 is used to select the $\overline{\text{IRQ}}$[0:15] pins as inputs to the IRQs. See the *MPC5644A Microcontroller Reference Manual* for more information.
$\overline{\text{NMI}}$	SIU - External Interrupts	Non-Maskable Interrupt

Table 10. Thermal characteristics for 208-pin MAPBGA[1]

Symbol		C	Parameter	Conditions	Value	Unit
$R_{\theta JA}$	CC	D	Junction-to-Ambient, Natural Convection[2,3]	One layer board - 1s	39	°C/W
$R_{\theta JA}$	CC	D	Junction-to-Ambient, Natural Convection[2,4]	Four layer board - 2s2p	24	°C/W
$R_{\theta JMA}$	CC	D	Junction-to-Moving-Air, Ambient[2,4]	at 200 ft./min., one layer board	31	°C/W
$R_{\theta JMA}$	CC	D	Junction-to-Moving-Air, Ambient[2,4]	at 200 ft./min., four layer board 2s2p	20	°C/W
$R_{\theta JB}$	CC	D	Junction-to-board[5]	Four layer board - 2s2p	13	°C/W
$R_{\theta JC}$	CC	D	Junction-to-case[6]		6	°C/W
Ψ_{JT}	CC	D	Junction-to-package top natural convection[7]		2	°C/W

1 Thermal characteristics are targets based on simulation that are subject to change per device characterization.

2 Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

3 Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board horizontal.

4 Per JEDEC JESD51-6 with the board horizontal.

5 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

6 Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature.

7 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

Table 11. Thermal characteristics for 324-pin TEPBGA[1]

Symbol		C	Parameter	Conditions	Value	Unit
$R_{\theta JA}$	CC	D	Junction-to-Ambient, Natural Convection[2]	Single layer board - 1s	29	°C/W
$R_{\theta JA}$	CC	D	Junction-to-Ambient, Natural Convection[2]	Four layer board - 2s2p	19	°C/W
$R_{\theta JMA}$	CC	D	Junction-to-Moving-Air, Ambient[2]	at 200 ft./min., single layer board	23	°C/W
$R_{\theta JMA}$	CC	D	Junction-to-Moving-Air, Ambient[2]	at 200 ft./min., four layer board 2s2p	16	°C/W
$R_{\theta JB}$	CC	D	Junction-to-Board[3]		10	°C/W
$R_{\theta JCtop}$	CC	D	Junction-to-Case[4]		7	°C/W
Ψ_{JT}	CC	D	Junction-to-Package Top, Natural Convection[5]		2	°C/W

1 Thermal characteristics are targets based on simulation that are subject to change per device characterization.

2 Junction-to-Ambient Thermal Resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.

3 Junction-to-Board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.

4 Junction-to-Case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

Table 15. PMC Electrical Characteristics

ID	Name			Parameter	Min	Typ	Max	Unit	Notes
1	VBG	CC	C	Nominal bandgap voltage reference	—	1.219	—	V	
1a	—	CC	P	Untrimmed bandgap reference voltage	VBG - 7%	VBG	Vbg + 6%	V	
1b	—	CC	P	Trimmed bandgap reference voltage (5 V, 27 °C)	VBG -10mV	VBG	VBG + 10mV	V	
1c	—	CC	C	Bandgap reference temperature variation	—	100	—	ppm /°C	
1d	—	CC	C	Bandgap reference supply voltage variation	—	3000	—	ppm /V	
2	Vdd	CC	C	Nominal V_{DD} core supply internal regulator target DC output voltage[1]	—	1.28	—	V	
2a	—	CC	P	Nominal V_{DD} core supply internal regulator target DC output voltage variation at power-on reset	Vdd - 6%	Vdd	Vdd + 10%	V	
2b	—	CC	P	Nominal V_{DD} core supply internal regulator target DC output voltage variation after power-on reset	Vdd - 10%[2]	Vdd	Vdd + 3%	V	
2c	—	CC	C	Trimming step Vdd	—	20	—	mV	
2d	Ivrcctl	CC	C	Voltage regulator controller for core supply maximum DC output current	20	—	—	mA	
3	Lvi1p2	CC	C	Nominal LVI for rising core supply[3]	—	1.160	—	V	
3a	—	CC	C	Variation of LVI for rising core supply at power-on reset	1.120	1.200	1.280	V	See note [4]
3b	—	CC	C	Variation of LVI for rising core supply after power-on reset	Lvi1p2 - 3%	Lvi1p2	Lvi1p2 + 3%	V	See note 4
3c	—	CC	C	Trimming step LVI core supply	—	20	—	mV	
3d	Lvi1p2_h	CC	C	LVI core supply hysteresis	—	40	—	mV	
4	Por1.2V_r	CC	C	POR 1.2 V rising	—	0.709	—	V	
4a	—	CC	C	POR 1.2 V rising variation	Por1.2V_r - 35%	Por1.2V_r	Por1.2V_r + 35%	V	
4b	Por1.2V_f	CC	C	POR 1.2 V falling	—	0.638	—	V	
4c	—	CC	C	POR 1.2 V falling variation	Por1.2V_f - 35%	Por1.2V_f	Por1.2V_f+ 35%	V	

Table 21. DC electrical specifications (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					min	typ	max	
V_{OL_S}	CC	P	Slow/medium pad I/O output low voltage[9]		—	—	$0.2*V_{DDEH}$	V
V_{OL_F}	CC	P	Fast I/O output low voltage[9]		—	—	$0.2*V_{DDE}$	V
V_{OL_LS}	CC	P	Multi-voltage pad I/O output low voltage in low-swing mode[5,6,7,8,9]		—	—	0.6	V
V_{OL_HS}	CC	P	Multi-voltage pad I/O output low voltage in high-swing mode[9]		—	—	$0.2*V_{DDEH}$	V
V_{OH_S}	CC	P	Slow/medium pad I/O output high voltage[9]		$0.8\ V_{DDEH}$	—	—	V
V_{OH_F}	CC	P	Fast pad I/O output high voltage[9]		$0.8\ V_{DDE}$	—	—	V
V_{OH_LS}	CC	P	Multi-voltage pad I/O output high voltage in low-swing mode[5,6,7,8]	I_{OH_LS} = 0.5 mA	2.1	3.1	3.7	V
V_{OH_HS}	CC	P	Multi-voltage pad I/O output high voltage in high-swing mode[9]		$0.8\ V_{DDEH}$	—	—	V
V_{HYS_S}	CC	C	Slow/medium/multi-voltage I/O input hysteresis	—	$0.1 * V_{DDEH}$	—	—	V
V_{HYS_F}	CC	C	Fast I/O input hysteresis	—	$0.1 * V_{DDE}$	—	—	V
V_{HYS_LS}	CC	C	Low-Swing-Mode Multi-Voltage I/O Input Hysteresis	hysteresis enabled	0.25	—	—	v
$I_{DD}+I_{DDPLL}$	CC	P	Operating current 1.2 V supplies	V_{DD} at 1.32 V at 80 MHz	—		380	mA
		P		V_{DD} at 1.32V at 120 MHz	—		400	mA
		P		V_{DD} at 1.32V at 150 MHz	—		400	mA

3.9 I/O pad current specifications

The power consumption of an I/O segment depends on the usage of the pins on a particular segment. The power consumption is the sum of all output pin currents for a particular segment. The output pin current can be calculated from Table 22 based on the voltage, frequency, and load on the pin. Use linear scaling to calculate pin currents for voltage, frequency, and load parameters that fall outside the values given in Table 22.

Table 22. I/O pad average I_{DDE} specifications[1]

Pad Type	Symbol		C	Period (ns)	Load[2] (pF)	V_{DDE} (V)	Drive/Slew Rate Select	I_{DDE} Avg (mA)[3]	I_{DDE} RMS (mA)
Slow	$I_{DRV\_SSR\_HV}$	CC	D	37	50	5.5	11	9	—
		CC	D	130	50	5.5	01	2.5	—
		CC	D	650	50	5.5	00	0.5	—
		CC	D	840	200	5.5	00	1.5	—
Medium	$I_{DRV\_MSR\_HV}$	CC	D	24	50	5.5	11	14	—
		CC	D	62	50	5.5	01	5.3	—
		CC	D	317	50	5.5	00	1.1	—
		CC	D	425	200	5.5	00	3	—
Fast	I_{DRV_FC}	CC	D	10	50	3.6	11	22.7	68.3
		CC	D	10	30	3.6	10	12.1	41.1
		CC	D	10	20	3.6	01	8.3	27.7
		CC	D	10	10	3.6	00	4.44	14.3
		CC	D	10	50	1.98	11	12.5	31
		CC	D	10	30	1.98	10	7.3	18.6
		CC	D	10	20	1.98	01	5.42	12.6
		CC	D	10	10	1.98	00	2.84	6.4
MultiV (High Swing Mode)	$I_{DRV\_MULTV\_HV}$	CC	D	20	50	5.5	11	9	—
		CC	D	30	50	5.5	01	6.1	—
		CC	D	117	50	5.5	00	2.3	—
		CC	D	212	200	5.5	00	5.8	—
MultiV (Low Swing Mode)	$I_{DRV\_MULTV\_HV}$	CC	D	30	30	5.5	11	3.4	—

1 Numbers from simulations at best case process, 150 °C.

2 All loads are lumped.

3 Average current is for pad configured as output only.

Table 24. V_{RC33} pad average DC current[1]

Pad Type	Symbol		C	Period (ns)	Load[2] (pF)	V_{RC33} (V)	V_{DDE} (V)	Drive Select	I_{DD33} Avg (µA)	I_{DD33} RMS (µA)
Fast	I_{DRV_FC}	CC	D	10	50	3.6	3.6	11	2.35	6.12
		CC	D	10	30	3.6	3.6	10	1.75	4.3
		CC	D	10	20	3.6	3.6	01	1.41	3.43
		CC	D	10	10	3.6	3.6	00	1.06	2.9
		CC	D	10	50	3.6	1.98	11	1.75	4.56
		CC	D	10	30	3.6	1.98	10	1.32	3.44
		CC	D	10	20	3.6	1.98	01	1.14	2.95
		CC	D	10	10	3.6	1.98	00	0.95	2.62

1 These are typical values that are estimated from simulation and not tested. Currents apply to output pins only.

2 All loads are lumped.

3.9.2 LVDS pad specifications

LVDS pads are implemented to support the MSC (Microsecond Channel) protocol which is an enhanced feature of the DSPI module. The LVDS pads are compliant with LVDS specifications and support data rates up to 50 MHz.

Table 25. DSPI LVDS pad specification

#	Characteristic	Symbol	C		Condition	Min. Value	Typ. Value	Max. Value	Unit
Data Rate									
4	Data Frequency	$f_{LVDSCLK}$	CC	D	—		50		MHz
Driver Specs									
5	Differential output voltage	V_{OD}	CC	P	SRC=0b00 or 0b11	150		400	mV
			CC	P	SRC=0b01	90		320	
			CC	P	SRC=0b10	160		480	
6	Common mode voltage (LVDS), VOS	V_{OD}	CC	P		1.06	1.2	1.39	V
7	Rise/Fall time	T_R/T_F	CC	D	—		2		ns
8	Propagation delay (Low to High)	T_{PLH}	CC	D			4		ns
9	Propagation delay (High to Low)	T_{PHL}	CC	D	—		4		ns
10	Delay (H/L), sync Mode	t_{PDSYNC}	CC	D			4		ns

3.13 Configuring SRAM wait states

Use the SWSC field in the ECSM_MUDCR register to specify an additional wait state for the device SRAM. By default, no wait state is added.

Table 31. Cutoff frequency for additional SRAM wait state

[1]	SWSC Value
98	0
153	1

[1] Max frequencies including 2% PLL FM.

Please see the device reference manual for details.

3.14 Platform flash controller electrical characteristics

Table 32. APC, RWSC, WWSC settings vs. frequency of operation[1,2]

Max. Flash Operating Frequency (MHz)[3]	APC[4]	RWSC[4]	WWSC
20 MHz	0b000	0b000	0b11
61 MHz	0b001	0b001	0b11
90 MHz	0b010	0b010	0b11
123 MHz	0b011	0b011	0b11
153 MHz	0b100	0b100	0b11

[1] APC, RWSC and WWSC are fields in the flash memory BIUCR register used to specify wait states for address pipelining and read/write accesses. Illegal combinations exist—all entries must be taken from the same row.

[2] TBD: To Be Defined.

[3] Max frequencies including 2% PLL FM.

[4] APC must be equal to RWSC.

3.15 Flash memory electrical characteristics

Table 33. Flash program and erase specifications[1]

#	Symbol		C	Parameter	Min. Value	Typical Value	Initial Max[2]	Max[3]	Unit
1	$T_{dwprogram}$	CC	P	Double Word (64 bits) Program Time	—	38	—	500	µs
2	$T_{pprogram}$	CC	P	Page Program Time	—	45	160[4]	500	µs
3	$T_{16kpperase}$	CC	P	16 KB Block Pre-program and Erase Time	—	270	1000	5000	ms
5	$T_{64kpperase}$	CC	P	64 KB Block Pre-program and Erase Time	—	800	1800	5000	ms

3.16 AC specifications

3.16.1 Pad AC specifications

Table 35. Pad AC specifications (5.0 V)[1]

Name		C	Output Delay (ns)[2,3] Low-to-High / High-to-Low		Rise/Fall Edge (ns)[3,4]		Drive Load (pF)	SRC/DSC
			Min	Max	Min	Max		MSB,LSB
Medium[5,6,7]	CC	D	4.6/3.7	12/12	2.2/2.2	7/7	50	11[8]
	N/A							10[9]
	CC	D	12/13	28/34	5.6/6	15/15	50	01
	CC	D	69/71	152/165	34/35	74/74	50	00
Slow[7,10]	CC	D	7.3/5.7	19/18	4.4/4.3	14/14	50	11[8]
	N/A							10[9]
	CC	D	26/27	61/69	13/13	34/34	50	01
	CC	D	137/142	320/330	72/74	164/164	50	00
MultiV[11] (High Swing Mode)	CC	D	4.1/3.6	10.3/8.9	3.28/2.98	8/8	50	11[8]
	N/A							10[9]
	CC	D	8.38/6.11	16/12.9	5.48/4.81	11/11	50	01
	CC	D	61.7/10.4	92.2/24.3	42.0/12.2	63/63	50	00
MultiV (Low Swing Mode)	CC	D	2.31/2.34	7.62/6.33	1.26/1.67	6.5/4.4	30	11[8]
Fast[12]	N/A							
pad_i_hv[13]	CC	D	0.5/0.5	1.9/1.9	0.3/0.3	±1.5/1.5	0.5	N/A
pull_hv	CC	D	NA	6000		5000/5000	50	N/A

1 These are worst case values that are estimated from simulation and not tested. The values in the table are simulated at V_{DD} = 1.14 V to 1.32 V, V_{DDEH} = 4.5 V to 5.5 V, $T_A = T_L$ to T_H

2 This parameter is supplied for reference and is not guaranteed by design and not tested.

3 Delay and rise/fall are measured to 20% or 80% of the respective signal.

4 This parameter is guaranteed by characterization before qualification rather than 100% tested.

5 In high swing mode, high/low swing pad Vol and Voh values are the same as those of the slew controlled output pads

6 Medium Slew-Rate Controlled Output buffer. Contains an input buffer and weak pullup/pulldown.

7 Output delay is shown in Figure 9. Add a maximum of one system clock to the output delay for delay with respect to system clock.

8 Can be used on the tester.

9 This drive select value is not supported. If selected, it will be approximately equal to 11.

10 Slow Slew-Rate Controlled Output buffer. Contains an input buffer and weak pullup/pulldown.

11 Selectable high/low swing IO pad with selectable slew in high swing mode only.

12 Fast pads are 3.3 V pads.

Table 39. Nexus debug port timing[1] (continued)

#	Symbol		C	Characteristic	Min. Value	Max. Value	Unit
11	t_{NTDIS}	CC	D	TDI Data Setup Time	5	—	ns
12	t_{NTDIH}	CC	D	TDI Data Hold Time	25	—	ns
13	t_{NTMSS}	CC	D	TMS Data Setup Time	5	—	ns
14	t_{NTMSH}	CC	D	TMS Data Hold Time	25	—	ns
15	—	CC	D	TDO propagation delay from falling edge of TCK	—	19.5	ns
16	—	CC	D	TDO hold time with respect to TCK falling edge (minimum TDO propagation delay)	5.25	—	ns

1 All Nexus timing relative to MCKO is measured from 50% of MCKO and 50% of the respective signal. Nexus timing specified at V_{DD} = 1.14 V to 1.32 V, V_{DDEH} = 4.5 V to 5.5 V with multi-voltage pads programmed to Low-Swing mode, $T_A = T_L$ to T_H, and C_L = 30 pF with DSC = 0b10.

2 Achieving the absolute minimum MCKO cycle time may require setting the MCKO divider to more than its minimum setting (NPC_PCR[MCKO_DIV] depending on the actual system frequency being used.

3 This is a functionally allowable feature. However, this may be limited by the maximum frequency specified by the Absolute minimum MCKO period specification.

4 This may require setting the MCO divider to more than its minimum setting (NPC_PCR[MCKO_DIV]) depending on the actual system frequency being used.

5 MDO, $\overline{\text{MSEO}}$, and $\overline{\text{EVTO}}$ data is held valid until next MCKO low cycle.

6 Achieving the absolute minimum TCK cycle time may require a maximum clock speed (system frequency / 8) that is less than the maximum functional capability of the design (system frequency / 4) depending on the actual system frequency being used.

7 This is a functionally allowable feature. However, this may be limited by the maximum frequency specified by the Absolute minimum TCK period specification.

8 This may require a maximum clock speed (system frequency / 8) that is less than the maximum functional capability of the design (system frequency / 4) depending on the actual system frequency being used.

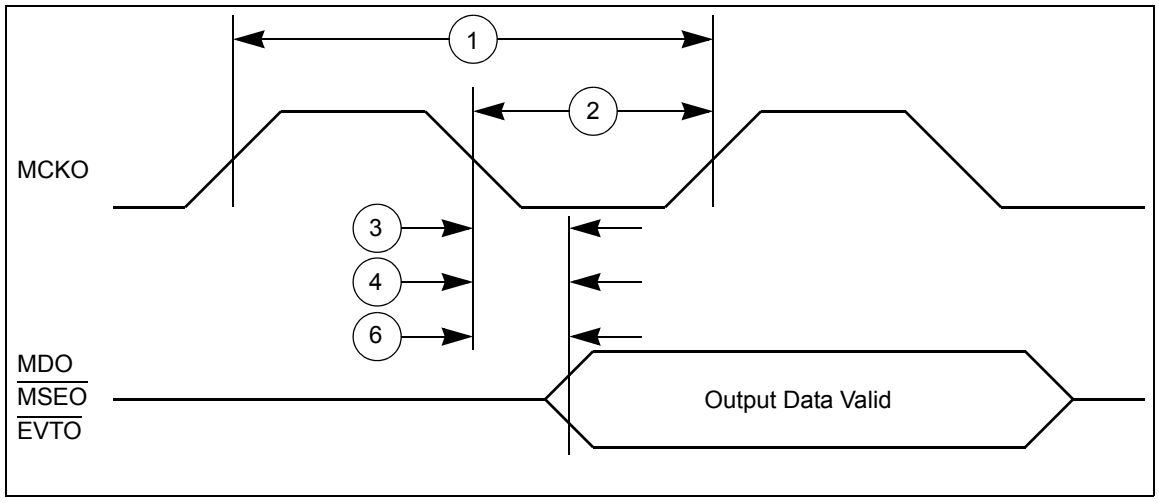

Figure 15. Nexus output timing

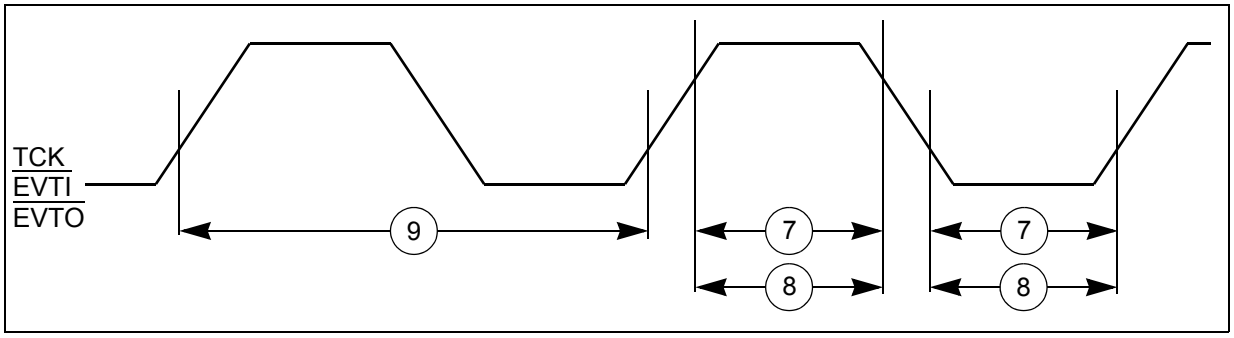

Figure 16. Nexus event trigger and test clock timings

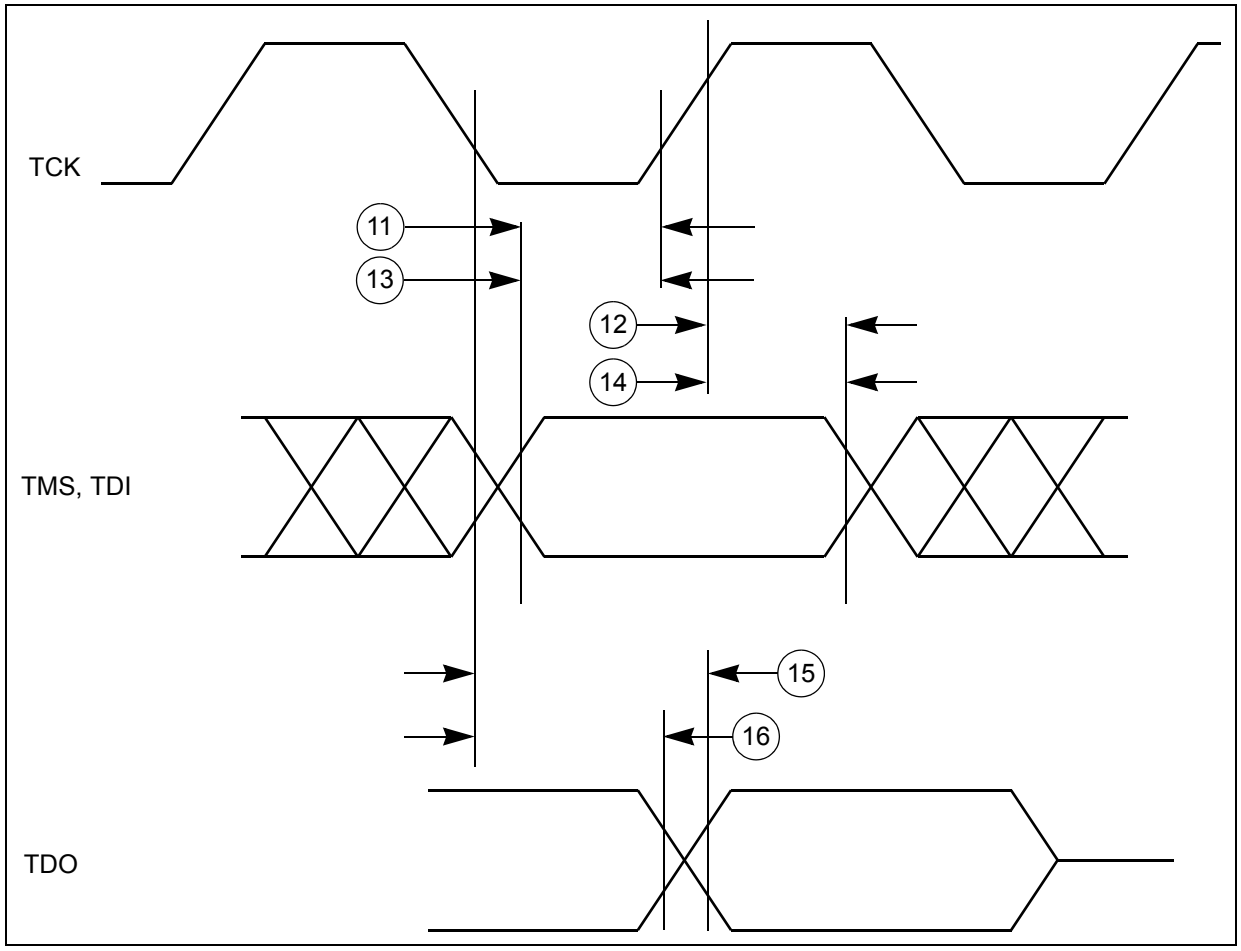

Figure 17. Nexus TDI, TMS, TDO timing

3.17.4 External Bus Interface (EBI) and calibration bus interface timing

Table 41. External Bus Interface maximum operating frequency

Port Width	Multiplexed Mode	ADDR[12:15] Pin Usage	ADDR[16:31] Pin Usage	DATA[0:15] Pin Usage	Max. Operating Frequency
16-bit	Yes	ADDR[12:15]	GPIO	ADDR[16:31] DATA[0:15]	66 MHz[1]
16-bit	No	ADDR[12:15]	ADDR[16:31]	DATA[0:15]	33 MHz[2,3]
32-bit	Yes	ADDR[12:15]	ADDR[16:31] DATA[16:31]	DATA[0:15]	33 MHz[2,3]

1 Set SIU_ECCR[EBDF] to divide by two or divide by four if the system frequency is greater than 66 MHz.

2 System Frequency must be ≤132 MHz and SIU_ECCR[EBDF] set to divide by four.

3 Pad restrictions limit the maximum operating frequency.

Table 42. Calibration bus interface maximum operating frequency

Port Width	Multiplexed Mode	CAL_ADDR[12:15] Pin Usage	CAL_ADDR[16:30] Pin Usage	CAL_DATA[0:15] Pin Usage	Max. Operating Frequency
16-bit	Yes	GPIO	GPIO	CAL_ADDR[12:30] CAL_DATA[0:15]	66 MHz[1]
16-bit	No	CAL_ADDR[12:15]	CAL_ADDR[16:30]	CAL_DATA[0:15]	66 MHz[1]
32-bit	Yes	CAL_WE[2:3] CAL_DATA[31]	CAL_ADDR[16:30] CAL_DATA[16:30]	CAL_ADDR[0:15] CAL_DATA[0:15]	66 MHz[1]

1 Set SIU_ECCR[EBDF] to divide by two or divide by four if the system frequency is greater than 66 MHz

Table 43. External bus interface (EBI) and calibration bus operation timing [1]

#	Symbol		C	Characteristic	66 MHz (ext. bus)[2]		Unit	Notes
					Min	Max		
1	T_C	CC	P	CLKOUT Period	15.2	—	ns	Signals are measured at 50% V_{DDE}.
2	t_{CDC}	CC	D	CLKOUT duty cycle	45%	55%	T_C	
3	t_{CRT}	CC	D	CLKOUT rise time	—	[3]	ns	
4	t_{CFT}	CC	D	CLKOUT fall time	—	[3]	ns	
5	t_{COH}	CC	D	CLKOUT Posedge to Output Signal Invalid or High Z(Hold Time) • ADDR[8:31] • CS[0:3] • DATA[0:31] • OE • RD_WR • TS • WE[0:3]/BE[0:3]	1.3	—	ns	

3.17.5 External interrupt timing (IRQ pin)

Table 44. External interrupt timing[1]

#	Characteristic	Symbol	Min	Max	Unit
1	IRQ Pulse Width Low	t_{IPWL}	3	—	t_{cyc}
2	IRQ Pulse Width High	t_{IPWH}	3	—	t_{cyc}
3	IRQ Edge to Edge Time[2]	t_{ICYC}	6	—	t_{cyc}

1 IRQ timing specified at V_{DD} = 1.14 V to 1.32 V, V_{DDEH} = 3.0 V to 5.5 V, V_{DD33} and V_{DDSYN} = 3.0 V to 3.6 V, $T_A = T_L$ to T_H.

2 Applies when IRQ pins are configured for rising edge or falling edge events, but not both.

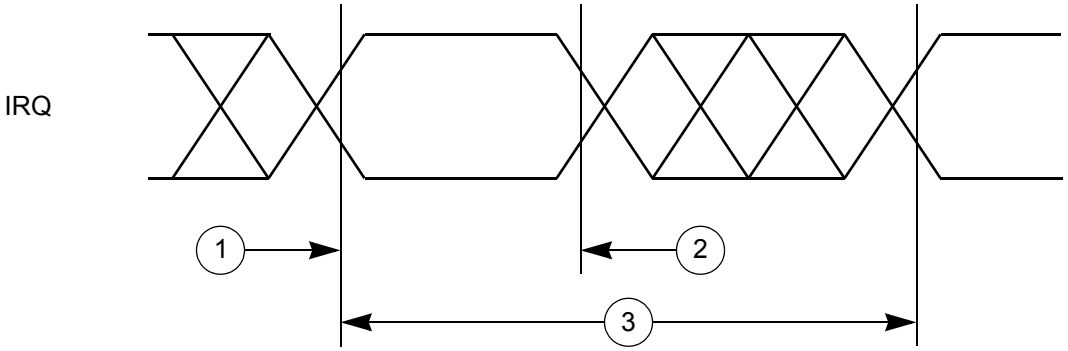

Figure 22. External Interrupt Timing

3.17.6 eTPU timing

Table 45. eTPU timing[1]

#	Characteristic	Symbol	Min	Max	Unit
1	eTPU Input Channel Pulse Width	t_{ICPW}	4	—	t_{cyc}
2	eTPU Output Channel Pulse Width	t_{OCPW}	2^2	—	t_{cyc}

1 eTPU timing specified at V_{DD} = 1.08 V to 1.32 V, V_{DDEH} = 3.0 V to 5.5 V, V_{DD33} and V_{DDSYN} = 3.0 V to 3.6 V, $T_A = T_L$ to T_H, and C_L = 200 pF with SRC = 0b00.

2 This specification does not include the rise and fall times. When calculating the minimum eTPU pulse width, include the rise and fall times defined in the slew rate control fields (SRC) of the pad configuration registers (PCR).

3.17.10 FlexCAN system clock source

Table 50. FlexCAN engine system clock divider threshold

#	Symbol	Characteristic	Value	Unit
1	F_{CAN_TH}	FlexCAN engine system clock threshold	100	MHz

Table 51. FlexCAN engine system clock divider

System Frequency	Required SIU_SYSDIV[CAN_SRC] Value
<= F_{CAN_TH}	0[1,2]
> F_{CAN_TH}	1[2,3]

1 Divides system clock source for FlexCAN engine by 1.

2 System clock is only selected for FlexCAN when CAN_CR[CLK_SRC] = 1.

3 Divides system clock source for FlexCAN engine by 2.

Figure 33. 176 LQFP package mechanical drawing (part 1)

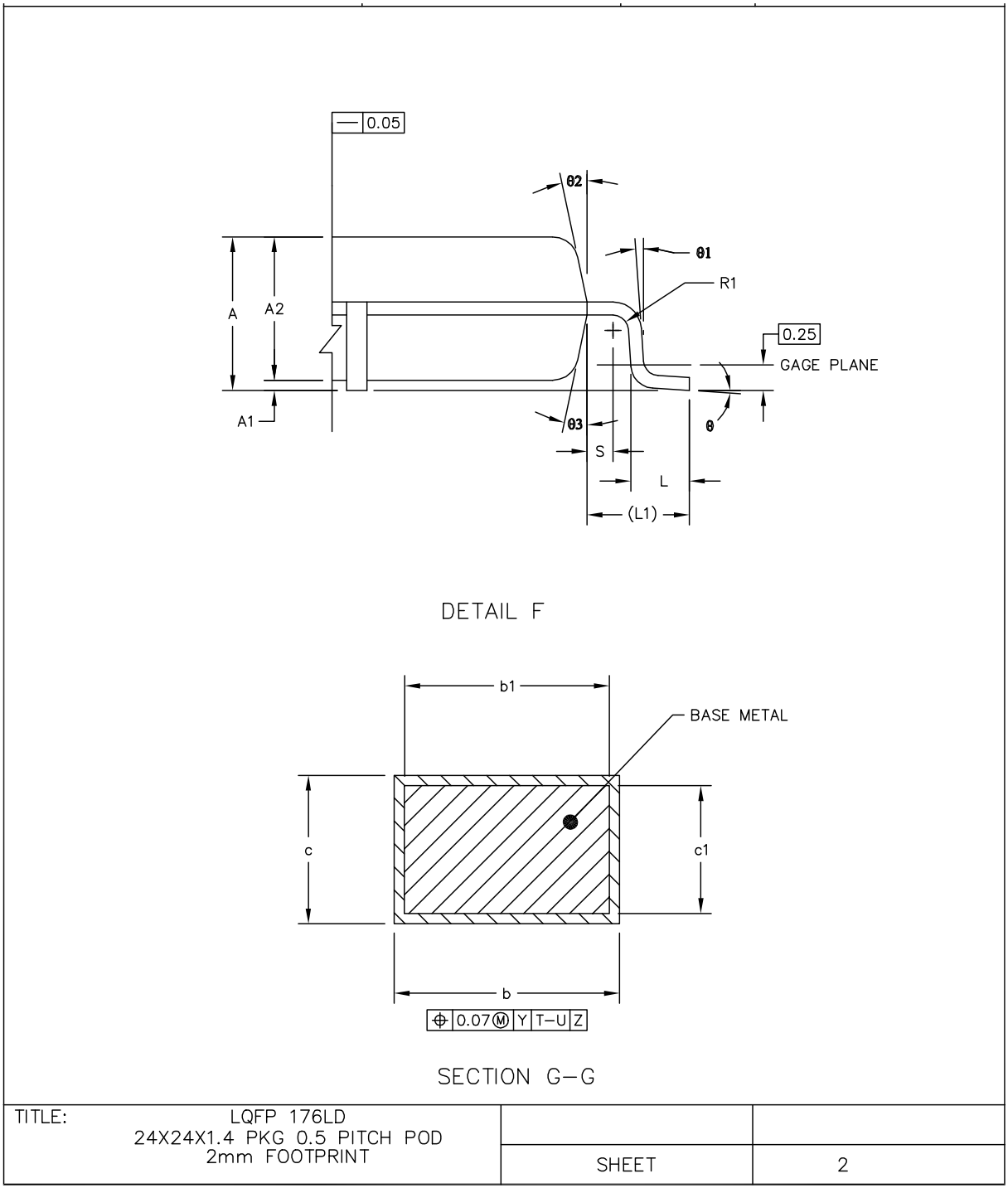

Figure 34. 176 LQFP package mechanical drawing (part 2)