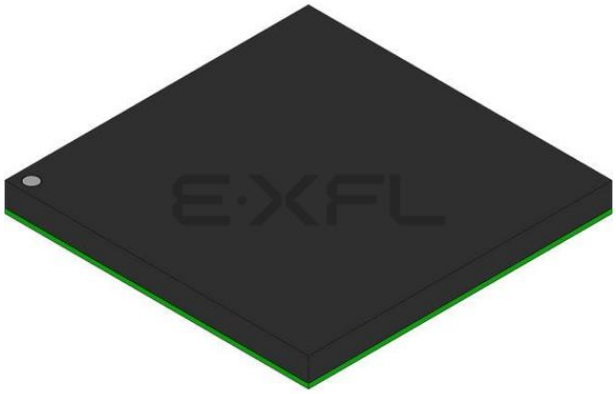

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, EBI/EMI, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	151
Program Memory Size	4MB (4M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	1.14V ~ 5.25V
Data Converters	A/D 40x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	324-BBGA
Supplier Device Package	324-PBGA (23x23)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=spc5644af0mvz3

1.4.5 Memory protection unit (MPU)

The Memory Protection Unit (MPU) provides hardware access control for all memory references generated in a device. Using preprogrammed region descriptors, which define memory spaces and their associated access rights, the MPU concurrently monitors all system bus transactions and evaluates the appropriateness of each transfer. Memory references with sufficient access control rights are allowed to complete; references that are not mapped to any region descriptor or have insufficient rights are terminated with a protection error response.

The MPU has these major features:

- Support for 16 memory region descriptors, each 128 bits in size
  - Specification of start and end addresses provide granularity for region sizes from 32 bytes to 4 GB
  - MPU is invalid at reset, thus no access restrictions are enforced
  - Two types of access control definitions: processor core bus master supports the traditional {read, write, execute} permissions with independent definitions for supervisor and user mode accesses; the remaining non-core bus masters (eDMA, FlexRay, and EBI[1]) support {read, write} attributes
  - Automatic hardware maintenance of the region descriptor valid bit removes issues associated with maintaining a coherent image of the descriptor
  - Alternate memory view of the access control word for each descriptor provides an efficient mechanism to dynamically alter the access rights of a descriptor only[1]
  - For overlapping region descriptors, priority is given to permission granting over access denying as this approach provides more flexibility to system software
- Support for two XBAR slave port connections (SRAM and PBRIDGE)
  - For each connected XBAR slave port (SRAM and PBRIDGE), MPU hardware monitors every port access using the pre-programmed memory region descriptors
  - An access protection error is detected if a memory reference does not hit in any memory region or the reference is flagged as illegal in all memory regions where it does hit. In the event of an access error, the XBAR reference is terminated with an error response and the MPU inhibits the bus cycle being sent to the targeted slave device
  - 64-bit error registers, one for each XBAR slave port, capture the last faulting address, attributes, and detail information

1.4.6 FMPLL

The FMPLL allows the user to generate high speed system clocks from a 4 MHz to 40 MHz crystal oscillator or external clock generator. Further, the FMPLL supports programmable frequency modulation of the system clock. The PLL multiplication factor, output clock divider ratio are all software configurable. The PLL has the following major features:

- Input clock frequency from 4 MHz to 40 MHz
- Reduced frequency divider (RFD) for reduced frequency operation without forcing the PLL to relock
- Three modes of operation
  - Bypass mode with PLL off
  - Bypass mode with PLL running (default mode out of reset)
  - PLL normal mode
- Each of the three modes may be run with a crystal oscillator or an external clock reference
- Programmable frequency modulation
  - Modulation enabled/disabled through software
  - Triangle wave modulation up to 100 kHz modulation frequency
  - Programmable modulation depth (0% to 2% modulation depth)
  - Programmable modulation frequency dependent on reference frequency

1. EBI not available on all packages and is not available, as a master, for customer.

and 128- and 256-bit read data interfaces to flash memory. The module contains a prefetch controller which prefetches sequential lines of data from the flash array into the buffers. Prefetch buffer hits allow no-wait responses.

The flash memory provides the following features:

- Supports a 64-bit data bus for instruction fetch, CPU loads and DMA access. Byte, halfword, word and doubleword reads are supported. Only aligned word and doubleword writes are supported.
- Fetch Accelerator
  - Architected to optimize the performance of the flash
  - Configurable read buffering and line prefetch support
  - Four-entry 256-bit wide line read buffer
  - Prefetch controller
- Hardware and software configurable read and write access protections on a per-master basis
- Interface to the flash array controller pipelined with a depth of one, allowing overlapped accesses to proceed in parallel for interleaved or pipelined flash array designs
- Configurable access timing usable in a wide range of system frequencies
- Multiple-mapping support and mapping-based block access timing (0-31 additional cycles) usable for emulation of other memory types
- Software programmable block program/erase restriction control
- Erase of selected block(s)
- Read page size of 128 bits (four words)
- ECC with single-bit correction, double-bit detection
- Program page size of 128 bits (four words) to accelerate programming
- ECC single-bit error corrections are visible to software
- Minimum program size is two consecutive 32-bit words, aligned on a 0-modulo-8 byte address, due to ECC
- Embedded hardware program and erase algorithm
- Erase suspend, program suspend and erase-suspended program
- Shadow information stored in non-volatile shadow block
- Independent program/erase of the shadow block

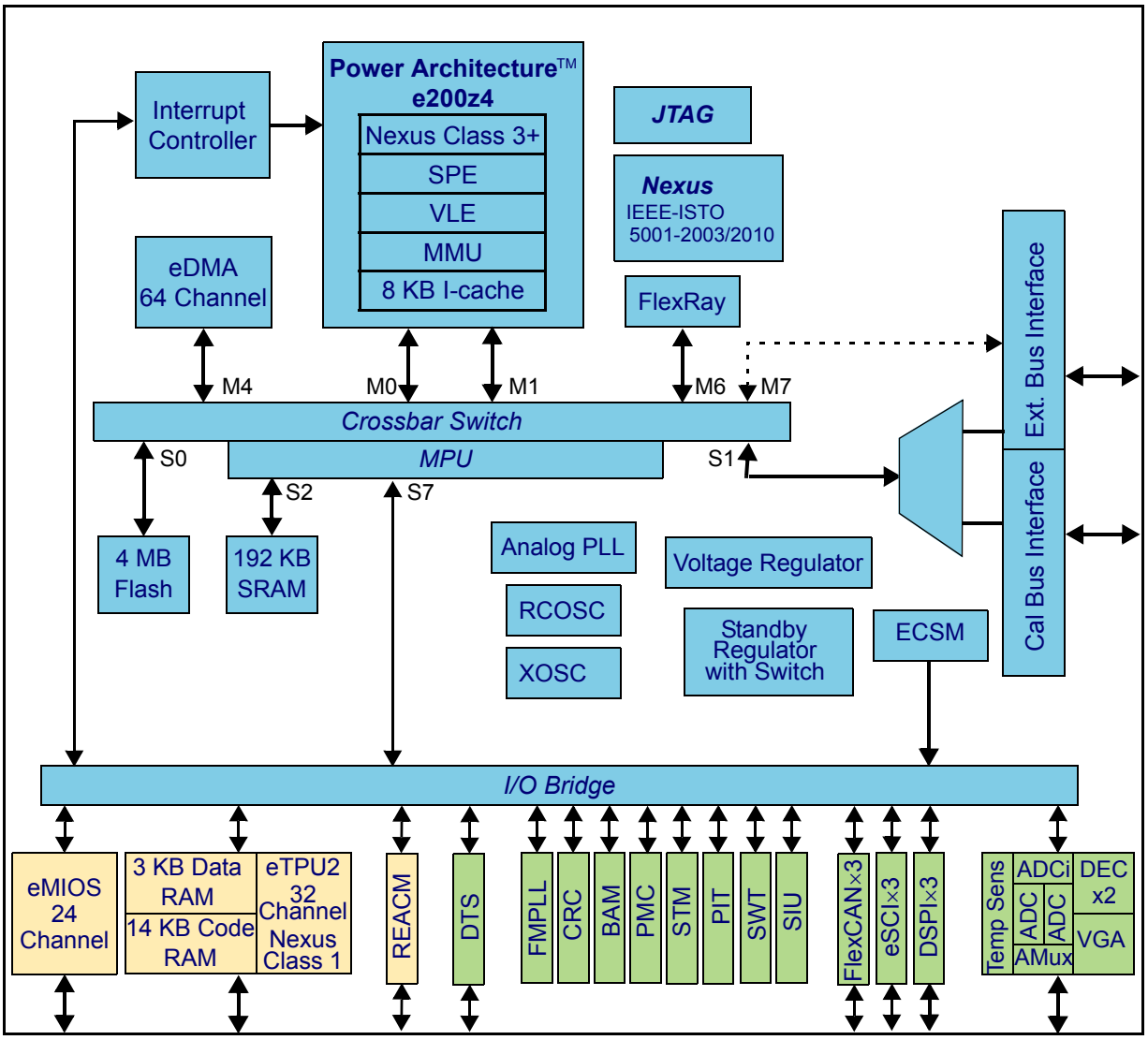
1.4.9 BAM

The BAM (Boot Assist Module) is a block of read-only memory that is programmed once by Freescale and is identical for all MPC5644A MCUs. The BAM program is executed every time the MCU is powered-on or reset in normal mode. The BAM supports different modes of booting. They are:

- Booting from internal flash memory
- Serial boot loading (A program is downloaded into RAM via eSCI or the FlexCAN and then executed)
- Booting from external memory on external bus

The BAM also reads the reset configuration half word (RCHW) from internal flash memory and configures the MPC5644A hardware accordingly. The BAM provides the following features:

- Sets up MMU to cover all resources and mapping of all physical addresses to logical addresses with minimum address translation
- Sets up MMU to allow user boot code to execute as either Power Architecture embedded category (default) or as Freescale VLE code
- Location and detection of user boot code
- Automatic switch to serial boot mode if internal flash is blank or invalid
- Supports user programmable 64-bit password protection for serial boot mode
- Supports serial bootloading via FlexCAN bus and eSCI using Freescale protocol



LEGEND

ADC	– Analog to Digital Converter	**JTAG**	– IEEE 1149.1 test controller
ADCi	– ADC interface	**MMU**	– Memory Management Unit
AMux	– Analog Multiplexer	**MPU**	– Memory Protection Unit
BAM	– Boot Assist Module	**PMC**	– Power Management Controller
CRC	– Cyclic Redundancy Check unit	**PIT**	– Periodic Interrupt Timer
DEC	– Decimation Filter	**RCOSC**	– low-speed RC oscillator
DTS	– Development Trigger Semaphore	**REACM**	– Reaction module
DSPI	– Deserial/Serial Peripheral Interface	**SIU**	– System Integration Unit
EBI	– External Bus Interface	**SPE**	– Signal Processing Extension
ECSM	– Error Correction Status Module	**SRAM**	– Static RAM
eDMA	– Enhanced Direct Memory Access	**STM**	– System Timer Module
eMIOS	– Enhanced Modular Input Output System	**SWT**	– Software Watchdog Timer
eSCI	– Enhanced Serial Communications Interface	**VGA**	– Variable Gain Amplifier
eTPU2	– Second gen. Enhanced Time Processing Unit	**VLE**	– Variable Length (instruction) Encoding
FlexCAN	– Controller Area Network (FlexCAN)	**XOSC**	– XTAL Oscillator
FMPLL	– Frequency-Modulated Phase Locked Loop		

Figure 1. MPC5644A series block diagram

2 Pinout and signal description

This section contains the pinouts for all production packages for the MPC5644A family of devices.

CAUTION

Any pins labeled “NC” are to be left unconnected. Any connection to an external circuit or voltage may cause unpredictable device behavior or damage.

VSS	VSS	VSS					VRC33	NC	NC	VDDEH6AB	M
VSS	VSS	VSS					NC	SCI_A_TX	VSS	NC	N
VSS	VSS	VSS					CAN_C_TX	SCI_A_RX	RSTOUT	RSTCFG	P
							NC	NC	NC	RESET	R
							VSS	BOOTCFG0	VSS[1]	VSS	T
							VDDEH6AB	PLLCFG1	BOOTCFG1	EXTAL	U
							SCI_C_RX	CAN_C_RX	PLLREF	XTAL	V
ETPUA1	EMIOS1	VDDEH4AB	EMIOS8	EMIOS15	EMIOS16	EMIOS23	SCI_C_TX	VDD	CAN_B_RX	VDDPLL	W
ETPUA0	EMIOS2	EMIOS5	EMIOS9	EMIOS14	EMIOS17	EMIOS22	CAN_A_RX	VSS	VDD	CAN_B_TX	Y
EMIOS0	EMIOS3	EMIOS6	EMIOS10	EMIOS13	EMIOS18	EMIOS21	VDDEH4AB	WKPCFG	VSS	VDD	AA
TCRCLKA	EMIOS4	EMIOS7	EMIOS11	EMIOS12	EMIOS19	EMIOS20	CAN_A_TX	SCI_B_RX	SCI_B_TX	VSS	AB
12	13	14	15	16	17	18	19	20	21	22	

1 This pin (T21) should be tied low.

Figure 7. 324-pin TEPBGA package ballmap (southeast, viewed from above)

2.4 Signal summary

Table 3. MPC5644A signal properties

Name	Function[1]	PAG[2]	PCR PA Field[3]	PCR[4]	I/O Type	Voltage[5] / Pad Type[6]	Status[7]		Package pin #		
							During Reset	After Reset	176	208	324
GPIO											
EMIOS14[8] GPIO[203]	eMIOS channel GPIO	P G	01 00	203	O I/O	VDDEH7 Slow	— / Up	— / Up	—	—	A15
EMIOS15[8] GPIO[204]	eMIOS channel GPIO	P G	01 00	204	O I/O	VDDEH7 Slow	— / Up	—/ Up	—	—	D14
GPIO[206] ETRIG0	GPIO / eQADC Trigger Input	G	00	206	I/O[9]	VDDEH7 Slow[10]	— / Up	— / Up	143	R4	C14
GPIO[207] ETRIG1	GPIO / eQADC Trigger Input	G	00	207	I/O[9]	VDDEH7 Slow	— / Up	— / Up	144	P5	B14
GPIO[219]	GPIO	G	—	219[11]	I/O	VDDEH7 MultiV[12]	— / Up	— / Up	122	T6	—
Reset / Configuration											
$\overline{\text{RESET}}$	External Reset Input	P	—	—	I	VDDEH6 Slow	$\overline{\text{RESET}}$ / Up	$\overline{\text{RESET}}$ / Up	97	L16	R22
$\overline{\text{RSTOUT}}$	External Reset Output	P	01	230	O	VDDEH6 Slow	$\overline{\text{RSTOUT}}$ / Down	$\overline{\text{RSTOUT}}$ / Down	102	K15	P21
PLLREF $\overline{\text{IRQ}}$[4] ETRIG2 GPIO[208]	FMPLL Mode Selection External Interrupt Request eQADC Trigger Input GPIO	P A1 A2 G	001 010 100 000	208	I I I I/O	VDDEH6 Slow	— / Up	PLLREF / Up	83	M14	V21
PLLCFG1[13] $\overline{\text{IRQ}}$[5] DSPI_D_SOUT GPIO[209]	— External interrupt request DSPI D data output GPIO	— A1 A2 G	— 010 100 000	209	— I O I/O	VDDEH6 Medium	— / Up	— / Up	—	—	U20
RSTCFG GPIO[210]	RSTCFG GPIO	P G	01 00	210	I I/O	VDDEH6 Slow	— / Down	—	—	—	P22
BOOTCFG[0] $\overline{\text{IRQ}}$[2] GPIO[211]	Boot Config. Input External Interrupt Request GPIO	P A1 G	01 10 00	211	I I I/O	VDDEH6 Slow	— / Down	BOOTCFG[0] / Down	—	—	T20

Table 3. MPC5644A signal properties (continued)

Name	Function[1]	PAG[2]	PCR PA Field[3]	PCR[4]	I/O Type	Voltage[5] / Pad Type[6]	Status[7]		Package pin #		
							During Reset	After Reset	176	208	324
ADDR16 FR_A_TX DATA16 GPIO[12]	External address bus Flexray TX data channel A External data bus GPIO	P A1 A2 G	001 010 100 000	12	I/O O I/O I/O	VDDE-EH Medium	— / Up	— / Up	—	—	P3
ADDR17 FR_A_TX_EN DATA17 GPIO[13]	External address bus FlexRay ch. A TX data enable External data bus GPIO	P A1 A2 G	001 010 100 000	13	I/O O I/O I/O	VDDE-EH Medium	— / Up	— / Up	—	—	P4
ADDR18 FR_A_RX DATA18 GPIO[14]	External address bus Flexray RX data ch. A External data bus GPIO	P A1 A2 G	001 010 100 000	14	I/O I I/O I/O	VDDE-EH Medium	— / Up	— / Up	—	—	R1
ADDR19 FR_B_TX DATA19 GPIO[15]	External address bus Flexray TX data ch. B External data bus GPIO	P A1 A2 G	001 010 100 000	15	I/O O I/O I/O	VDDE-EH Medium	— / Up	— / Up	—	—	R2
ADDR20 FR_B_TX_EN DATA20 GPIO[16]	External address bus Flexray TX data enable for ch. B External data bus GPIO	P A1 A2 G	001 010 100 000	16	I/O O I/O I/O	VDDE-EH Medium	— / Up	— / Up	—	—	R4
ADDR21 FR_B_RX DATA21 GPIO[17]	External address bus Flexray RX data channel B External data bus GPIO	P A1 A2 G	001 010 100 000	17	I/O I I/O I/O	VDDE-EH Medium	— / Up	— / Up	—	—	T1
ADDR22 DATA22 GPIO[18]	External address bus External data bus GPIO	P A2 G	001 100 000	18	I/O I/O I/O	VDDE-EH Medium	— / Up	— / Up	—	—	T2
ADDR23 DATA23 GPIO[19]	External address bus External data bus GPIO	P A2 G	001 100 000	19	I/O I/O I/O	VDDE-EH Medium	— / Up	— / Up	—	—	T3
ADDR24 DATA24 GPIO[20]	External address bus External data bus GPIO	P A2 G	001 100 000	20	I/O I/O I/O	VDDE-EH Medium	— / Up	— / Up	—	—	T4
ADDR25 DATA25 GPIO[21]	External address bus External data bus GPIO	P A2 G	001 100 000	21	I/O I/O I/O	VDDE-EH Medium	— / Up	— / Up	—	—	U1

Table 3. MPC5644A signal properties (continued)

Name	Function[1]	PAG[2]	PCR PA Field[3]	PCR[4]	I/O Type	Voltage[5] / Pad Type[6]	Status[7]		Package pin #		
							During Reset	After Reset	176	208	324
MDO2[16]	Nexus message data out	P	01	222	O	VRC33 Fast	—	MDO[2] / —	19	A13	G3
MDO3[16]	Nexus message data out	P	01	223	O	VRC33 Fast	—	MDO[3] / —	20	B13	G4
MDO4[16] ETPUA2_O[8] GPIO[75]	Nexus message data out eTPU A channel (output only) GPIO[	P A1 G	01 10 00	75	O O I/O	VDDEH7 MultiV[12,14]	—	— / —	126	P10	B19
MDO5[16] ETPUA4_O[8] GPIO[76]	Nexus message data out eTPU A channel (output only) GPIO	P A1 G	01 10 00	76	O O I/O	VDDEH7 MultiV[12,14]	—	— / —	129	T10	B20
MDO6[16] ETPUA13_O[8] GPIO[77]	Nexus message data out eTPU A channel (output only) GPIO	P A1 G	01 10 00	77	O O I/O	VDDEH7 MultiV[12,14]	—	— / —	135	T11	C18
MDO7[16] ETPUA19_O[8] GPIO[78]	Nexus message data out eTPU A channel (output only) GPIO	P A1 G	01 10 00	78	O O I/O	VDDEH7 MultiV[12,14]	—	— / —	136	N11	B18
MDO8[16] ETPUA21_O[8] GPIO[79]	Nexus message data out eTPU A channel (output only) GPIO	P A1 G	01 10 00	79	O O I/O	VDDEH7 MultiV[12,14]	—	— / —	137	P11	A18
MDO9[16] ETPUA25_O[8] GPIO[80]	Nexus message data out eTPU A channel (output only) GPIO	P A1 G	01 10 00	80	O O I/O	VDDEH7 MultiV[12,14]	—	— / —	139	T7	D18
MDO10[16] ETPUA27_O[8] GPIO[81]	Nexus message data out eTPU A channel (output only) GPIO	P A1 G	01 10 00	81	O O I/O	VDDEH7 MultiV[12,14]	—	— / —	134	R10	A19
MDO11[16] ETPUA29_O[8] GPIO[82]	Nexus message data out eTPU A channel (output only) GPIO[82]	P A1 G	01 10 00	82	O O I/O	VDDEH7 MultiV[12,14]	—	— / —	124	P9	C19
$\overline{\text{MSEO}}$[0][16]	Nexus message start/end out	P	01	224	O	VDDEH7 MultiV[12,14]	—	$\overline{\text{MSEO}}$[0] / —	118	C15	G21
$\overline{\text{MSEO}}$[1][16]	Nexus message start/end out	P	01	225	O	VDDEH7 MultiV[12,14]	—	$\overline{\text{MSEO}}$[1] / —	117	E16	G22
$\overline{\text{RDY}}$	Nexus ready output	P	01	226	O	VDDEH7 MultiV[12,14]	—	—	—	—	G19
JTAG											

Table 3. MPC5644A signal properties (continued)

Name	Function[1]	PAG[2]	PCR PA Field[3]	PCR[4]	I/O Type	Voltage[5] / Pad Type[6]	Status[7]		Package pin #		
							During Reset	After Reset	176	208	324
ETPUA25 IRQ[13] DSPI_C_SCK_LVDS+ GPIO[139]	eTPU A channel External interrupt request LVDS positive DSPI clock GPIO	P A1 A2 G	001 010 100 000	139	I/O I O I/O	VDDEH1 Medium + LVDS	— / WKPCFG	— / WKPCFG	27	G3	M3
ETPUA26 IRQ[14] DSPI_C_SOUT_LVDS- GPIO[140]	eTPU A channel External interrupt request LVDS negative DSPI data out GPIO	P A1 A2 G	001 010 100 000	140	I/O I O I/O	VDDEH1 Slow + LVDS	— / WKPCFG	— / WKPCFG	26	F3	L2
ETPUA27 IRQ[15] DSPI_C_SOUT_LVDS+ DSPI_B_SOUT GPIO[141]	eTPU A channel External interrupt request LVDS positive DSPI data out DSPI data out GPIO	P A1 A2 A3 G	0001 0010 0100 1000 0000	141	I/O I O O I/O	VDDEH1 Slow + LVDS	— / WKPCFG	— / WKPCFG	25	G2	L1
ETPUA28 DSPI_C_PCS[1] RCH5_B GPIO[142]	eTPU A channel DSPI C peripheral chip select Reaction channel 5B GPIO	P A1 A2 G	001 010 100 000	142	I/O O O I/O	VDDEH1 Medium	— / WKPCFG	— / WKPCFG	24	F1	M4
ETPUA29 DSPI_C_PCS[2] RCH5_C GPIO[143]	eTPU A channel DSPI C peripheral chip select Reaction channel 5C GPIO	P A1 A2 G	001 010 100 000	143	I/O O O I/O	VDDEH1 Medium	— / WKPCFG	— / WKPCFG	23	F2	L3
ETPUA30 DSPI_C_PCS[3] ETPUA11_O[8] GPIO[144]	eTPU A channel DSPI C peripheral chip select eTPU A channel (output only) GPIO	P A1 A2 G	001 010 100 000	144	I/O O O I/O	VDDEH1 Medium	— / WKPCFG	— / WKPCFG	22	E1	L4
ETPUA31 DSPI_C_PCS[4] ETPUA13_O[8] GPIO[145]	eTPU A channel DSPI C peripheral chip select eTPU A channel (output only) GPIO	P A1 A2 G	001 010 100 000	145	I/O O O I/O	VDDEH1 Medium	— / WKPCFG	— / WKPCFG	21	E2	K1
eMIOS											
EMIOS0 ETPUA0_O[8] ETPUA25_O[8] GPIO[179]	eMIOS channel eTPU A channel (output only) eTPU A channel (output only) GPIO	P A1 A2 G	001 010 100 000	179	I/O O O I/O	VDDEH4 Slow	— / Up	— / Up	63	T4	AA12

Table 3. MPC5644A signal properties (continued)

Name	Function[1]	PAG[2]	PCR PA Field[3]	PCR[4]	I/O Type	Voltage[5] / Pad Type[6]	Status[7]		Package pin #		
							During Reset	After Reset	176	208	324
EMIOS11 DSPI_D_PCS[4] RCH3_C GPIO[190]	eMIOS channel DSPI D peripheral chip select Reaction channel 3C GPIO	P A1 A2 G	001 010 100 000	190	I/O O O I/O	VDDEH4 Medium	— / WKPCFG	— / WKPCFG	75	R8	AB15
EMIOS12 DSPI_C_SOUT ETPUA27_O[8] GPIO[191]	eMIOS channel DSPI C data output eTPU A channel (output only) GPIO	P A1 A2 G	001 010 100 000	191	I/O O O I/O	VDDEH4 Medium	— / WKPCFG	— / WKPCFG	76	N10	AB16
EMIOS13 DSPI_D_SOUT GPIO[192]	eMIOS channel DSPI D data output GPIO	P A1 G	01 10 00	192	I/O O I/O	VDDEH4 Medium	— / WKPCFG	— / WKPCFG	77	T8	AA16
EMIOS14 IRQ[0] ETPUA29_O[8] GPIO[193]	eMIOS channel External interrupt request eTPU A channel (output only) GPIO	P A1 A2 G	001 010 100 000	193	I/O I O I/O	VDDEH4 Slow	— / Down	— / Down	78	R9	Y16
EMIOS15 IRQ[1] GPIO[194]	eMIOS channel External interrupt request GPIO	P A1 G	01 10 00	194	I/O I I/O	VDDEH4 Slow	— / Down	— / Down	79	T9	W16
EMIOS16 GPIO[195]	eMIOS channel GPIO	P G	01 00	195	I/O I/O	VDDEH4 Slow	— / Up	— / Up	—	—	W17
EMIOS17 GPIO[196]	eMIOS channel GPIO	P G	01 00	196	I/O I/O	VDDEH4 Slow	— / Up	— / Up	—	—	Y17
EMIOS18 GPIO[197]	eMIOS channel GPIO	P G	01 00	197	I/O I/O	VDDEH4 Slow	— / Up	— / Up	—	—	AA17
EMIOS19 GPIO[198]	eMIOS channel GPIO	P G	01 00	198	I/O I/O	VDDEH4 Slow	— / WKPCFG	— / WKPCFG	—	—	AB17
EMIOS20 GPIO[199]	eMIOS channel GPIO	P G	01 00	199	I/O I/O	VDDEH4 Slow	— / WKPCFG	— / WKPCFG	—	—	AB18
EMIOS21 GPIO[200]	eMIOS channel GPIO	P G	01 00	200	I/O I/O	VDDEH4 Slow	— / WKPCFG	— / WKPCFG	—	—	AA18
EMIOS22 GPIO[201]	eMIOS channel GPIO	P G	01 00	201	I/O I/O	VDDEH4 Slow	— / Down	— / Down	—	—	Y18
EMIOS23 GPIO[202]	eMIOS channel GPIO	P G	01 00	202	I/O I/O	VDDEH4 Slow	— / Down	— / Down	80	R11	W18
Clock Synthesizer											

Table 3. MPC5644A signal properties (continued)

Name	Function[1]	PAG[2]	PCR PA Field[3]	PCR[4]	I/O Type	Voltage[5] / Pad Type[6]	Status[7]		Package pin #		
							During Reset	After Reset	176	208	324
VDDE12	External supply input for calibration bus interfaces	—		—	I	1.8 V - 3.3 V	I / —	VDDE12	—	—	—
VDDE2[23]	External supply input for EBI interfaces	—		—	I	1.8 V - 3.3 V	I / —	VDDE2[24]	—	—	M9, M10
VDDE5	External supply input for ENGCLK, CLKOUT and EBI signals DATA[0:15]	—		—	I	1.8 V - 3.3 V	I / —	VDDE5	—	T13	N11, W5, W8
VDDE-EH	External supply for EBI interfaces	—		—	I	3.0 V - 5 V	I / —	VDDE-EH	—	—	R3, V2
VDDEH1A[25]	I/O Supply Input	—		—	I	3.3 V - 5.0 V	I / —	VDDEH1A[25]	31	—	—
VDDEH1B[25]	I/O Supply Input	—		—	I	3.3 V - 5.0 V	I / —	VDDEH1B[25]	41	—	—
VDDEH1AB[25]	I/O Supply Input	—		—	I	3.3 V - 5.0 V	I / —	VDDEH1AB[25]	—	K4	K4
VDDEH4[26]	I/O Supply Input	—		—	I	3.3 V - 5.0 V	I / —	VDDEH4[26]	—	—	—
VDDEH4A[26]	I/O Supply Input	—		—	I	3.3 V - 5.0 V	I / —	VDDEH4A[26]	55	—	—
VDDEH4B[26]	I/O Supply Input	—		—	I	3.3 V - 5.0 V	I / —	VDDEH4B[26]	74	—	—
VDDEH4AB[26]	I/O Supply Input	—		—	I	3.3 V - 5.0 V	I / —	VDDEH4AB[26]	—	N9	W14, AA19
VDDEH6[27]	I/O Supply Input	—		—	I	3.3 V - 5.0 V	I / —	VDDEH6[27]	—	—	—
VDDEH6A[27]	I/O Supply Input	—		—	I	3.3 V - 5.0 V	I / —	VDDEH6A[27]	95	—	—
VDDEH6B[27]	I/O Supply Input	—		—	I	3.3 V - 5.0 V	I / —	VDDEH6B[27]	110	—	—
VDDEH6AB[27]	I/O Supply Input	—		—	I	3.3 V - 5.0 V	I / —	VDDEH6AB[27]	—	F13	M22, U19

Table 3. MPC5644A signal properties (continued)

Name	Function[1]	PAG[2]	PCR PA Field[3]	PCR[4]	I/O Type	Voltage[5] / Pad Type[6]	Status[7]		Package pin #		
							During Reset	After Reset	176	208	324
VDDEH7	I/O Supply Input	—		—	I	3.3 V - 5.0 V	I / —	VDDEH7	—	D12	B22, C21, D15, D20, E19, F19, H19, J14
VDDEH7A	I/O Supply Input	—		—	I	3.3 V - 5.0 V	I / —	VDDEH7A	125	—	—
VDDEH7B	I/O Supply Input	—		—	I	3.3 V - 5.0 V	I / —	VDDEH7B	138	—	—
VSS	Ground	—		—	I	—	I / —	VSS	15, 29, 43, 57, 72, 90, 94, 96, 108, 115, 127, 133, 140	A1, A16, B2, B15, C3, C14, D4, D13, G7, G8, G9, G10, H7, H8, H9, H10, J7, J8, J9, J10, K7, K8, K9, K10, M16, N4, N13, P3, P14, R2, R15, T1, T16	A1, A22, B2, B21, C3, C20, D4, D17, D19, F21, H21, J9, J10, J11, J12, J13, K9, K10, K11, K12, K13, K14, L9, L10, L11, L12, L13, L14, L21, M11, M12, M13, M14, N9, N10, N12, N13, N14, N21, P9, P10, P12, P13, P14, T19, T21, T22, W4, Y3, Y20, AA21, AB1, AB22

1 For each pin in the table, each line in the Function column is a separate function of the pin. For all I/O pins the selection of primary pin function or secondary function or GPIO is done in the SIU except where explicitly noted. See the Signal details table for a description of each signal.

2 The P/A/G column indicates the position a signal occupies in the muxing order for a pin—Primary, Alternate 1, Alternate 2, Alternate 3, or GPIO. Signals are selected by setting the PA field value in the appropriate PCR register in the SIU module. The PA field values are as follows: P - 0b0001, A1 - 0b0010, A2 - 0b0100, A3 - 0b1000, or G - 0b0000. Depending on the register, the PA field size can vary in length. For PA fields having fewer than four bits, remove the appropriate number of leading zeroes from these values.

3 The Pad Configuration Register (PCR) PA field is used by software to select pin function.

4 Values in the PCR No. column refer to registers in the System Integration Unit (SIU). The actual register name is “SIU_PCR” suffixed by the PCR number. For example, PCR[190] refers to the SIU register named SIU_PCR190.

Table 4. Pad types

Pad Type	Name	I/O Voltage Range
Slow	pad_ssr_hv	3.0V - 5.5 V
Medium	pad_msr_hv	3.0 V - 5.5 V
Fast	pad_fc	3.0 V - 3.6 V
MultiV[1,2]	pad_multv_hv	3.0 V - 5.5 V (high swing mode) 3.0 V - 3.6 V (low swing mode)
Analog	pad_ae_hv	0.0 - 5.5 V
LVDS	pad_lo_lv	—

1 Multivoltage pads are automatically configured in low swing mode when a JTAG or Nexus function is selected, otherwise they are high swing.

2 VDDEH7 supply cannot be below 4.5 V when in low-swing mode.

2.5 Signal details

Table 5. Signal details

Signal	Module or Function	Description
CLKOUT	Clock Generation	MPC5644A clock output for the external/calibration bus interface
ENGCLK	Clock Generation	Clock for external ASIC devices
EXTAL	Clock Generation	Input pin for an external crystal oscillator or an external clock source based on the value driven on the PLLREF pin at reset.
PLLREF	Clock Generation Reset/Configuration	PLLREF is used to select whether the oscillator operates in xtal mode or external reference mode from reset. PLLREF=0 selects external reference mode. On the 324BGA package, PLLREF is bonded to the ball used for PLLCFG[0] for compatibility with MPC55xx devices . For the 176-pin QFP and 208-ball BGA packages: 0: External reference clock is selected. 1: XTAL oscillator mode is selected For the 324 ball BGA package: If RSTCFG is 0: 0: External reference clock is selected. 1: XTAL oscillator mode is selected. If RSTCFG is 1, XTAL oscillator mode is selected.
XTAL	Clock Generation	Crystal oscillator input
DSPI_B_SCK_LVDS- DSPI_B_SCK_LVDS+	DSPI	LVDS pair used for DSPI_B TSB mode transmission
DSPI_B_SOUT_LVDS- DSPI_B_SOUT_LVDS+	DSPI	LVDS pair used for DSPI_B TSB mode transmission
DSPI_C_SCK_LVDS- DSPI_C_SCK_LVDS+	DSPI	LVDS pair used for DSPI_C TSB mode transmission

Table 6. Power/ground segmentation

Power Segment	Voltage	I/O Pins Powered by Segment
VDDE2	1.8 V - 3.3 V	CS0, CS1, CS2, CS3,RD_WR, BDIP, WE0, WE1, OE, TS, TA
VDDE3	1.8 V - 3.3 V	ADDR12, ADDR13, ADDR14, ADDR15
VDDE5	1.8 V - 3.3 V	DATA0, DATA1, DATA2, DATA3, DATA4, DATA5, DATA6, DATA7, DATA8, DATA9, DATA10, DATA11, DATA12, DATA13, DATA14, DATA15, CLKOUT, ENGCLK
VDDE12	1.8 V - 3.3 V	CAL_CS0, CAL_CS2, CAL_CS3 CAL_ADDR12, CAL_ADDR13, CAL_ADDR14, CAL_ADDR15, CAL_ADDR16, CAL_ADDR17, CAL_ADDR18, CAL_ADDR19, CAL_ADDR20, CAL_ADDR21, CAL_ADDR22, CAL_ADDR23, CAL_ADDR24, CAL_ADDR25, CAL_ADDR26, CAL_ADDR27, CAL_ADDR28, CAL_ADDR29, CAL_ADDR30, CAL_DATA0, CAL_DATA1, CAL_DATA2, CAL_DATA3, CAL_DATA4, CAL_DATA5, CAL_DATA6, CAL_DATA7, CAL_DATA8, CAL_DATA9, CAL_DATA10, CAL_DATA11, CAL_DATA12, CAL_DATA13, CAL_DATA14, CAL_DATA15, CAL_RD_WR, CAL_WE0, CAL_WE1, CAL_OE, CAL_TS
VDDE-EH	3.0 V - 5 V	ADDR16, ADDR17, ADDR18, ADDR19, ADDR20, ADDR21, ADDR22, ADDR23, ADDR24, ADDR25, ADDR26, ADDR27, ADDR28, ADDR29, ADDR30, ADDR31
VDDEH1	3.3 V - 5.0 V	ETPUA10, ETPUA11, ETPUA12, ETPUA13, ETPUA14, ETPUA15, ETPUA16, ETPUA17, ETPUA18, ETPUA19, ETPUA20, ETPUA21, ETPUA22, ETPUA23, ETPUA24, ETPUA25, ETPUA26, ETPUA27, ETPUA28, ETPUA29, ETPUA30, ETPUA31
VDDEH4	3.3 V - 5.0 V	EMIOS0, EMIOS1, EMIOS2, EMIOS3, EMIOS4, EMIOS5, EMIOS6, EMIOS7, EMIOS8, EMIOS9, EMIOS10, EMIOS11, EMIOS12, EMIOS13, EMIOS14, EMIOS15, EMIOS16, EMIOS17, EMIOS18, EMIOS19, EMIOS20, EMIOS21, EMIOS22, EMIOS23, TCRCLKA, ETPUA0, ETPUA1, ETPUA2, ETPUA3, ETPUA4, ETPUA5, ETPUA6, ETPUA7, ETPUA8, ETPUA9, ETPUA0
VDDEH6	3.3 V - 5.0 V	$\overline{\text{RESET}}$, $\overline{\text{RSTOUT}}$, PLLREF, PLLCFG1, RSTCFG, BOOTCFG0, BOOTCFG1, WKPCFG, CAN_A_TX, CAN_A_RX, CAN_B_TX, CAN_B_RX, CAN_C_TX, CAN_C_RX, SCI_A_TX, SCI_A_RX, SCI_B_TX, SCI_C_RX, DSPI_B_SCK, DSPI_B_SIN, DSPI_B_SOUT, DSPI_B_PCS[0], DSPI_B_PCS[1], DSPI_B_PCS[2], DSPI_B_PCS[3], DSPI_B_PCS[4], DSPI_B_PCS[5], SCI_B_RX, SCI_C_TX, EXTAL, XTAL
VDDEH7	3.3 V - 5.0 V	EMIOS14, EMIOS 15, GPIO98, GPIO99, GPIO203, GPIO204, GPIO206, GPIO207, GPIO219, EVTI, EVTO, MDO4, MDO5, MDO6, MDO7, MDO8, MDO9, MDO10, MDO11, MSEO0, MSEO1, RDY, TCK, TDI, TDO, TMS, JCOMP, DSPI_A_SCK, DSPI_A_SIN, DSPI_A_SOUT, DSPI_A_PCS[0], DSPI_A_PCS[1], DSPI_A_PCS[4], DSPI_A_PCS[5], AN12-SDS, AN13-SDO, AN14-SDI, AN15-FCK

Table 15. PMC Electrical Characteristics

ID	Name			Parameter	Min	Typ	Max	Unit	Notes
1	VBG	CC	C	Nominal bandgap voltage reference	—	1.219	—	V	
1a	—	CC	P	Untrimmed bandgap reference voltage	VBG - 7%	VBG	Vbg + 6%	V	
1b	—	CC	P	Trimmed bandgap reference voltage (5 V, 27 °C)	VBG -10mV	VBG	VBG + 10mV	V	
1c	—	CC	C	Bandgap reference temperature variation	—	100	—	ppm /°C	
1d	—	CC	C	Bandgap reference supply voltage variation	—	3000	—	ppm /V	
2	Vdd	CC	C	Nominal V_{DD} core supply internal regulator target DC output voltage[1]	—	1.28	—	V	
2a	—	CC	P	Nominal V_{DD} core supply internal regulator target DC output voltage variation at power-on reset	Vdd - 6%	Vdd	Vdd + 10%	V	
2b	—	CC	P	Nominal V_{DD} core supply internal regulator target DC output voltage variation after power-on reset	Vdd - 10%[2]	Vdd	Vdd + 3%	V	
2c	—	CC	C	Trimming step Vdd	—	20	—	mV	
2d	Ivrcctl	CC	C	Voltage regulator controller for core supply maximum DC output current	20	—	—	mA	
3	Lvi1p2	CC	C	Nominal LVI for rising core supply[3]	—	1.160	—	V	
3a	—	CC	C	Variation of LVI for rising core supply at power-on reset	1.120	1.200	1.280	V	See note [4]
3b	—	CC	C	Variation of LVI for rising core supply after power-on reset	Lvi1p2 - 3%	Lvi1p2	Lvi1p2 + 3%	V	See note 4
3c	—	CC	C	Trimming step LVI core supply	—	20	—	mV	
3d	Lvi1p2_h	CC	C	LVI core supply hysteresis	—	40	—	mV	
4	Por1.2V_r	CC	C	POR 1.2 V rising	—	0.709	—	V	
4a	—	CC	C	POR 1.2 V rising variation	Por1.2V_r - 35%	Por1.2V_r	Por1.2V_r + 35%	V	
4b	Por1.2V_f	CC	C	POR 1.2 V falling	—	0.638	—	V	
4c	—	CC	C	POR 1.2 V falling variation	Por1.2V_f - 35%	Por1.2V_f	Por1.2V_f+ 35%	V	

3.17.2 IEEE 1149.1 interface timing

Table 38. JTAG pin AC electrical characteristics[1]

#	Symbol		C	Characteristic	Min. Value	Max. Value	Unit
1	t_{JCYC}	CC	D	TCK Cycle Time	100	—	ns
2	t_{JDC}	CC	D	TCK Clock Pulse Width	40	60	ns
3	$t_{TCKRISE}$	CC	D	TCK Rise and Fall Times (40% - 70%)	—	3	ns
4	t_{TMSS}, t_{TDIS}	CC	D	TMS, TDI Data Setup Time	5	—	ns
5	t_{TMSH}, t_{TDIH}	CC	D	TMS, TDI Data Hold Time	25	—	ns
6	t_{TDOV}	CC	D	TCK Low to TDO Data Valid	—	22[2]	ns
7	t_{TDOI}	CC	D	TCK Low to TDO Data Invalid	0	—	ns
8	t_{TDOHZ}	CC	D	TCK Low to TDO High Impedance	—	22	ns
9	t_{JCMPPW}	CC	D	JCOMP Assertion Time	100	—	ns
10	t_{JCMPS}	CC	D	JCOMP Setup Time to TCK Low	40	—	ns
11	t_{BSDV}	CC	D	TCK Falling Edge to Output Valid	—	50	ns
12	t_{BSDVZ}	CC	D	TCK Falling Edge to Output Valid out of High Impedance	—	50	ns
13	t_{BSDHZ}	CC	D	TCK Falling Edge to Output High Impedance	—	50	ns
14	t_{BSDST}	CC	D	Boundary Scan Input Valid to TCK Rising Edge	25[3]	—	ns
15	t_{BSDHT}	CC	D	TCK Rising Edge to Boundary Scan Input Invalid	25[3]	—	ns

1 JTAG timing specified at V_{DD} = 1.14 V to 1.32 V, V_{DDEH} = 4.5 V to 5.5 V with multi-voltage pads programmed to Low-Swing mode, $T_A = T_L$ to T_H, and C_L = 30 pF with DSC = 0b10, SRC = 0b11. These specifications apply to JTAG boundary scan only. See Table 39 for functional specifications.

2 Pad delay is 8–10 ns. Remainder includes TCK pad delay, clock tree delay logic delay and TDO output pad delay.

3 For 20 MHz TCK.

NOTE

The Nexus/JTAG Read/Write Access Control/Status Register (RWCS) write (to begin a read access) or the write to the Read/Write Access Data Register (RWD) (to begin a write access) does not actually begin its action until 1 JTAG clock (TCK) after leaving the JTAG Update-DR state. This prevents the access from being performed and therefore will not signal its completion via the READY (RDY) output unless the JTAG controller receives an additional TCK. In addition, EVTI is not latched into the device unless there are clock transitions on TCK.

Table 39. Nexus debug port timing[1] (continued)

#	Symbol		C	Characteristic	Min. Value	Max. Value	Unit
11	t_{NTDIS}	CC	D	TDI Data Setup Time	5	—	ns
12	t_{NTDIH}	CC	D	TDI Data Hold Time	25	—	ns
13	t_{NTMSS}	CC	D	TMS Data Setup Time	5	—	ns
14	t_{NTMSH}	CC	D	TMS Data Hold Time	25	—	ns
15	—	CC	D	TDO propagation delay from falling edge of TCK	—	19.5	ns
16	—	CC	D	TDO hold time with respect to TCK falling edge (minimum TDO propagation delay)	5.25	—	ns

1 All Nexus timing relative to MCKO is measured from 50% of MCKO and 50% of the respective signal. Nexus timing specified at V_{DD} = 1.14 V to 1.32 V, V_{DDEH} = 4.5 V to 5.5 V with multi-voltage pads programmed to Low-Swing mode, $T_A = T_L$ to T_H, and C_L = 30 pF with DSC = 0b10.

2 Achieving the absolute minimum MCKO cycle time may require setting the MCKO divider to more than its minimum setting (NPC_PCR[MCKO_DIV] depending on the actual system frequency being used.

3 This is a functionally allowable feature. However, this may be limited by the maximum frequency specified by the Absolute minimum MCKO period specification.

4 This may require setting the MCO divider to more than its minimum setting (NPC_PCR[MCKO_DIV]) depending on the actual system frequency being used.

5 MDO, $\overline{\text{MSEO}}$, and $\overline{\text{EVTO}}$ data is held valid until next MCKO low cycle.

6 Achieving the absolute minimum TCK cycle time may require a maximum clock speed (system frequency / 8) that is less than the maximum functional capability of the design (system frequency / 4) depending on the actual system frequency being used.

7 This is a functionally allowable feature. However, this may be limited by the maximum frequency specified by the Absolute minimum TCK period specification.

8 This may require a maximum clock speed (system frequency / 8) that is less than the maximum functional capability of the design (system frequency / 4) depending on the actual system frequency being used.

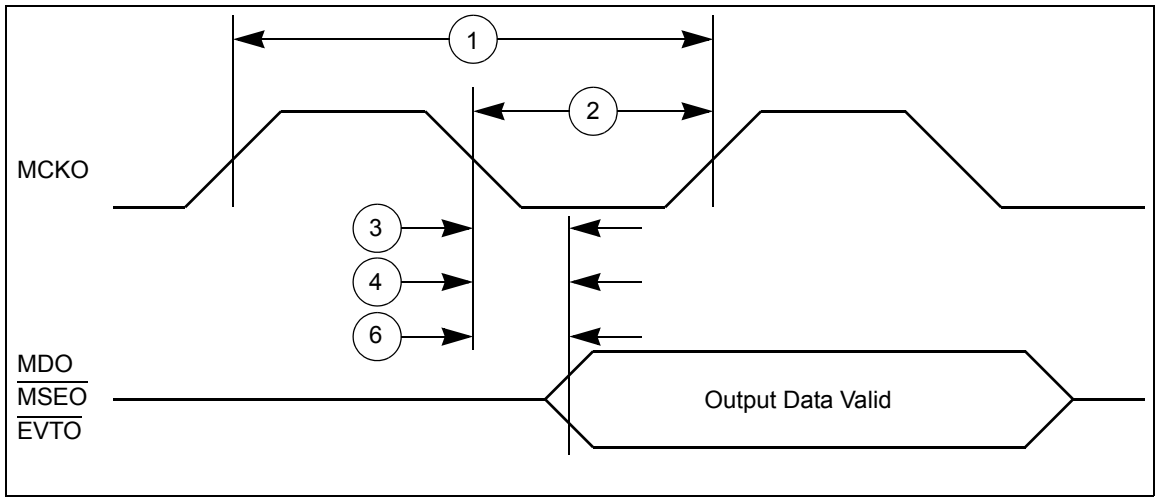


Figure 15. Nexus output timing

Table 53. Revision history (continued)

Revision	Date	Substantive changes
Rev. 3 (cont)	04/2010	Changes to Power/ground segmentation table: • ADDR[20:21] removed from VDDE2 segment; they are in VDDE-EH • CAL_CS1 removed from VDDE12 segment (there is no CAL_CS1 on this device) • CAL_EVTO and CAL_MCKO removed from VDDE12 segment. Those pins do not exist • VDDE-VDDEH renamed to VDDE-EH • EMIOS24 removed from VDDEH segment. That pin does not exist. • ETPUA[0:9] added to VDDEH4 segment • Renamed TCR_A in VDDEH4 segment to TCRCLKA. • EXTAL and XTAL added to VDDEH6 segment • AN15-FCK added to VDDEH7 segment • GPIO98, GPIO99, GPIO206, GPIO207 and GPIO219 added to VDDEH7 segment. • MSEO1 added to VDDEH7 segment • Power segment VDDEH1A renamed to VDDEH1 Changes to 176-pin package pinout: • Changed pin 9 from AN38 to AN8. • Added note that pin 96 (VSS) should be tied low. Changes to 208-ball package ballmap: • Changed ball B3 from AN38 to AN8. • Added note that ball N13 (VSS) should be tied low. 324-ball package ballmap updated for Rev. 2 silicon: • AN8 was on ball D3; it is now on E1 • AN38 was on ball E1; it is now on D3 Changes to features list: • Correction: there are 6 reaction channels (was noted as 5) • Development Trigger Semaphore (DTS) added to features list and feature details • FlexRay module now has 128 message buffers (was 64) and ECC support Added note after JTAG pin AC electrical characteristics table detailing JTAG EVTI and RDY signal clocking with TCK. This affects debuggers. Part numbers and part number decoder updated.

Table 53. Revision history (continued)

Revision	Date	Substantive changes
Rev. 5	2/2011	• Minor editorial updates. • Re-organized the first few subsections of the “Overview” section. • Added ECSM to the block diagram. • Added information on the REACM, SIU, and ECS modules to the “Block summary” section. • Added DATA[0:15] to V_{DDE5} in the “signal properties” table. • Updated VSTBY parameters in the “Power/ground segmentation” table. • Updated the parameter symbols and classifications throughout the document. • Updated footnote instances in the “Absolute maximum ratings” table. • Removed I_{MAXA} footnote in the “Absolute Maximum Ratings” table. • Updated the format of the “EMI (electromagnetic interference) characteristics” table. • Removed the footnote on V_{DDREG} in the “Power management control (PMC) and power on reset (POR) electrical specifications” table. • Updated values for Vbg, Idd3p3, Por3.3V_r, Por3.3V_f, Por5V_r, and Por5V_f in the “PMC electrical characteristics” table. • Updated “Bandgap reference supply voltage variation” in the “PMC Electrical Characteristics” table. • Updated VCE_{SAT} and V_{BE}in the “Recommended power transistors” operating characteristics” table. • Updated V_{IH_LS} in the “DC electrical specifications” table. • Updated the V_{OH_LS} min value in the “DC electrical specifications” table. • Updated I_{DDSTBY} and $I_{DDSTBY150}$ in the “DC electrical specifications” table. • Updated the $I_{DDA}/I_{REF}/I_{DDREG}$ max value in the “DC electrical specifications” table. • Updated I_{ACT_F}, $I_{ACT\_MV\_PU}$, $I_{ACT\_MV\_PD}$, R_{PUPD5K}, $R_{PUPDMTCH}$, and footnotes in the “DC electrical specifications” table. • Updated Medium pad type I_{DD33} values in the “I/O pad V_{RC33} average I_{DDE} specifications” table. • Updated values for V_{OD} in the “DSPI LVDS pad specification” table. • Removed the footnotes from the “DSPI LVDS pad specifications” table. • Removed the redundant “XTAL Load Capacitance” parameter instance from the “PLLMRFM electrical specifications” table. • Updated footnotes in the “PLLMRFM electrical specifications” table. • Updated values for OFFNC and GAINNC in the “eQADC conversion specifications (operating)” table. • Added $DIFF_{max}$, $DIFF_{max2}$, $DIFF_{max4}$, and $DIFF_{cmv}$ parameters to the “eQADC conversion specifications (operating)” table. • Added the maximum operating frequency values in the “Cutoff frequency for additional SRAM wait state” table. • Updated multiple entries in the “APC, RWSC, WWSC settings vs. frequency of operation” table. • Removed footnote in the “APC, RWSC, WWSC settings vs. frequency of operation” table. • Changed the voltage in the “Pad AC specifications” table title from 4.5 V to 5.0 V. • Added the maximum LH/HL output delay values for pad type MultiV in the “Pad AC specifications (V_{DDE} = 3.3 V)” table.
Rev. 6	—	• Rev. 6 not published.

Table 53. Revision history (continued)

Revision	Date	Substantive changes
Rev. 7	01/2012	• Minor editorial changes. • In MPC5644A feature list, moved “24 unified channels” after “1 x eMIOS”. • In Table 3MPC5644A signal properties/Column “Name” updated the following rows: DSPI_D_SCK /GPIO [98] -Changed “-” to CS[2] DSPI_D_SIN /GPIO[99] -Changed “-” to CS[3]. • In Table 11Thermal characteristics for 324-pin TEPBGA/ Column “Value” added conditional text. • In Table 21DC electrical specifications made the following changes: -For the value “V_{OL_S}” parameter changed from “Slow/ medium/multi-voltage pad I/O output low voltage” to “Slow/medium pad I/O output low voltage”. -Added a new row for “$I_{DDSTBY27}$”. -For row “I_{DDSTBY}(operating current 0.95 -1.2V)” added max value “100” and changed typ value from “125” to “35”. -For row “I_{DDSTBY} (operating current 2 - 5.5V)” added max value “110” and changed typ value from “135” to “45”. -For symbol “$I_{DDSTBY\ 150}$(operating current 0.95 -1.2V)” added max value “2000”, changed typ value from “1050” to “790”,C cell changed from “T” to “P” and for symbol “I_{DDSTBY} (operating current 2 - 5.5V)” added max value “2000”, changed typ value from “1050” to “760”, C cell changed from “T” to “P”. -Removed note 9 and note 10 (Characterization based capability) from symbol “V_{OL_HS}”. • Splitted Table 28eQADC conversion specifications (operating)into Table 29eQADC single ended conversion specifications (operating) and Table 30eQADC differential ended conversion specifications (operating). • In Table 30 eQADC differential ended conversion specifications (operating)made the following changes: -Added the note of $DIFF_{cmv}$ on all of the DIFF specs. -Min value changed from (VRH-VRL)/2-5% to (VRH+VRL)/2-5 % and max value changed from (VRH-VRL)/2+5 % to (VRH+VRL)/2+5 %for DIFFcmv. • In Table 31 Cutoff frequency for additional SRAM wait statemade the following changes: -Added note “Max frequencies including 2% PLL FM”. -Max operating frequency changed from “96” to “98” and “150” to “153”. • In Section 3.13, “Configuring SRAM wait states, changed text from “MPC5644A Microcontroller Reference Manual “ to “device reference manual”. • In Table 32APC, RWSC, WWSC settings vs. frequency of operation, - Added note for “Max Flash Operating Frequency(MHz). - Changed values from 30, 60,120, 150 to 20,61,123, 153 respectively in Max Flash Operating Frequency (MHz). • In Table 33,aFlash program and erase specificationsdded two parameter “T_{psrt}” and “T_{esrt}”. • In Table 41External Bus Interface maximum operating frequency, replacedthe <= symbol in notes with ≤ • Added note “Refer to table DSPI timing for the numbers” in all the figures under Section 3.17.8, “DSPI timing . • In Table 52Orderable part number summary, changed LBGA208 to MAPBGA and changed all packages to 123XXXX format.