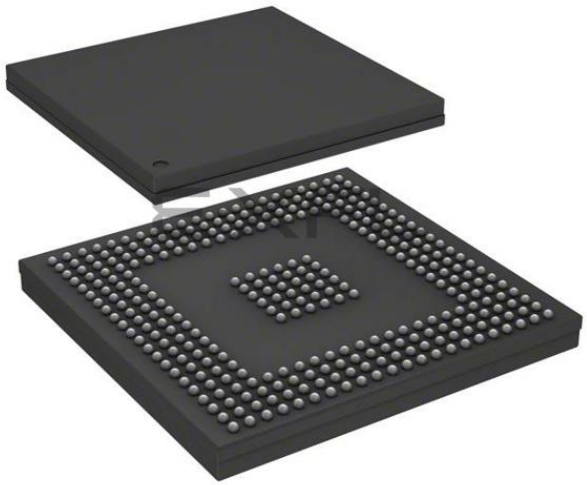

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, EBI/EMI, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	151
Program Memory Size	4MB (4M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	1.14V ~ 5.25V
Data Converters	A/D 40x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	324-BBGA
Supplier Device Package	324-PBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5644af0mvz3r

1.3 Device comparison

Table 1 summarizes the MPC5644A and compares it to the MPC5634M.

Table 1. MPC5644A, MPC5634M and MPC5642A comparison

Feature		MPC5644A	MPC5634M	MPC5642A
Process		90 nm		
Core		e200z4	e200z3	e200z4
	SIMD	Yes		
	VLE	Yes		
	Cache	8 KB instruction	No	8 KB instruction
	Non-Maskable Interrupt (NMI)	NMI & Critical Interrupt		
	MMU	24 entry	16 entry	24 entry
	MPU	16 entry	No	16 entry
	Crossbar switch	5 × 4	3 × 4	4 × 4
	Core performance	0–150 MHz	0–80 MHz	0–150 MHz
Windowing software watchdog		Yes		
Core Nexus		Class 3+	Class 2+	Class 3+
SRAM		192 KB	94 KB	128 KB
Flash		4 MB	1.5 MB	2 MB
Flash fetch accelerator		4 × 256-bit	4 × 128-bit	
External bus		16-bit (incl 32-bit muxed)	None	
Calibration bus		16-bit (incl 32-bit muxed)	16-bit	16-bit (incl 32-bit muxed)
DMA		64 ch.	32 ch.	64 ch.
DMA Nexus		None		
Serial		3	2	3
	eSCI_A	Yes (MSC Uplink)		
	eSCI_B	Yes (MSC Uplink)		
	eSCI_C	Yes	No	Yes
CAN		3	2	3
	CAN_A	64 buf		
	CAN_B	64 buf	No	64 buf
	CAN_C	64 buf	32 buf	64 buf
SPI		3	2	3

Table 1. MPC5644A, MPC5634M and MPC5642A comparison (continued)

Feature		MPC5644A	MPC5634M	MPC5642A
	Micro Second Channel (MSC) bus downlink	Yes		
	DSPI_A	No		
	DSPI_B	Yes (with LVDS)		
	DSPI_C	Yes (with LVDS)		
	DSPI_D	Yes	No	Yes
FlexRay		Yes	No	Yes
System timers		5 PIT channels 4 STM channels 1 Software Watchdog		
eMIOS		24 ch.	16 ch.	24 ch.
eTPU		32 ch. eTPU2		
	Code memory	14 KB		
	Data memory	3 KB		
Interrupt controller		486 ch.[1]	307 ch.	486 ch.[1]
ADC		40 ch.	34 ch.	40 ch.
	ADC_A	Yes		
	ADC_B	Yes		
	Temp sensor	Yes		
	Variable gain amp.	Yes		
	Decimation filter	2	1	2
	Sensor diagnostics	Yes		
CRC		Yes	No	Yes
FMPLL		Yes		
VRC		Yes		
Supplies		5 V, 3.3 V[2]	5 V, 3.3 V[3]	5 V, 3.3 V[2]
Low-power modes		Stop Mode Slow Mode		
Packages		176 LQFP[4] 208 MAPBGA[4,5] 324 TEPBGA324[6] 496-pin CSP[7]	144 LQFP 176 LQFP 208 MAPBGA 496-pin CSP[7]	176 LQFP[4] 208 MAPBGA[4,5] 324 TEPBGA324[6] 496-pin CSP[7]

1 199 interrupt vectors are reserved.

2 5 V single supply only for 176 LQFP.

3 5 V single supply only for 144 LQFP.

4 Pinout compatible with Freescale's MPC5634M devices.

5 Pinout compatible with Freescale's MPC5534.

6 Ballmap upwardly compatible with the standardized package ballmap used for various Freescale MPC5xxx family members, including MPC5554, MPC5567 and MPC5666.

7 For Freescale VertiCal Calibration System only.

- Lock detect circuitry reports when the PLL has achieved frequency lock and continuously monitors lock status to report loss of lock conditions
- Clock Quality Module
  - Detects the quality of the crystal clock and causes interrupt request or system reset if error is detected
  - Detects the quality of the PLL output clock; if error detected, causes system reset or switches system clock to crystal clock and causes interrupt request
- Programmable interrupt request or system reset on loss of lock
- Self-clocked mode (SCM) operation

1.4.7 SIU

The MPC5644A SIU controls MCU reset configuration, pad configuration, external interrupt, general purpose I/O (GPIO), internal peripheral multiplexing, and the system reset operation. The reset configuration block contains the external pin boot configuration logic. The pad configuration block controls the static electrical characteristics of I/O pins. The GPIO block provides uniform and discrete input/output control of the I/O pins of the MCU. The reset controller performs reset monitoring of internal and external reset sources, and drives the $\overline{\text{RSTOUT}}$ pin. Communication between the SIU and the e200z4 CPU core is via the crossbar switch. The SIU provides the following features:

- System configuration
  - MCU reset configuration via external pins
  - Pad configuration control for each pad
  - Pad configuration control for virtual I/O via DSPI serialization
- System reset monitoring and generation
  - Power-on reset support
  - Reset status register provides last reset source to software
  - Glitch detection on reset input
  - Software controlled reset assertion
- External interrupt
  - Rising or falling edge event detection
  - Programmable digital filter for glitch rejection
  - Critical Interrupt request
  - Non-Maskable Interrupt request
- GPIO
  - Centralized control of I/O and bus pins
  - Virtual GPIO via DSPI serialization (requires external deserialization device)
  - Dedicated input and output registers for setting each GPIO and Virtual GPIO pin
- Internal multiplexing
  - Allows serial and parallel chaining of DSPIs
  - Allows flexible selection of eQADC trigger inputs
  - Allows selection of interrupt requests between external pins and DSPI

1.4.8 Flash memory

The MPC5644A provides up to 4 MB of programmable, non-volatile, flash memory. The non-volatile memory (NVM) can be used to store instructions or data, or both. The flash module includes a Fetch Accelerator that optimizes the performance of the flash array to match the CPU architecture. The flash module interfaces the system bus to a dedicated flash memory array controller. For CPU ‘loads’, DMA transfers and CPU instruction fetch, it supports a 64-bit data bus width at the system bus port,

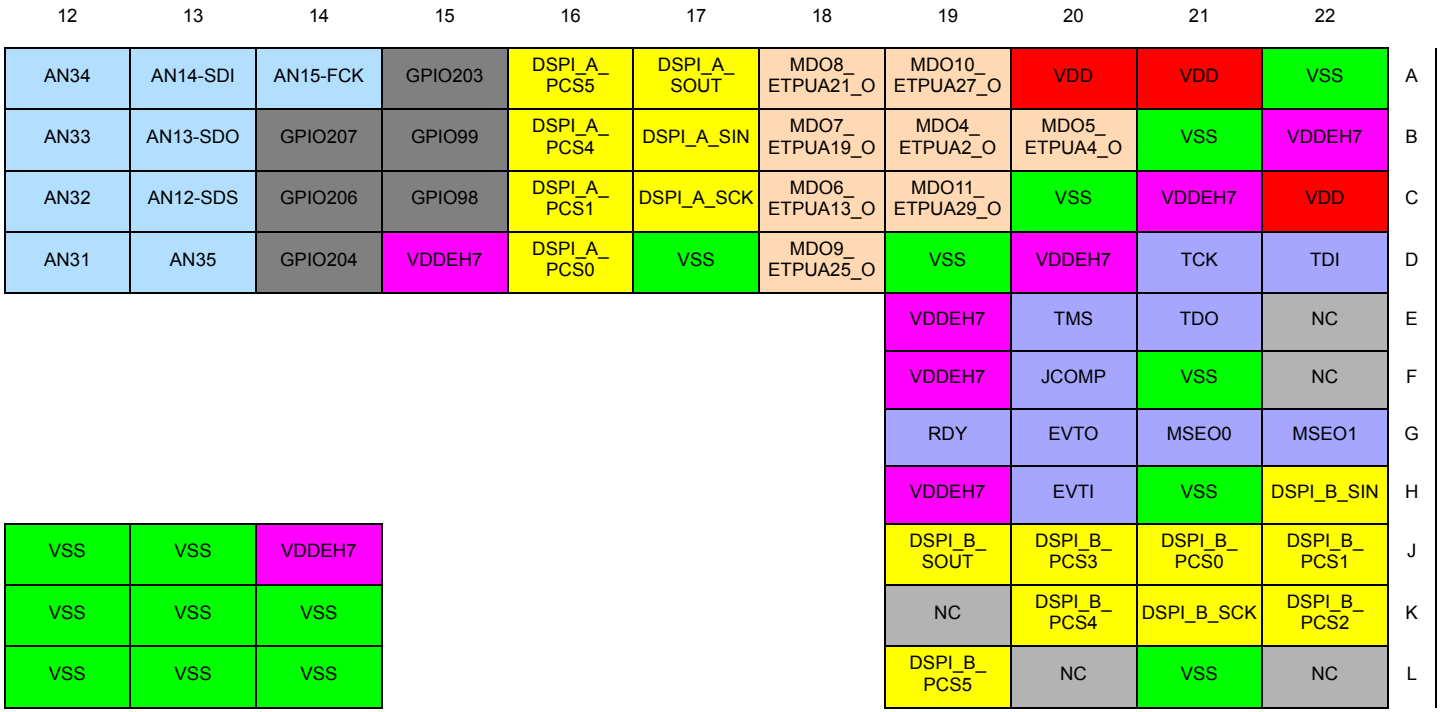


Figure 6. 324-pin TEPBGA package ballmap (northeast, viewed from above)

Table 3. MPC5644A signal properties (continued)

Name	Function[1]	PAG[2]	PCR PA Field[3]	PCR[4]	I/O Type	Voltage[5] / Pad Type[6]	Status[7]		Package pin #		
							During Reset	After Reset	176	208	324
ADDR26 DATA26 GPIO[22]	External address bus External data bus GPIO	P A2 G	001 100 000	22	I/O I/O I/O	VDDE-EH Medium	— / Up	— / Up	—	—	U2
ADDR27 DATA27 GPIO[23]	External address bus External data bus GPIO	P A2 G	001 100 000	23	I/O I/O I/O	VDDE-EH Medium	— / Up	— / Up	—	—	U3
ADDR28 DATA28 GPIO[24]	External address bus External data bus GPIO	P A2 G	001 100 000	24	I/O I/O I/O	VDDE-EH Medium	— / Up	— / Up	—	—	U4
ADDR29 DATA29 GPIO[25]	External address bus External data bus GPIO	P A2 G	001 100 000	25	I/O I/O I/O	VDDE-EH Medium	— / Up	— / Up	—	—	V1
ADDR30 ADDR6[8] DATA30 GPIO[26]	External address bus External address bus External data bus GPIO	P A1 A2 G	001 010 100 000	26	I/O O I/O I/O	VDDE-EH Medium	— / Up	— / Up	—	—	V3
ADDR31 ADDR7[8] DATA31 GPIO[27]	External address bus External address bus External data bus GPIO	P A1 A2 G	001 010 100 000	27	I/O O I/O I/O	VDDE-EH Medium	— / Up	— / Up	—	—	V4
DATA0 ADDR16 GPIO[28]	External data bus External address bus GPIO	P A1 G	001 010 000	28	I/O I/O I/O	VDDE5 Fast	— / Up	— / Up	—	—	Y5
DATA1 ADDR17 GPIO[29]	External data bus External address bus GPIO	P A1 G	001 010 000	29	I/O I/O I/O	VDDE5 Fast	— / Up	— / Up	—	—	AA5
DATA2 ADDR18 GPIO[30]	External data bus External address bus GPIO	P A1 G	001 010 000	30	I/O I/O I/O	VDDE5 Fast	— / Up	— / Up	—	—	AB5
DATA3 ADDR19 GPIO[31]	External data bus External address bus GPIO	P A1 G	001 010 000	31	I/O I/O I/O	VDDE5 Fast	— / Up	— / Up	—	—	AB6
DATA4 ADDR20 GPIO[32]	External data bus External address bus GPIO	P A1 G	001 010 000	32	I/O I/O I/O	VDDE5 Fast	— / Up	— / Up	—	—	AA6

Table 3. MPC5644A signal properties (continued)

Name	Function[1]	PAG[2]	PCR PA Field[3]	PCR[4]	I/O Type	Voltage[5] / Pad Type[6]	Status[7]		Package pin #		
							During Reset	After Reset	176	208	324
CAL_DATA[2]	Calibration data bus	P	01	341	I/O	VDDE12 Fast	— / Up	— / Up	—	—	—
CAL_DATA[3]	Calibration data bus	P	01	341	I/O	VDDE12 Fast	— / Up	— / Up	—	—	—
CAL_DATA[4]	Calibration data bus	P	01	341	I/O	VDDE12 Fast	— / Up	— / Up	—	—	—
CAL_DATA[5]	Calibration data bus	P	01	341	I/O	VDDE12 Fast	— / Up	— / Up	—	—	—
CAL_DATA[6]	Calibration data bus	P	01	341	I/O	VDDE12 Fast	— / Up	— / Up	—	—	—
CAL_DATA[7]	Calibration data bus	P	01	341	I/O	VDDE12 Fast	— / Up	— / Up	—	—	—
CAL_DATA[8]	Calibration data bus	P	01	341	I/O	VDDE12 Fast	— / Up	— / Up	—	—	—
CAL_DATA[9]	Calibration data bus	P	01	341	I/O	VDDE12 Fast	— / Up	— / Up	—	—	—
CAL_DATA[10]	Calibration data bus	P	01	341	I/O	VDDE12 Fast	— / Up	— / Up	—	—	—
CAL_DATA[11]	Calibration data bus	P	01	341	I/O	VDDE12 Fast	— / Up	— / Up	—	—	—
CAL_DATA[12]	Calibration data bus	P	01	341	I/O	VDDE12 Fast	— / Up	— / Up	—	—	—
CAL_DATA[13]	Calibration data bus	P	01	341	I/O	VDDE12 Fast	— / Up	— / Up	—	—	—
CAL_DATA[14]	Calibration data bus	P	01	341	I/O	VDDE12 Fast	— / Up	— / Up	—	—	—
CAL_DATA[15]	Calibration data bus	P	01	341	I/O	VDDE12 Fast	— / Up	— / Up	—	—	—
CAL_RD_WR	Calibration read/write enable	P	01	342	O	VDDE12 Fast		— / —	—	—	—
CAL_$\overline{WE}$[0]/$\overline{BE}$[0]	Calibration write/byte enable	P	01	342	O	VDDE12 Fast		— / —	—	—	—

Table 3. MPC5644A signal properties (continued)

Name	Function[1]	PAG[2]	PCR PA Field[3]	PCR[4]	I/O Type	Voltage[5] / Pad Type[6]	Status[7]		Package pin #		
							During Reset	After Reset	176	208	324
CAL_$\overline{WE}$[1]/$\overline{BE}$[1]	Calibration write/byte enable	P	01	342	O	VDDE12 Fast		— / —	—	—	—
CAL_OE	Calibration output enable	P	01	342	O	VDDE12 Fast		— / —	—	—	—
CAL_TS CAL_ALE	Calibration transfer start Address Latch Enable	P A	01 10	343	O O	VDDE12 Fast		— / —	—	—	—
CAL_MDO[4]	Calibration Nexus Message Data Out	P	01	—	O	VDDE12 Fast	—	CAL_MDO[4] / —	—	—	—
CAL_MDO[5]	Calibration Nexus Message Data Out	P	01	—	O	VDDE12 Fast	—	CAL_MDO[5] / —	—	—	—
CAL_MDO[6]	Calibration Nexus Message Data Out	P	01	—	O	VDDE12 Fast	—	CAL_MDO[6] / —	—	—	—
CAL_MDO[7]	Calibration Nexus Message Data Out	P	01	—	O	VDDE12 Fast	—	CAL_MDO[7] / —	—	—	—
CAL_MDO[8]	Calibration Nexus Message Data Out	P	01	—	O	VDDE12 Fast	—	CAL_MDO[8] / —	—	—	—
CAL_MDO[9]	Calibration Nexus Message Data Out	P	01	—	O	VDDE12 Fast	—	CAL_MDO[9] / —	—	—	—
CAL_MDO[10]	Calibration Nexus Message Data Out	P	01	—	O	VDDE12 Fast	—	CAL_MDO[10] / —	—	—	—
CAL_MDO[11]	Calibration Nexus Message Data Out	P	01	—	O	VDDE12 Fast	—	CAL_MDO[11] / —	—	—	—
NEXUS											
$\overline{EVTI}$	Nexus event in	P	01	231	I	VDDEH7 MultiV[12,14]	— / Up	$\overline{EVTI}$ / Up	116	E15	H20
$\overline{EVTO}$	Nexus event out	P	01	227	O	VDDEH7 MultiV[12,14,15]	—	$\overline{EVTO}$ / —	120	D15	G20
MCKO	Nexus message clock out	P	—	219[11]	O	VRC33 Fast	—	MCKO / —	14	F15	F1
MDO0[16]	Nexus message data out	P	01	220	O	VRC33 Fast	—	MDO[0] / —	17	A14	F3
MDO1[16]	Nexus message data out	P	01	221	O	VRC33 Fast	—	MDO[1] / —	18	B14	G2

Table 3. MPC5644A signal properties (continued)

Name	Function[1]	PAG[2]	PCR PA Field[3]	PCR[4]	I/O Type	Voltage[5] / Pad Type[6]	Status[7]		Package pin #		
							During Reset	After Reset	176	208	324
TCK	JTAG test clock input	P	01	—	I	VDDEH7 MultiV[12]	TCK / Down	TCK / Down	128	C16	D21
TDI	JTAG test data input	P	01	232	I	VDDEH7 MultiV[12]	TDI / Up	TDI / Up	130	E14	D22
TDO	JTAG test data output	P	01	228	O	VDDEH7 MultiV[12]	TDO / Up	TDO / Up	123	F14	E21
TMS	JTAG test mode select input	P	01	—	I	VDDEH7 MultiV[12]	TMS / Up	TMS / Up	131	D14	E20
JCOMP	JTAG TAP controller enable	P	01	—	I	VDDEH7 MultiV[12]	JCOMP / Down	JCOMP / Down	121	F16	F20
FlexCAN											
CAN_A_TX SCI_A_TX GPIO[83]	FlexCAN A TX eSCI A TX GPIO	P A1 G	01 10 00	83	O O I/O	VDDEH6 Slow	— / Up	— / Up	81	P12	AB19
CAN_A_RX SCI_A_RX GPIO[84]	FlexCAN A RX eSCI A RX GPIO	P A1 G	01 10 00	84	I I I/O	VDDEH6 Slow	— / Up	— / Up	82	R12	Y19
CAN_B_TX DSPI_C_PCS[3] SCI_C_TX GPIO[85]	FlexCAN B TX DSPI C peripheral chip select eSCI C TX GPIO	P A1 A2 G	001 010 100 000	85	O O O I/O	VDDEH6 Slow	— / Up	— / Up	88	T12	Y22
CAN_B_RX DSPI_C_PCS[4] SCI_C_RX GPIO[86]	FlexCAN B RX DSPI C peripheral chip select eSCI C RX GPIO	P A1 A2 G	001 010 100 000	86	I O I I/O	VDDEH6 Slow	— / Up	— / Up	89	R13	W21
CAN_C_TX DSPI_D_PCS[3] GPIO[87]	FlexCAN C TX DSPI D peripheral chip select GPIO	P A1 G	01 10 00	87	O O I/O	VDDEH6 Medium	— / Up	— / Up	101	K13	P19
CAN_C_RX DSPI_D_PCS[4] GPIO[88]	FlexCAN C RX DSPI D peripheral chip select GPIO	P A1 G	01 10 00	88	I O I/O	VDDEH6 Slow	— / Up	— / Up	98	L14	V20
eSCI											

[5] The VDDE and VDDEH supply inputs are broken into segments. Each segment of slow I/O pins (VDDEH) may have a separate supply in the 3.3 V to 5.0 V range (-10%/+5%). Each segment of fast I/O (VDDE) may have a separate supply in the 1.8 V to 3.3 V range (+/- 10%).

[6] See Table 4 for details on pad types.

[7] The Status During Reset pin is sampled after the internal POR is negated. Prior to exiting POR, the signal has a high impedance. Terminology is O - output, I - input, Up - weak pull up enabled, Down - weak pull down enabled, Low - output driven low, High - output driven high. A dash for the function in this column denotes that both the input and output buffer are turned off. The signal name to the left or right of the slash indicates the pin is enabled.

[8] Output only.

[9] When used as ETRIG, this pin must be configured as an input. For GPIO it can be configured either as an input or output.

[10] Maximum frequency is 50 kHz.

[11] The SIU_PCR219 register is unusual in that it controls pads for two separate device pins: GPIO[219] and MCKO. See the MPC5644A Microcontroller Reference Manual (SIU chapter) for details.

[12] Multivoltage pads are automatically configured in low swing mode when a JTAG or Nexus function is selected, otherwise they are high swing.

[13] On 176 LQFP and 208 MAPBGA packages, this pin is tied low internally.

[14] Nexus multivoltage pads default to 5 V operation until the Nexus module is enabled.

[15] $\overline{\text{EVTO}}$ should be clamped to 3.3 V to prevent possible damage to external tools that only support 3.3 V.

[16] Do not connect pin directly to a power supply or ground.

[17] This signal name is used to support legacy naming.

[18] During and just after POR negates, internal pull resistors can be enabled, resulting in as much as 4 mA of current draw. The pull resistors are disabled when the system clock propagates through the device.

[19] For pins AN12-AN15, if the analog features are used the VDDEH7 input pins should be tied to VDDA because that segment must meet the VDDA specification to support analog input function.

[20] Do not use VRC33 to drive external circuits.

[21] VDDA0 and VDDA1 are shorted together internally in BGA packages. In the QFP package the two pads are double bonded on one pin called VDDA.

[22] VSSA0 and VSSA1 are shorted together internally in BGA packages. In the QFP package the two pads are double bonded on one pin called VSSA.

[23] VDDE2 and VDDE3 are shorted together in all production packages.

[24] VDDE2 and VDDE3 are shorted together in all production packages.

[25] VDDEH1A, VDDEH1B, and VDDEH1AB are shorted together in all production packages. The separation of the signal names is present to support legacy naming, however they should be considered as the same signal in this document.

[26] VDDEH4, VDDEH4A, VDDEH4B, and VDDEH4AB are shorted together in all production packages. The separation of the signal names is present to support legacy naming, however they should be considered as the same signal in this document.

[27] VDDEH6, VDDEH6A, VDDEH6B, and VDDEH6AB are shorted together in all production packages. The separation of the signal names is present to support legacy naming, however they should be considered as the same signal in this document.

Table 15. PMC Electrical Characteristics

ID	Name			Parameter	Min	Typ	Max	Unit	Notes
1	VBG	CC	C	Nominal bandgap voltage reference	—	1.219	—	V	
1a	—	CC	P	Untrimmed bandgap reference voltage	VBG - 7%	VBG	Vbg + 6%	V	
1b	—	CC	P	Trimmed bandgap reference voltage (5 V, 27 °C)	VBG -10mV	VBG	VBG + 10mV	V	
1c	—	CC	C	Bandgap reference temperature variation	—	100	—	ppm /°C	
1d	—	CC	C	Bandgap reference supply voltage variation	—	3000	—	ppm /V	
2	Vdd	CC	C	Nominal V_{DD} core supply internal regulator target DC output voltage[1]	—	1.28	—	V	
2a	—	CC	P	Nominal V_{DD} core supply internal regulator target DC output voltage variation at power-on reset	Vdd - 6%	Vdd	Vdd + 10%	V	
2b	—	CC	P	Nominal V_{DD} core supply internal regulator target DC output voltage variation after power-on reset	Vdd - 10%[2]	Vdd	Vdd + 3%	V	
2c	—	CC	C	Trimming step Vdd	—	20	—	mV	
2d	Ivrcctl	CC	C	Voltage regulator controller for core supply maximum DC output current	20	—	—	mA	
3	Lvi1p2	CC	C	Nominal LVI for rising core supply[3]	—	1.160	—	V	
3a	—	CC	C	Variation of LVI for rising core supply at power-on reset	1.120	1.200	1.280	V	See note [4]
3b	—	CC	C	Variation of LVI for rising core supply after power-on reset	Lvi1p2 - 3%	Lvi1p2	Lvi1p2 + 3%	V	See note 4
3c	—	CC	C	Trimming step LVI core supply	—	20	—	mV	
3d	Lvi1p2_h	CC	C	LVI core supply hysteresis	—	40	—	mV	
4	Por1.2V_r	CC	C	POR 1.2 V rising	—	0.709	—	V	
4a	—	CC	C	POR 1.2 V rising variation	Por1.2V_r - 35%	Por1.2V_r	Por1.2V_r + 35%	V	
4b	Por1.2V_f	CC	C	POR 1.2 V falling	—	0.638	—	V	
4c	—	CC	C	POR 1.2 V falling variation	Por1.2V_f - 35%	Por1.2V_f	Por1.2V_f+ 35%	V	

3.9 I/O pad current specifications

The power consumption of an I/O segment depends on the usage of the pins on a particular segment. The power consumption is the sum of all output pin currents for a particular segment. The output pin current can be calculated from Table 22 based on the voltage, frequency, and load on the pin. Use linear scaling to calculate pin currents for voltage, frequency, and load parameters that fall outside the values given in Table 22.

Table 22. I/O pad average I_{DDE} specifications[1]

Pad Type	Symbol		C	Period (ns)	Load[2] (pF)	V_{DDE} (V)	Drive/Slew Rate Select	I_{DDE} Avg (mA)[3]	I_{DDE} RMS (mA)
Slow	$I_{DRV\_SSR\_HV}$	CC	D	37	50	5.5	11	9	—
		CC	D	130	50	5.5	01	2.5	—
		CC	D	650	50	5.5	00	0.5	—
		CC	D	840	200	5.5	00	1.5	—
Medium	$I_{DRV\_MSR\_HV}$	CC	D	24	50	5.5	11	14	—
		CC	D	62	50	5.5	01	5.3	—
		CC	D	317	50	5.5	00	1.1	—
		CC	D	425	200	5.5	00	3	—
Fast	I_{DRV_FC}	CC	D	10	50	3.6	11	22.7	68.3
		CC	D	10	30	3.6	10	12.1	41.1
		CC	D	10	20	3.6	01	8.3	27.7
		CC	D	10	10	3.6	00	4.44	14.3
		CC	D	10	50	1.98	11	12.5	31
		CC	D	10	30	1.98	10	7.3	18.6
		CC	D	10	20	1.98	01	5.42	12.6
		CC	D	10	10	1.98	00	2.84	6.4
MultiV (High Swing Mode)	$I_{DRV\_MULTV\_HV}$	CC	D	20	50	5.5	11	9	—
		CC	D	30	50	5.5	01	6.1	—
		CC	D	117	50	5.5	00	2.3	—
		CC	D	212	200	5.5	00	5.8	—
MultiV (Low Swing Mode)	$I_{DRV\_MULTV\_HV}$	CC	D	30	30	5.5	11	3.4	—

1 Numbers from simulations at best case process, 150 °C.

2 All loads are lumped.

3 Average current is for pad configured as output only.

3.9.1 I/O pad V_{RC33} current specifications

The power consumption of the V_{RC33} supply is dependent on the usage of the pins on all I/O segments. The power consumption is the sum of all input and output pin V_{RC33} currents for all I/O segments. The output pin V_{RC33} current can be calculated from Table 23 based on the voltage, frequency, and load on all fast pad pins. The input pin V_{RC33} current can be calculated from Table 23 based on the voltage, frequency, and load on all medium-speed pads. Use linear scaling to calculate pin currents for voltage, frequency, and load parameters that fall outside the values given in Table 23.

Table 23. I/O pad V_{RC33} average I_{DDE} specifications[1]

Pad Type	Symbol		C	Period (ns)	Load[2] (pF)	Drive Select	I_{DD33} Avg (µA)	I_{DD33} RMS (µA)
Slow	$I_{DRV\_SSR\_HV}$	CC	D	100	50	11	0.8	235.7
		CC	D	200	50	01	0.04	87.4
		CC	D	800	50	00	0.06	47.4
		CC	D	800	200	00	0.009	47
Medium	$I_{DRV\_MSR\_HV}$	CC	D	40	50	11	2.75	258
		CC	D	100	50	01	0.11	76.5
		CC	D	500	50	00	0.02	56.2
		CC	D	500	200	00	0.01	56.2
MultiV[3] (High Swing Mode)	$I_{DRV\_MULTV\_HV}$	CC	D	20	50	11	33.4	35.4
		CC	D	30	50	01	33.4	34.8
		CC	D	117	50	00	33.4	33.8
		CC	D	212	200	00	33.4	33.7
MultiV[4] (Low Swing Mode)	$I_{DRV\_MULTV\_HV}$	CC	D	30	30	11	33.4	34.9

1 These are typical values that are estimated from simulation and not tested. Currents apply to output pins only.

2 All loads are lumped.

3 Average current is for pad configured as output only.

4 In low swing mode, multi-voltage pads must operate in highest slew rate setting.

Table 25. DSPI LVDS pad specification (continued)

11	Delay, Z to Normal (High/Low)	T_{DZ}	CC	D	—		500		ns
12	Diff Skew ltphla-tplhbl or ltplhb-tphlal	T_{SKEW}	CC	D	—			0.5	ns
Termination									
13	Trans. Line (differential Zo)		CC	D	—	95	100	105	Ω
14	Temperature		CC	D		–40		150	°C

3.10 Oscillator and PLLMRFM electrical characteristics

Table 26. PLLMRFM electrical specifications

(V_{DDPLL} = 1.08 V to 3.6 V, V_{SS} = V_{SSPLL} = 0 V, T_A = T_L to T_H)

Symbol		C	Parameter		Conditions	Value		Unit
						min	max	
$f_{ref\_crystal}$ f_{ref_ext}	CC	D	PLL reference frequency range[1]		Crystal reference	4	40	MHz
		C			External reference	4	80	
f_{pll_in}	CC	P	Phase detector input frequency range (after pre-divider)		—	4	16	MHz
f_{vco}	CC	P	VCO frequency range		—	256	512	MHz
f_{sys}	CC	C	On-chip PLL frequency[2]		—	16	150	MHz
f_{sys}	CC	T	System frequency in bypass mode[2]		Crystal reference	4	40	MHz
		P			External reference	0	80	
t_{CYC}	CC	D	System clock period		—	—	1 / f_{sys}	ns
f_{LORL} f_{LORH}	CC	D	Loss of reference frequency window[3]		Lower limit	1.6	3.7	MHz
		D			Upper limit	24	56	
f_{SCM}	CC	P	Self-clocked mode frequency [4,5]		—	1.2	72.25	MHz
C_{JITTER}	CC	T	CLKOUT period jitter[6,7,8,9]	Peak-to-peak (clock edge to clock edge)	f_{SYS} maximum	–5	5	% f_{CLKOUT}
		T		Long-term jitter (avg. over 2 ms interval)		–6	6	ns
t_{cst}	CC	T	Crystal start-up time [10, 11]		—	—	10	ms

[4] The actual minimum SCK cycle time is limited by pad performance.

[5] For DSPI channels using LVDS output operation, up to 40 MHz SCK cycle time is supported. For non-LVDS output, maximum SCK frequency is 20 MHz. Appropriate clock division must be applied.

[6] The maximum value is programmable in DSPI_CTARx[PSSCK] and DSPI_CTARx[CSSCK].

[7] Timing met when pcssck = 3(01), and cssck =2 (0000).

[8] The maximum value is programmable in DSPI_CTARx[PASC] and DSPI_CTARx[ASC].

[9] Timing met when ASC = 2 (0000), and PASC = 3 (01).

[10] Timing met when pcssck = 3.

[11] Timing met when ASC = 3.

[12] This number is calculated assuming the SMPL_PT bitfield in DSPI_MCR is set to 0b10.

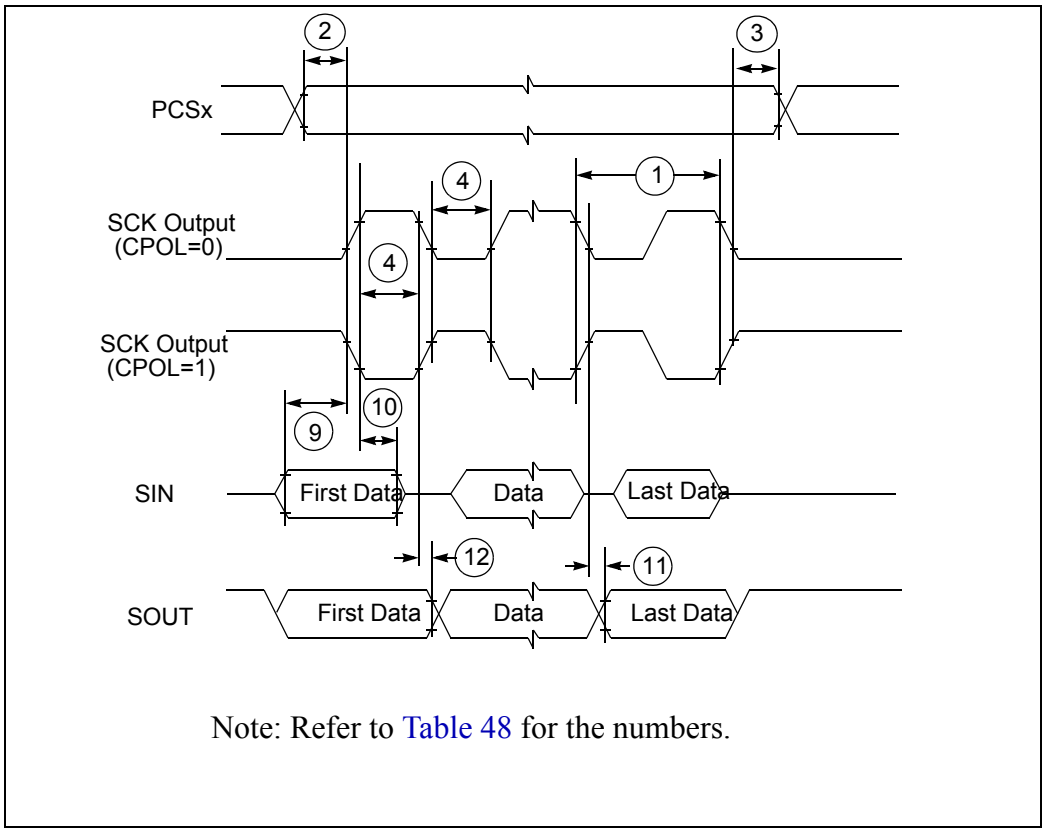


Figure 23. DSPI classic SPI timing — master, CPHA = 0

3.17.10 FlexCAN system clock source

Table 50. FlexCAN engine system clock divider threshold

#	Symbol	Characteristic	Value	Unit
1	F_{CAN_TH}	FlexCAN engine system clock threshold	100	MHz

Table 51. FlexCAN engine system clock divider

System Frequency	Required SIU_SYSDIV[CAN_SRC] Value
<= F_{CAN_TH}	0[1,2]
> F_{CAN_TH}	1[2,3]

1 Divides system clock source for FlexCAN engine by 1.

2 System clock is only selected for FlexCAN when CAN_CR[CLK_SRC] = 1.

3 Divides system clock source for FlexCAN engine by 2.

NOTES:

1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25MM PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE DATUM H.

2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THEN 0.08MM. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07MM FOR 0.4MM AND 0.5MM PITCH PACKAGES.

DIM	MIN	NOM	MAX	DIM	MIN	NOM	MAX	DIM	MIN	NOM	MAX
A	---		1.6	L1		1 REF					
A1	0.05		0.15	R1	0.08		---				
A2	1.35	1.4	1.45	R2	0.08		0.2				
b	0.17	0.22	0.27	S		0.2 REF					
b1	0.17	0.2	0.23	θ	0°	3.5°	7°				
c	0.09		0.2	θ1	0°		---				
c1	0.09		0.16	θ2	11°	12°	13°				
D		26 BSC		θ3	11°	12°	13°				
D1		24 BSC									
e		0.5 BSC									
E		26 BSC									
E1		24 BSC									
L	0.45	0.6	0.75								

UNIT	DIMENSION AND TOLERANCES	REFERANCE DOCUMENT
MM	ASME Y14.5M	64-06-280-1392

TITLE:		
LQFP 176LD 24X24X1.4 PKG 0.5 PITCH POD 2mm FOOTPRINT		
	SHEET	3

Figure 35. 176 LQFP package mechanical drawing (part 3)

4.1.2 208 MAPBGA

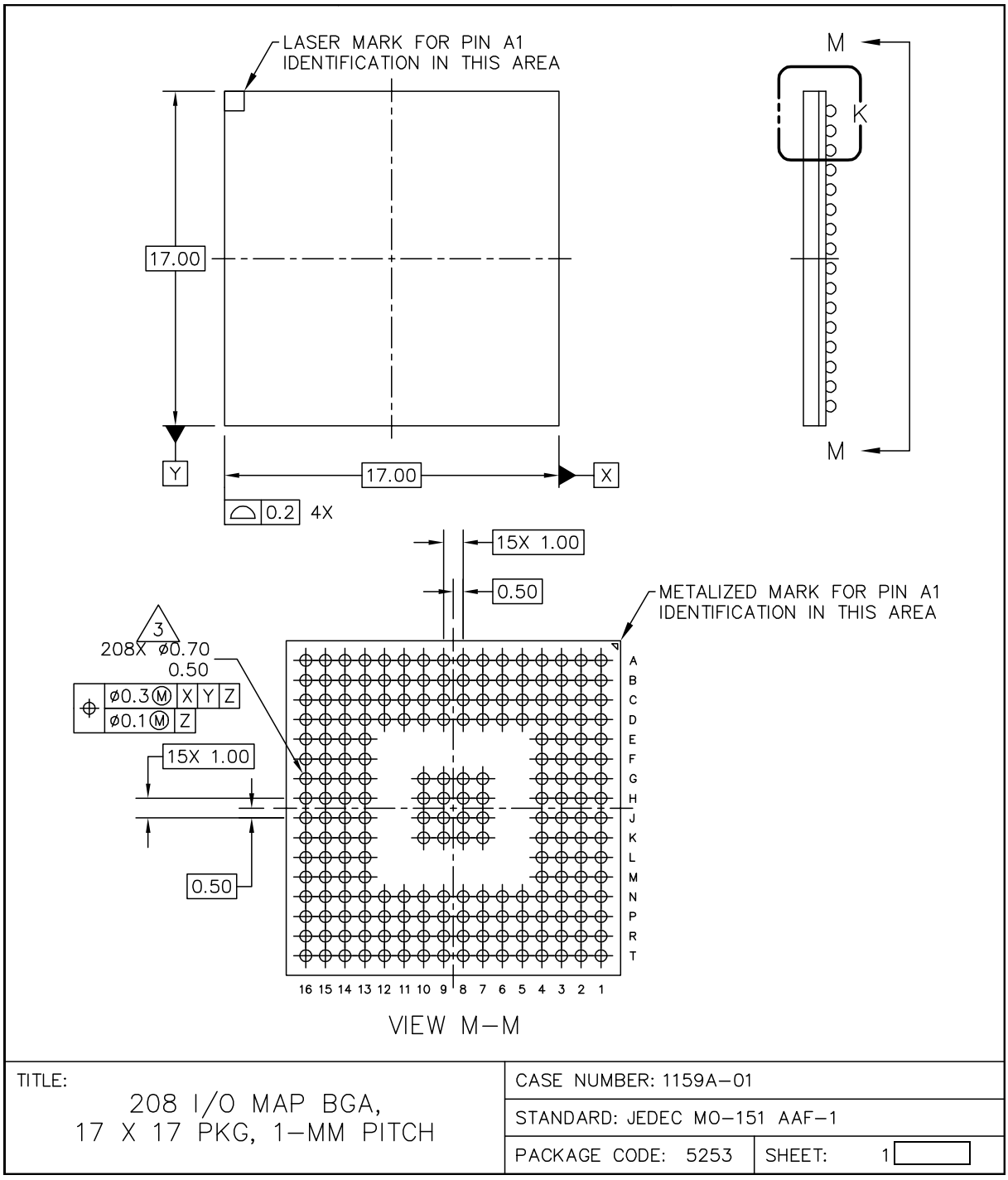
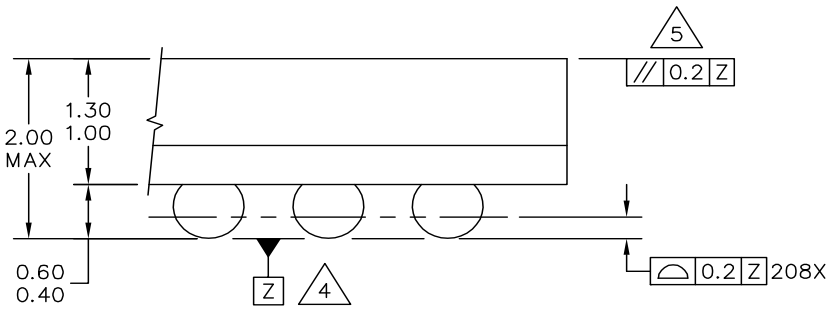


Figure 36. 208 MAPBGA package mechanical drawing (part 1)



DETAIL K
(ROTATED 90° CLOCKWISE)

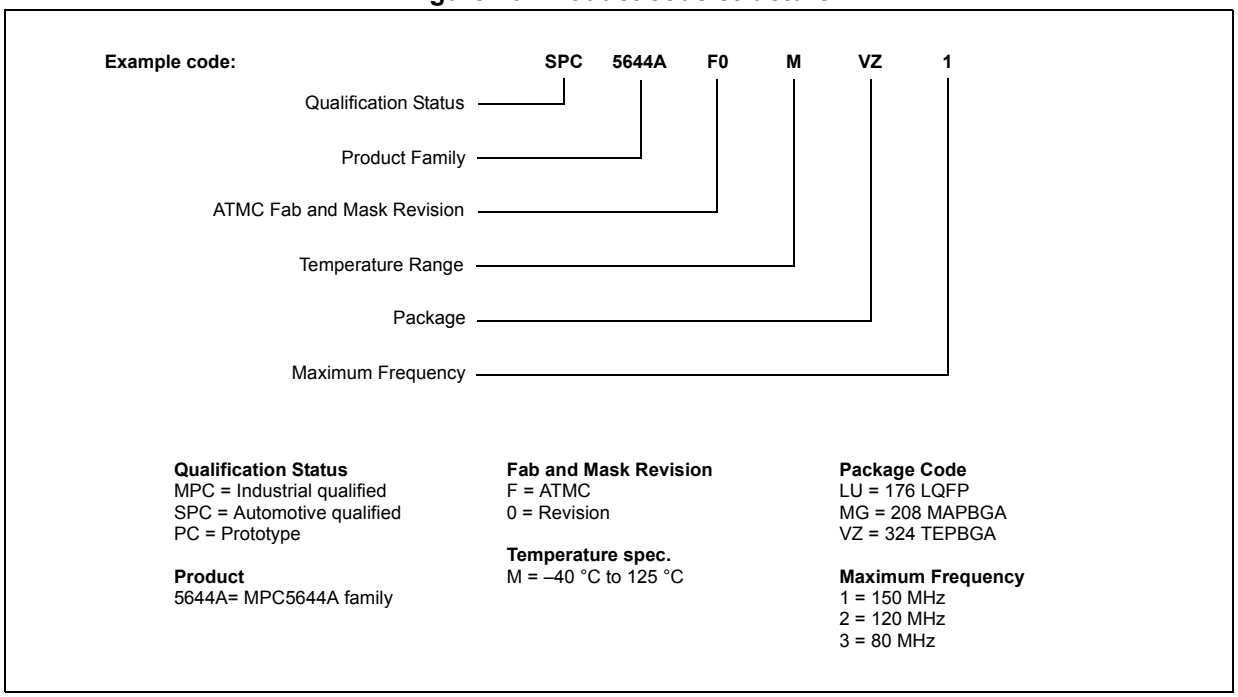
NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE Z.
4. DATUM Z (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

TITLE: 208 I/O MAP BGA, 17 X 17 PKG, 1–MM PITCH	CASE NUMBER: 1159A–01	
	STANDARD: JEDEC MO–151 AAF–1	
	PACKAGE CODE: 5253	SHEET: 2

Figure 37. 208 MAPBGA package mechanical drawing (part 2)

Figure 40. Product code structure



6 Document revision history

Table 53 summarizes revisions to this document.

Table 53. Revision history

Revision	Date	Substantive changes
Rev. 1	4/2008	Initial release

Table 53. Revision history (continued)

Revision	Date	Substantive changes
Rev. 3	04/2010	Changes to Signal Properties table (changes apply to Revision 2 and later devices: EBI changes: • WE_BE[2] (A2) and CAL_WE_BE[2] (A3) signals added to CS[2] (PCR 2) • WE_BE[3] (A2) and CAL_WE_BE[3] (A3) signals added to CS[3] (PCR 3) Calibration bus changes: • CAL_WE[2]/BE[2] (A2) signal added to CAL_CS[2] (PCR 338) • CAL_WE[3]/BE[3] (A2) signal added to CAL_CS[3] (PCR 339) • CAL_ALE (A1) added to CAL_ADDR[15] (PCR 340) eQADC changes: • AN[8] and AN[38] pins swapped. AN[8] Is now on pins 9 (176-pin), B3 (208-ball) and E1 (324-ball). AN[8] was on D3 (324-ball) on previous devices. AN[38] Is now on D3 (324-ball). AN[38] was on pins 9 (176-pin), B3 (208-ball) and E1 (324-ball) on previous devices. • ANZ function added to AN11 pin Reaction channels added to eTPU2: • RCH0_A (A3) added to ETPU_A[14] (PCR 128) • RCH0_B (A2) added to ETPU_A[20] (PCR 134) • RCH0_C (A2) added to ETPU_A[21] (PCR 135) • RCH1_A (A2) added to ETPU_A[15] (PCR 129) • RCH1_B (A2) added to ETPU_A[9] (PCR 123) • RCH1_C (A2) added to ETPU_A[10] (PCR 124) • RCH2_A (A2) added to ETPU_A[16] (PCR 130) • RCH3_A (A2) added to ETPU_A[17] (PCR 131 • RCH4_A (A2) added to ETPU_A[18] (PCR 132)) • RCH4_B (A2) added to ETPU_A[11] (PCR 125) • RCH4_C (A2) added to ETPU_A[12] (PCR 126) • RCH5_A (A2) added to ETPU_A[19] (PCR 133) • RCH5_B (A2) added to ETPU_A[28] (PCR 142) • RCH5_C (A2) added to ETPU_A[29] (PCR 143) Reaction channels added to eMIOS: • RCH2_B (A2) added to EMIOS[2] (PCR 181) • RCH2_C (A2) added to EMIOS[4] (PCR 183) • RCH3_B (A2) added to EMIOS[10] (PCR 189) • RCH3_C (A2) added to EMIOS[11] (PCR 190) Pad changes: • ETPUA16 (PCR 130) has Medium (was Slow) pad • ETPUA17 (PCR 131) has Medium (was Slow) pad • ETPUA18 (PCR 132) has Medium (was Slow) pad • ETPUA19 (PCR 133) has Medium (was Slow) pad • ETPUA25 (PCR 139) has Slow+LVDS (was Medium+LVDS) pads Signal Details table updated: • Added eTPU2 reaction channels • Changed IRQ[0:15] to two ranges, excluding IRQ6, which does not exist on this device • Changed TCR_A to TCRCLKA (TCR_A is the pin name, not the signal name) • Changed WE_BE[0:1] to WE_BE[0:3] (2 new signals added to Rev. 2). Also changed notation from “WE_BE[n]” to “WE[n]/BE[n]” to be consistent.