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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	PowerPC e5500
Number of Cores/Bus Width	2 Core, 64-Bit
Speed	2.2GHz
Co-Processors/DSP	-
RAM Controllers	DDR3, DDR3L
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	1Gbps (10), 10Gbps (2)
SATA	SATA 3Gbps (2)
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.0V, 1.2V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Boot Security, Cryptography, Secure Fusebox, Secure Debug, Tamper Detection, Volatile key Storage
Package / Case	1295-BBGA, FCBGA
Supplier Device Package	1295-FCPBGA (37.5x37.5)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=p5021nse72qc

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Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
D2_MDQ55	Data	AT3	I/O	GV_{DD}	—
D2_MDQ56	Data	AP5	I/O	GV_{DD}	—
D2_MDQ57	Data	AT5	I/O	GV_{DD}	—
D2_MDQ58	Data	AP8	I/O	GV_{DD}	—
D2_MDQ59	Data	AT8	I/O	GV_{DD}	—
D2_MDQ60	Data	AR4	I/O	GV_{DD}	—
D2_MDQ61	Data	AT4	I/O	GV_{DD}	—
D2_MDQ62	Data	AR7	I/O	GV_{DD}	—
D2_MDQ63	Data	AT7	I/O	GV_{DD}	—
D2_MECC0	Error Correcting Code	J1	I/O	GV_{DD}	—
D2_MECC1	Error Correcting Code	K3	I/O	GV_{DD}	—
D2_MECC2	Error Correcting Code	M5	I/O	GV_{DD}	—
D2_MECC3	Error Correcting Code	N5	I/O	GV_{DD}	—
D2_MECC4	Error Correcting Code	J4	I/O	GV_{DD}	—
D2_MECC5	Error Correcting Code	J2	I/O	GV_{DD}	—
D2_MECC6	Error Correcting Code	L3	I/O	GV_{DD}	—
D2_MECC7	Error Correcting Code	L4	I/O	GV_{DD}	—
$\overline{\text{D2\_MAPAR\_ERR}}$	Address Parity Error	N2	I	GV_{DD}	—
D2_MAPAR_OUT	Address Parity Out	Y1	O	GV_{DD}	—
D2_MDM0	Data Mask	B12	O	GV_{DD}	—
D2_MDM1	Data Mask	B6	O	GV_{DD}	—
D2_MDM2	Data Mask	C4	O	GV_{DD}	—
D2_MDM3	Data Mask	G3	O	GV_{DD}	—
D2_MDM4	Data Mask	AG1	O	GV_{DD}	—
D2_MDM5	Data Mask	AL3	O	GV_{DD}	—
D2_MDM6	Data Mask	AP2	O	GV_{DD}	—
D2_MDM7	Data Mask	AP6	O	GV_{DD}	—
D2_MDM8	Data Mask	K2	O	GV_{DD}	—
D2_MDQS0	Data Strobe	A10	I/O	GV_{DD}	—
D2_MDQS1	Data Strobe	A5	I/O	GV_{DD}	—
D2_MDQS2	Data Strobe	C2	I/O	GV_{DD}	—
D2_MDQS3	Data Strobe	G6	I/O	GV_{DD}	—
D2_MDQS4	Data Strobe	AH2	I/O	GV_{DD}	—
D2_MDQS5	Data Strobe	AM4	I/O	GV_{DD}	—

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
$\overline{\text{LCS4}}$	Chip Selects	D22	O	BV_{DD}	5
$\overline{\text{LCS5}}$	Chip Selects	B23	O	BV_{DD}	5
$\overline{\text{LCS6}}$	Chip Selects	F24	O	BV_{DD}	5
$\overline{\text{LCS7}}$	Chip Selects	G26	O	BV_{DD}	5
$\overline{\text{LWE0}}$	Write Enable	D24	O	BV_{DD}	—
$\overline{\text{LWE1}}$	Write Enable	A24	O	BV_{DD}	—
$\overline{\text{LWE2}}$	Write Enable	J16	O	BV_{DD}	—
$\overline{\text{LWE3}}$	Write Enable	K15	O	BV_{DD}	—
LBCTL	Buffer Control	C22	O	BV_{DD}	—
LALE	Address Latch Enable	A23	I/O	BV_{DD}	—
LGPL0/LFCLE	UPM General Purpose Line 0/ LFCLE—FCM	B25	O	BV_{DD}	3, 4
LGPL1/LFALE	UPM General Purpose Line 1/ LFALE—FCM	E25	O	BV_{DD}	3, 4
LGPL2/$\overline{\text{LOE}}$/$\overline{\text{LFRE}}$	UPM General Purpose Line 2/ LOE_B—Output Enable	D25	O	BV_{DD}	3, 4
LGPL3/$\overline{\text{LFWP}}$	UPM General Purpose LIne 3/ LFWP_B—FCM	H26	O	BV_{DD}	3, 4
LGPL4/$\overline{\text{LGTA}}$/LUPWAIT/LPBSE	UPM General Purpose Line 4/ LGTA_B—FCM	C25	I/O	BV_{DD}	39
LGPL5	UPM General Purpose Line 5 / Amux	E26	O	BV_{DD}	3, 4
LCLK0	Local Bus Clock	C24	O	BV_{DD}	—
LCLK1	Local Bus Clock	C23	O	BV_{DD}	—
DMA					
$\overline{\text{DMA1\_DREQ0}}$/GPIO18	DMA1 Channel 0 Request	AP21	I	OV_{DD}	26
$\overline{\text{DMA1\_DACK0}}$/GPIO19	DMA1 Channel 0 Acknowledge	AL19	O	OV_{DD}	26
$\overline{\text{DMA1\_DDONE0}}$	DMA1 Channel 0 Done	AN21	O	OV_{DD}	27
$\overline{\text{DMA2\_DREQ0}}$/GPIO20/ALT_MDVAL	DMA2 Channel 0 Request	AJ20	I	OV_{DD}	26
$\overline{\text{DMA2\_DACK0}}$/$\overline{\text{EVT7}}$/ALT_MDSRCID0	DMA2 Channel 0 Acknowledge	AG19	O	OV_{DD}	26
$\overline{\text{DMA2\_DDONE0}}$/$\overline{\text{EVT8}}$/ALT_MDSRCID1	DMA2 Channel 0 Done	AP20	O	OV_{DD}	26
USB Port 1					
USB1_UDP	USB1 PHY Data Plus	AT27	I/O	USB_V_{DD}_3P3	—
USB1_UDM	USB1 PHY Data Minus	AT26	I/O	USB_V_{DD}_3P3	—
USB1_VBUS_CLMP	USB1 PHY VBUS Divided Signal	AK25	I	USB_V_{DD}_3P3	38

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GND	Ground	T13	—	—	—
GND	Ground	V13	—	—	—
GND	Ground	Y13	—	—	—
GND	Ground	AB13	—	—	—
GND	Ground	AD13	—	—	—
GND	Ground	AE14	—	—	—
GND	Ground	AC14	—	—	—
GND	Ground	AA14	—	—	—
GND	Ground	W14	—	—	—
GND	Ground	U14	—	—	—
GND	Ground	R14	—	—	—
GND	Ground	N14	—	—	—
GND	Ground	L14	—	—	—
GND	Ground	M15	—	—	—
GND	Ground	P15	—	—	—
GND	Ground	T15	—	—	—
GND	Ground	V15	—	—	—
GND	Ground	Y15	—	—	—
GND	Ground	AB15	—	—	—
GND	Ground	AD15	—	—	—
GND	Ground	AF15	—	—	—
GND	Ground	W16	—	—	—
GND	Ground	AC16	—	—	—
GND	Ground	AA16	—	—	—
GND	Ground	AE16	—	—	—
GND	Ground	U16	—	—	—
GND	Ground	R16	—	—	—
GND	Ground	N16	—	—	—
GND	Ground	M17	—	—	—
GND	Ground	P17	—	—	—
GND	Ground	T17	—	—	—
GND	Ground	N18	—	—	—
GND	Ground	R18	—	—	—
GND	Ground	U18	—	—	—

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
USB1_AGND	USB1 PHY Transceiver GND	AR26	—	—	—
USB1_AGND	USB1 PHY Transceiver GND	AR27	—	—	—
USB1_AGND	USB1 PHY Transceiver GND	AR28	—	—	—
USB1_AGND	USB1 PHY Transceiver GND	AT25	—	—	—
USB1_AGND	USB1 PHY Transceiver GND	AT28	—	—	—
USB2_AGND	USB2 PHY Transceiver GND	AH27	—	—	—
USB2_AGND	USB2 PHY Transceiver GND	AL28	—	—	—
USB2_AGND	USB2 PHY Transceiver GND	AM28	—	—	—
USB2_AGND	USB2 PHY Transceiver GND	AN25	—	—	—
USB2_AGND	USB2 PHY Transceiver GND	AN26	—	—	—
USB2_AGND	USB2 PHY Transceiver GND	AN27	—	—	—
USB2_AGND	USB2 PHY Transceiver GND	AN28	—	—	—
USB2_AGND	USB2 PHY Transceiver GND	AP25	—	—	—
USB2_AGND	USB2 PHY Transceiver GND	AP28	—	—	—
OVDD	General I/O Supply	AN22	—	OV_{DD}	—
OVDD	General I/O Supply	AJ14	—	OV_{DD}	—
OVDD	General I/O Supply	AJ18	—	OV_{DD}	—
OVDD	General I/O Supply	AL16	—	OV_{DD}	—
OVDD	General I/O Supply	AJ12	—	OV_{DD}	—
OVDD	General I/O Supply	AN18	—	OV_{DD}	—
OVDD	General I/O Supply	AG21	—	OV_{DD}	—
OVDD	General I/O Supply	AL20	—	OV_{DD}	—
OVDD	General I/O Supply	AT15	—	OV_{DD}	—
OVDD	General I/O Supply	AJ23	—	OV_{DD}	—
OVDD	General I/O Supply	AP16	—	OV_{DD}	—
OVDD	General I/O Supply	AR24	—	OV_{DD}	—
CVDD	eSPI & eSDHC Supply	AG24	—	CV_{DD}	—
CVDD	eSPI & eSDHC Supply	AJ29	—	CV_{DD}	—
CVDD	eSPI & eSDHC Supply	AP29	—	CV_{DD}	—
GVDD	DDR Supply	B2	—	GV_{DD}	—
GVDD	DDR Supply	B8	—	GV_{DD}	—
GVDD	DDR Supply	B14	—	GV_{DD}	—
GVDD	DDR Supply	C18	—	GV_{DD}	—
GVDD	DDR Supply	C12	—	GV_{DD}	—

WARNING

Only 100,000 POR cycles are permitted per lifetime of a device.

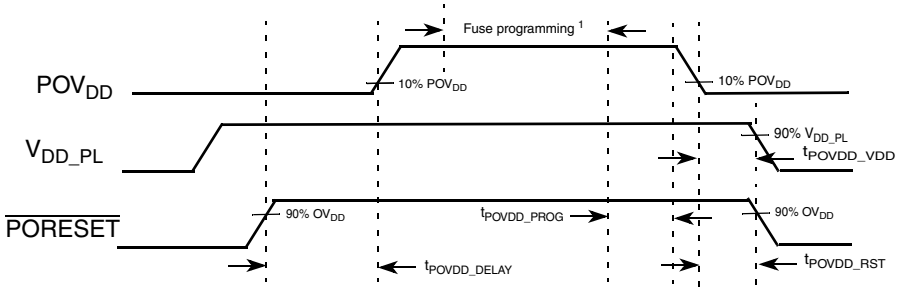
WARNING

While VDD is ramping, current may be supplied from VDD through the P5021 to GVDD. Nevertheless, GVDD from an external supply should follow the sequencing described above.

All supplies must be at their stable values within 75 ms.

Items on the same line have no ordering requirement with respect to one another. Items on separate lines must be ordered sequentially such that voltage rails on a previous step must reach 90% of their value before the voltage rails on the current step reach 10% of theirs.

This figure provides the POV_{DD} timing diagram.



NOTE: POV_{DD} must be stable at 1.5 V prior to initiating fuse programming.

Figure 8. POV_{DD} timing diagram

This table provides information on the power-down and power-up sequence parameters for POV_{DD}.

Table 5. POV_{DD} timing [5]

Driver type	Min	Max	Unit	Notes
t_{POVDD_DELAY}	100	—	SYSCLKs	1
t_{POVDD_PROG}	0	—	µs	2
t_{POVDD_VDD}	0	—	µs	3
t_{POVDD_RST}	0	—	µs	4

Notes:

1. Delay required from the negation of $\overline{\text{PORESET}}$ to driving POV_{DD} ramp up. Delay measured from $\overline{\text{PORESET}}$ negation at 90% OV_{DD} to 10% POV_{DD} ramp up.
2. Delay required from fuse programming finished to POV_{DD} ramp down start. Fuse programming must complete while POV_{DD} is stable at 1.5 V. No activity other than that required for secure boot fuse programming is permitted while POV_{DD} driven to any voltage above GND, including the reading of the fuse block. The reading of the fuse block may only occur while POV_{DD} = GND. After fuse programming is completed, it is required to return POV_{DD} = GND.
3. Delay required from POV_{DD} ramp down complete to V_{DD_PL} ramp down start. POV_{DD} must be grounded to minimum 10% POV_{DD} before V_{DD_PL} is at 90% V_{DD}.
4. Delay required from POV_{DD} ramp down complete to $\overline{\text{PORESET}}$ assertion. POV_{DD} must be grounded to minimum 10% POV_{DD} before $\overline{\text{PORESET}}$ assertion reaches 90% OV_{DD}.
5. Only two secure boot fuse programming events are permitted per lifetime of a device.

To guarantee MCKE low during power up, the above sequencing for GV_{DD} is required. If there is no concern about any of the DDR signals being in an indeterminate state during power up, the sequencing for GV_{DD} is not required.

Table 10. Package thermal characteristics (continued)[6]

Rating	Board	Symbol	Value	Unit	Notes
Junction to board	—	$R_{\Theta JB}$	3	°C/W	3
Junction to case top	—	$R_{\Theta JCtop}$	0.44	°C/W	4
Junction to lid top	—	$R_{\Theta JClid}$	0.17	°C/W	5

Notes:

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Junction-to-board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.
3. Junction-to-case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.
4. Junction-to-Lid-Top thermal resistance determined using the using MIL-STD 883 Method 1012.1. However, instead of the cold plate, the lid top temperature is used here for the reference case temperature. The reported value does not include the thermal resistance of the interface layer between the package and cold plate.
5. Junction-to-lid-top thermal resistance determined using the using MIL-STD 883 Method 1012.1. However, instead of the cold plate, the lid top temperature is used here for the reference case temperature. Reported value does not include the thermal resistance of the interface layer between the package and cold plate.
6. Reference Section 3.8, “Thermal management information,” for additional details.

2.6 Input clocks

This section discusses the system clock timing specifications for DC and AC power, spread spectrum sources, real time clock timing, and dTSEC gigabit Ethernet reference clocks AC timing.

2.6.1 System clock (SYSCLK) timing specifications

This table provides the system clock (SYSCLK) DC specifications.

Table 11. SYSCLK DC electrical characteristics (OV_{DD} = 3.3 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Input high voltage	V_{IH}	2.0	—	—	V	1
Input low voltage	V_{IL}	—	—	0.8	V	1
Input current (OV_{IN}= 0 V or OV_{IN} = OV_{DD})	I_{IN}	—	—	±40	μA	2

Notes:

1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. The symbol OV_{IN}, in this case, represents the OV_{IN} symbol referenced in Section 2.1.2, “Recommended operating conditions.”

2.9.1 DDR3 and DDR3L SDRAM interface DC electrical characteristics

This table provides the recommended operating conditions for the DDR SDRAM controller when interfacing to DDR3 SDRAM.

Table 18. DDR3 SDRAM interface DC electrical characteristics (GV_{DD} = 1.5 V)[1]

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
I/O reference voltage	MV_{REF}	0.49 × GV_{DD}	0.51 × GV_{DD}	V	2, 3, 4
Input high voltage	V_{IH}	MV_{REF} + 0.100	GV_{DD}	V	5
Input low voltage	V_{IL}	GND	MV_{REF} – 0.100	V	5
I/O leakage current	I_{OZ}	–50	50	μA	6

Notes:

1. GV_{DD} is expected to be within 50 mV of the DRAM's voltage supply at all times. The DRAM's and memory controller's voltage supply may or may not be from the same source.
2. MV_{REF} is expected to be equal to 0.5 × GV_{DD} and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed the MV_{REF} DC level by more than ±1% of the DC value (that is, ±15 mV).
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made, and it is expected to be equal to MV_{REF} with a min value of MV_{REF} – 0.04 and a max value of MV_{REF} + 0.04. V_{TT} should track variations in the DC level of MV_{REF}
4. The voltage regulator for MV_{REF} must meet the specifications stated in Table 21.
5. Input capacitance load for DQ, DQS, and $\overline{DQS}$ are available in the IBIS models.
6. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GV_{DD}.

This table provides the recommended operating conditions for the DDR SDRAM controller when interfacing to DDR3L SDRAM.

Table 19. DDR3L SDRAM interface DC electrical characteristics (GV_{DD} = 1.35 V)[1]

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
I/O reference voltage	MV_{REF}	0.49 × GV_{DD}	0.51 × GV_{DD}	V	2, 3, 4
Input high voltage	V_{IH}	MV_{REF} + 0.090	GV_{DD}	V	5
Input low voltage	V_{IL}	GND	MV_{REF} – 0.090	V	5

2.9.2.2 DDR3 and DDDR3L SDRAM interface output AC timing specifications

This table contains the output AC timing targets for the DDR3 SDRAM interface.

Table 25. DDR3 and DDR3L SDRAM interface output AC timing specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol[1]	Min	Max	Unit	Notes
MCK[n] cycle time	t_{MCK}	1.25	2.5	ns	2
ADDR/CMD output setup with respect to MCK	t_{DDKHAS}			ns	3
1600 MT/s data rate		0.495	—		
1333 MT/s data rate		0.606	—		
1200 MT/s data rate		0.675	—		
1066 MT/s data rate		0.744	—		
800 MT/s data rate		0.917	—		
ADDR/CMD output hold with respect to MCK	t_{DDKHAX}			ns	3
1600 MT/s data rate		0.495	—		
1333 MT/s data rate		0.606	—		
1200 MT/s data rate		0.675	—		
1066 MT/s data rate		0.744	—		
800 MT/s data rate		0.917	—		
$\overline{\text{MCS}}$[n] output setup with respect to MCK	t_{DDKHCS}			ns	3
1600 MT/s data rate		0.495	—		
1333 MT/s data rate		0.606	—		
1200 MT/s data rate		0.675	—		
1066 MT/s data rate		0.744	—		
800 MT/s data rate		0.917	—		
$\overline{\text{MCS}}$[n] output hold with respect to MCK	t_{DDKHCX}			ns	3
1600 MT/sdata rate		0.495	—		
1333 MT/s data rate		0.606	—		
1200 MT/s data rate		0.675	—		
1066 MT/sdata rate		0.744	—		
800 MT/s data rate		0.917	—		
MCK to MDQS Skew	t_{DDKHMH}			ns	4
≥ 1066 MT/s data rate		–0.245	0.245		
800 MT/s data rate		–0.375	0.375		

Table 25. DDR3 and DDR3L SDRAM interface output AC timing specifications (continued)

For recommended operating conditions, see Table 3.

Parameter	Symbol[1]	Min	Max	Unit	Notes
MDQ/MECC/MDM output setup with respect to MDQS	t_{DDKHDS}, t_{DDKLDS}			ps	5
1600 MT/s data rate		200	—		
1333 MT/s data rate		250	—		
1200 MT/s data rate		275	—		
1066 MT/s data rate		300	—		
800 MT/s data rate		375	—		
MDQ/MECC/MDM output hold with respect to MDQS	t_{DDKHDX}, t_{DDKLDX}			ps	5
1600 MT/s data rate		200	—		
1333 MT/s data rate		250	—		
1200 MT/s data rate		275	—		
1066 MT/s data rate		300	—		
800 MT/s data rate		375	—		
MDQS preamble	t_{DDKHMP}	$0.9 \times t_{MCK}$	—	ns	—
MDQS post-amble	t_{DDKHME}	$0.4 \times t_{MCK}$	$0.6 \times t_{MCK}$	ns	—

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{\text{MCK}}$ and MDQS/$\overline{\text{MDQS}}$ referenced measurements are made from the crossing of the two signals.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{\text{MCK}}$, $\overline{\text{MCS}}$, and MDQ/MECC/MDM/MDQS.
4. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the MDQS override bits (called WR_DATA_DELAY) in the TIMING_CFG_2 register. This is typically set to the same delay as in DDR_SDRAM_CLK_CNTL[CLK_ADJUST]. The timing parameters listed in the table assume that these two parameters have been set to the same adjustment value. See the applicable chip reference manual for a description and explanation of the timing modifications enabled by use of these bits.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.

NOTE

For the ADDR/CMD setup and hold specifications in Table 25, it is assumed that the clock control register is set to adjust the memory clocks by ½ applied cycle.

This figure provides the AC test load for eTSEC.

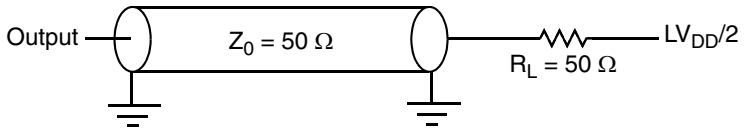


Figure 16. eTSEC AC test load

This figure shows the MII receive AC timing diagram.

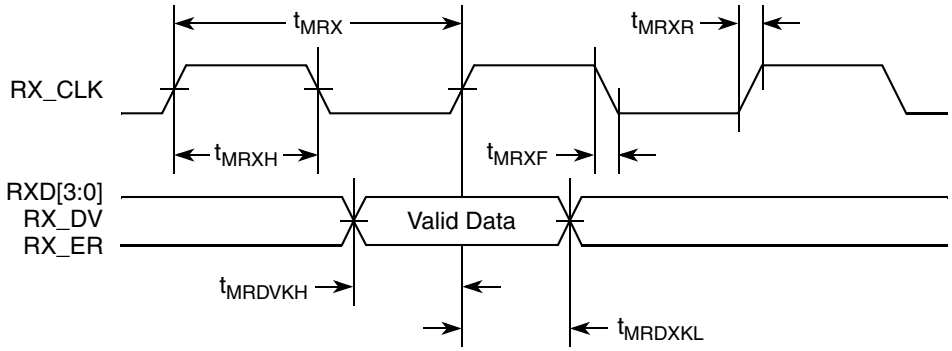


Figure 17. MII Receive AC timing diagram

2.12.2.3 RGMII AC timing specifications

This table presents the RGMII AC timing specifications.

Table 36. RGMII AC timing specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol[1]	Min	Typ	Max	Unit	Notes
Data to clock output skew (at transmitter)	t_{SKRGT_TX}	–500	0	500	ps	5
Data to clock input skew (at receiver)	t_{SKRGT_RX}	1.0	—	2.6	ns	2
Clock period duration	t_{RGT}	7.2	8.0	8.8	ns	3
Duty cycle for 10BASE-T and 100BASE-TX	t_{RGTH}/t_{RGT}	40	50	60	%	3, 4
Duty cycle for Gigabit	t_{RGTH}/t_{RGT}	45	50	55	%	—
Rise time (20%–80%)	t_{RGTR}	—	—	0.75	ns	—

Table 42. eTSEC IEEE 1588 DC electrical characteristics (LV_{DD} = 3.3 V) (continued)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Notes
Input low current (LV_{DD} = Max, V_{IN} = 0.5 V)	I_{IL}	–600	—	μA	1
Output high voltage (LV_{DD} = Min, I_{OH} = –1.0 mA)	V_{OH}	2.4	—	V	—
Output low voltage (LV_{DD} = Min, I_{OL} = 1.0 mA)	V_{OL}	—	0.4	V	—

Note:

1. Note that the symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 2 and Table 3.
2. The min V_{IL} and max V_{IH} values are based on the respective LV_{IN} values found in Table 3.

2.12.4.2 eTSEC IEEE Std 1588 AC specifications

This table provides the IEEE 1588 AC timing specifications.

Table 43. eTSEC IEEE 1588 AC timing specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
TSEC_1588_CLK clock period	$t_{T1588CLK}$	3.3	—	$T_{RX\_CLK} \times 7$	ns	1, 2
TSEC_1588_CLK duty cycle	$t_{T1588CLKH}/t_{T1588CLK}$	40	50	60	%	3
TSEC_1588_CLK peak-to-peak jitter	$t_{T1588CLKINJ}$	—	—	250	ps	—
Rise time eTSEC_1588_CLK (20%–80%)	$t_{T1588CLKINR}$	1.0	—	2.0	ns	—
Fall time eTSEC_1588_CLK (80%–20%)	$t_{T1588CLKINF}$	1.0	—	2.0	ns	—
TSEC_1588_CLK_OUT clock period	$t_{T1588CLKOUT}$	$2 \times t_{T1588CLK}$	—	—	ns	—
TSEC_1588_CLK_OUT duty cycle	$t_{T1588CLKOTH}/t_{T1588CLKOUT}$	30	50	70	%	—
TSEC_1588_PULSE_OUT	$t_{T1588OV}$	0.5	—	3.0	ns	—
TSEC_1588_TRIG_IN pulse width	$t_{T1588TRIGH}$	$2 \times t_{T1588CLK\_MAX}$	—	—	ns	2

Notes:

1. T_{RX_CLK} is the maximum clock period of eTSEC receiving clock selected by TMR_CTRL[CKSEL]. See the *QorIQ Integrated Processor Reference Manual* for a description of TMR_CTRL registers.
2. The maximum value of $t_{T1588CLK}$ is not only defined by the value of T_{RX_CLK}, but also defined by the recovered clock. For example, for 10/100/1000 Mbps modes, the maximum value of $t_{T1588CLK}$ be 2800, 280, and 56 ns, respectively.
3. It needs to be at least two times the clock period of the clock selected by TMR_CTRL[CKSEL]. See the *QorIQ Integrated Processor Reference Manual* for a description of TMR_CTRL registers.

This figure shows the AC timing diagram of the local bus interface.

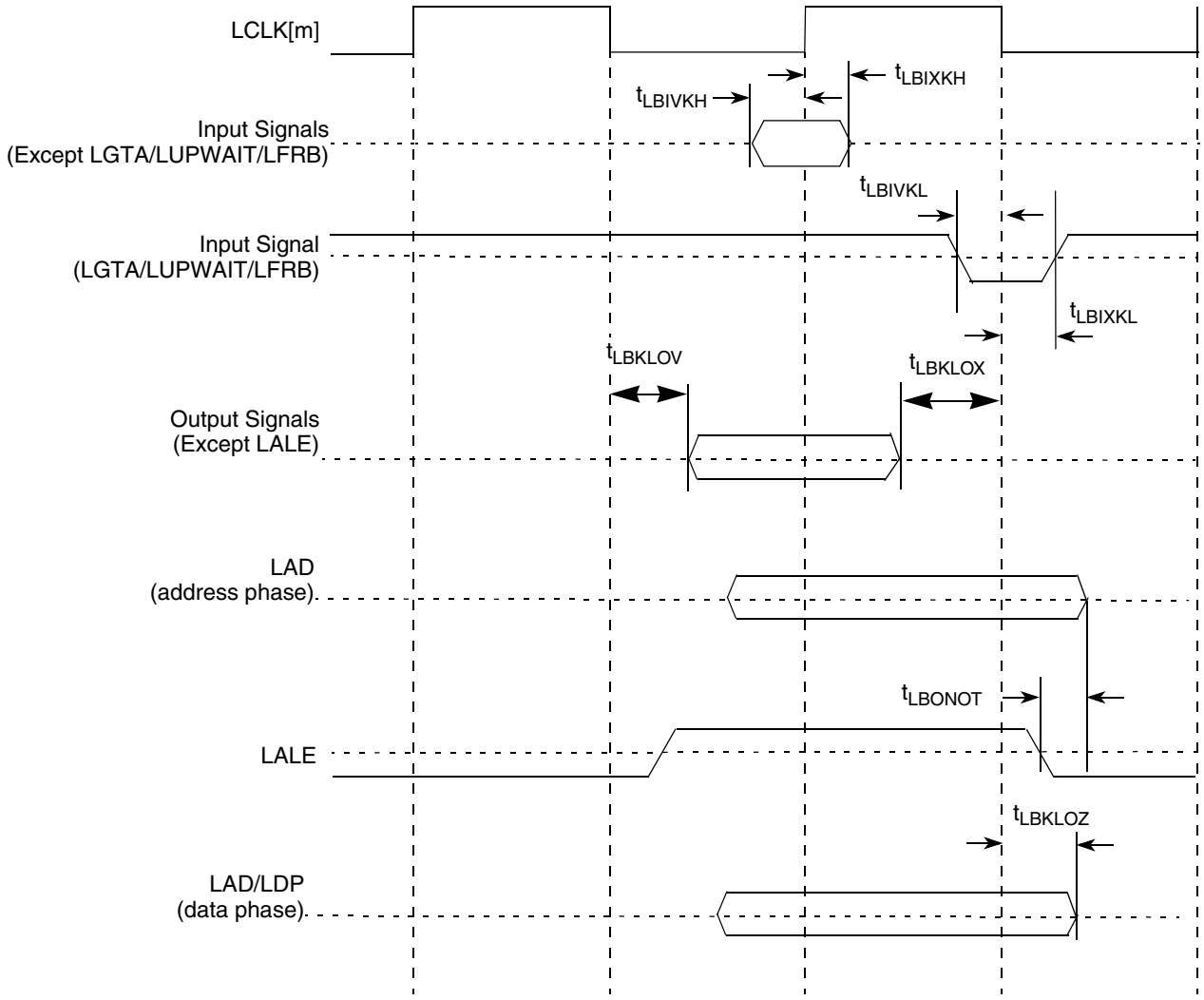


Figure 24. Enhanced local bus signals

Figure 25 applies to all three controllers that eLBC supports: GPCM, UPM, and FCM.

For input signals, the local bus AC timing data is used directly for all three controllers.

For output signals, each type of controller provides its own unique method to control the signal timing. The final signal delay value for output signals is the programmed delay plus the AC timing delay. For example, for GPCM, LCS can be programmed to delay by t_{acs} (0, ¼, ½, 1, 1 + ¼, 1 + ½, 2, 3 cycles), so the final delay is $t_{acs} + t_{LBKLOV}$.

— For an external AC-coupled connection, there is no common mode voltage requirement for the clock driver. Because the external AC-coupling capacitor blocks the DC level, the clock driver and the SerDes reference clock receiver operate in different common mode voltages. The SerDes reference clock receiver in this connection scheme has its common mode voltage set to SGND. Each signal wire of the differential inputs is allowed to swing below and above the common mode voltage (SGND). Figure 38 shows the SerDes reference clock input requirement for AC-coupled connection scheme.

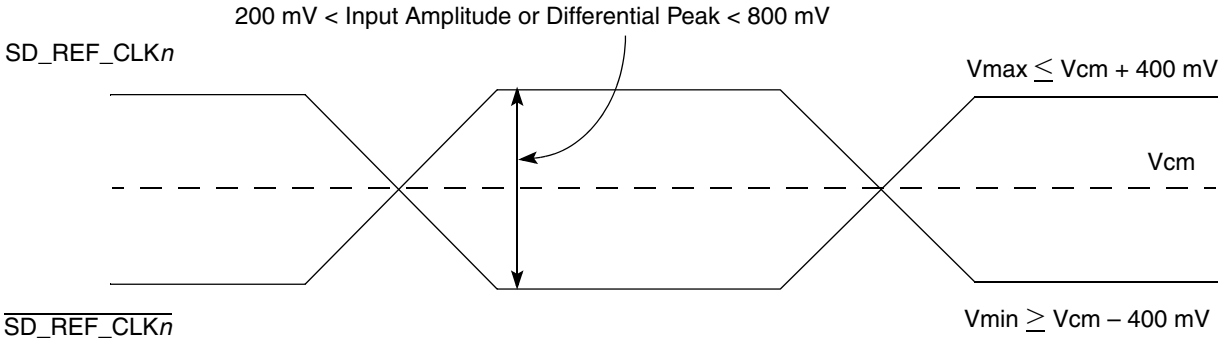


Figure 38. Differential reference clock input DC requirements (external AC-coupled)

- Single-Ended Mode
  — The reference clock can also be single-ended. The SD_REF_CLK*n* input amplitude (single-ended swing) must be between 400 mV and 800 mV peak-peak (from V_{MIN} to V_{MAX}) with $\overline{\text{SD\_REF\_CLK}n}$ either left unconnected or tied to ground.
  — The SD_REF_CLK*n* input average voltage must be between 200 and 400 mV. Figure 39 shows the SerDes reference clock input requirement for single-ended signaling mode.
  — To meet the input amplitude requirement, the reference clock inputs may need to be DC- or AC-coupled externally. For the best noise performance, the reference of the clock could be DC- or AC-coupled into the unused phase ($\overline{\text{SD\_REF\_CLK}n}$) through the same source impedance as the clock input (SD_REF_CLK*n*) in use.

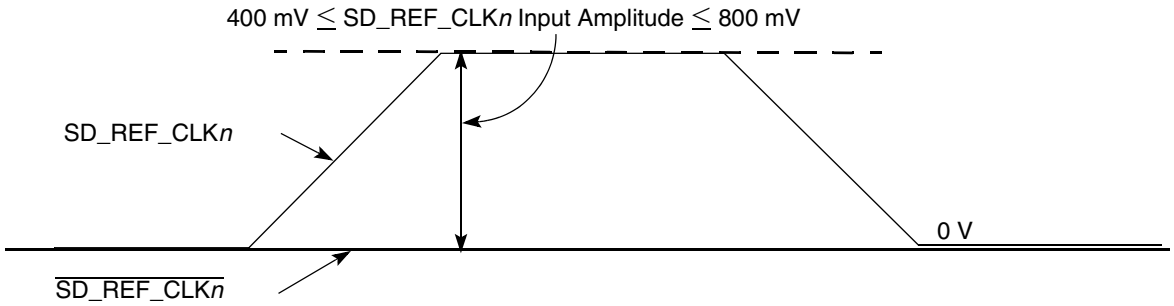


Figure 39. Single-ended reference clock input DC requirements

This table defines the AC specifications for the PCI Express 2.0 (2.5 GT/s) differential input at all receivers. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 68. PCI Express 2.0 (2.5 GT/s) differential receiver Input AC specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typ	Max	Units	Notes
Unit Interval	UI	399.88	400.00	400.12	ps	Each UI is 400 ps ± 300 ppm. UI does not account for spread spectrum clock dictated variations. See Note 1.
Minimum receiver eye width	T_{RX-EYE}	0.4	—	—	UI	The maximum interconnect media and transmitter jitter that can be tolerated by the receiver can be derived as $T_{RX-MAX-JITTER} = 1 - T_{RX-EYE} = 0.6$ UI. See Notes 2 and 3.
Maximum time between the jitter median and maximum deviation from the median.	$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	—	—	0.3	UI	Jitter is defined as the measurement variation of the crossing points ($V_{RX-DIFFp-p} = 0$ V) in relation to a recovered transmitter UI. A recovered transmitter UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the transmitter UI. See Notes 2, 3 and 4.

Notes:

1. No test load is necessarily associated with this value.
2. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 43 should be used as the receiver device when taking measurements. If the clocks to the receiver and transmitter are not derived from the same reference clock, the transmitter UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.
3. A $T_{RX-EYE} = 0.40$ UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the transmitter and interconnect collected any 250 consecutive UIs. The TRX-EYE-MEDIAN-to-MAX-JITTER specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive transmitter UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the receiver and transmitter are not derived from the same reference clock, the transmitter UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.
4. It is recommended that the recovered transmitter UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.

This table provides the Gen2i or 3 Gbits/s differential receiver input DC characteristics for the SATA interface.

Table 82. Gen2i/3 G receiver Input DC specifications (XV_{DD} = 1.5 V or 1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typical	Max	Units	Notes
Differential input voltage	V_{SATA_RXDIFF}	275	—	750	mV p-p	1
Differential receiver input impedance	Z_{SATA_RXSEIM}	85	100	115	Ω	2
OOB signal detection threshold	V_{SATA_OOB}	75	120	240	mV p-p	2

Notes:
1. Voltage relative to common of either signal comprising a differential pair
2. DC impedance

2.20.7.2 SATA AC timing specifications

This section discusses the SATA AC timing specifications.

2.20.7.2.1 AC requirements for SATA REF_CLK

The AC requirements for the SATA reference clock are listed in this table to be guaranteed by the customer's application design.

Table 83. SATA reference clock input requirements

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ frequency range	t_{CLK_REF}	—	100/125	—	MHz	1
SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ clock frequency tolerance	t_{CLK_TOL}	–350	—	+350	ppm	—
SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ reference clock duty cycle	t_{CLK_DUTY}	40	50	60	%	5
SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ cycle-to-cycle clock jitter (period jitter)	t_{CLK_CJ}	—	—	100	ps	2
SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ total reference clock jitter, phase jitter (peak-peak)	t_{CLK_PJ}	–50	—	+50	ps	2, 3, 4

Notes:
1. **Caution:** Only 100, and 125 MHz have been tested. In-between values do not work correctly with the rest of the system.
2. At RefClk input
3. In a frequency band from 150 kHz to 15 MHz at BER of 10^{-12}
4. Total peak-to-peak deterministic jitter should be less than or equal to 50 ps.
5. Measurement taken from differential waveform

Table 87. Gen 2i/3G receiver AC specifications (continued)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typical	Max	Units	Notes
Deterministic jitter, $f_{C3dB} = f_{BAUD} \div 10$	$U_{SATA\_TXDJfB/10}$	—	—	0.35	UI p-p	1
Deterministic jitter, $f_{C3dB} = f_{BAUD} \div 500$	$U_{SATA\_TXDJfB/500}$	—	—	0.42	UI p-p	1
Deterministic jitter, $f_{C3dB} = f_{BAUD} \div 1667$	$U_{SATA\_TXDJfB/1667}$	—	—	0.35	UI p-p	1

Note:

1. Measured at receiver

2.20.8 SGMII interface

Each SGMII port features a 4-wire AC-coupled serial link from the SerDes interface of the chip, as shown in Figure 46, where C_{TX} is the external (on board) AC-coupled capacitor. Each output pin of the SerDes transmitter differential pair features 50-Ω output impedance. Each input of the SerDes receiver differential pair features 50-Ω on-die termination to XGND. The reference circuit of the SerDes transmitter and receiver is shown in Figure 42.

2.20.8.0.1 SGMII clocking requirements for SD_REF_CLK*n* and $\overline{\text{SD\_REF\_CLK}n}$

When operating in SGMII mode, the EC_GTX_CLK125 clock is not required for this port. Instead, a SerDes reference clock is required on SD_REF_CLK[1:3] and $\overline{\text{SD\_REF\_CLK}[1:3]}$ pins. SerDes banks 1-3 may be used for SerDes SGMII configurations based on the RCW Configuration field SRDS_PRTCL.

For more information on these specifications, see Section 2.20.2, "SerDes reference clocks."

2.20.8.1 SGMII DC electrical characteristics

This section discusses the electrical characteristics for the SGMII interface.

2.20.8.1.1 SGMII transmit DC timing specifications

This table describe the SGMII SerDes transmitter and receiver AC-coupled DC electrical characteristics for 1.25 GBaud. Transmitter DC characteristics are measured at the transmitter outputs (SD_TX*n* and $\overline{\text{SD\_TX}n}$) as shown in Figure 47.

Table 88. SGMII DC transmitter electrical characteristics (XV_{DD} = 1.5 V or 1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Output high voltage	V_{OH}	—	—	1.5 x $\lvert V_{OD}\rvert_{-max}$	mV	1
Output low voltage	V_{OL}	$\lvert V_{OD}\rvert_{-min}/2$	—	—	mV	1

This figure shows an example of a 4-wire AC-coupled SGMII serial link connection.

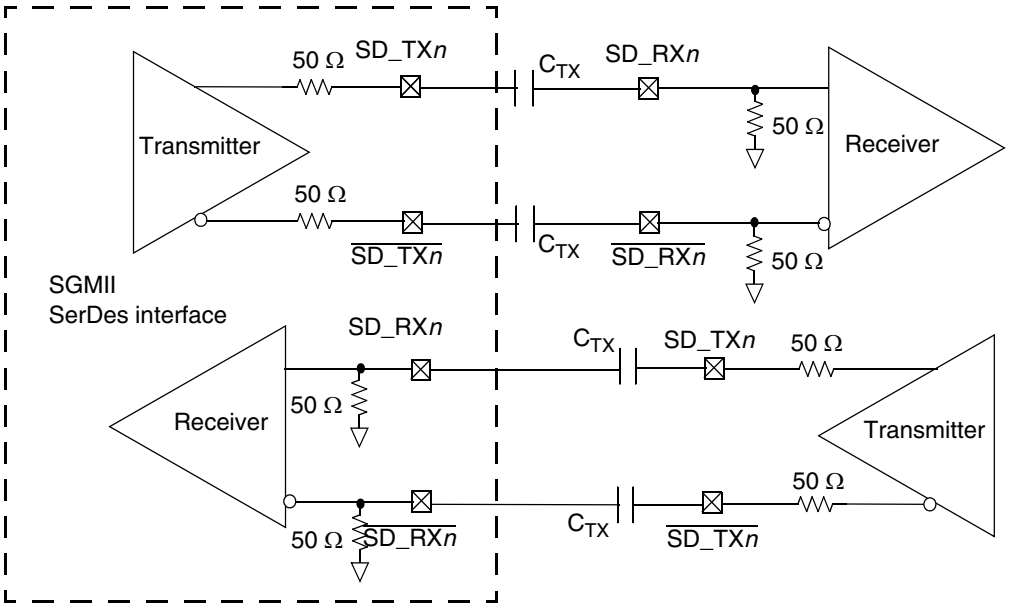


Figure 46. 4-wire, AC-coupled, SGMII serial link connection example

This figure shows the SGMII transmitter DC measurement circuit.

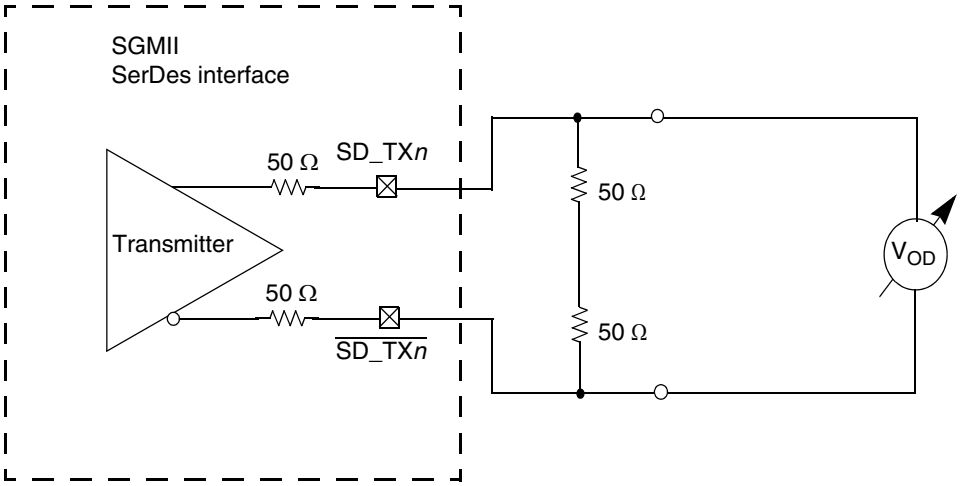


Figure 47. SGMII transmitter DC measurement circuit

3.1.8 Frame Manager (FMan) clock select

The Frame Managers (FM) can each be synchronous with or asynchronous to the platform, depending on configuration.

This table describes the clocking options that may be applied to each FM. The clock selection is determined by the binary value of the RCW Clocking Configuration fields FM1_CLK_SEL and FM2_CLK_SEL.

Table 105. Frame Manager (FMan) clock select

Binary value of FM*n*_CLK_SEL	FM frequency
0b0	Platform Clock Frequency /2
0b1	FMan PLL Frequency /2 [1,2]

Notes:

1. For asynchronous mode, max frequency see Table 94.
2. For PLL settings, see Table 96.

3.2 Supply power default setting

This chip is capable of supporting multiple power supply levels on its I/O supplies. The I/O voltage select inputs, shown in the following table, properly configure the receivers and drivers of the I/Os associated with the BVDD, CVDD, and LVDD power planes, respectively.

WARNING

Incorrect voltage select settings can lead to irreversible device damage.

3.7 Recommended thermal model

Information about Flotherm models of the package or thermal data not available in this document can be obtained from your local Freescale sales office.

3.8 Thermal management information

This section provides thermal management information for the flip-chip, plastic-ball, grid array (FC-PBGA) package for air-cooled applications. Proper thermal control design is primarily dependent on the system-level design—the heat sink, airflow, and thermal interface material.

The recommended attachment method to the heat sink is illustrated in this figure. The heat sink should be attached to the printed-circuit board with the spring force centered over the die. This spring force should not exceed 10 pounds force (45 Newton).

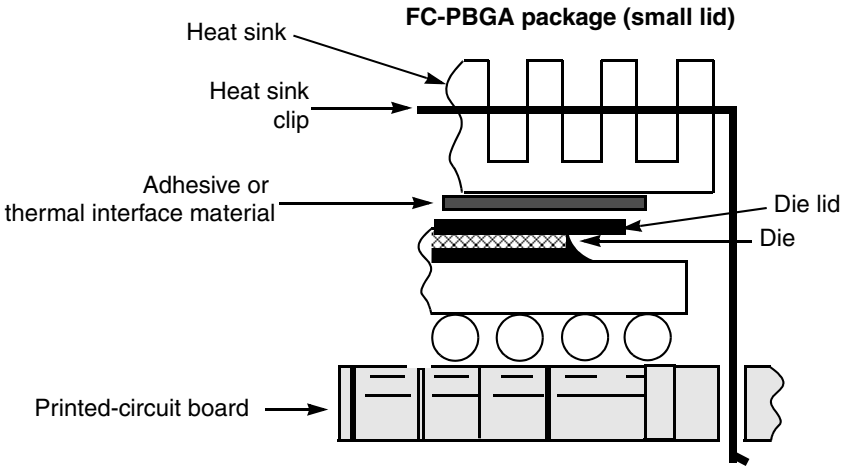


Figure 62. Exploded cross-sectional view—FC-PBGA (with lid) package

The system board designer can choose between several types of heat sinks to place on the device. There are several commercially-available thermal interfaces to choose from in the industry. Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost.

3.8.1 Internal package conduction resistance

For the package, the intrinsic internal conduction thermal resistance paths are as follows:

- The die junction-to-case thermal resistance
- The die junction-to-lid-top thermal resistance
- The die junction-to-board thermal resistance