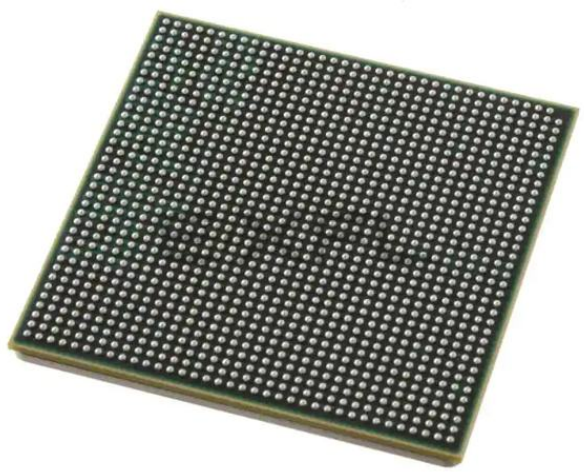

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e5500
Number of Cores/Bus Width	2 Core, 64-Bit
Speed	1.8GHz
Co-Processors/DSP	-
RAM Controllers	DDR3, DDR3L
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	1Gbps (10), 10Gbps (2)
SATA	SATA 3Gbps (2)
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.0V, 1.1V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Boot Security, Cryptography, Secure Fusebox, Secure Debug, Tamper Detection, Volatile key Storage
Package / Case	1295-BBGA, FCBGA
Supplier Device Package	1295-FCPBGA (37.5x37.5)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p5021nse7tmc

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
D1_MCK2	Clock	V8	O	GV_{DD}	—
D1_MCK3	Clock	W9	O	GV_{DD}	—
$\overline{\text{D1\_MCK0}}$	Clock Complements	W5	O	GV_{DD}	—
$\overline{\text{D1\_MCK1}}$	Clock Complements	V5	O	GV_{DD}	—
$\overline{\text{D1\_MCK2}}$	Clock Complements	V9	O	GV_{DD}	—
$\overline{\text{D1\_MCK3}}$	Clock Complements	W8	O	GV_{DD}	—
D1_MODT0	On Die Termination	AD10	O	GV_{DD}	—
D1_MODT1	On Die Termination	AG10	O	GV_{DD}	—
D1_MODT2	On Die Termination	AD8	O	GV_{DD}	—
D1_MODT3	On Die Termination	AF10	O	GV_{DD}	—
D1_MDIC0	Driver Impedance Calibration	T6	I/O	GV_{DD}	16
D1_MDIC1	Driver Impedance Calibration	AA5	I/O	GV_{DD}	16
DDR SDRAM Memory interface 2					
D2_MDQ00	Data	C13	I/O	GV_{DD}	—
D2_MDQ01	Data	A12	I/O	GV_{DD}	—
D2_MDQ02	Data	B9	I/O	GV_{DD}	—
D2_MDQ03	Data	A8	I/O	GV_{DD}	—
D2_MDQ04	Data	A13	I/O	GV_{DD}	—
D2_MDQ05	Data	B13	I/O	GV_{DD}	—
D2_MDQ06	Data	B10	I/O	GV_{DD}	—
D2_MDQ07	Data	A9	I/O	GV_{DD}	—
D2_MDQ08	Data	A7	I/O	GV_{DD}	—
D2_MDQ09	Data	D6	I/O	GV_{DD}	—
D2_MDQ10	Data	A4	I/O	GV_{DD}	—
D2_MDQ11	Data	B4	I/O	GV_{DD}	—
D2_MDQ12	Data	C7	I/O	GV_{DD}	—
D2_MDQ13	Data	B7	I/O	GV_{DD}	—
D2_MDQ14	Data	C5	I/O	GV_{DD}	—
D2_MDQ15	Data	D5	I/O	GV_{DD}	—
D2_MDQ16	Data	B1	I/O	GV_{DD}	—
D2_MDQ17	Data	B3	I/O	GV_{DD}	—
D2_MDQ18	Data	D3	I/O	GV_{DD}	—
D2_MDQ19	Data	E1	I/O	GV_{DD}	—
D2_MDQ20	Data	A3	I/O	GV_{DD}	—

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
$\overline{\text{D2\_MCS0}}$	Chip Select	AC1	O	GV_{DD}	—
$\overline{\text{D2\_MCS1}}$	Chip Select	AE1	O	GV_{DD}	—
$\overline{\text{D2\_MCS2}}$	Chip Select	AB3	O	GV_{DD}	—
$\overline{\text{D2\_MCS3}}$	Chip Select	AE2	O	GV_{DD}	—
D2_MCKE0	Clock Enable	R5	O	GV_{DD}	—
D2_MCKE1	Clock Enable	T5	O	GV_{DD}	—
D2_MCKE2	Clock Enable	P4	O	GV_{DD}	—
D2_MCKE3	Clock Enable	M4	O	GV_{DD}	—
D2_MCK0	Clock	W3	O	GV_{DD}	—
D2_MCK1	Clock	V3	O	GV_{DD}	—
D2_MCK2	Clock	V1	O	GV_{DD}	—
D2_MCK3	Clock	W2	O	GV_{DD}	—
$\overline{\text{D2\_MCK0}}$	Clock Complements	W4	O	GV_{DD}	—
$\overline{\text{D2\_MCK1}}$	Clock Complements	V4	O	GV_{DD}	—
$\overline{\text{D2\_MCK2}}$	Clock Complements	V2	O	GV_{DD}	—
$\overline{\text{D2\_MCK3}}$	Clock Complements	W1	O	GV_{DD}	—
D2_MODT0	On Die Termination	AD2	O	GV_{DD}	—
D2_MODT1	On Die Termination	AF1	O	GV_{DD}	—
D2_MODT2	On Die Termination	AD1	O	GV_{DD}	—
D2_MODT3	On Die Termination	AE3	O	GV_{DD}	—
D2_MDIC0	Driver Impedance Calibration	AA4	I/O	GV_{DD}	16
D2_MDIC1	Driver Impedance Calibration	Y6	I/O	GV_{DD}	16
Local bus controller interface					
LAD00	Muxed Data/Address	K26	I/O	BV_{DD}	3
LAD01	Muxed Data/Address	L26	I/O	BV_{DD}	3
LAD02	Muxed Data/Address	J26	I/O	BV_{DD}	3
LAD03	Muxed Data/Address	H25	I/O	BV_{DD}	3
LAD04	Muxed Data/Address	F25	I/O	BV_{DD}	3
LAD05	Muxed Data/Address	H24	I/O	BV_{DD}	3
LAD06	Muxed Data/Address	G24	I/O	BV_{DD}	3
LAD07	Muxed Data/Address	G23	I/O	BV_{DD}	3
LAD08	Muxed Data/Address	E23	I/O	BV_{DD}	3
LAD09	Muxed Data/Address	D23	I/O	BV_{DD}	3
LAD10	Muxed Data/Address	J22	I/O	BV_{DD}	3

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
USB1_UID	USB1 PHY ID Detect	AK24	I	USB1_V_{DD}_1P8_DECAP	—
USB1_DRVVBUS/GPIO04	USB1 5V Supply Enable	AH21	O	OV_{DD}	26,38
USB1_PWRFAULT/GPIO05	USB1 Power Fault	AJ21	I	OV_{DD}	26,38
USB_CLKIN	USB PHY Clock Input	AM24	I	OV_{DD}	—
USB Port 2					
USB2_UDP	USB2 PHY Data Plus	AP27	I/O	USB_V_{DD}_3P3	—
USB2_UDM	USB2 PHY Data Minus	AP26	I/O	USB_V_{DD}_3P3	—
USB2_VBUS_CLMP	USB2 PHY VBUS Divided Signal	AK26	I	USB_V_{DD}_3P3	38
USB2_UID	USB2 PHY ID Detect	AK27	I	USB2_V_{DD}_1P8_DECAP	—
USB2_DRVVBUS/GPIO06	USB2 5V Supply Enable	AK21	O	OV_{DD}	26,38
USB2_PWRFAULT/GPIO07	USB2 Power Fault	AG20	O	OV_{DD}	26,38
Programmable Interrupt controller					
IRQ00	External Interrupts	AJ16	I	OV_{DD}	—
IRQ01	External Interrupts	AH16	I	OV_{DD}	—
IRQ02	External Interrupts	AK12	I	OV_{DD}	—
IRQ03/GPIO21	External Interrupts	AJ15	I	OV_{DD}	26
IRQ04/GPIO22	External Interrupts	AH17	I	OV_{DD}	26
IRQ05/GPIO23	External Interrupts	AJ13	I	OV_{DD}	26
IRQ06/GPIO24	External Interrupts	AG17	I	OV_{DD}	26
IRQ07/GPIO25	External Interrupts	AM13	I	OV_{DD}	26
IRQ08/GPIO26	External Interrupts	AG13	I	OV_{DD}	26
IRQ09/GPIO27	External Interrupts	AK11	I	OV_{DD}	26
IRQ10/GPIO28	External Interrupts	AH14	I	OV_{DD}	26
IRQ11/GPIO29	External Interrupts	AL12	I	OV_{DD}	26
$\overline{\text{IRQ\_OUT}}$/EVT9	Interrupt Output	AK14	O	OV_{DD}	1, 2, 26
Trust					
$\overline{\text{TMP\_DETECT}}$	Tamper Detect	AN19	I	OV_{DD}	27
$\overline{\text{LP\_TMP\_DETECT}}$	Low Power Tamper Detect	AE28	I	V_{DD_LP}	—
eSDHC					
SDHC_CMD	Command/Response	AG23	I/O	CV_{DD}	—

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
EC2_GTX_CLK/ EC2_TX_ER	Transmit Clock Out (RGMII) Transmit Error (MII)	AN31	O	LV_{DD}	26
EC2_RXD3	Receive Data	AP33	I	LV_{DD}	27
EC2_RXD2	Receive Data	AN32	I	LV_{DD}	27
EC2_RXD1	Receive Data	AP32	I	LV_{DD}	26, 27
EC2_RXD0	Receive Data	AT32	I	LV_{DD}	26, 27
EC2_RX_DV	Receive Data Valid	AR33	I	LV_{DD}	27
EC2_RX_CLK	Receive Clock	AT33	I	LV_{DD}	27
EC2_RX_ER	Receive Error (MII)	AH29	I	LV_{DD}	—
EC2_COL/EC_XTRNL_TX_STMP2	Collision Detect (MII)	AJ31	O	LV_{DD}	26
EC2_CRS/EC_XTRNL_RX_STMP2	Carrier Sense (MII)	AK31	O	LV_{DD}	26
UART					
UART1_SOUT/GPIO8	Transmit Data	AL22	O	OV_{DD}	26
UART2_SOUT/GPIO9	Transmit Data	AJ22	O	OV_{DD}	26
UART1_SIN/GPIO10	Receive Data	AR23	I	OV_{DD}	26
UART2_SIN/GPIO11	Receive Data	AN23	I	OV_{DD}	26
$\overline{\text{UART1\_RTS}}$/UART3_SOUT/GPIO12	Ready to Send	AM22	O	OV_{DD}	26
$\overline{\text{UART2\_RTS}}$/UART4_SOUT/GPIO13	Ready to Send	AK23	O	OV_{DD}	26
$\overline{\text{UART1\_CTS}}$/UART3_SIN/GPIO14	Clear to Send	AP22	I	OV_{DD}	26
$\overline{\text{UART2\_CTS}}$/UART4_SIN/GPIO15	Clear to Send	AH23	I	OV_{DD}	26
I^2C interface					
IIC1_SCL	Serial Clock	AH15	I/O	OV_{DD}	2, 14
IIC1_SDA	Serial Data	AN14	I/O	OV_{DD}	2, 14
IIC2_SCL	Serial Clock	AM15	I/O	OV_{DD}	2, 14
IIC2_SDA	Serial Data	AL14	I/O	OV_{DD}	2, 14
IIC3_SCL/$\overline{\text{SDHC\_CD}}$/GPIO16	Serial Clock	AK13	I/O	OV_{DD}	2, 14, 27
IIC3_SDA/SDHC_WP/GPIO17	Serial Data	AM14	I/O	OV_{DD}	2, 14, 27
IIC4_SCL/$\overline{\text{EVT5}}$	Serial Clock	AG14	I/O	OV_{DD}	2, 14
IIC4_SDA/$\overline{\text{EVT6}}$	Serial Data	AL15	I/O	OV_{DD}	2, 14
SerDes (x20) PCIe, Aurora, 10GE, 1GE, SATA					
SD_TX19	Transmit Data (positive)	AG25	O	XV_{DD}	—
SD_TX18	Transmit Data (positive)	AB28	O	XV_{DD}	—
SD_TX17	Transmit Data (positive)	AG31	O	XV_{DD}	—
SD_TX16	Transmit Data (positive)	AE31	O	XV_{DD}	—

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GND	Ground	J27	—	—	—
GND	Ground	F27	—	—	—
GND	Ground	G21	—	—	—
GND	Ground	K25	—	—	—
GND	Ground	B18	—	—	—
GND	Ground	L18	—	—	—
GND	Ground	J21	—	—	—
GND	Ground	M27	—	—	—
GND	Ground	G13	—	—	—
GND	Ground	F15	—	—	—
GND	Ground	H11	—	—	—
GND	Ground	J9	—	—	—
GND	Ground	K7	—	—	—
GND	Ground	L5	—	—	—
GND	Ground	M3	—	—	—
GND	Ground	R3	—	—	—
GND	Ground	P5	—	—	—
GND	Ground	N7	—	—	—
GND	Ground	M9	—	—	—
GND	Ground	V25	—	—	—
GND	Ground	R9	—	—	—
GND	Ground	T7	—	—	—
GND	Ground	U5	—	—	—
GND	Ground	U3	—	—	—
GND	Ground	Y3	—	—	—
GND	Ground	Y5	—	—	—
GND	Ground	W7	—	—	—
GND	Ground	V10	—	—	—
GND	Ground	AA9	—	—	—
GND	Ground	AB7	—	—	—
GND	Ground	AC5	—	—	—
GND	Ground	AD3	—	—	—
GND	Ground	AD9	—	—	—
GND	Ground	AE7	—	—	—

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
VDD_PL	Platform Supply	U17	—	V_{DD_PL}	—
VDD_PL	Platform Supply	U19	—	V_{DD_PL}	—
VDD_PL	Platform Supply	T14	—	V_{DD_PL}	—
VDD_PL	Platform Supply	AD14	—	V_{DD_PL}	—
VDD_PL	Platform Supply	AD16	—	V_{DD_PL}	—
VDD_PL	Platform Supply	AD18	—	V_{DD_PL}	—
VDD_PL	Platform Supply	AD20	—	V_{DD_PL}	—
VDD_PL	Platform Supply	Y14	—	V_{DD_PL}	—
VDD_CA	Core/L2 Group A Supply	T20	—	V_{DD_CA}	—
VDD_CA	Core/L2 Group A Supply	P20	—	V_{DD_CA}	—
VDD_CA	Core/L2 Group A Supply	R21	—	V_{DD_CA}	—
VDD_CA	Core/L2 Group A Supply	R19	—	V_{DD_CA}	—
VDD_CA	Core/L2 Group A Supply	P14	—	V_{DD_CA}	—
VDD_CA	Core/L2 Group A Supply	N19	—	V_{DD_CA}	—
VDD_CA	Core/L2 Group A Supply	M20	—	V_{DD_CA}	—
VDD_CA	Core/L2 Group A Supply	N21	—	V_{DD_CA}	—
VDD_CA	Core/L2 Group A Supply	M16	—	V_{DD_CA}	—
VDD_CA	Core/L2 Group A Supply	N15	—	V_{DD_CA}	—
VDD_CA	Core/L2 Group A Supply	P16	—	V_{DD_CA}	—
VDD_CA	Core/L2 Group A Supply	T16	—	V_{DD_CA}	—
VDD_CA	Core/L2 Group A Supply	R17	—	V_{DD_CA}	—
VDD_CA	Core/L2 Group A Supply	T18	—	V_{DD_CA}	—
VDD_CA	Core/L2 Group A Supply	R15	—	V_{DD_CA}	—
VDD_CA	Core/L2 Group A Supply	N17	—	V_{DD_CA}	—
VDD_CA	Core/L2 Group A Supply	M18	—	V_{DD_CA}	—
VDD_CA	Core/L2 Group A Supply	P18	—	V_{DD_CA}	—
VDD_LP	Low Power Security Monitor Supply	AD28	—	V_{DD_LP}	—
AVDD_CC1	Core Cluster PLL1 Supply	A20	—	—	13
AVDD_CC2	Core Cluster PLL2 Supply	AT18	—	—	13
AVDD_PLAT	Platform PLL Supply	AT20	—	—	13
AVDD_DDR	DDR PLL Supply	A19	—	—	13
AVDD_FM	FMan PLL Supply	AT19	—	—	13
AVDD_SRDS1	SerDes PLL1 Supply	A33	—	—	13

Table 6. Power dissipation (continued)

Power Mode	Core freq (MHz)	Plat freq (MHz)	DDR data rate (MHz)	FM freq (MHz)	V_{DD_PL}, SV_{DD} (V)	V_{DD_CA} (V)	Junction temp (°C)	Core and platform power[1] (W)	V_{DD_PL} power (W)	V_{DD_CA} power (W)	SV_{DD} power (W)	Note
Typical	1800	600	1200	450	1.0	1.1	65	20	—	—	—	—
Thermal							105	29	—	—	—	—
Maximum								30	15	13	13	2.2

Notes:
1. Combined power of VDD_PL, VDD_CA, SVDD with both DDR controllers and all SerDes banks active. Does not include I/O power.
2. Typical power assumes Dhrystone running with activity factor of 80% (on all cores) and executing DMA on the platform with 90% activity factor.
3. Typical power based on nominal processed device.
4. Maximum power assumes Dhrystone running with activity factor at 100% (on all cores) and executing DMA on the platform at 100% activity factor.
5. Thermal power assumes Dhrystone running with activity factor of 80% (on all cores) and executing DMA on the platform at 90% activity factor.
6. Maximum power provided for power supply design sizing.
7. Thermal and maximum power are based on worst case processed device.

This table shows the estimated power dissipation on the AV_{DD} and AV_{DD_SRDS} supplies for the chip's PLLs, at allowable voltage levels.

Table 7. AV_{DD} power dissipation

AV_{DD}s	Typical	Maximum	Unit	Notes
AV_{DD_DDR}	5	15	mW	1
AV_{DD_CC1}	5	15	mW	
AV_{DD_CC2}	5	15	mW	
AV_{DD_PLAT}	5	15	mW	
AV_{DD_FM}	5	15	mW	
AV_{DD_SRDS1}	—	36	mW	2
AV_{DD_SRDS2}	—	36	mW	
AV_{DD_SRDS3}	—	36	mW	
AV_{DD_SRDS4}	—	36	mW	
USB_V_{DD}_1P0	—	10	mW	3
V_{DD_LP}	—	5	mW	

Note:
1. V_{DD_CA} = 1.2 V, T_A = 80°C, T_J = 105°C
2. V_{DD_PL}, SV_{DD} = 1.0 V, T_A = 80°C, T_J = 105°C
3. USB_V_{DD}_1P0, V_{DD_LP} = 1.0 V, T_A = 80°C, T_J = 105°C

Table 10. Package thermal characteristics (continued)[6]

Rating	Board	Symbol	Value	Unit	Notes
Junction to board	—	$R_{\Theta JB}$	3	°C/W	3
Junction to case top	—	$R_{\Theta JCtop}$	0.44	°C/W	4
Junction to lid top	—	$R_{\Theta JClid}$	0.17	°C/W	5

Notes:

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Junction-to-board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.
3. Junction-to-case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.
4. Junction-to-Lid-Top thermal resistance determined using the using MIL-STD 883 Method 1012.1. However, instead of the cold plate, the lid top temperature is used here for the reference case temperature. The reported value does not include the thermal resistance of the interface layer between the package and cold plate.
5. Junction-to-lid-top thermal resistance determined using the using MIL-STD 883 Method 1012.1. However, instead of the cold plate, the lid top temperature is used here for the reference case temperature. Reported value does not include the thermal resistance of the interface layer between the package and cold plate.
6. Reference Section 3.8, “Thermal management information,” for additional details.

2.6 Input clocks

This section discusses the system clock timing specifications for DC and AC power, spread spectrum sources, real time clock timing, and dTSEC gigabit Ethernet reference clocks AC timing.

2.6.1 System clock (SYSCLK) timing specifications

This table provides the system clock (SYSCLK) DC specifications.

Table 11. SYSCLK DC electrical characteristics (OV_{DD} = 3.3 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Input high voltage	V_{IH}	2.0	—	—	V	1
Input low voltage	V_{IL}	—	—	0.8	V	1
Input current (OV_{IN}= 0 V or OV_{IN} = OV_{DD})	I_{IN}	—	—	±40	μA	2

Notes:

1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. The symbol OV_{IN}, in this case, represents the OV_{IN} symbol referenced in Section 2.1.2, “Recommended operating conditions.”

2.13.1 USB DC electrical characteristics

This table provides the DC electrical characteristics for the USB interface at USB_V_{DD}_3P3 = 3.3 V.

Table 44. USB DC electrical characteristics (USB_V_{DD}_3P3 = 3.3 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage[1]	V_{IH}	2.0	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (USB_V_{IN}_3P3 = 0 V or USB_V_{IN}_3P3 = USB_V_{DD}_3P3)	I_{IN}	—	±40	μA	2
Output high voltage (USB_V_{DD}_3P3 = min, I_{OH} = –2 mA)	V_{OH}	2.8	—	V	—
Output low voltage (USB_V_{DD}_3P3 = min, I_{OL} = 2 mA)	V_{OL}	—	0.3	V	—

Notes:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max USB_V_{IN}_3P3 values found in Table 3.
2. The symbol USB_V_{IN}_3P3, in this case, represents the USB_V_{IN}_3P3 symbol referenced in Section 2.1.2, "Recommended operating conditions."

2.13.2 USB AC electrical specifications

This table provides the USB clock input (USB*n*_CLKIN) AC timing specifications.

Table 45. USB*n*_CLKIN AC timing specifications

For recommended operating conditions, see Table 3.

Parameter/Condition	Conditions	Symbol	Min	Typ	Max	Unit
Frequency range	—	$f_{USB\_CLK\_IN}$	—	24	—	MHz
Clock frequency tolerance	—	t_{CLK_TOL}	–0.005	0	0.005	%
Reference clock duty cycle	Measured at 1.6 V	t_{CLK_DUTY}	40	50	60	%
Total input jitter/time interval error	Peak-to-peak value measured with a second-order high-pass filter of 500 kHz bandwidth	t_{CLK_PJ}	—	—	5	ps

This figure provides the USB AC test load.

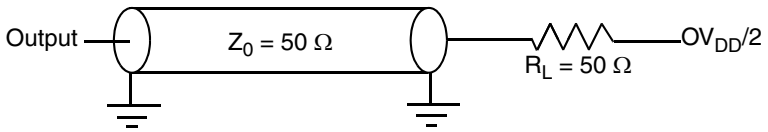

Figure 22. USB AC test load

2.14 Enhanced local bus interface (eLBC)

This section describes the DC and AC electrical specifications for the enhanced local bus interface.

Table 50. eSDHC interface DC electrical characteristics (continued)

For recommended operating conditions, see Table 3.

Characteristic	Symbol	Condition	Min	Max	Unit	Notes
Output low voltage	V_{OL}	I_{OL} = 100μA at CV_{DD} min	—	0.125 × CV_{DD}	V	—
Output high voltage	V_{OH}	I_{OH} = –100 μA at CV_{DD} min	CV_{DD} – 0.2	—	V	2
Output low voltage	V_{OL}	I_{OL} = 2 mA at CV_{DD} min	—	0.3	V	2

Notes:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max CV_{IN} values found in Table 3.
2. Open drain mode for MMC cards only.

2.15.2 eSDHC AC timing specifications

This table provides the eSDHC AC timing specifications as defined in Figure 26 and Figure 27.

Table 51. eSDHC AC timing specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol[1]	Min	Max	Unit	Notes
SD_CLK clock frequency: SD Full speed/high speed mode MMC Full speed/high speed mode	f_{SHSCK}	0	 25/50 20/52	MHz	2, 4
SD_CLK clock low time—Full-speed/High-speed mode	t_{SHSCKL}	10/7	—	ns	4
SD_CLK clock high time—Full-speed/High-speed mode	t_{SHSCKH}	10/7	—	ns	4
SD_CLK clock rise and fall times	t_{SHSCKR}/ t_{SHSCKF}	—	3	ns	4
Input setup times: SD_CMD, SD_DATx, SD_CD to SD_CLK	$t_{SHSIVKH}$	5	—	ns	3, 4, 5
Input hold times: SD_CMD, SD_DATx, SD_CD to SD_CLK	$t_{SHSIXKH}$	2.5	—	ns	4, 5
Output delay time: SD_CLK to SD_CMD, SD_DATx valid	$t_{SHSKHOV}$	–3	3	ns	4, 5

Notes:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first three letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first three letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{FHSKHOV}$ symbolizes eSDHC high-speed mode device timing (SHS) clock reference (K) going to the high (H) state, with respect to the output (O) reaching the invalid state (X) or output hold time. Note that in general, the clock reference symbol is based on five letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. In full-speed mode, the clock frequency value can be 0–25 MHz for an SD card and 0–20 MHz for an MMC card. In high-speed mode, the clock frequency value can be 0–50 MHz for an SD card and 0–52 MHz for an MMC card.
3. To satisfy setup timing, one way board routing delay between Host and Card, on SD_CLK, SD_CMD and SD_DATx should not exceed 1 ns. For any high speed or default speed mode SD card, the oneway routing delay between Host and Card on SD_CLK, SD_CMD and SD_DATx should not exceed 1.5 ns.
4. $C_{CARD} \leq 10$ pF, (1 card), and $C_L = C_{BUS} + C_{HOST} + C_{CARD} \leq 40$ pF
5. The parameter values apply to both full speed and high speed modes.

Table 64. PCI Express 2.0 (2.5 GT/s) differential receiver input DC specifications (XV_{DD} = 1.5 V or 1.8 V) (continued)

Parameter	Symbol	Min	Typ	Max	Units	Notes
Powered down DC input impedance	$Z_{RX-HIGH-IMP-DC}$	50 k	—	—	Ω	Required receiver D+ as well as D– DC Impedance when the receiver terminations do not have power. See Note 3.
Electrical idle detect threshold	$V_{RX-IDLE-DET-DIFFp-p}$	65	—	175	mV	$V_{RX-IDLE-DET-DIFFp-p}$ = 2 × $\lvert V_{RX-D+} - V_{RX-D-} \rvert$ Measured at the package pins of the receiver

Notes:
1. Measured at the package pins with a test load of 50 Ω to GND on each pin.
2. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all unconfigured lanes of a port.
3. The receiver DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the receiver ground.

This table defines the DC specifications for the PCI Express 2.0 (5 GT/s) differential input at all receivers. The parameters are specified at the component pins.

Table 65. PCI Express 2.0 (5 GT/s) differential receiver input DC specifications (XV_{DD} = 1.5 V or 1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typ	Max	Units	Notes
Differential input peak-to-peak voltage	$V_{RX-DIFFp-p}$	120	—	1200	V	$V_{RX-DIFFp-p} = 2 \times \lvert V_{RX-D+} - V_{RX-D-} \rvert$ See Note 1.
DC differential input impedance	$Z_{RX-DIFF-DC}$	80	100	120	Ω	Receiver DC Differential mode impedance. See Note 2
DC input impedance	Z_{RX-DC}	40	50	60	Ω	Required receiver D+ as well as D– DC Impedance (50 ±20% tolerance). See Notes 1 and 2.
Powered down DC input impedance	$Z_{RX-HIGH-IMP-DC}$	50	—	—	kΩ	Required receiver D+ as well as D– DC Impedance when the receiver terminations do not have power. See Note 3.
Electrical idle detect threshold	$V_{RX-IDLE-DET-DIFFp-p}$	65	—	175	mV	$V_{RX-IDLE-DET-DIFFp-p}$ = 2 × $\lvert V_{RX-D+} - V_{RX-D-} \rvert$ Measured at the package pins of the receiver

Notes:
1. Measured at the package pins with a test load of 50Ω to GND on each pin.
2. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all unconfigured lanes of a port.
3. The receiver DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the receiver ground.

2.20.7.1.1 SATA DC transmitter Output Characteristics

This table provides the DC differential transmitter output DC characteristics for the transmission.

Table 79. Gen1i/1.5G transmitter DC specifications (XV_{DD} = 1.5 V or 1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typ	Max	Units	Notes
Transmitter differential output voltage	V_{SATA_TXDIFF}	400	—	600	mV p-p	1
Transmitter differential pair impedance	$Z_{SATA\_TXDIFFIM}$	85	100	115	Ω	2

Notes:
1. Terminated by 50 Ω load
2. DC impedance

This table provides the differential transmitter output DC characteristics for the SATA interface at Gen2i or 3.0 Gbits/s transmission.

Table 80. Gen 2i/3G transmitter DC specifications (XV_{DD} = 1.5 V or 1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typ	Max	Units	Notes
Transmitter diff output voltage	V_{SATA_TXDIFF}	400	—	700	mV p-p	1
Transmitter differential pair impedance	$Z_{SATA\_TXDIFFIM}$	85	100	115	Ω	—

Note:
1. Terminated by 50 Ω load

2.20.7.1.2 SATA DC receiver Input Characteristics

This table provides the Gen1i or 1.5 Gbits/s differential receiver input DC characteristics for the SATA interface.

Table 81. Gen1i/1.5 G receiver Input DC specifications (XV_{DD} = 1.5 V or 1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typical	Max	Units	Notes
Differential input voltage	V_{SATA_RXDIFF}	240	—	600	mV p-p	1
Differential receiver input impedance	Z_{SATA_RXSEIM}	85	100	115	Ω	2
OOB signal detection threshold	V_{SATA_OOB}	50	120	240	mV p-p	2

Notes:
1. Voltage relative to common of either signal comprising a differential pair
2. DC impedance

Table 87. Gen 2i/3G receiver AC specifications (continued)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typical	Max	Units	Notes
Deterministic jitter, $f_{C3dB} = f_{BAUD} \div 10$	$U_{SATA\_TXDJfB/10}$	—	—	0.35	UI p-p	1
Deterministic jitter, $f_{C3dB} = f_{BAUD} \div 500$	$U_{SATA\_TXDJfB/500}$	—	—	0.42	UI p-p	1
Deterministic jitter, $f_{C3dB} = f_{BAUD} \div 1667$	$U_{SATA\_TXDJfB/1667}$	—	—	0.35	UI p-p	1

Note:

1. Measured at receiver

2.20.8 SGMII interface

Each SGMII port features a 4-wire AC-coupled serial link from the SerDes interface of the chip, as shown in Figure 46, where C_{TX} is the external (on board) AC-coupled capacitor. Each output pin of the SerDes transmitter differential pair features 50-Ω output impedance. Each input of the SerDes receiver differential pair features 50-Ω on-die termination to XGND. The reference circuit of the SerDes transmitter and receiver is shown in Figure 42.

2.20.8.0.1 SGMII clocking requirements for SD_REF_CLK*n* and $\overline{\text{SD\_REF\_CLK}n}$

When operating in SGMII mode, the EC_GTX_CLK125 clock is not required for this port. Instead, a SerDes reference clock is required on SD_REF_CLK[1:3] and $\overline{\text{SD\_REF\_CLK}[1:3]}$ pins. SerDes banks 1-3 may be used for SerDes SGMII configurations based on the RCW Configuration field SRDS_PRTCL.

For more information on these specifications, see Section 2.20.2, "SerDes reference clocks."

2.20.8.1 SGMII DC electrical characteristics

This section discusses the electrical characteristics for the SGMII interface.

2.20.8.1.1 SGMII transmit DC timing specifications

This table describe the SGMII SerDes transmitter and receiver AC-coupled DC electrical characteristics for 1.25 GBaud. Transmitter DC characteristics are measured at the transmitter outputs (SD_TX*n* and $\overline{\text{SD\_TX}n}$) as shown in Figure 47.

Table 88. SGMII DC transmitter electrical characteristics (XV_{DD} = 1.5 V or 1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Output high voltage	V_{OH}	—	—	1.5 x $\lvert V_{OD}\rvert_{-max}$	mV	1
Output low voltage	V_{OL}	$\lvert V_{OD}\rvert_{-min}/2$	—	—	mV	1

3.1.4 Core complex PLL select

The clock frequency of each of the core 0–1 complex is determined by the binary value of the RCW field C*n*_PLL_SEL. This table describes the supported ratios for each core complex 0-1, where each individual core complex can select a frequency from the table.

Table 97. Core complex [0,1] PLL select

Binary value of C*n*_PLL_SEL	Core cluster ratio
0000	CC1 PLL /1
0001	CC1 PLL /2
0100	CC2 PLL /1
0101	CC2 PLL/2
All Others	Reserved

Note: If CC2 PLL is used by core0 or core1, then CC2 PLL must be operated at a lower frequency than the CC1 PLL, and its maximum allowed frequency is 80% of the maximum rated frequency of the core at nominal voltage.

3.1.5 DDR controller PLL ratios

The dual DDR memory controller complexes can be synchronous with or asynchronous to the platform, depending on configuration. Both DDR controllers operate at the same frequency configuration.

Table 98 describes the clock ratio between the DDR memory controller PLLs and the externally supplied SYSCLK input (asynchronous mode) or from the platform clock (synchronous mode).

In asynchronous DDR mode, the DDR data rate to SYSCLK ratios supported are listed in Table 98. This ratio is determined by the binary value of the RCW Configuration field MEM_PLL_RAT[10:14]. The corresponding setting for MEM_PLL_CFG[0:1] is listed in Table 99.

NOTE

The RCW Configuration field DDR_SYNC (bit 184) must be set to b’0 for asynchronous mode, and b’1 for synchronous mode.

The RCW Configuration field DDR_RATE (bit 232) must be set to b’0 for asynchronous mode, and b’1 for synchronous mode.

The RCW Configuration field DDR_RSV0 (bit 234) must be set to b’0 for all ratios.

Table 98. Asynchronous DDR clock ratio

Binary value of MEM_PLL_RAT[10:14]	DDR:SYSCLK ratio
0_0101	5:1
0_0110	6:1
0_1000	8:1
0_1001	9:1
0_1010	10:1

Table 98. Asynchronous DDR clock ratio (continued)

Binary value of MEM_PLL_RAT[10:14]	DDR:SYSCLK ratio
0_1100	12:1
0_1101	13:1
1_0000	16:1
1_0010	18:1
1_0011	19:1
1_0100	20:1
1_1000	24:1
All Others	Reserved

Note:
1. RCW[MEM_PLL_CFG] is set dependant on the DDR clock ratio used. See Table 99 for valid setttings of DDR clock ratio and MEM_PLL_CFG.

Table 99. Supported DDR ratios and RCW MEM_PLL_CFG settings

MEM:SYSCLK Ratio	SYSCLK (MHz)			
	100	125	133.3	150
	DDR Rate (MT/s)/MEM_PLL_CFG			
1 (Sync Mode)	Platform Clock/01			
6	Reserved		800/11	900/11[3]
8	800/10[1]	1000/01[1]	1067/01	1200/01
9	900/10[2]	1125/01[2]	1200/01	1350/01
10	1000/01	1250/01	1333/01	1500/01
12	1200/11	1500/11	1600/11	Reserved
13	1300/11	Reserved		
16	1600/11	Reserved		

Notes:
1. For MEM SYSYCLK RATIO = 8, MEM_PLL_CFG changes from 10 to 01 when SYSCLK is greater than or equal to 120.9MHz
2. For MEM SYSYCLK RATIO = 9, MEM_PLL_CFG changes from 10 to 01 when SYSCLK is greater than or equal to 107.4MHz
3. Maximum SYSCLK is 161.2MHz when MEM:SYSCLK ratio = 6

In synchronous mode, the DDR data rate to platform clock ratios supported are listed in this table. This ratio is determined by the binary value of the RCW Configuration field MEM_PLL_RAT[10:14].

Table 100. Synchronous DDR clock ratio

Binary Value of MEM_PLL_RAT[10:14]	DDR:Platform CLK ratio	Set MEM_PLL_CFG=01 for platform CLK freq[1]
0_0001	1:1	>600 MHz
All Others	Reserved	—

Note:
1. Set RCW field MEM_PLL_CFG=0b01

3.1.6 Frequency options

This section discusses interface frequency options.

3.1.6.1 SYSCLK and platform frequency options

This table shows the expected frequency options for SYSCLK and platform frequencies.

Table 101. SYSCLK and platform frequency options

Platform: SYSCLK ratio	SYSCLK (MHz)			
	100	125	133.3	150
	Platform frequency (MHz)[1]			
5:1		625	666	750
6:1	600	750	800	
7:1	700			
8:1	800			

1 Platform frequency values are shown rounded down to the nearest whole number (decimal place accuracy removed)

3.1.6.2 Minimum platform frequency requirements for high-speed interfaces

The platform clock frequency must be considered for proper operation of high-speed interfaces as described below.

For proper PCI Express operation, the platform clock frequency must be greater than or equal to the values shown in these figures.

$$\frac{527\ \text{MHz} \times (\text{PCI Express link width})}{16}$$

Figure 49. Gen 1 PEX minimum platform frequency

$$\frac{527\ \text{MHz} \times (\text{PCI Express link width})}{8}$$

Figure 50. Gen 2 PEX minimum platform frequency

3.1.8 Frame Manager (FMan) clock select

The Frame Managers (FM) can each be synchronous with or asynchronous to the platform, depending on configuration.

This table describes the clocking options that may be applied to each FM. The clock selection is determined by the binary value of the RCW Clocking Configuration fields FM1_CLK_SEL and FM2_CLK_SEL.

Table 105. Frame Manager (FMan) clock select

Binary value of FM*n*_CLK_SEL	FM frequency
0b0	Platform Clock Frequency /2
0b1	FMan PLL Frequency /2 [1,2]

Notes:

1. For asynchronous mode, max frequency see Table 94.
2. For PLL settings, see Table 96.

3.2 Supply power default setting

This chip is capable of supporting multiple power supply levels on its I/O supplies. The I/O voltage select inputs, shown in the following table, properly configure the receivers and drivers of the I/Os associated with the BVDD, CVDD, and LVDD power planes, respectively.

WARNING

Incorrect voltage select settings can lead to irreversible device damage.

Boundary-scan testing is enabled through the JTAG interface signals. The TRST signal is optional in the IEEE Std 1149.1 specification, but it is provided on all processors built on Power Architecture technology. The device requires TRST to be asserted during power-on reset flow to ensure that the JTAG boundary logic does not interfere with normal device operation. While the TAP controller can be forced to the reset state using only the TCK and TMS signals, generally systems assert TRST during the power-on reset flow. Simply tying TRST to PORESET is not practical because the JTAG interface is also used for accessing the common on-chip processor (COP), which implements the debug interface to the chip.

The COP function of these processors allow a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert PORESET or TRST in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 56 allows the COP port to independently assert PORESET or TRST, while ensuring that the target can drive PORESET as well.

The COP interface has a standard header, shown in Figure 55, for connection to the target system, and is based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

The COP header adds many benefits such as breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features. An inexpensive option can be to leave the COP header unpopulated until needed.

There is no standardized way to number the COP header; so emulator vendors have issued many different pin numbering schemes. Some COP headers are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom. Still others number the pins counter-clockwise from pin 1 (as with an IC). Regardless of the numbering scheme, the signal placement recommended in Figure 55 is common to all known emulators.

3.6.1.1 Termination of unused signals

If the JTAG interface and COP header is not used, Freescale recommends the following connections:

- TRST should be tied to PORESET through a 0 kΩ isolation resistor so that it is asserted when the system reset signal (PORESET) is asserted, ensuring that the JTAG scan chain is initialized during the power-on reset flow. Freescale recommends that the COP header be designed into the system as shown in Figure 56. If this is not possible, the isolation resistor allows future access to TRST in case a JTAG interface may need to be wired onto the system in future debug situations.
- No pull-up/pull-down is required for TDI, TMS, or TDO.

3.6.2 Aurora configuration signals

Correct operation of the Aurora interface requires configuration of a group of system control pins as demonstrated in Figure 57 and Figure 58. Care must be taken to ensure that these pins are maintained at a valid negated state under normal operating conditions as most have asynchronous behavior and spurious assertion gives unpredictable results.

Freescale recommends that the Aurora 22 pin duplex connector be designed into the system as shown in Figure 59 or the 70 pin duplex connector be designed into the system as shown in Figure 60.

If the Aurora interface is not used, Freescale recommends the legacy COP header be designed into the system as described in Section 3.6.1.1, "Termination of unused signals."

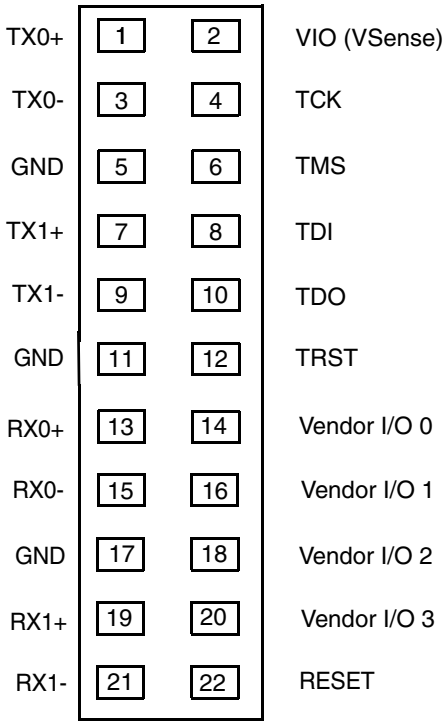

Figure 57. Aurora 22 pin connector duplex pinout

3.7 Recommended thermal model

Information about Flotherm models of the package or thermal data not available in this document can be obtained from your local Freescale sales office.

3.8 Thermal management information

This section provides thermal management information for the flip-chip, plastic-ball, grid array (FC-PBGA) package for air-cooled applications. Proper thermal control design is primarily dependent on the system-level design—the heat sink, airflow, and thermal interface material.

The recommended attachment method to the heat sink is illustrated in this figure. The heat sink should be attached to the printed-circuit board with the spring force centered over the die. This spring force should not exceed 10 pounds force (45 Newton).

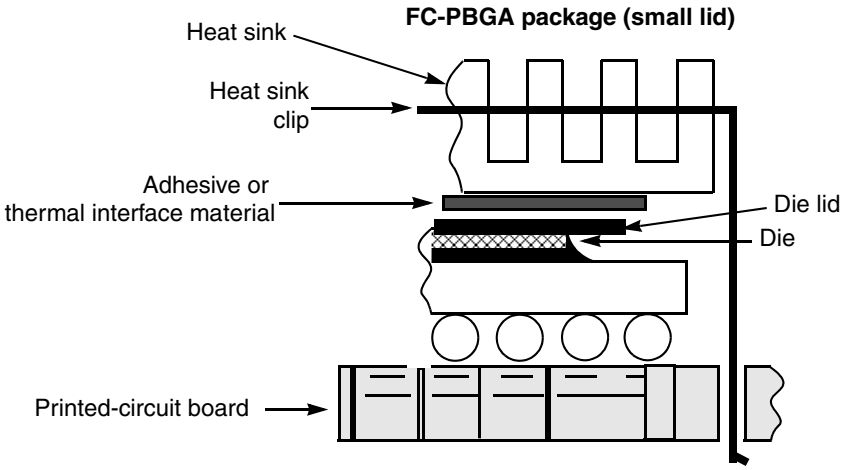

Figure 62. Exploded cross-sectional view—FC-PBGA (with lid) package

The system board designer can choose between several types of heat sinks to place on the device. There are several commercially-available thermal interfaces to choose from in the industry. Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost.

3.8.1 Internal package conduction resistance

For the package, the intrinsic internal conduction thermal resistance paths are as follows:

- The die junction-to-case thermal resistance
- The die junction-to-lid-top thermal resistance
- The die junction-to-board thermal resistance