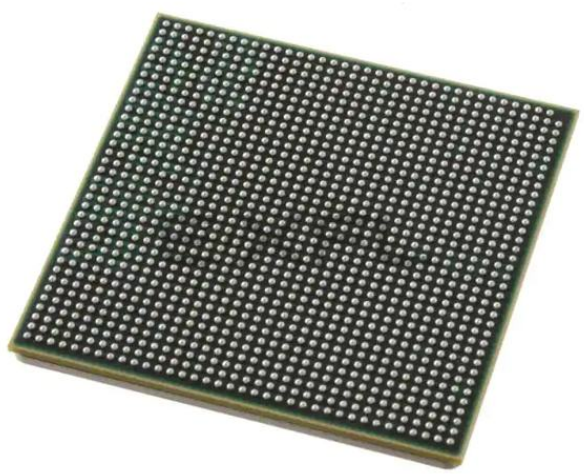

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e5500
Number of Cores/Bus Width	2 Core, 64-Bit
Speed	2.0GHz
Co-Processors/DSP	-
RAM Controllers	DDR3, DDR3L
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	1Gbps (10), 10Gbps (2)
SATA	SATA 3Gbps (2)
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.0V, 1.1V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Boot Security, Cryptography, Secure Fusebox, Secure Debug, Tamper Detection, Volatile key Storage
Package / Case	1295-BBGA, FCBGA
Supplier Device Package	1295-FCPBGA (37.5x37.5)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p5021nse7vnc

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
D2_MDQ55	Data	AT3	I/O	GV_{DD}	—
D2_MDQ56	Data	AP5	I/O	GV_{DD}	—
D2_MDQ57	Data	AT5	I/O	GV_{DD}	—
D2_MDQ58	Data	AP8	I/O	GV_{DD}	—
D2_MDQ59	Data	AT8	I/O	GV_{DD}	—
D2_MDQ60	Data	AR4	I/O	GV_{DD}	—
D2_MDQ61	Data	AT4	I/O	GV_{DD}	—
D2_MDQ62	Data	AR7	I/O	GV_{DD}	—
D2_MDQ63	Data	AT7	I/O	GV_{DD}	—
D2_MECC0	Error Correcting Code	J1	I/O	GV_{DD}	—
D2_MECC1	Error Correcting Code	K3	I/O	GV_{DD}	—
D2_MECC2	Error Correcting Code	M5	I/O	GV_{DD}	—
D2_MECC3	Error Correcting Code	N5	I/O	GV_{DD}	—
D2_MECC4	Error Correcting Code	J4	I/O	GV_{DD}	—
D2_MECC5	Error Correcting Code	J2	I/O	GV_{DD}	—
D2_MECC6	Error Correcting Code	L3	I/O	GV_{DD}	—
D2_MECC7	Error Correcting Code	L4	I/O	GV_{DD}	—
$\overline{\text{D2\_MAPAR\_ERR}}$	Address Parity Error	N2	I	GV_{DD}	—
D2_MAPAR_OUT	Address Parity Out	Y1	O	GV_{DD}	—
D2_MDM0	Data Mask	B12	O	GV_{DD}	—
D2_MDM1	Data Mask	B6	O	GV_{DD}	—
D2_MDM2	Data Mask	C4	O	GV_{DD}	—
D2_MDM3	Data Mask	G3	O	GV_{DD}	—
D2_MDM4	Data Mask	AG1	O	GV_{DD}	—
D2_MDM5	Data Mask	AL3	O	GV_{DD}	—
D2_MDM6	Data Mask	AP2	O	GV_{DD}	—
D2_MDM7	Data Mask	AP6	O	GV_{DD}	—
D2_MDM8	Data Mask	K2	O	GV_{DD}	—
D2_MDQS0	Data Strobe	A10	I/O	GV_{DD}	—
D2_MDQS1	Data Strobe	A5	I/O	GV_{DD}	—
D2_MDQS2	Data Strobe	C2	I/O	GV_{DD}	—
D2_MDQS3	Data Strobe	G6	I/O	GV_{DD}	—
D2_MDQS4	Data Strobe	AH2	I/O	GV_{DD}	—
D2_MDQS5	Data Strobe	AM4	I/O	GV_{DD}	—

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
D2_MDQS6	Data Strobe	AR1	I/O	GV_{DD}	—
D2_MDQS7	Data Strobe	AR6	I/O	GV_{DD}	—
D2_MDQS8	Data Strobe	L1	I/O	GV_{DD}	—
$\overline{\text{D2\_MDQS0}}$	Data Strobe	A11	I/O	GV_{DD}	—
$\overline{\text{D2\_MDQS1}}$	Data Strobe	A6	I/O	GV_{DD}	—
$\overline{\text{D2\_MDQS2}}$	Data Strobe	C1	I/O	GV_{DD}	—
$\overline{\text{D2\_MDQS3}}$	Data Strobe	G5	I/O	GV_{DD}	—
$\overline{\text{D2\_MDQS4}}$	Data Strobe	AH3	I/O	GV_{DD}	—
$\overline{\text{D2\_MDQS5}}$	Data Strobe	AM3	I/O	GV_{DD}	—
$\overline{\text{D2\_MDQS6}}$	Data Strobe	AP1	I/O	GV_{DD}	—
$\overline{\text{D2\_MDQS7}}$	Data Strobe	AT6	I/O	GV_{DD}	—
$\overline{\text{D2\_MDQS8}}$	Data Strobe	K1	I/O	GV_{DD}	—
D2_MBA0	Bank Select	AA3	O	GV_{DD}	—
D2_MBA1	Bank Select	AA1	O	GV_{DD}	—
D2_MBA2	Bank Select	M1	O	GV_{DD}	—
D2_MA00	Address	Y4	O	GV_{DD}	—
D2_MA01	Address	U1	O	GV_{DD}	—
D2_MA02	Address	U4	O	GV_{DD}	—
D2_MA03	Address	T1	O	GV_{DD}	—
D2_MA04	Address	T2	O	GV_{DD}	—
D2_MA05	Address	T3	O	GV_{DD}	—
D2_MA06	Address	R1	O	GV_{DD}	—
D2_MA07	Address	R4	O	GV_{DD}	—
D2_MA08	Address	R2	O	GV_{DD}	—
D2_MA09	Address	P1	O	GV_{DD}	—
D2_MA10	Address	AA2	O	GV_{DD}	—
D2_MA11	Address	P3	O	GV_{DD}	—
D2_MA12	Address	N1	O	GV_{DD}	—
D2_MA13	Address	AC4	O	GV_{DD}	—
D2_MA14	Address	N3	O	GV_{DD}	—
D2_MA15	Address	M2	O	GV_{DD}	—
$\overline{\text{D2\_MWE}}$	Write Enable	AB2	O	GV_{DD}	—
$\overline{\text{D2\_MRAS}}$	Row Address Strobe	AB1	O	GV_{DD}	—
$\overline{\text{D2\_MCAS}}$	Column Address Strobe	AC3	O	GV_{DD}	—

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
VDD_PL	Platform Supply	AF22	—	V_{DD_PL}	—
VDD_PL	Platform Supply	AF20	—	V_{DD_PL}	—
VDD_PL	Platform Supply	AF16	—	V_{DD_PL}	—
VDD_PL	Platform Supply	W13	—	V_{DD_PL}	—
VDD_PL	Platform Supply	AF18	—	V_{DD_PL}	—
VDD_PL	Platform Supply	V14	—	V_{DD_PL}	—
VDD_PL	Platform Supply	V18	—	V_{DD_PL}	—
VDD_PL	Platform Supply	L13	—	V_{DD_PL}	—
VDD_PL	Platform Supply	L15	—	V_{DD_PL}	—
VDD_PL	Platform Supply	L17	—	V_{DD_PL}	—
VDD_PL	Platform Supply	L19	—	V_{DD_PL}	—
VDD_PL	Platform Supply	L21	—	V_{DD_PL}	—
VDD_PL	Platform Supply	L23	—	V_{DD_PL}	—
VDD_PL	Platform Supply	L25	—	V_{DD_PL}	—
VDD_PL	Platform Supply	AF14	—	V_{DD_PL}	—
VDD_PL	Platform Supply	N23	—	V_{DD_PL}	—
VDD_PL	Platform Supply	R23	—	V_{DD_PL}	—
VDD_PL	Platform Supply	AA23	—	V_{DD_PL}	—
VDD_PL	Platform Supply	AC23	—	V_{DD_PL}	—
VDD_PL	Platform Supply	U21	—	V_{DD_PL}	—
VDD_PL	Platform Supply	W21	—	V_{DD_PL}	—
VDD_PL	Platform Supply	U15	—	V_{DD_PL}	—
VDD_PL	Platform Supply	AC21	—	V_{DD_PL}	—
VDD_PL	Platform Supply	AD22	—	V_{DD_PL}	—
VDD_PL	Platform Supply	M22	—	V_{DD_PL}	—
VDD_PL	Platform Supply	N13	—	V_{DD_PL}	—
VDD_PL	Platform Supply	AC13	—	V_{DD_PL}	—
VDD_PL	Platform Supply	P22	—	V_{DD_PL}	—
VDD_PL	Platform Supply	T22	—	V_{DD_PL}	—
VDD_PL	Platform Supply	Y22	—	V_{DD_PL}	—
VDD_PL	Platform Supply	AB22	—	V_{DD_PL}	—
VDD_PL	Platform Supply	AA13	—	V_{DD_PL}	—
VDD_PL	Platform Supply	R13	—	V_{DD_PL}	—
VDD_PL	Platform Supply	M14	—	V_{DD_PL}	—

This table shows the estimated power dissipation on the POV_{DD} supply for the chip, at allowable voltage levels.

Table 8. POV_{DD} power dissipation

Supply	Maximum	Unit	Notes
POV_{DD}	450	mW	1

Note:

1. To ensure device reliability, fuse programming must be performed within the recommended fuse programming temperature range per Table 3.

This table shows the estimated power dissipation on the V_{DD_LP} supply for the chip, at allowable voltage levels.

Table 9. V_{DD_LP} Power Dissipation

Supply	Maximum	Unit	Note
V_{DD_LP} (P5021 on, 105C)	1.5	mW	1
V_{DD_LP} (P5021 off, 70C)	195	uW	2
V_{DD_LP} (P5021 off, 40C)	132	uW	2

Note:

1. V_{DD_LP} = 1.0 V, T_J = 105°C.
2. When P5021 is off, V_{DD_LP} may be supplied by battery power to the Zeroizable Master Key and other Trust Architecture state. Board should implement a PMIC which switches V_{DD_LP} to battery when P5021 is powered down. See P5040 Reference Manual Trust Architecture chapter for more information.

2.5 Thermal

This table shows the thermal characteristics for the chip.

Table 10. Package thermal characteristics [6]

Rating	Board	Symbol	Value	Unit	Notes
Junction to ambient, natural convection	Single-layer board (1s)	$R_{\Theta JA}$	14	°C/W	1, 2
Junction to ambient, natural convection	Four-layer board (2s2p)	$R_{\Theta JA}$	10	°C/W	1, 2
Junction to ambient (at 200 ft./min.)	Single-layer board (1s)	$R_{\Theta JMA}$	9	°C/W	1, 2
Junction to ambient (at 200 ft./min.)	Four-layer board (2s2p)	$R_{\Theta JMA}$	7	°C/W	1, 2

This table provides the DC electrical characteristics for the eSPI interface operating at CV_{DD} = 1.8 V.

Table 28. eSPI DC electrical characteristics (CV_{DD} = 1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	1.25	—	V	1
Input low voltage	V_{IL}	—	0.6	V	1
Input current (V_{IN} = 0 V or V_{IN} = CV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (CV_{DD} = min, I_{OH} = –0.5 mA)	V_{OH}	1.35	—	V	—
Output low voltage (CV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	—	0.4	V	—

Notes:

1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max CV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the CV_{IN} symbol referenced in Section 2.1.2, “Recommended operating conditions.”

2.10.2 eSPI AC timing specifications

This table provides the eSPI input and output AC timing specifications.

Table 29. eSPI AC timing specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol[1]	Min	Max	Unit	Note
SPI_MOSI output—Master data (internal clock) hold time	t_{NIKHOX}	2.36 + ($t_{PLATFORM\_CLK}$ * SPMODE[HO_ADJ])	— —	ns	2, 3
SPI_MOSI output—Master data (internal clock) delay	t_{NIKHOV}	—	5.24 + ($t_{PLATFORM\_CLK}$ * SPMODE[HO_ADJ])	ns	2, 3
SPI_CS outputs—Master data (internal clock) hold time	$t_{NIKHOX2}$	0	—	ns	2
SPI_CS outputs—Master data (internal clock) delay	$t_{NIKHOV2}$	—	6.0	ns	2
eSPI inputs—Master data (internal clock) input setup time	t_{NIIVKH}	5	—	ns	—
eSPI inputs—Master data (internal clock) input hold time	t_{NIIXKH}	0	—	ns	—

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{NIKHOV} symbolizes the NMSI outputs internal timing (NI) for the time t_{SPI} memory clock reference (K) goes from the high state (H) until outputs (O) are valid (V).
2. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
3. See the applicable chip reference manual for details on the SPMODE register.

Table 39. Ethernet management interface 2 DC electrical characteristics (1.2 V) (continued)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Output low voltage (I_{OL} = 100 μA)	V_{OL}	—	0.2	V	—
Output low current (V_{OL} = 0.2 V)	I_{OL}	4	—	mA	—
Input capacitance	C_{IN}	—	10	pF	—

2.12.3.3 Ethernet management interface 1 AC timing specifications

This table provides the Ethernet management interface 1 AC timing specifications.

Table 40. Ethernet management interface 1 AC timing specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol[1]	Min	Typ	Max	Unit	Note
MDC frequency	f_{MDC}	—	—	2.5	MHz	2
MDC clock pulse width high	t_{MDCH}	160	—	—	ns	—
MDC to MDIO delay	t_{MDKHDX}	$(16 \times t_{plb\_clk}) - 6$	—	$(16 \times t_{plb\_clk}) + 6$	ns	3, 4
MDIO to MDC setup time	t_{MDDVKH}	8	—	—	ns	—
MDIO to MDC hold time	t_{MDDXKH}	0	—	—	ns	—

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. This parameter is dependent on the platform clock frequency (MIIMCFG [MgmtClk] field determines the clock frequency of the MgmtClk Clock EC_MDC).
3. This parameter is dependent on the frame manager clock frequency. The delay is equal to 16 frame manager clock periods ±6 ns. For example, with a frame manager clock of 333 MHz, the min/max delay is 48 ns ± 6 ns. Similarly, if the frame manager clock is 400 MHz, the min/max delay is 40 ns ± 6 ns.
4. t_{plb_clk} is the frame manager clock period.

2.12.3.4 Ethernet management interface 2 AC electrical characteristics

This table provides the Ethernet management interface 2 AC timing specifications.

Table 41. Ethernet management interface 2 AC timing specifications

For recommended operating conditions, see Table 3.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Note
MDC frequency	f_{MDC}	—	—	2.5	MHz	2
MDC clock pulse width high	t_{MDCH}	160	—	—	ns	—
MDC to MDIO delay	t_{MDKHDX}	$(0.5 \times (1/f_{MDC})) - 6$	—	$(0.5 \times (1/f_{MDC})) + 6$	ns	3
MDIO to MDC setup time	t_{MDDVKH}	8	—	—	ns	—

Table 42. eTSEC IEEE 1588 DC electrical characteristics (LV_{DD} = 3.3 V) (continued)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Notes
Input low current (LV_{DD} = Max, V_{IN} = 0.5 V)	I_{IL}	–600	—	μA	1
Output high voltage (LV_{DD} = Min, I_{OH} = –1.0 mA)	V_{OH}	2.4	—	V	—
Output low voltage (LV_{DD} = Min, I_{OL} = 1.0 mA)	V_{OL}	—	0.4	V	—

Note:

1. Note that the symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 2 and Table 3.
2. The min V_{IL} and max V_{IH} values are based on the respective LV_{IN} values found in Table 3.

2.12.4.2 eTSEC IEEE Std 1588 AC specifications

This table provides the IEEE 1588 AC timing specifications.

Table 43. eTSEC IEEE 1588 AC timing specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
TSEC_1588_CLK clock period	$t_{T1588CLK}$	3.3	—	$T_{RX\_CLK} \times 7$	ns	1, 2
TSEC_1588_CLK duty cycle	$t_{T1588CLKH}/t_{T1588CLK}$	40	50	60	%	3
TSEC_1588_CLK peak-to-peak jitter	$t_{T1588CLKINJ}$	—	—	250	ps	—
Rise time eTSEC_1588_CLK (20%–80%)	$t_{T1588CLKINR}$	1.0	—	2.0	ns	—
Fall time eTSEC_1588_CLK (80%–20%)	$t_{T1588CLKINF}$	1.0	—	2.0	ns	—
TSEC_1588_CLK_OUT clock period	$t_{T1588CLKOUT}$	$2 \times t_{T1588CLK}$	—	—	ns	—
TSEC_1588_CLK_OUT duty cycle	$t_{T1588CLKOTH}/t_{T1588CLKOUT}$	30	50	70	%	—
TSEC_1588_PULSE_OUT	$t_{T1588OV}$	0.5	—	3.0	ns	—
TSEC_1588_TRIG_IN pulse width	$t_{T1588TRIGH}$	$2 \times t_{T1588CLK\_MAX}$	—	—	ns	2

Notes:

1. T_{RX_CLK} is the maximum clock period of eTSEC receiving clock selected by TMR_CTRL[CKSEL]. See the *QorIQ Integrated Processor Reference Manual* for a description of TMR_CTRL registers.
2. The maximum value of $t_{T1588CLK}$ is not only defined by the value of T_{RX_CLK}, but also defined by the recovered clock. For example, for 10/100/1000 Mbps modes, the maximum value of $t_{T1588CLK}$ be 2800, 280, and 56 ns, respectively.
3. It needs to be at least two times the clock period of the clock selected by TMR_CTRL[CKSEL]. See the *QorIQ Integrated Processor Reference Manual* for a description of TMR_CTRL registers.

Table 49. Enhanced local bus timing specifications (continued)

For recommended operating conditions, see Table 3.

Parameter	Symbol[1]	Min	Max	Unit	Notes
Input setup (for LGTA/LUPWAIT/LFRB)	t_{LBIVKL}	6	—	ns	—
Input hold (for LGTA/LUPWAIT/LFRB)	t_{LBIXKL}	1	—	ns	—
Output delay (Except LALE)	t_{LBKLOV}	—	1.5	ns	—
Output hold (Except LALE)	t_{LBKLOX}	-3.5	—	ns	5
Local bus clock to output high impedance for LAD/LDP	t_{LBKLOZ}	—	2	ns	3
LALE output negation to LAD/LDP output transition (LATCH hold time)	t_{LBONOT}	2 platform clock cycles—1ns (LBCR[AHD]=1)	—	ns	4
		4 platform clock cycles—1ns (LBCR[AHD]=0)	—		

Notes:

1. All signals are measured from $BV_{DD}/2$ of rising/falling edge of LCLK to $BV_{DD}/2$ of the signal in question.
2. Skew measured between different LCLKs at $BV_{DD}/2$.
3. For purposes of active/float timing measurements, the high impedance or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
4. t_{LBONOT} is a measurement of the minimum time between the negation of LALE and any change in LAD. t_{LBONOT} is determined by LBCR[AHD]. The unit is the eLBC controller clock cycle, which is the internal clock that runs the local bus controller, not the external LCLK. LCLK cycle = eLBC controller clock cycle x LCRR[CLKDIV]. After power on reset, LBCR[AHD] defaults to 0 and eLBC runs at maximum hold time.
5. Output hold is negative. This means that output transition happens earlier than the falling edge of LCLK.

This figure provides the JTAG clock input timing diagram.

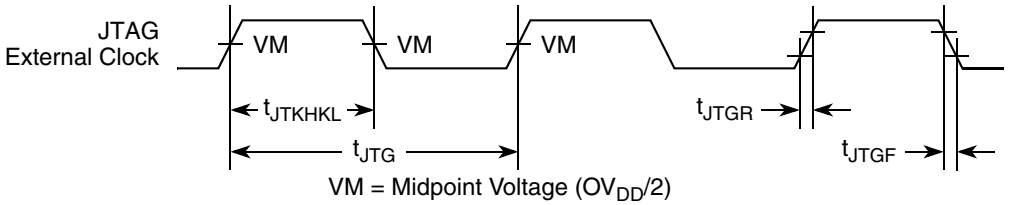


Figure 29. JTAG clock input timing diagram

This figure provides the $\overline{\text{TRST}}$ timing diagram.

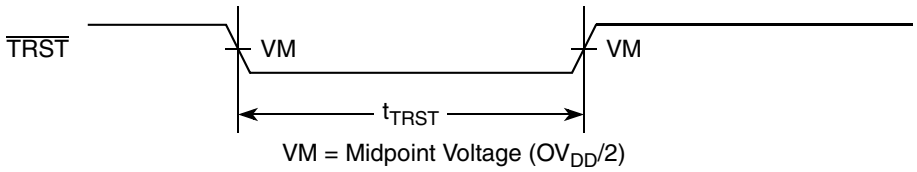


Figure 30. $\overline{\text{TRST}}$ timing diagram

This figure provides the boundary-scan timing diagram.

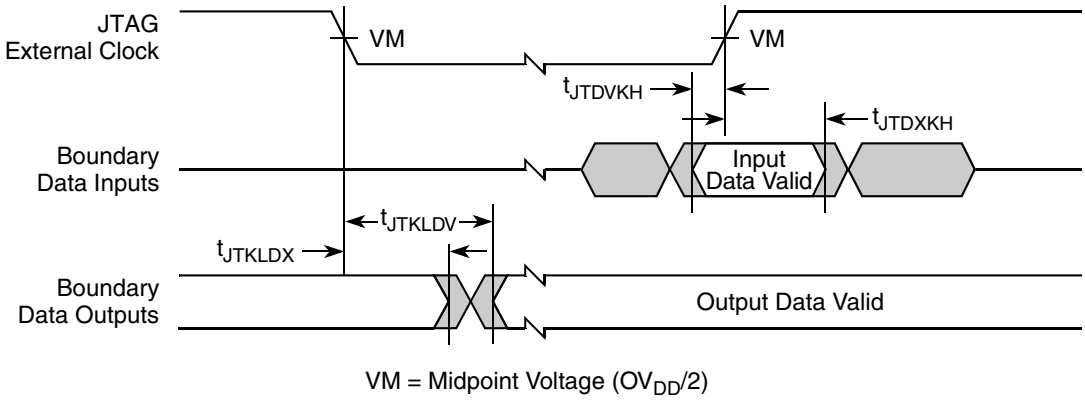


Figure 31. Boundary-scan timing diagram

2.18 I^2C

This section describes the DC and AC electrical characteristics for the I^2C interface.

2.18.1 I²C DC electrical characteristics

This table provides the DC electrical characteristics for the I²C interfaces.

Table 56. I²C DC electrical characteristics (OV_{DD} = 3.3 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2.0	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Output low voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	0	0.4	V	2
Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	3
Input current each I/O pin (input voltage is between 0.1 × OV_{DD} and 0.9 × OV_{DD}(max)	I_I	–40	40	μA	4
Capacitance for each I/O pin	C_I	0	10	pF	—

Notes:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. Output voltage (open drain or open collector) condition = 3 mA sink current.
3. See the applicable chip reference manual for information about the digital filter used.
4. I/O pins obstruct the SDA and SCL lines if OV_{DD} is switched off.

2.18.2 I²C AC electrical specifications

This table provides the AC timing parameters for the I²C interfaces.

Table 57. I²C AC timing specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol[1]	Min	Max	Unit	Notes
SCL clock frequency	f_{I2C}	0	400	kHz	2
Low period of the SCL clock	t_{I2CL}	1.3	—	μs	—
High period of the SCL clock	t_{I2CH}	0.6	—	μs	—
Setup time for a repeated START condition	t_{I2SVKH}	0.6	—	μs	—
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t_{I2SXKL}	0.6	—	μs	—
Data setup time	t_{I2DVKH}	100	—	ns	—
Data input hold time: CBUS compatible masters I²C bus devices	t_{I2DXKL}	 — 0	 — —	μs	3
Data output delay time	t_{I2OVKL}	—	0.9	μs	4
Setup time for STOP condition	t_{I2PVKH}	0.6	—	μs	—
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	—	μs	—

2.19.2 GPIO AC timing specifications

This table provides the GPIO input and output AC timing specifications.

Table 60. GPIO Input AC timing specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Unit	Notes
GPIO inputs—minimum pulse width	t_{PIWID}	20	ns	1
Trust inputs—minimum pulse width	t_{TIWID}	3	SYSCLK	2

Note:

1. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least t_{PIWID} to ensure proper operation.
2. Trust inputs are asynchronous to any visible clock. Trust inputs are required to be valid for at least t_{TIWID} to ensure proper operation. For low power trust input pin LP_TMP_DETECT, the voltage is VDD_LP and see Table 3.for the voltage requirement.

This figure provides the AC test load for the GPIO.

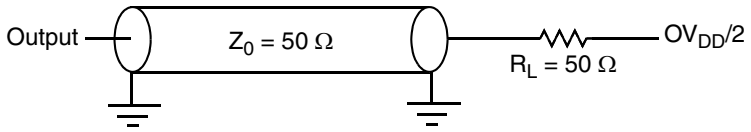


Figure 34. GPIO AC test load

2.20 High-speed serial interfaces (HSSI)

The chip features a serializer/deserializer (SerDes) interface to be used for high-speed serial interconnect applications. The SerDes interface can be used for PCI Express, XAUI, Aurora and SGMII data transfers.

This section describes the common portion of SerDes DC electrical specifications: the DC requirement for SerDes reference clocks. The SerDes data lane's transmitter and receiver reference circuits are also shown.

2.20.1 Signal terms definition

The SerDes utilizes differential signaling to transfer data across the serial link. This section defines terms used in the description and specification of differential signals.

waveform is not referenced to ground. See Figure 40, “Differential measurement points for rise and fall time,” as an example for differential waveform.

Common Mode Voltage, V_{cm}

The common mode voltage is equal to half of the sum of the voltages between each conductor of a balanced interchange circuit and ground. In this example, for SerDes output, $V_{cm\_out} = (V_{SD\_TXn} + V_{\overline{SD\_TXn}}) \div 2 = (A + B) \div 2$, which is the arithmetic mean of the two complementary output voltages within a differential pair. In a system, the common mode voltage may often differ from one component’s output to the other’s input. It may be different between the receiver input and driver output circuits within the same component. It is also referred to as the DC offset on some occasions.

To illustrate these definitions using real values, consider the example of a current mode logic (CML) transmitter that has a common mode voltage of 2.25 V and outputs, TD and $\overline{TD}$. If these outputs have a swing from 2.0 V to 2.5 V, the peak-to-peak voltage swing of each signal (TD or $\overline{TD}$) is 500 mV p-p, which is referred to as the single-ended swing for each signal. Because the differential signaling environment is fully symmetrical in this example, the transmitter output’s differential swing (V_{OD}) has the same amplitude as each signal’s single-ended swing. The differential output signal ranges between 500 mV and –500 mV. In other words, V_{OD} is 500 mV in one phase and –500 mV in the other phase. The peak differential voltage (V_{DIFFp}) is 500 mV. The peak-to-peak differential voltage ($V_{DIFFp-p}$) is 1000 mV p-p.

2.20.2 SerDes reference clocks

The SerDes reference clock inputs are applied to an internal PLL whose output creates the clock used by the corresponding SerDes lanes. The SerDes reference clocks inputs are SD_REF_CLK1 and $\overline{SD\_REF\_CLK1}$ for SerDes bank1, SD_REF_CLK2 and $\overline{SD\_REF\_CLK2}$ for SerDes bank2, SD_REF_CLK3 and $\overline{SD\_REF\_CLK3}$ for SerDes bank3, and SD_REF_CLK4 and $\overline{SD\_REF\_CLK4}$ for SerDes bank4.

SerDes banks 1–4 may be used for various combinations of the following IP blocks based on the RCW Configuration field SRDS_PRTCL:

- SerDes bank 1: PEX1/2/3, SGMII (1.25 Gbps only) or Aurora.
- SerDes bank 2: SGMII (1.25 or 3.125 GBaud) or XAUI.
- SerDes bank 3: SATA, or XAUI.
- SerDes bank 4: SATA

The following sections describe the SerDes reference clock requirements and provide application information.

2.20.2.1 SerDes reference clock receiver characteristics

This figure shows a receiver reference diagram of the SerDes reference clocks.

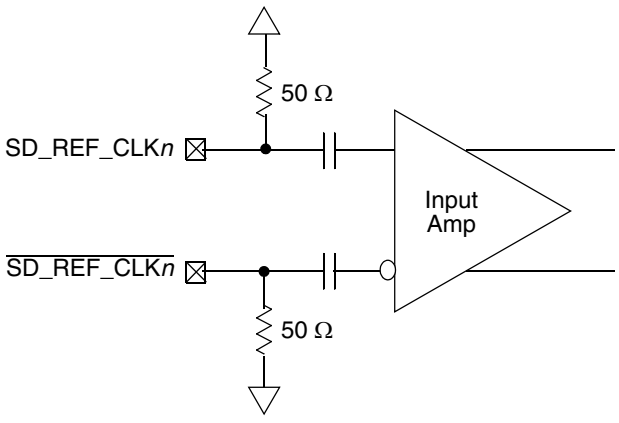


Figure 36. Receiver of SerDes reference clocks

This table defines the PCI Express 2.0 (5 GT/s) AC specifications for the differential output at all transmitters. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 67. PCI Express 2.0 (5 GT/s) differential transmitter Output AC specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typ	Max	Units	Notes
Unit Interval	UI	199.94	200.00	200.06	ps	Each UI is 400 ps ± 300 ppm. UI does not account for spread spectrum clock dictated variations. See Note 1.
Minimum transmitter eye width	T_{TX-EYE}	0.75	—	—	UI	The maximum transmitter jitter can be derived as: $T_{TX-MAX-JITTER} = 1 - T_{TX-EYE} = 0.25$ UI. See Notes 2 and 3.
Transmitter RMS deterministic jitter > 1.5 MHz	$T_{TX-HF-DJ-DD}$	—	—	0.15	ps	—
Transmitter RMS deterministic jitter < 1.5 MHz	$T_{TX-LF-RMS}$	—	3.0	—	ps	Reference input clock RMS jitter (< 1.5 MHz) at pin < 1 ps
AC coupling capacitor	C_{TX}	75	—	200	nF	All transmitters must be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See Note 4.

Notes:
1. No test load is necessarily associated with this value.
2. Specified at the measurement point into a timing and voltage test load as shown in Figure 43 and measured over any 250 consecutive transmitter UIs.
3. A $T_{TX-EYE} = 0.75$ UI provides for a total sum of deterministic and random jitter budget of $T_{TX-JITTER-MAX} = 0.25$ UI for the transmitter collected over any 250 consecutive transmitter UIs. The $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ median is less than half of the total transmitter jitter budget collected over any 250 consecutive transmitter UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.
4. The chip's SerDes transmitter does not have C_{TX} built-in. An external AC coupling capacitor is required.

2.20.4.5.2 PCI Express AC physical layer receiver specifications

This section discusses the PCI Express AC physical layer receiver specifications 2.5 GT/s, and 5 GT/s.

2.20.5.2.1 AC requirements for XAUI SD_REF_CLK*n* and $\overline{\text{SD\_REF\_CLK}n}$

This table specifies AC requirements for SD_REF_CLK*n* and $\overline{\text{SD\_REF\_CLK}n}$, where n = [2:3]. Only SerDes banks 2–3 may be used for various SerDes XAUI configurations based on the RCW Configuration field SRDS_PRTCL. XAUI is not supported on SerDes bank 1.

Table 72. XAUI AC SD_REF_CLK*n* and $\overline{\text{SD\_REF\_CLK}n}$ input clock requirements (SV_{DD} = 1.0 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ frequency range	t_{CLK_REF}	—	125/ 156.25	—	MHz	—
SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ clock frequency tolerance	t_{CLK_TOL}	–100	—	100	ppm	—
SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ reference clock duty cycle	t_{CLK_DUTY}	40	50	60	%	2
SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ cycle to cycle jitter (period jitter at refClk input)	t_{CLK_CJ}	—	—	100	ps	—
SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ total reference clock jitter (peak-to-peak phase jitter at refClk input)	t_{CLK_PJ}	-50	—	50	ps	—
SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ rising/falling edge rate	t_{CLKRR}/t_{CLKFR}	1	—	4	V/ns	1
Differential input high voltage	V_{IH}	200	—	—	mV	2
Differential input low voltage	V_{IL}	—	—	–200	mV	2
Rising edge rate (SD_REF_CLK*n*) to falling edge rate (SD_REF_CLK*n*) matching	Rise-Fall Matching	—	—	20	%	3, 4

Notes:
1. Measured from –200 mV to +200 mV on the differential waveform (derived from SD_REF_CLK*n* – $\overline{\text{SD\_REF\_CLK}n}$). The signal must be monotonic through the measurement region for rise and fall time. The 400 mV measurement window is centered on the differential zero crossing. See Figure 40.
2. Measurement taken from differential waveform
3. Measurement taken from single-ended waveform
4. Matching applies to rising edge for SD_REF_CLK*n* and falling edge rate for $\overline{\text{SD\_REF\_CLK}n}$. It is measured using a 200 mV window centered on the median cross point where SD_REF_CLK*n* rising meets $\overline{\text{SD\_REF\_CLK}n}$ falling. The median cross point is used to calculate the voltage thresholds that the oscilloscope uses for the edge rate calculations. The rise edge rate of SD_REF_CLK*n* should be compared to the fall edge rate of $\overline{\text{SD\_REF\_CLK}n}$, the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 41.

2.20.5.2.2 XAUI transmitter AC timing specifications

This table defines the XAUI transmitter AC timing specifications. RefClk jitter is not included.

Table 73. XAUI transmitter AC timing specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Deterministic jitter	J_D	—	—	0.17	UI p-p	—
Total jitter	J_T	—	—	0.35	UI p-p	—
Unit Interval: 3.125 GBaud	UI	320 – 100 ppm	320	320 + 100 ppm	ps	—

Table 93. SGMII receive AC timing specifications (continued)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Bit error ratio	BER	—	—	10^{-12}	—	—
Unit Interval: 1.25 GBaud	UI	800 – 100 ppm	800	800 + 100 ppm	ps	1
Unit Interval: 3.125 GBaud	UI	320 – 100 ppm	320	320 + 100 ppm	ps	1

Notes:

1. Measured at receiver
2. See the RapidIO™ 1×/4× LP Serial Physical Layer Specification for interpretation of jitter specifications.
3. Total jitter is composed of three components: deterministic jitter, random jitter, and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 44. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk and other variable system effects.

The sinusoidal jitter in the total jitter tolerance may have any amplitude and frequency in the unshaded region of Figure 44.

3 Hardware design considerations

3.1 System clocking

This section describes the PLL configuration of the chip.

This device includes nine PLLs, as follows:

- There are two selectable core cluster PLLs which generate a core clock from the externally supplied SYSCLK input. Core complex 0–1 can select from either CC1 PLL or CC2 PLL. The frequency ratio between the core cluster PLLs and SYSCLK is selected using the configuration bits as described in Section 3.1.3, "e5500-64 core complex/ FMan to SYSCLK PLL ratio." The frequency for each core complex 0–1 is selected using the configuration bits as described in Table 97.
- The platform PLL generates the platform clock from the externally supplied SYSCLK input. The frequency ratio between the platform and SYSCLK is selected using the platform PLL ratio configuration bits as described in Section 3.1.2, "Platform to SYSCLK PLL ratio."
- The DDR block PLL generates the DDR clock from the externally supplied SYSCLK input (asynchronous mode) or from the platform clock (synchronous mode). The frequency ratio is selected using the Memory Controller Complex PLL multiplier/ratio configuration bits as described in Section 3.1.5, "DDR controller PLL ratios."
- The FMan PLL generates the FMan clock from the platform PLL when operating synchronously, or from CC3 PLL when operating asynchronously. Described in Section 3.1.8, "Frame Manager (FMan) clock select."
- Each of the four SerDes blocks has a PLL which generate a core clock from their respective externally supplied SD_REF_CLK*n*/$\overline{\text{SD\_REF\_CLK}n}$ inputs. The frequency ratio is selected using the SerDes PLL ratio configuration bits as described in Section 3.1.6, "Frequency options."

Note that “PCI Express link width” in the above equation refers to the negotiated link width as the result of PCI Express link training, which may or may not be the same as the link width POR selection.

3.1.7 SerDes PLL ratio

The clock ratio between each of the four SerDes PLLs and their respective externally supplied SD_REF_CLK*n*/$\overline{\text{SD\_REF\_CLK}n}$ inputs is determined by the binary value of the RCW Configuration field SRDS_RATIO_B*n* as shown in this table. Furthermore, each SerDes lane grouping can be run at a SerDes PLL frequency divider determined by the binary value of the RCW field SRDS_DIV_B*n* as shown in Table 103 and Table 104.

This table lists the supported SerDes PLL Bank *n* to SD_REF_CLK*n* ratios.

Table 102. SerDes PLL bank *n* to SD_REF_CLK*n* ratios

Binary value of SRDS_RATIO_B*n*	SRDS_PLL_*n*:SD_REF_CLK*n* ratio			
	***n* = 1 (bank 1)**	***n* = 2 (bank 2)**	***n* = 3 (bank 3)**	***n* = 4(bank 4)**
001	Reserved	20:1	20:1	Reserved
010	25:1	25:1	25:1	Reserved
011	40:1	40:1	40:1	Reserved
100	50:1	50:1	50:1	Reserved
101	Reserved	Reserved	24:1	24:1
110	Reserved	Reserved	30:1	30:1
All Others	Reserved	Reserved	Reserved	Reserved

This table shows the PLL divider support for each pair of lanes on SerDes Bank 1.

Table 103. SerDes bank 1 PLL dividers

Binary value of SRDS_DIV_B1[0:4]	SerDes bank 1 PLL divider
0b0	Divide by 1 off Bank 1 PLL
0b1	Divide by 2 off Bank 1 PLL

Note:

1. 1 bit (of 5 total SRDS_DIV_B1 bits) controls each pair of lanes, where the first bit controls configuration of lanes A/B (or 0/1) and the last bit controls configuration of lanes I/J (or 8/9).

This table shows the PLL dividers supported for each 4 lane group for SerDes Banks 2, 3, and 4.

Table 104. SerDes banks 2, 3, and 4 PLL dividers

Binary value of SRDS_DIV_B*n*	SerDes Bank *n* PLL divider
0b0	Divide by 1 off Bank *n* PLL
0b1	Divide by 2 off Bank *n* PLL

Notes:

1. One bit controls all 4 lanes of each bank.
2. n = 2 or 3 (SerDes bank 2 or bank 3)

Table 106. I/O voltage selection

Signals	Value (binary)	VDD voltage selection		
		BVDD	CVDD	LVDD
IO_VSEL[0:4] Default (0_0000)	0_0000	3.3 V	3.3 V	3.3 V
	0_0001	3.3 V	3.3 V	2.5 V
	0_0011	3.3 V	2.5 V	3.3 V
	0_0100	3.3 V	2.5 V	2.5 V
	0_0110	3.3 V	1.8 V	3.3 V
	0_0111	3.3 V	1.8 V	2.5 V
	0_1001	2.5 V	3.3 V	3.3 V
	0_1010	2.5 V	3.3 V	2.5 V
	0_1100	2.5 V	2.5 V	3.3 V
	0_1101	2.5 V	2.5 V	2.5 V
	0_1111	2.5 V	1.8 V	3.3 V
	1_0000	2.5 V	1.8 V	2.5 V
	1_0010	1.8 V	3.3 V	3.3 V
	1_0011	1.8 V	3.3 V	2.5 V
	1_0101	1.8 V	2.5 V	3.3 V
	1_0110	1.8 V	2.5 V	2.5 V
	1_1000	1.8 V	1.8 V	3.3 V
	1_1001	1.8 V	1.8 V	2.5 V
	1_1011	3.3 V	3.3 V	3.3 V
	1_1100	3.3 V	3.3 V	3.3 V
	1_1101	3.3 V	3.3 V	3.3 V
	1_1110	3.3 V	3.3 V	3.3 V
	1_1111	3.3 V	3.3 V	3.3 V
	All Others	Reserved		

3.3 Power supply design

3.3.1 PLL power supply filtering

Each of the PLLs described in Section 3.1, "System clocking," is provided with power through independent power supply pins (AV_{DD_PLAT}, AV_{DD_CCn}, AV_{DD_DDR}, AV_{DD_FM}, and AV_{DD_SRDSn}). AV_{DD_PLAT}, AV_{DD_CCn}, AV_{DD_FM}, and AV_{DD_DDR} voltages must be derived directly from the V_{DD_PL} source through a low frequency filter scheme. AV_{DD_SRDSn} voltages must be derived directly from the SV_{DD} source through a low frequency filter scheme.

The recommended solution for PLL filtering is to provide independent filter circuits per PLL power supply, as illustrated in Figure 51, one for each of the AV_{DD} pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLL's resonant frequency range from a 500-kHz to 10-MHz range.

Each circuit should be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of the footprint, without the inductance of vias.

Figure 51 shows the PLL power supply filter circuit.

Where:

R = 5 Ω ± 5%
C1 = 10µF ± 10%, 0603, X5R, with ESL ≤ 0.5 nH
C2 = 1.0 µF ± 10%, 0402, X5R, with ESL ≤ 0.5 nH

NOTE

A higher capacitance value for C2 may be used to improve the filter as long as the other C2 parameters do not change (0402 body, X5R, ESL ≤ 0.5 nH).

Voltage for AV_{DD} is defined at the PLL supply filter and not the pin of AV_{DD}.

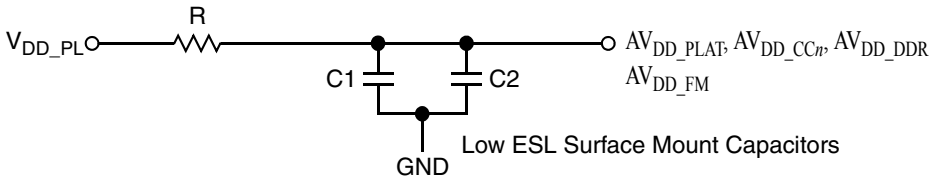


Figure 51. PLL power supply filter circuit

The AV_{DD_SRDSn} signals provides power for the analog portions of the SerDes PLL. To ensure stability of the internal clock, the power supplied to the PLL is filtered using a circuit similar to the one shown in following Figure 52. For maximum effectiveness, the filter circuit is placed as closely as possible to the AV_{DD_SRDSn} balls to ensure it filters out as much noise as possible. The ground connection should be near the AV_{DD_SRDSn} balls. The 0.003-µF capacitor is closest to the balls, followed by two 2.2-µF capacitors, and finally the 1-Ω resistor to the board supply plane. The capacitors are connected from AV_{DD_SRDSn} to the ground plane. Use ceramic chip capacitors with the highest possible self-resonant frequency. All traces should be kept short, wide, and direct.

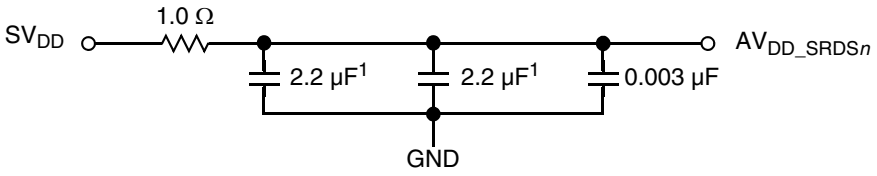


Figure 52. SerDes PLL power supply filter circuit

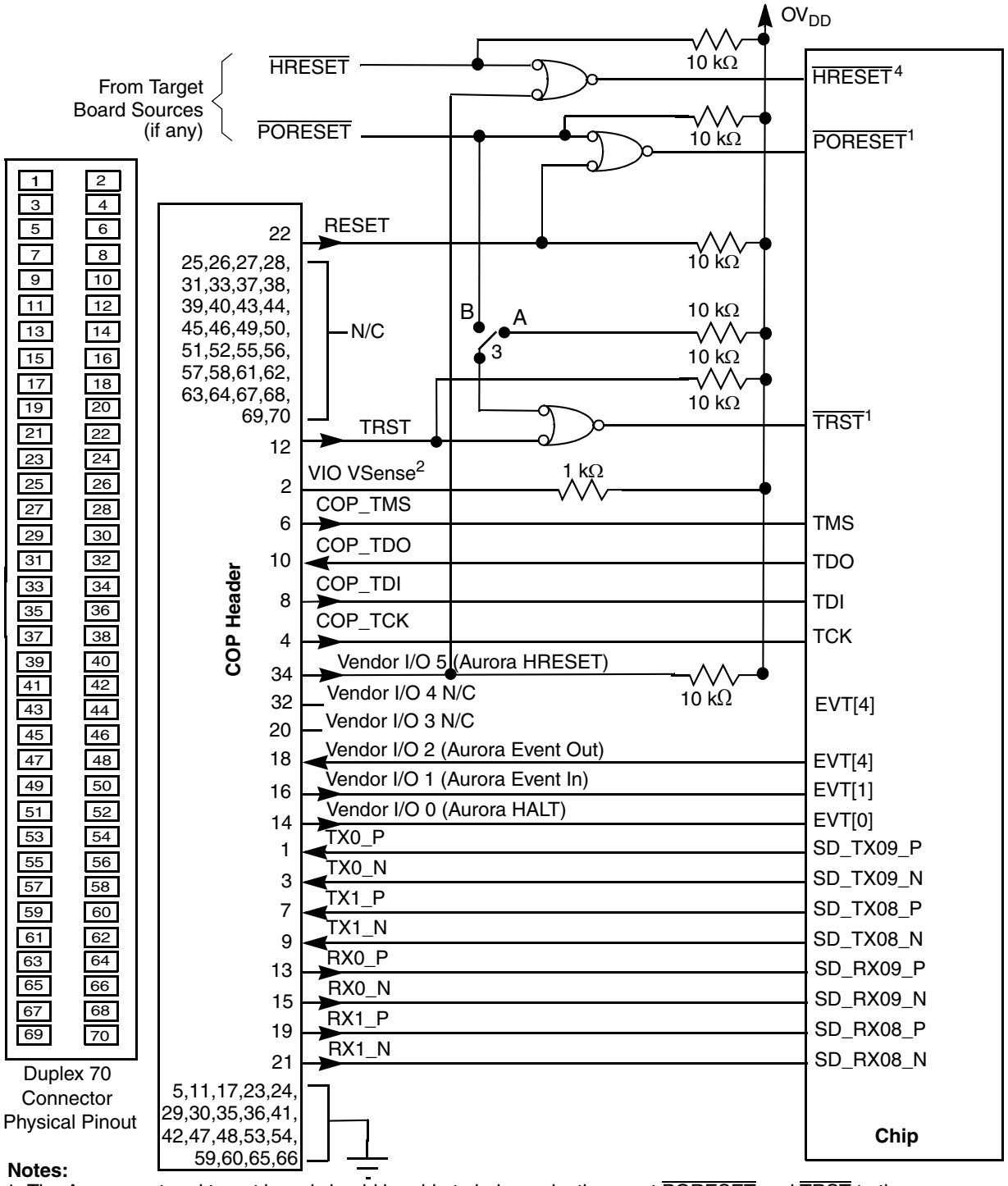
Note the following:

- AV_{DD_SRDSn} should be a filtered version of SV_{DD}.
- Signals on the SerDes interface are fed from the XV_{DD} power plane.
- Voltage for AV_{DD_SRDSn} is defined at the PLL supply filter and not the pin of AV_{DD_SRDSn}.
- An 0805 sized capacitor is recommended for system initial bring-up.

3.3.2 XV_{DD} power supply filtering

XV_{DD} may be supplied by a linear regulator or sourced by a filtered 1.5 V or 1.8 V voltage source. Systems may design in both options to allow flexibility to address system noise dependencies.

An example solution for XV_{DD} filtering, where 1.5 V or 1.8 V is sourced from voltage source (for example, GV_{DD} at 1.5 V when using DDR3, or CV_{DD} at 1.8 V), is illustrated in Figure 53. The component values in this example filter is system



Notes:

1. The Aurora port and target board should be able to independently assert $\overline{\text{PORESET}}$ and $\overline{\text{TRST}}$ to the processor in order to fully control the processor as shown here.
2. Populate this with a 1 kΩ resistor for short-circuit/current-limiting protection.
3. This switch is included as a precaution for BSDL testing. The switch should be closed to position A during BSDL testing to avoid accidentally asserting the $\overline{\text{TRST}}$ line. If BSDL testing is not being performed, this switch should be closed to position B.
4. Asserting $\overline{\text{HRESET}}$ causes a hard reset on the device.

Figure 60. Aurora 70 pin connector duplex interface connection

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