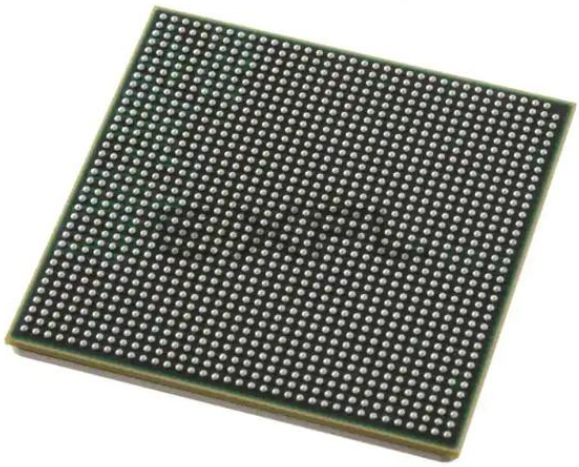

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e5500
Number of Cores/Bus Width	2 Core, 64-Bit
Speed	1.8GHz
Co-Processors/DSP	-
RAM Controllers	DDR3, DDR3L
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	1Gbps (10), 10Gbps (2)
SATA	SATA 3Gbps (2)
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.0V, 1.1V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	1295-BBGA, FCBGA
Supplier Device Package	1295-FCPBGA (37.5x37.5)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p5021nsn7tmc

Table 2. Absolute maximum operating conditions [1] (continued)

Parameter		Symbol	Maximum value	Unit	Notes
Input voltage[7]	DDR3 and DDR3L DRAM signals	MV_{IN}	–0.3 to (GV_{DD} + 0.3)	V	2, 7
	DDR3 and DDR3L DRAM reference	MV_{REF}	–0.3 to (GV_{DD}/2+ 0.3)	V	2, 7
	Ethernet signals (except EMI2)	LV_{IN}	–0.3 to (LV_{DD} + 0.3)	V	3, 7
	eSPI, eSHDC	CV_{IN}	–0.3 to (CV_{DD} + 0.3)	V	4, 7
	Enhanced local bus signals	BV_{IN}	–0.3 to (BV_{DD} + 0.3)	V	5, 7
	DUART, I^2C, DMA, MPIC, GPIO, system control and power management, clocking, debug, I/O voltage select, and JTAG I/O voltage	OV_{IN}	–0.3 to (OV_{DD} + 0.3)	V	6, 7
	SerDes signals	XV_{IN}	–0.4 to (XV_{DD} + 0.3)	V	7
	USB PHY transceiver signals	$USB_V_{IN}_3P3$	–0.3 to ($USB_V_{DD}_3P3$ + 0.3)	V	7
	Ethernet management interface 2 (EMI2) signals	—	–0.3 to (1.2 + 0.3)	V	7
Storage junction temperature range		T_{stg}	–55 to 150	°C	—

Notes:

1. Functional operating conditions are given in Table 3. Absolute maximum ratings are stress ratings only; functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. Caution: MV_{IN} must not exceed GV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
3. Caution: LV_{IN} must not exceed LV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. Caution: CV_{IN} must not exceed CV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
5. Caution: BV_{IN} must not exceed BV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
6. Caution: OV_{IN} must not exceed OV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
7. (C,X,B,G,L,O)V_{IN} may overshoot (for V_{IH}) or undershoot (for V_{IL}) to the voltages and maximum duration shown in Figure 7.
8. Ethernet Management interface 2 pins function as open drain I/Os. The interface shall conform to 1.2 V nominal voltage levels. LV_{DD} must be powered to use this interface.
9. Supply voltage specified at the voltage sense pin. Voltage input pins should be regulated to provide specified voltage at the sense pin.
10. Implementation may choose either V_{DD_PL} pin for feedback loop. If the platform and core groups are supplied by a single regulator, it is recommended that V_{DD_CA} be used.
11. V_{DD_PL} voltage must not exceed V_{DD_CA}.

2.1.2 Recommended operating conditions

This table provides the recommended operating conditions for the device. Note that proper device operation outside these conditions is not guaranteed.

Table 3. Recommended operating conditions

Parameter		Symbol	Recommended value	Unit	Notes
Core group A (core 0,1) supply voltage		V_{DD_CA}	1.1 ± 50mV (core frequency ≤ 2000 MHz) 1.2V ± 30mV (core frequency > 2000 MHz)	V	1,6
Platform supply voltage		V_{DD_PL}	1.0 ± 50mV	V	1,6
PLL supply voltage (core, platform, DDR, FMan)		AV_{DD}	1.0 ± 50mV	V	—
PLL supply voltage (SerDes)		AV_{DD_SRDS}	1.0 ± 50mV	V	—
Fuse programming override supply		POV_{DD}	1.5 ± 75mV	V	2
DUART, I^2C, DMA, MPIC, GPIO, system control and power management, clocking, debug, I/O voltage select, and JTAG I/O voltage		OV_{DD}	3.3 ± 165mV	V	—
eSPI, eSDHC		CV_{DD}	3.3 ± 165mV 2.5 ± 125mV 1.8 ± 90mV	V	—
DDR DRAM I/O voltage	DDR3	GV_{DD}	1.5 ± 75mV	V	—
	DDR3L		1.35 ± 67mV		
Enhanced local bus I/O voltage		BV_{DD}	3.3 ± 165mV 2.5 ± 125mV 1.8 ± 90mV	V	—
Main power supply for internal circuitry of SerDes and pad power supply for SerDes receiver		SV_{DD}	1.0 + 50mV 1.0 – 30mV	V	—
Pad power supply for SerDes transmitter		XV_{DD}	1.8 ± 90mV 1.5 ± 75mV	V	—
Ethernet I/O, Ethernet Management interface 1 (EMI1), 1588, GPIO		LV_{DD}	3.3 ± 165mV 2.5 ± 125mV	V	3
USB PHY transceiver supply voltage		$USB_V_{DD}_3P3$	3.3 ± 165mV	V	—
USB PHY PLL supply voltage		$USB_V_{DD}_1P0$	1.0 ± 50mV	V	—
Low-power security monitor supply		V_{DD_LP}	1.0 ± 50mV	V	—

Table 3. Recommended operating conditions (continued)

Parameter		Symbol	Recommended value	Unit	Notes
Input voltage	DDR3 and DDR3L DRAM signals	MV_{IN}	GND to GV_{DD}	V	7
	DDR3 and DDR3L DRAM reference	MV_{REF}	$GV_{DD}/2 \pm 1\%$	V	7
	Ethernet signals (except EMI2)	LV_{IN}	GND to LV_{DD}	V	7
	eSPI, eSHDC	CV_{IN}	GND to CV_{DD}	V	7
	Enhanced local bus signals	BV_{IN}	GND to BV_{DD}	V	7
	DUART, I^2C, DMA, MPIC, GPIO, system control and power management, clocking, debug, I/O voltage select, and JTAG I/O voltage	OV_{IN}	GND to OV_{DD}	V	7
	SerDes signals	SV_{IN}	GND to SV_{DD}	V	7
	USB PHY Transceiver signals	$USB_V_{IN}_3P3$	GND to $USB_V_{DD}_3P3$	V	7
	Ethernet Management interface 2 (EMI2) signals	—	GND to 1.2V	V	4, 7
Operating Temperature range	Normal Operation	T_A, T_J	T_A = 0 (min) to T_J = 105 (max) (90 (max) core frequency > 2000 MHz)	°C	—
	Extended Temperature	T_A, T_J	T_A = -40 (min) to T_J = 105 (max)	°C	—
	Secure Boot Fuse Programming	T_A, T_J	T_A = 0 (min) to T_J = 70 (max)	°C	2

Notes:

1. V_{DD_PL} voltage must not exceed V_{DD_CA}.
2. POV_{DD} must be supplied 1.5 V and the chip must operate in the specified fuse programming temperature range only during secure boot fuse programming. For all other operating conditions, POV_{DD} must be tied to GND, subject to the power sequencing constraints shown in Section 2.2, “Power-up sequencing.”
3. Selecting RGMII limits LV_{DD} to 2.5V.
4. Ethernet Management interface 2 pins function as open drain I/Os. The interface shall conform to 1.2 V nominal voltage levels. LV_{DD} must be powered to use this interface.6. Supply voltage specified at the voltage sense pin. Voltage input pins must be regulated to provide specified voltage at the sense pin.
7. All input signals must increase/decrease monotonically throughout the entire rise/fall duration.

Table 15. RESET initialization timing specifications (continued)

Parameter	Min	Max	Unit [1]	Notes
Input hold time for all POR configurations with respect to negation of $\overline{\text{PORESET}}$	2	—	SYSCLKs	1
Maximum valid-to-high impedance time for actively driven POR configurations with respect to negation of $\overline{\text{PORESET}}$	—	5	SYSCLKs	1

Notes:
1. SYSCLK is the primary clock input for the chip.
2. The device asserts $\overline{\text{HRESET}}$ as an output when $\overline{\text{PORESET}}$ is asserted to initiate the power-on reset process. The device releases $\overline{\text{HRESET}}$ sometime after $\overline{\text{PORESET}}$ is negated. The exact sequencing of HRESET negation is documented in Section 4.4.1 “Power-On Reset Sequence,” of the applicable chip reference manual.
3. $\overline{\text{PORESET}}$ must be driven asserted before the core and platform power supplies are powered up , see Section 2.2, “Power-up sequencing.”

This table provides the PLL lock times.

Table 16. PLL lock times

Parameter	Min	Max	Unit	Notes
PLL lock times	—	100	µs	—

2.8 Power-on ramp rate

This section describes the AC electrical specifications for the power-on ramp rate requirements. Controlling the maximum Power-On Ramp Rate is required to avoid falsely triggering ESD circuitry. This table provides the power supply ramp rate specifications.

Table 17. Power supply ramp rate

Parameter	Min	Max	Unit	Notes
Required ramp rate for all voltage supplies (including OV_{DD}/CV_{DD}/ GV_{DD}/BV_{DD}/SV_{DD}/XV_{DD}/LV_{DD} all V_{DD} supplies, MVREF and all AV_{DD} supplies.)	—	36000	V/s	1, 2

Notes:
1. Ramp rate is specified as a linear ramp from 10 to 90%. If non-linear (for example, exponential), the maximum rate of change from 200 to 500 mV is the most critical as this range might falsely trigger the ESD circuitry.
2. Over full recommended operating temperature range (see Table 3).

2.9 DDR3 and DDR3L SDRAM controller

This section describes the DC and AC electrical specifications for the DDR3 and DDR3L SDRAM controller interface. Note that the required GV_{DD}(typ) voltage is 1.5 V when interfacing to DDR3 SDRAM and GV_{DD}(typ) voltage is 1.35 V when interfacing to DDR3L SDRAM.

NOTE

When operating at DDR data rates of 1600 MT/s only one dual-ranked module per memory controller is supported.

This table provides the DC electrical characteristics for the eSPI interface operating at CV_{DD} = 1.8 V.

Table 28. eSPI DC electrical characteristics (CV_{DD} = 1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	1.25	—	V	1
Input low voltage	V_{IL}	—	0.6	V	1
Input current (V_{IN} = 0 V or V_{IN} = CV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (CV_{DD} = min, I_{OH} = –0.5 mA)	V_{OH}	1.35	—	V	—
Output low voltage (CV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	—	0.4	V	—

Notes:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max CV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the CV_{IN} symbol referenced in Section 2.1.2, “Recommended operating conditions.”

2.10.2 eSPI AC timing specifications

This table provides the eSPI input and output AC timing specifications.

Table 29. eSPI AC timing specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol [1]	Min	Max	Unit	Note
SPI_MOSI output—Master data (internal clock) hold time	t_{NIKHOX}	2.36 + ($t_{PLATFORM_CLK}$ * SP MODE[HO_ADJ])	— —	ns	2, 3
SPI_MOSI output—Master data (internal clock) delay	t_{NIKHOV}	—	5.24 + ($t_{PLATFORM_CLK}$ * SPMODE[HO_ADJ])	ns	2, 3
SPI_CS outputs—Master data (internal clock) hold time	$t_{NIKHOX2}$	0	—	ns	2
SPI_CS outputs—Master data (internal clock) delay	$t_{NIKHOV2}$	—	6.0	ns	2
eSPI inputs—Master data (internal clock) input setup time	t_{NIIVKH}	5	—	ns	—
eSPI inputs—Master data (internal clock) input hold time	t_{NIIXKH}	0	—	ns	—

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{NIKHOV} symbolizes the NMSI outputs internal timing (NI) for the time t_{SPI} memory clock reference (K) goes from the high state (H) until outputs (O) are valid (V).
2. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
3. See the applicable chip reference manual for details on the SPMODE register.

Table 30. DUART DC electrical characteristics (OV_{DD} = 3.3 V) (continued)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Notes
Input current (OV_{IN} = 0 V or OV_{IN} = OV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (OV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Notes:
1. The symbol OV_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 3.
2. The symbol OV_{IN}, in this case, represents the OV_{IN} symbol referenced in Section 2.1.2, "Recommended operating conditions."

2.11.2 DUART AC electrical specifications

This table provides the AC timing parameters for the DUART interface.

Table 31. DUART AC timing specifications

For recommended operating conditions, see Table 3.

Parameter	Value	Unit	Notes
Minimum baud rate	f_{PLAT}/(2*1,048,576)	baud	1
Maximum baud rate	f_{PLAT}/(2*16)	baud	1,2
Oversample rate	16	—	3

Notes:
1. f_{PLAT} refers to the internal platform clock.
2. The actual attainable baud rate is limited by the latency of interrupt processing.
3. The middle of a start bit is detected as the eighth sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16th sample.

2.12 Ethernet: data path three-speed Ethernet (dTSEC), management interface, IEEE Std 1588

This section provides the AC and DC electrical characteristics for the data path three-speed Ethernet controller, the Ethernet management interface, and the IEEE Std 1588 interface.

2.12.1 SGMII timing specifications

See Section 2.20.8, "SGMII interface."

2.12.2 MII and RGMII timing specifications

This section discusses the electrical characteristics for the MII and RGMII interfaces.

2.14.1 Enhanced local bus DC electrical characteristics

This table provides the DC electrical characteristics for the enhanced local bus interface operating at BV_{DD} = 3.3 V.

Table 46. Enhanced local bus DC electrical characteristics (BV_{DD} = 3.3 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2.0	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (V_{IN} = 0 V or V_{IN} = BV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (BV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Output low voltage (BV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Notes:
1. The min V_{IL} and max V_{IH} values are based on the respective min and max BV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the BV_{IN} symbol referenced in Section 2.1.2, “Recommended operating conditions.”

This table provides the DC electrical characteristics for the enhanced local bus interface operating at BV_{DD} = 2.5 V.

Table 47. Enhanced local bus DC electrical characteristics (BV_{DD} = 2.5 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	1.7	—	V	1
Input low voltage	V_{IL}	—	0.7	V	1
Input current (V_{IN} = 0 V or V_{IN} = BV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (BV_{DD} = min, I_{OH} = –1 mA)	V_{OH}	2.0	—	V	—
Output low voltage (BV_{DD} = min, I_{OL} = 1 mA)	V_{OL}	—	0.4	V	—

Notes:
1. The min V_{IL} and max V_{IH} values are based on the respective min and max BV_{IN} values found in Table 3
2. The symbol V_{IN}, in this case, represents the BV_{IN} symbol referenced in Section 2.1.2, “Recommended operating conditions.”

This table provides the DC electrical characteristics for the enhanced local bus interface operating at BV_{DD} = 1.8 V.

Table 48. Enhanced local bus DC electrical characteristics (BV_{DD} = 1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	1.25	—	V	1
Input low voltage	V_{IL}	—	0.6	V	1

This figure shows the AC timing diagram of the local bus interface.

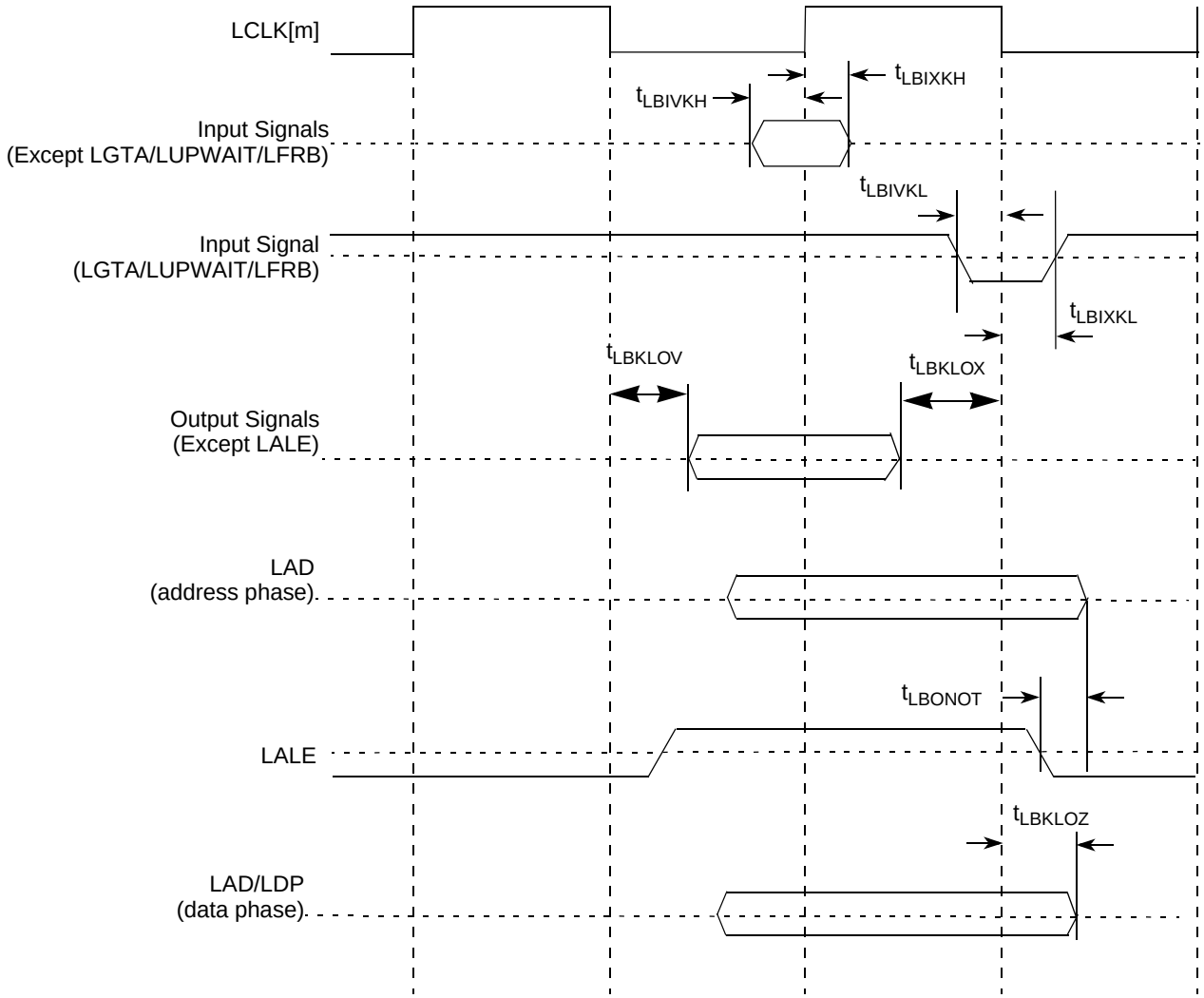

Figure 24. Enhanced local bus signals

Figure 25 applies to all three controllers that eLBC supports: GPCM, UPM, and FCM.

For input signals, the local bus AC timing data is used directly for all three controllers.

For output signals, each type of controller provides its own unique method to control the signal timing. The final signal delay value for output signals is the programmed delay plus the AC timing delay. For example, for GPCM, LCS can be programmed to delay by t_{acs} (0, ¼, ½, 1, 1 + ¼, 1 + ½, 2, 3 cycles), so the final delay is $t_{acs} + t_{LBKLOV}$.

2.20.2.3 AC requirements for SerDes reference clocks

This table lists AC requirements for the PCI Express, SGMII, Serial RapidIO and Aurora SerDes reference clocks to be guaranteed by the customer's application design.

Table 61. SD_REF_CLK ***n*** and $\overline{\text{SD_REF_CLK}}$ ***n*** input clock requirements (SV_{DD} = 1.0 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
SD_REF_CLK/$\overline{\text{SD_REF_CLK}}$ frequency range	t_{CLK_REF}	—	100/125	—	MHz	1
SD_REF_CLK/$\overline{\text{SD_REF_CLK}}$ clock frequency tolerance	t_{CLK_TOL}	–350	—	350	ppm	—
SD_REF_CLK/$\overline{\text{SD_REF_CLK}}$ reference clock duty cycle	t_{CLK_DUTY}	40	50	60	%	4
SD_REF_CLK/$\overline{\text{SD_REF_CLK}}$ max deterministic peak-peak jitter at 10^{-6} BER	t_{CLK_DJ}	—	—	42	ps	—
SD_REF_CLK/$\overline{\text{SD_REF_CLK}}$ total reference clock jitter at 10^{-6} BER (peak-to-peak jitter at refClk input)	t_{CLK_TJ}	—	—	86	ps	2
SD_REF_CLK/$\overline{\text{SD_REF_CLK}}$ rising/falling edge rate	t_{CLKRR}/t_{CLKFR}	1	—	4	V/ns	3
Differential input high voltage	V_{IH}	200	—	—	mV	4
Differential input low voltage	V_{IL}	—	—	–200	mV	4
Rising edge rate (SD_REF_CLK*n*) to falling edge rate ($\overline{\text{SD_REF_CLK}}$*n*) matching	Rise-Fall Matching	—	—	20	%	5, 6

Notes:
1. Caution: Only 100 and 125 have been tested. In-between values not work correctly with the rest of the system.
2. Limits from PCI Express CEM Rev 2.0
3. Measured from –200 mV to +200 mV on the differential waveform (derived from SD_REF_CLK*n* minus $\overline{\text{SD_REF_CLK}}$*n*). The signal must be monotonic through the measurement region for rise and fall time. The 400 mV measurement window is centered on the differential zero crossing. See Figure 40.
4. Measurement taken from differential waveform
5. Measurement taken from single-ended waveform
6. Matching applies to rising edge for SD_REF_CLK*n* and falling edge rate for $\overline{\text{SD_REF_CLK}}$*n*. It is measured using a 200 mV window centered on the median cross point where SD_REF_CLK*n* rising meets $\overline{\text{SD_REF_CLK}}$*n* falling. The median cross point is used to calculate the voltage thresholds that the oscilloscope uses for the edge rate calculations. The rise edge rate of SD_REF_CLK*n* should be compared to the fall edge rate of $\overline{\text{SD_REF_CLK}}$*n*, the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 41.

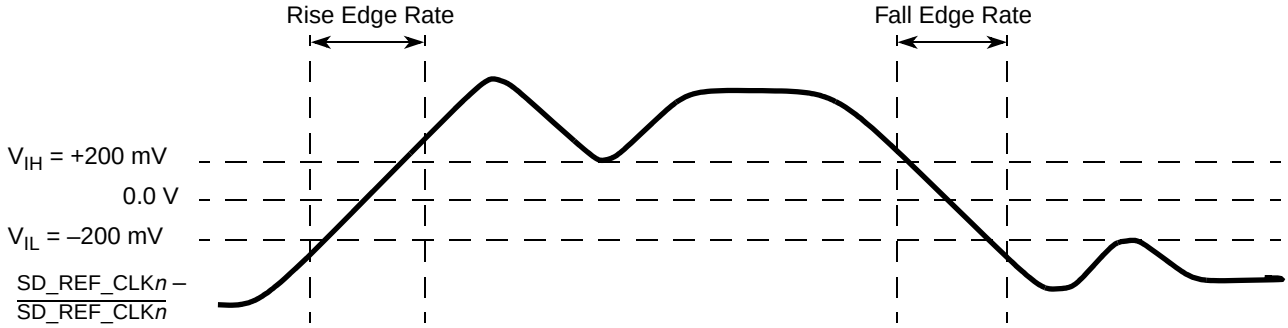

Figure 40. Differential measurement points for rise and fall time

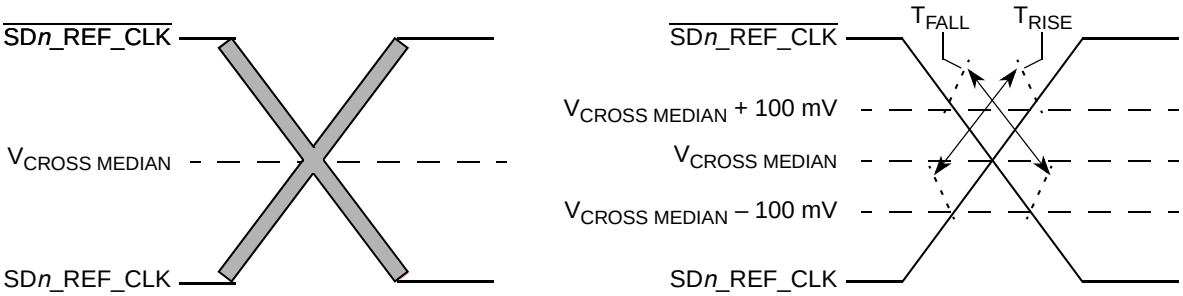

Figure 41. Single-ended measurement points for rise and fall time matching

2.20.2.4 Spread-spectrum clock

SD_REF_CLK1/$\overline{\text{SD_REF_CLK1}}$ were designed to work with a spread spectrum clock (+0 to 0.5% spreading at 30–33 kHz rate is allowed), assuming both ends have same reference clock. For better results, a source without significant unintended modulation should be used.

SD_REF_CLK2/$\overline{\text{SD_REF_CLK2}}$ were designed to work with a spread spectrum clock (+0 to 0.5% spreading at 30–33 kHz rate is allowed), assuming both ends have same reference clock and industry protocol specifications supports it. For better results, a source without significant unintended modulation should be used.

SD_REF_CLK3/$\overline{\text{SD_REF_CLK3}}$ are not intended to be used with, and should not be clocked by, a spread spectrum clock source.

SD_REF_CLK4/$\overline{\text{SD_REF_CLK4}}$ are not intended to be used with, and should not be clocked by, a spread spectrum clock source.

2.20.3 SerDes transmitter and receiver reference circuits

This figure shows the reference circuits for SerDes data lane's transmitter and receiver.

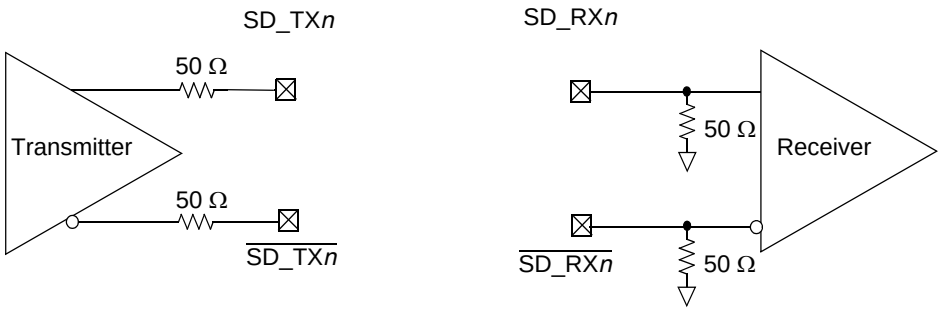

Figure 42. SerDes transmitter and receiver reference circuits

The DC and AC specification of SerDes data lanes are defined in each interface protocol section below based on the application usage:

- Section 2.20.4, "PCI Express"
- Section 2.20.5, "XAUI"
- Section 2.20.6, "Aurora"
- Section 2.20.7, "Serial ATA (SATA)
- Section 2.20.8, "SGMII interface"

Note that external AC-coupling capacitor is required for the above serial transmission protocols per the protocol's standard requirements.

2.20.4 PCI Express

This section describes the clocking dependencies, DC and AC electrical specifications for the PCI Express bus.

2.20.4.1 Clocking dependencies

The ports on the two ends of a link must transmit data at a rate that is within 600 parts per million (ppm) of each other at all times. This is specified to allow bit rate clock sources with a ±300 ppm tolerance.

2.20.4.2 PCI Express clocking requirements for SD_REF_CLK*n* and $\overline{\text{SD_REF_CLK}}$*n*

SerDes banks 1–2 (SD_REF_CLK[1:2] and $\overline{\text{SD_REF_CLK}}$[1:2]) may be used for various SerDes PCI Express configurations based on the RCW Configuration field SRDS_PRTCL. PCI Express is not supported on SerDes bank 3.

For more information on these specifications, see Section 2.20.2, “SerDes reference clocks.”

2.20.4.3 PCI Express DC physical layer specifications

This section contains the DC specifications for the physical layer of PCI Express on this device.

2.20.4.3.1 PCI Express DC physical layer transmitter specifications

This section discusses the PCI Express DC physical layer transmitter specifications for 2.5 GT/s and 5 GT/s.

This table defines the PCI Express 2.0 (2.5 GT/s) DC specifications for the differential output at all transmitters. The parameters are specified at the component pins.

Table 62. PCI Express 2.0 (2.5 GT/s) differential transmitter output DC specifications (XV_{DD} = 1.5 V or 1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typical	Max	Units	Notes
Differential peak-to-peak output voltage	$V_{TX\text{-}DIFFp\text{-}p}$	800	—	1200	mV	$V_{TX\text{-}DIFFp\text{-}p} = 2 \times \lvert V_{TX\text{-}D+} - V_{TX\text{-}D-} \rvert$ See Note 1.
De-emphasized differential output voltage (ratio)	$V_{TX\text{-}DE\text{-}RATIO}$	3.0	3.5	4.0	dB	Ratio of the $V_{TX\text{-}DIFFp\text{-}p}$ of the second and following bits after a transition divided by the $V_{TX\text{-}DIFFp\text{-}p}$ of the first bit after a transition. See Note 1.
DC differential transmitter impedance	$Z_{TX\text{-}DIFF\text{-}DC}$	80	100	120	Ω	Transmitter DC differential mode low Impedance
Transmitter DC impedance	$Z_{TX\text{-}DC}$	40	50	60	Ω	Required transmitter D+ as well as D– DC Impedance during all states

Note:
1. Measured at the package pins with a test load of 50Ω to GND on each pin.

2.20.5.2.3 XAUI receiver AC timing specifications

This table defines the receiver AC specifications for XAUI. RefClkjitter is not included.

Table 74. XAUI receiver AC timing specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Deterministic jitter tolerance	J_D	0.37	—	—	UI p-p	1
Combined deterministic and random jitter tolerance	J_{DR}	0.55	—	—	UI p-p	1
Total jitter tolerance	J_T	0.65	—	—	UI p-p	1, 2
Bit error rate	BER	—	—	10^{-12}	—	—
Unit Interval: 3.125 GBaud	UI	320 – 100 ppm	320	320 + 100 ppm	ps	—

Notes:
1. Measured at receiver
2. Total jitter is composed of three components: deterministic jitter, random jitter, and single frequency sinusoidal jitter. The sinusoidal jitter may have any amplitude and frequency in the unshaded region of Figure 44. The sinusoidal jitter component is included to ensure margin for low frequency jitter, wander, noise, crosstalk, and other variable system effects.

This figure shows the single-frequency sinusoidal jitter limits.

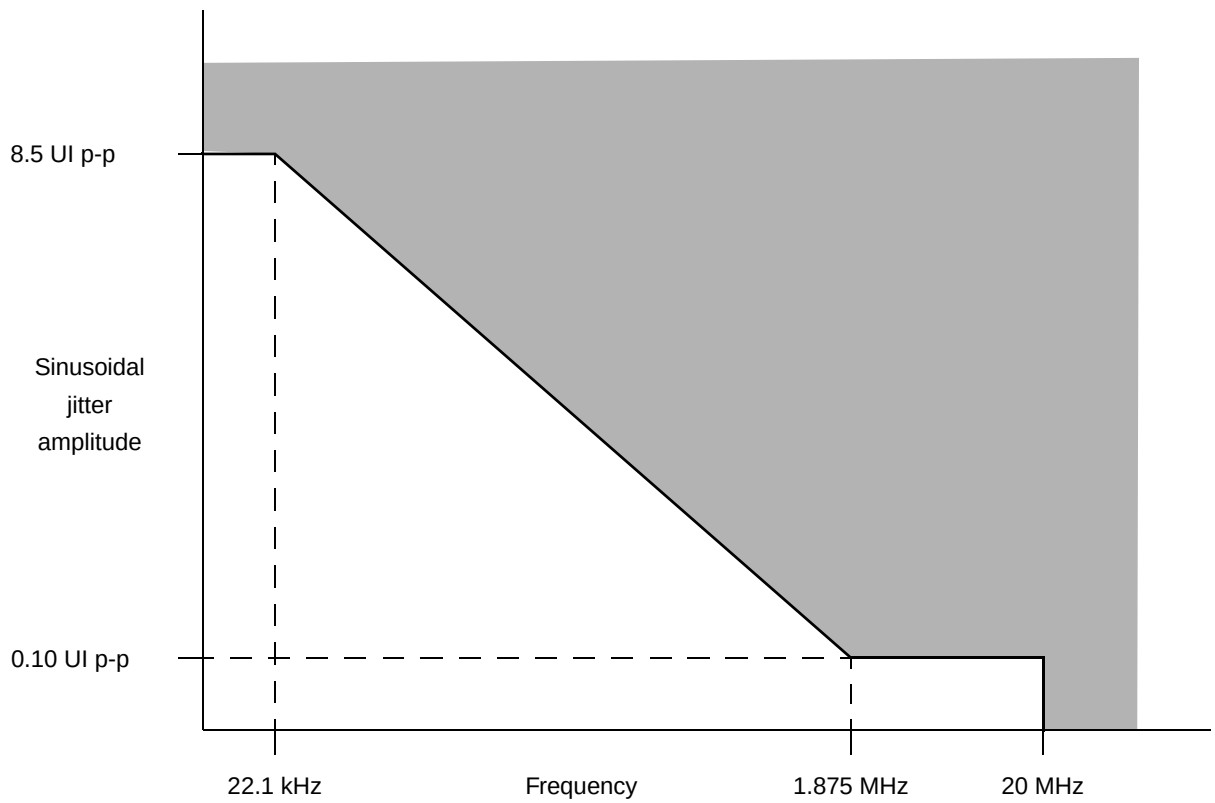

Figure 44. Single-Frequency Sinusoidal Jitter Limits

3.1.1 Clock ranges

This table provides the clocking specifications for the processor core, platform, memory, and local bus.

Table 94. Processor clocking specifications

Characteristic	Maximum Processor Core Frequency						Unit	Notes
	1800 MHz		2000 MHz		2200 MHz			
	Min	Max	Min	Max	Min	Max		
Core PLL frequency	1000	1800	1000	2000	1000	2200	MHz	1,4
Core frequency	667	1800	667	2000	667	2200	MHz	4
Platform clock frequency	600	600	600	700	600	800	MHz	1
Memory bus clock frequency	400	600	400	667	400	800	MHz	1,2,5,6
Local bus clock frequency	—	75	—	87.5	—	100	MHz	3
FMan frequency	300	450	300	600	300	600	MHz	7

Notes:

1. Caution: The platform clock to SYSCLK ratio and core to SYSCLK ratio settings must be chosen such that the resulting SYSCLK frequency, core frequency, and platform clock frequency do not exceed their respective maximum or minimum operating frequencies.
2. The memory bus clock speed is half the DDR3/DDR3L data rate. DDR3/DDR3L memory bus clock frequency is limited to min = 400 MHz.
3. The local bus clock speed on LCLK[0:1] is determined by the platform clock divided by the local bus ratio programmed in LCRR[CLKDIV]. See the applicable chip reference manual for more information.
4. The core can run at core complex PLL/1 or PLL/2. With a core complex PLL frequency of 1333 MHz, this results in the minimum allowable core frequency of 667MHz for PLL/2.
5. In synchronous mode, the memory bus clock speed is half the platform clock frequency. In other words, the DDR data rate is the same as the platform frequency. If the desired DDR data rate is higher than the platform frequency, asynchronous mode must be used.
6. In asynchronous mode, the memory bus clock speed is dictated by its own PLL.
7. The minimum frequencies for the FMan to support the specified interfaces are: 300 MHz for a 1G interface, 450 MHz for a 10 G interface, 500 MHz for a 10 G interface with PCD and 600 MHz for a 10 G and two 1 G interfaces. The FMAN PLL frequency range is the same as the Core PLL frequency range.

Table 98. Asynchronous DDR clock ratio (continued)

Binary value of MEM_PLL_RAT[10:14]	DDR:SYSCLK ratio
0_1100	12:1
0_1101	13:1
1_0000	16:1
1_0010	18:1
1_0011	19:1
1_0100	20:1
1_1000	24:1
All Others	Reserved

Note:
1. RCW[MEM_PLL_CFG] is set dependant on the DDR clock ratio used. See Table 99 for valid setttings of DDR clock ratio and MEM_PLL_CFG.

Table 99. Supported DDR ratios and RCW MEM_PLL_CFG settings

MEM:SYSCLK Ratio	SYSCLK (MHz)			
	100	125	133.3	150
	DDR Rate (MT/s)/MEM_PLL_CFG			
1 (Sync Mode)	Platform Clock/01			
6	Reserved		800/11	900/11[3]
8	800/10[1]	1000/01[1]	1067/01	1200/01
9	900/10[2]	1125/01[2]	1200/01	1350/01
10	1000/01	1250/01	1333/01	1500/01
12	1200/11	1500/11	1600/11	Reserved
13	1300/11	Reserved		
16	1600/11	Reserved		

Notes:
1. For MEM SYSYCLK RATIO = 8, MEM_PLL_CFG changes from 10 to 01 when SYSCLK is greater than or equal to 120.9MHz
2. For MEM SYSYCLK RATIO = 9, MEM_PLL_CFG changes from 10 to 01 when SYSCLK is greater than or equal to 107.4MHz
3. Maximum SYSCLK is 161.2MHz when MEM:SYSCLK ratio = 6

In synchronous mode, the DDR data rate to platform clock ratios supported are listed in this table. This ratio is determined by the binary value of the RCW Configuration field MEM_PLL_RAT[10:14].

Table 100. Synchronous DDR clock ratio

Binary Value of MEM_PLL_RAT[10:14]	DDR:Platform CLK ratio	Set MEM_PLL_CFG=01 for platform CLK freq [1]
0_0001	1:1	>600 MHz
All Others	Reserved	—

Note:
1. Set RCW field MEM_PLL_CFG=0b01

3.1.6 Frequency options

This section discusses interface frequency options.

3.1.6.1 SYSCLK and platform frequency options

This table shows the expected frequency options for SYSCLK and platform frequencies.

Table 101. SYSCLK and platform frequency options

Platform: SYSCLK ratio	SYSCLK (MHz)			
	100	125	133.3	150
	Platform frequency (MHz) [1]			
5:1		625	666	750
6:1	600	750	800	
7:1	700			
8:1	800			

[1] Platform frequency values are shown rounded down to the nearest whole number (decimal place accuracy removed)

3.1.6.2 Minimum platform frequency requirements for high-speed interfaces

The platform clock frequency must be considered for proper operation of high-speed interfaces as described below.

For proper PCI Express operation, the platform clock frequency must be greater than or equal to the values shown in these figures.

$$\frac{527\ \text{MHz} \times (\text{PCI Express link width})}{16}$$

Figure 49. Gen 1 PEX minimum platform frequency

$$\frac{527\ \text{MHz} \times (\text{PCI Express link width})}{8}$$

Figure 50. Gen 2 PEX minimum platform frequency

3.6.3 Guidelines for high-speed interface termination

This section provides the guidelines for high-speed interface termination when the SerDes interface is entirely unused or when it is partly unused.

3.6.3.1 SerDes interface entirely unused

If the high-speed SerDes interface is not used at all, the unused pin should be terminated as described in this section.

The following pins must be left unconnected:

- SD_TX[19:0]
- $\overline{\text{SD_TX}}$[19:0]
- SD_IMP_CAL_RX
- SD_IMP_CAL_TX
- SD1_IMP_CAL_RX
- SD1_IMP_CAL_TX

The following pins must be connected to SGND:

- SD_RX[19:0]
- $\overline{\text{SD_RX}}$[19:0]
- SD_REF_CLK1, SD_REF_CLK2, SD_REF_CLK3, SD_REF_CLK4
- $\overline{\text{SD_REF_CLK1}}$, $\overline{\text{SD_REF_CLK2}}$, $\overline{\text{SD_REF_CLK3}}$, $\overline{\text{SD_REF_CLK4}}$

The RCW configuration fields SRDS_LPD_B1, SRDS_LPD_B2, SRDS_LPD_B3, and SRDS_LPD_B4, all bits must be set to power down all the lanes in each bank.

The RCW configuration field SRDS_EN may be cleared to power down the SerDes block for power saving. Setting RCW[SRDS_EN_S1] = 0 powers down the PLLs of banks 1, 3; RCW[SRDS_EN_S2]=0 powers down the PLL of bank 4.

Additionally, software may configure SRDSPRSTCTL[SDRD]= 1 for the unused banks to power down the SerDes bank PLLs to save power.

Note that both SV_{DD} and XV_{DD} must remain powered.

3.6.3.2 SerDes interface partly unused

If only part of the high speed SerDes interface pins are used, the remaining high-speed serial I/O pins should be terminated as described in this section.

The following pins must be left unconnected:

- SD_TX[*n*]
- $\overline{\text{SD_TX}}$[*n*]

The following unused pins must be connected to SGND:

- SD_RX[*n*]
- $\overline{\text{SD_RX}}$[*n*]
- SD_REF_CLK1, $\overline{\text{SD_REF_CLK1}}$ (If entire SerDes bank 1 unused)
- SD_REF_CLK2, $\overline{\text{SD_REF_CLK2}}$ (If entire SerDes bank 2 unused)
- SD_REF_CLK3, $\overline{\text{SD_REF_CLK3}}$ (If entire SerDes bank 3 unused)
- SD_REF_CLK4, $\overline{\text{SD_REF_CLK4}}$ (If entire SerDes bank 4 unused)