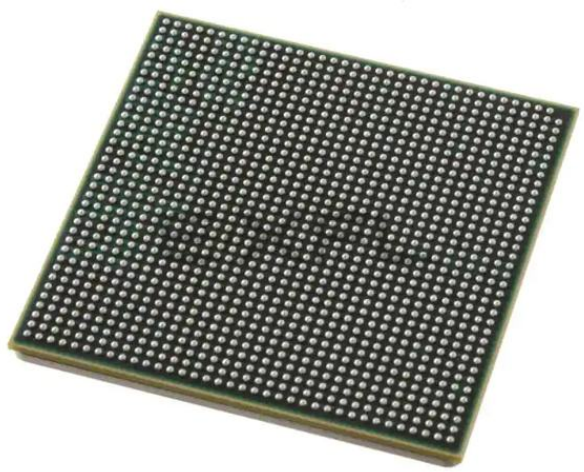


Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e5500
Number of Cores/Bus Width	2 Core, 64-Bit
Speed	2.0GHz
Co-Processors/DSP	-
RAM Controllers	DDR3, DDR3L
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	1Gbps (10), 10Gbps (2)
SATA	SATA 3Gbps (2)
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.0V, 1.1V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	1295-BBGA, FCBGA
Supplier Device Package	1295-FCPBGA (37.5x37.5)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p5021nsn7vnc

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GND	Ground	AF5	—	—	—
GND	Ground	AG3	—	—	—
GND	Ground	AG9	—	—	—
GND	Ground	AH7	—	—	—
GND	Ground	AJ5	—	—	—
GND	Ground	AK3	—	—	—
GND	Ground	AN3	—	—	—
GND	Ground	AM5	—	—	—
GND	Ground	AL7	—	—	—
GND	Ground	AK9	—	—	—
GND	Ground	AJ11	—	—	—
GND	Ground	AH13	—	—	—
GND	Ground	AR5	—	—	—
GND	Ground	AP7	—	—	—
GND	Ground	AN9	—	—	—
GND	Ground	AM11	—	—	—
GND	Ground	AL13	—	—	—
GND	Ground	AK15	—	—	—
GND	Ground	AG18	—	—	—
GND	Ground	AR11	—	—	—
GND	Ground	AP13	—	—	—
GND	Ground	AN15	—	—	—
GND	Ground	AM17	—	—	—
GND	Ground	AK19	—	—	—
GND	Ground	AF13	—	—	—
GND	Ground	AR18	—	—	—
GND	Ground	AB27	—	—	—
GND	Ground	AP19	—	—	—
GND	Ground	AH22	—	—	—
GND	Ground	AM21	—	—	—
GND	Ground	AL29	—	—	—
GND	Ground	AR16	—	—	—
GND	Ground	AT22	—	—	—
GND	Ground	AP23	—	—	—

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GVDD	DDR Supply	W10	—	GV_{DD}	—
GVDD	DDR Supply	AA6	—	GV_{DD}	—
GVDD	DDR Supply	AR2	—	GV_{DD}	—
GVDD	DDR Supply	Y2	—	GV_{DD}	—
GVDD	DDR Supply	Y8	—	GV_{DD}	—
GVDD	DDR Supply	AC2	—	GV_{DD}	—
GVDD	DDR Supply	AD6	—	GV_{DD}	—
GVDD	DDR Supply	AE10	—	GV_{DD}	—
GVDD	DDR Supply	AE4	—	GV_{DD}	—
GVDD	DDR Supply	AF2	—	GV_{DD}	—
GVDD	DDR Supply	AF8	—	GV_{DD}	—
GVDD	DDR Supply	AB4	—	GV_{DD}	—
GVDD	DDR Supply	AB10	—	GV_{DD}	—
GVDD	DDR Supply	AC8	—	GV_{DD}	—
GVDD	DDR Supply	AG6	—	GV_{DD}	—
GVDD	DDR Supply	AH10	—	GV_{DD}	—
GVDD	DDR Supply	AH4	—	GV_{DD}	—
GVDD	DDR Supply	AJ2	—	GV_{DD}	—
GVDD	DDR Supply	AJ8	—	GV_{DD}	—
GVDD	DDR Supply	AR14	—	GV_{DD}	—
GVDD	DDR Supply	AK6	—	GV_{DD}	—
GVDD	DDR Supply	AL4	—	GV_{DD}	—
GVDD	DDR Supply	AL10	—	GV_{DD}	—
GVDD	DDR Supply	AM2	—	GV_{DD}	—
GVDD	DDR Supply	AM8	—	GV_{DD}	—
GVDD	DDR Supply	AP10	—	GV_{DD}	—
GVDD	DDR Supply	AN12	—	GV_{DD}	—
GVDD	DDR Supply	AN6	—	GV_{DD}	—
GVDD	DDR Supply	AP4	—	GV_{DD}	—
BVDD	Local Bus Supply	B24	—	BV_{DD}	—
BVDD	Local Bus Supply	K22	—	BV_{DD}	—
BVDD	Local Bus Supply	F20	—	BV_{DD}	—
BVDD	Local Bus Supply	F26	—	BV_{DD}	—
BVDD	Local Bus Supply	E24	—	BV_{DD}	—

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
AVDD_SRDS2	SerDes PLL2 Supply	U36	—	—	13
AVDD_SRDS3	SerDes PLL3 Supply	AE35	—	—	13
AVDD_SRDS4	SerDes PLL4 Supply	R28	—	—	13
SENSEVDD_PL1	Platform Vdd Sense	AF11	—	—	8
SENSEVDD_PL2	Platform Vdd Sense	L27	—	—	8
SENSEVDD_CA	Core Group A Vdd Sense	K16	—	—	8
USB1_VDD_3P3	USB1 PHY Transceiver 3.3V Supply	AL24	—	—	—
USB1_VDD_3P3	USB1 PHY Transceiver 3.3V Supply	AJ25	—	—	—
USB2_VDD_3P3	USB2 PHY Transceiver 3.3V Supply	AJ26	—	—	—
USB2_VDD_3P3	USB2 PHY Transceiver 3.3V Supply	AJ27	—	—	—
USB1_VDD_1P0	USB1 PHY PLL 1.0V Supply	AH25	—	—	—
USB2_VDD_1P0	USB2 PHY PLL 1.0V Supply	AH26	—	—	—
Analog Signals					
MVREF	SSTL_1.5/1.35 Reference Voltage	B19	I	$GV_{DD}/2$	—
SD_IMP_CAL_TX	SerDes transmitter Impedance Calibration	AF30	I	200Ω (±1%) to XV_{DD}	23
SD1_IMP_CAL_TX	SerDes transmitter Impedance Calibration	AA28	I	200Ω (±1%) to XV_{DD}	23
SD_IMP_CAL_RX	SerDes receiver Impedance Calibration	B27	I	200Ω (±1%) to SV_{DD}	24
SD1_IMP_CAL_RX	SerDes receiver Impedance Calibration	AF26	I	200Ω (±1%) to SV_{DD}	24
TEMP_ANODE	Temperature Diode Anode	C21	—	internal diode	9
TEMP_CATHODE	Temperature Diode Cathode	B21	—	internal diode	9
USB1_IBIAS_REXT	USB PHY1 Reference Bias Current Generation	AM26	—	—	36
USB2_IBIAS_REXT	USB PHY2 Reference Bias Current Generation	AM27	—	—	36
USB1_VDD_1P8_DECAP	USB1 PHY 1.8V Output to External Decap	AL26	—	—	37

Table 2. Absolute maximum operating conditions[1] (continued)

Parameter	Symbol	Maximum value	Unit	Notes
Fuse programming override supply	POV_{DD}	–0.3 to 1.65	V	1
DUART, I^2C, DMA, MPIC, GPIO, system control and power management, clocking, debug, I/O voltage select, and JTAG I/O voltage	OV_{DD}	–0.3 to 3.63	V	—
eSPI, eSHDC	CV_{DD}	–0.3 to 3.63 –0.3 to 2.75 –0.3 to 1.98	V	—
DDR3 and DDR3L DRAM I/O voltage	GV_{DD}	–0.3 to 1.65	V	—
Enhanced local bus I/O voltage	BV_{DD}	–0.3 to 3.63 –0.3 to 2.75 –0.3 to 1.98	V	—
Core power supply for SerDes transceivers	SV_{DD}	–0.3 to 1.1	V	—
Pad power supply for SerDes transceivers	XV_{DD}	–0.3 to 1.98 –0.3 to 1.65	V	—
Ethernet I/O, Ethernet management interface 1 (EMI1), 1588, GPIO	LV_{DD}	–0.3 to 3.63 –0.3 to 2.75	V	3
Ethernet management interface 2 (EMI2)	—	–0.3 to 1.32	V	8
USB PHY Transceiver supply voltage	$USB\_V_{DD}\_3P3$	–0.3 to 3.63	V	—
USB PHY PLL supply voltage	$USB\_V_{DD}\_1P0$	–0.3 to 1.1	V	—
Low-power security monitor supply	V_{DD_LP}	–0.3 to 1.1	V	—

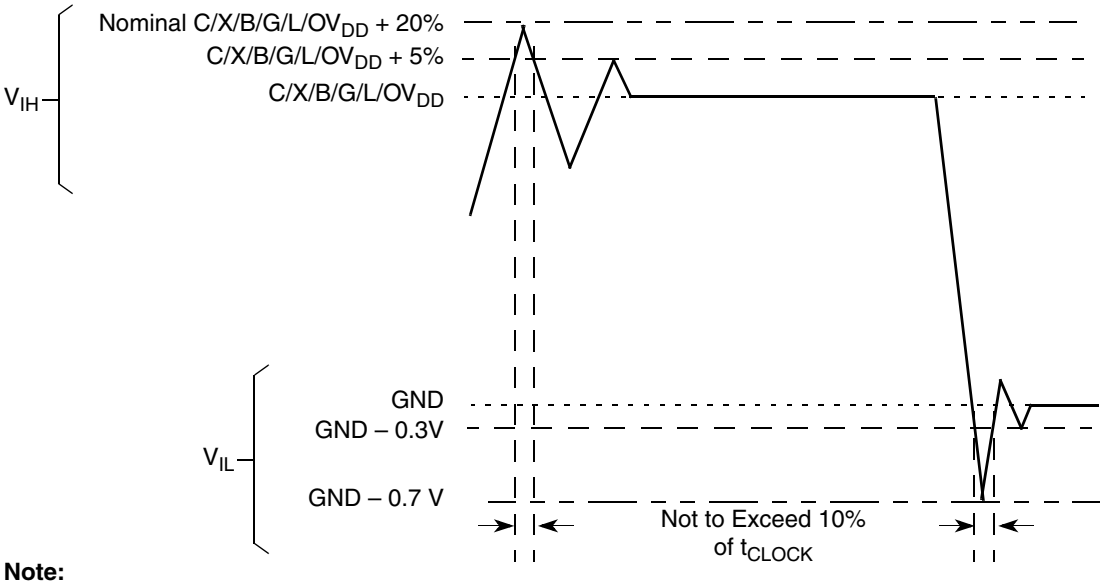
2.1.2 Recommended operating conditions

This table provides the recommended operating conditions for this device. Note that proper device operation outside these conditions is not guaranteed.

Table 3. Recommended operating conditions

Parameter		Symbol	Recommended value	Unit	Notes
Core group A (core 0,1) supply voltage		V_{DD_CA}	1.1 ± 50mV (core frequency ≤ 2000 MHz) 1.2V ± 30mV (core frequency > 2000 MHz)	V	1,6
Platform supply voltage		V_{DD_PL}	1.0 ± 50mV	V	1,6
PLL supply voltage (core, platform, DDR, FMan)		AV_{DD}	1.0 ± 50mV	V	—
PLL supply voltage (SerDes)		AV_{DD_SRDS}	1.0 ± 50mV	V	—
Fuse programming override supply		POV_{DD}	1.5 ± 75mV	V	2
DUART, I^2C, DMA, MPIC, GPIO, system control and power management, clocking, debug, I/O voltage select, and JTAG I/O voltage		OV_{DD}	3.3 ± 165mV	V	—
eSPI, eSDHC		CV_{DD}	3.3 ± 165mV 2.5 ± 125mV 1.8 ± 90mV	V	—
DDR DRAM I/O voltage	DDR3	GV_{DD}	1.5 ± 75mV	V	—
	DDR3L		1.35 ± 67mV		
Enhanced local bus I/O voltage		BV_{DD}	3.3 ± 165mV 2.5 ± 125mV 1.8 ± 90mV	V	—
Main power supply for internal circuitry of SerDes and pad power supply for SerDes receiver		SV_{DD}	1.0 + 50mV 1.0 – 30mV	V	—
Pad power supply for SerDes transmitter		XV_{DD}	1.8 ± 90mV 1.5 ± 75mV	V	—
Ethernet I/O, Ethernet Management interface 1 (EMI1), 1588, GPIO		LV_{DD}	3.3 ± 165mV 2.5 ± 125mV	V	3
USB PHY transceiver supply voltage		$USB\_V_{DD}\_3P3$	3.3 ± 165mV	V	—
USB PHY PLL supply voltage		$USB\_V_{DD}\_1P0$	1.0 ± 50mV	V	—
Low-power security monitor supply		V_{DD_LP}	1.0 ± 50mV	V	—

This figure shows the undershoot and overshoot voltages at the interfaces of the chip.



Note:

t_{CLOCK} refers to the clock period associated with the respective interface:
For I2C, t_{CLOCK} refers to SYSCLK.
For DDR GV_{DD}, t_{CLOCK} refers to D*n*_MCK.
For eSPI CV_{DD}, t_{CLOCK} refers to SPI_CLK.
For eLBC BV_{DD}, t_{CLOCK} refers to LCLK.
For SerDes XV_{DD}, t_{CLOCK} refers to SD_REF_CLK.
For dTSEC LV_{DD}, t_{CLOCK} refers to EC_GTX_CLK125.
For JTAG OV_{DD}, t_{CLOCK} refers to TCK.

Figure 7. Overshoot/Undershoot voltage for $BV_{DD}/GV_{DD}/LV_{DD}/OV_{DD}$

The core and platform voltages must always be provided at nominal 1.0 V or 1.2 V. See Table 3 for the actual recommended core voltage conditions. Voltage to the processor interface I/Os is provided through separate sets of supply pins and must be provided at the voltages shown in Table 3. The input voltage threshold scales with respect to the associated I/O supply voltage. CV_{DD}, BV_{DD}, OV_{DD}, and LV_{DD}-based receivers are simple CMOS I/O circuits and satisfy appropriate LVCMOS type specifications. The DDR SDRAM interface uses differential receivers referenced by the externally supplied MV_{REF} signal (nominally set to $GV_{DD}/2$) as is appropriate for the SSTL_1.5 electrical signaling standard. The DDR DQS receivers cannot be operated in single-ended fashion. The complement signal must be properly driven and cannot be grounded.

WARNING

Incorrect voltage select settings can lead to irreversible device damage. See Section 3.2, "Supply power default setting."

NOTE

From a system standpoint, if any of the I/O power supplies ramp prior to the V_{DD_CA}, or V_{DD_PL} supplies, the I/Os associated with that I/O supply may drive a logic one or zero during power-up, and extra current may be drawn by the device.

2.3 Power-down requirements

The power-down cycle must complete such that power supply values are below 0.4 V before a new power-up cycle can be started.

If performing secure boot fuse programming per Section 2.2, "Power-up sequencing," it is required that POV_{DD} = GND before the system is power cycled ($\overline{\text{PORESET}}$ assertion) or powered down (V_{DD_PL} ramp down) per the required timing specified in Table 5.

V_{DD_PL} and USB_V_{DD}_1P0 must be ramped down simultaneously. USB_V_{DD}_1P8_DECAP should starts ramping down only after USB_V_{DD}_3P3 is below 1.65 V.

2.4 Power characteristics

This table shows the power dissipations of the V_{DD_CA}, SV_{DD}, and V_{DD_PL} supply for various operating platform clock frequencies versus the core and DDR clock frequencies for the chip.

Table 6. Power dissipation

Power Mode	Core freq (MHz)	Plat freq (MHz)	DDR data rate (MHz)	FM freq (MHz)	V_{DD_PL}, SV_{DD} (V)	V_{DD_CA} (V)	Junction temp (°C)	Core and platform power[1] (W)	V_{DD_PL} power (W)	V_{DD_CA} power (W)	SV_{DD} power (W)	Note
Typical	2200	800	1600	600	1.0	1.2	65	23	—	—	—	—
Thermal							90	33	—	—	—	—
Maximum								34	17	15	15	2.2
Typical	2000	700	1333	600	1.0	1.1	65	21	—	—	—	—
Thermal							105	30	—	—	—	—
Maximum								31	16	13	13	2.2

This table shows the estimated power dissipation on the POV_{DD} supply for the chip, at allowable voltage levels.

Table 8. POV_{DD} power dissipation

Supply	Maximum	Unit	Notes
POV_{DD}	450	mW	1

Note:

1. To ensure device reliability, fuse programming must be performed within the recommended fuse programming temperature range per Table 3.

This table shows the estimated power dissipation on the V_{DD_LP} supply for the chip, at allowable voltage levels.

Table 9. V_{DD_LP} Power Dissipation

Supply	Maximum	Unit	Note
V_{DD_LP} (P5021 on, 105C)	1.5	mW	1
V_{DD_LP} (P5021 off, 70C)	195	uW	2
V_{DD_LP} (P5021 off, 40C)	132	uW	2

Note:

1. V_{DD_LP} = 1.0 V, T_J = 105°C.
2. When P5021 is off, V_{DD_LP} may be supplied by battery power to the Zeroizable Master Key and other Trust Architecture state. Board should implement a PMIC which switches V_{DD_LP} to battery when P5021 is powered down. See P5040 Reference Manual Trust Architecture chapter for more information.

2.5 Thermal

This table shows the thermal characteristics for the chip.

Table 10. Package thermal characteristics [6]

Rating	Board	Symbol	Value	Unit	Notes
Junction to ambient, natural convection	Single-layer board (1s)	$R_{\Theta JA}$	14	°C/W	1, 2
Junction to ambient, natural convection	Four-layer board (2s2p)	$R_{\Theta JA}$	10	°C/W	1, 2
Junction to ambient (at 200 ft./min.)	Single-layer board (1s)	$R_{\Theta JMA}$	9	°C/W	1, 2
Junction to ambient (at 200 ft./min.)	Four-layer board (2s2p)	$R_{\Theta JMA}$	7	°C/W	1, 2

2.9.1 DDR3 and DDR3L SDRAM interface DC electrical characteristics

This table provides the recommended operating conditions for the DDR SDRAM controller when interfacing to DDR3 SDRAM.

Table 18. DDR3 SDRAM interface DC electrical characteristics (GV_{DD} = 1.5 V)[1]

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
I/O reference voltage	MV_{REF}	0.49 × GV_{DD}	0.51 × GV_{DD}	V	2, 3, 4
Input high voltage	V_{IH}	MV_{REF} + 0.100	GV_{DD}	V	5
Input low voltage	V_{IL}	GND	MV_{REF} – 0.100	V	5
I/O leakage current	I_{OZ}	–50	50	μA	6

Notes:

1. GV_{DD} is expected to be within 50 mV of the DRAM's voltage supply at all times. The DRAM's and memory controller's voltage supply may or may not be from the same source.
2. MV_{REF} is expected to be equal to 0.5 × GV_{DD} and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed the MV_{REF} DC level by more than ±1% of the DC value (that is, ±15 mV).
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made, and it is expected to be equal to MV_{REF} with a min value of MV_{REF} – 0.04 and a max value of MV_{REF} + 0.04. V_{TT} should track variations in the DC level of MV_{REF}
4. The voltage regulator for MV_{REF} must meet the specifications stated in Table 21.
5. Input capacitance load for DQ, DQS, and $\overline{DQS}$ are available in the IBIS models.
6. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GV_{DD}.

This table provides the recommended operating conditions for the DDR SDRAM controller when interfacing to DDR3L SDRAM.

Table 19. DDR3L SDRAM interface DC electrical characteristics (GV_{DD} = 1.35 V)[1]

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
I/O reference voltage	MV_{REF}	0.49 × GV_{DD}	0.51 × GV_{DD}	V	2, 3, 4
Input high voltage	V_{IH}	MV_{REF} + 0.090	GV_{DD}	V	5
Input low voltage	V_{IL}	GND	MV_{REF} – 0.090	V	5

2.12.3.1 Ethernet management interface 1 DC electrical characteristics

The Ethernet management interface 1 is defined to operate at a supply voltage of 3.3 V. The DC electrical characteristics for the Ethernet management interface is provided in this table.

Table 37. Ethernet management Interface 1 DC electrical characteristics (LV_{DD} = 3.3 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	2.0	—	V	2
Input low voltage	V_{IL}	—	0.9	V	2
Input high current (LV_{DD} = Max, V_{IN} = 2.1 V)	I_{IH}	—	40	μA	1
Input low current (LV_{DD} = Max, V_{IN} = 0.5 V)	I_{IL}	–600	—	μA	1
Output high voltage (LV_{DD} = Min, I_{OH} = –1.0 mA)	V_{OH}	2.4	—	V	—
Output low voltage (LV_{DD} = Min, I_{OL} = 1.0 mA)	V_{OL}	—	0.4	V	—

Note:
1. The symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 2 and Table 3.
2. The min V_{IL} and max V_{IH} values are based on the respective LV_{IN} values found in Table 3.

The Ethernet management interface 1 is defined to operate at a supply voltage of 3.3 V. The DC electrical characteristics for the Ethernet management interface 1 is provided in Table 37.

Table 38. Ethernet management interface 1 DC electrical characteristics (LV_{DD} = 2.5 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	1.7	—	V	1
Input low voltage	V_{IL}	—	0.7	V	1
Input current (LV_{IN} = 0 V or LV_{IN} = LV_{DD})	I_{IH}	—	±40	μA	2
Output high voltage (LV_{DD} = Min, IOH = –1.0 mA)	V_{OH}	2.4	—	V	—
Output low voltage (LV_{DD} = Min, I_{OL} = 1.0 mA)	V_{OL}	—	0.4	V	—

Note:
1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max LV_{IN} values found in Table 3.
2. The symbol LV_{IN}, in this case, represents the LV_{IN} symbol referenced in Section 2.1.2, “Recommended operating conditions.”

2.12.3.2 Ethernet management interface 2 DC electrical characteristics

Ethernet management interface 2 pins function as open drain I/Os. The interface conforms to 1.2 V nominal voltage levels. LV_{DD} must be powered to use this interface. The DC electrical characteristics for EMI2_MDIO and EMI2_MDC are provided in this section.

Table 39. Ethernet management interface 2 DC electrical characteristics (1.2 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	0.84	—	V	—
Input low voltage	V_{IL}	—	0.36	V	—

Table 48. Enhanced local bus DC electrical characteristics (BV_{DD} = 1.8 V) (continued)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Notes
Input current (V_{IN} = 0 V or V_{IN} = BV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (BV_{DD} = min, I_{OH} = –0.5 mA)	V_{OH}	1.35	—	V	—
Output low voltage (BV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	—	0.4	V	—

Notes:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max BV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the BV_{IN} symbol referenced in Section 2.1.2, "Recommended operating conditions."

2.14.2 Enhanced local bus AC timing specifications

This section describes the AC timing specifications for the enhanced local bus interface.

2.14.2.1 Test condition

This figure provides the AC test load for the enhanced local bus.

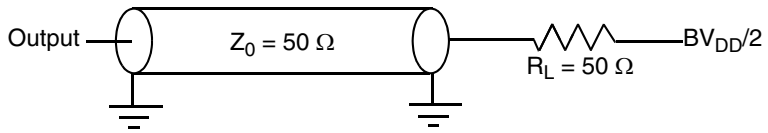


Figure 23. Enhanced local bus AC test load

2.14.2.2 Local bus AC timing specification

All output signal timings are relative to the falling edge of any LCLKs. The external circuit must use the rising edge of the LCLKs to latch the data.

All input timings except LGTA/LUPWAIT/LFRB are relative to the rising edge of LCLKs. LGTA/LUPWAIT/LFRB are relative to the falling edge of LCLKs.

This table describes the timing specifications of the local bus interface.

Table 49. Enhanced local bus timing specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol[1]	Min	Max	Unit	Notes
Local bus cycle time	t_{LBK}	10	—	ns	—
Local bus duty cycle	t_{LBKH}/t_{LBK}	45	55	%	—
LCLK[n] skew to LCLK[m]	$t_{LBKSKEW}$	—	150	ps	2
Input setup (except LGTA/LUPWAIT/LFRB)	t_{LBIVKH}	6	—	ns	—
Input hold (except LGTA/LUPWAIT/LFRB)	t_{LBIXKH}	1	—	ns	—

This figure shows the AC timing diagram of the local bus interface.

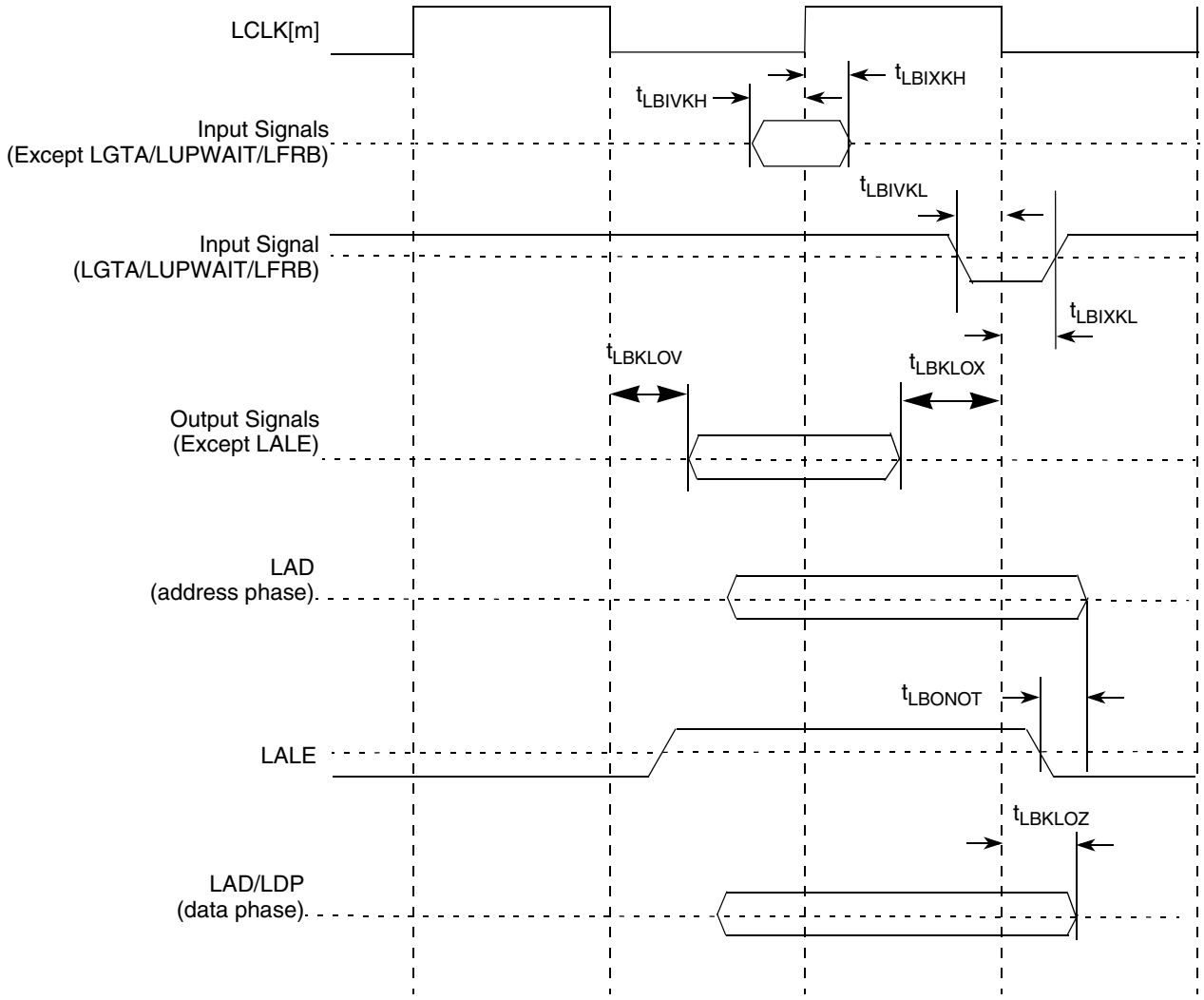


Figure 24. Enhanced local bus signals

Figure 25 applies to all three controllers that eLBC supports: GPCM, UPM, and FCM.

For input signals, the local bus AC timing data is used directly for all three controllers.

For output signals, each type of controller provides its own unique method to control the signal timing. The final signal delay value for output signals is the programmed delay plus the AC timing delay. For example, for GPCM, LCS can be programmed to delay by t_{acs} (0, ¼, ½, 1, 1 + ¼, 1 + ½, 2, 3 cycles), so the final delay is $t_{acs} + t_{LBKLOV}$.

This figure shows how the signals are defined. For illustration purposes only, one SerDes lane is used in the description. This figure shows the waveform for either a transmitter output (SD_TX*n* and $\overline{\text{SD\_TX}n}$) or a receiver input (SD_RX*n* and $\overline{\text{SD\_RX}n}$). Each signal swings between A volts and B volts where A > B.

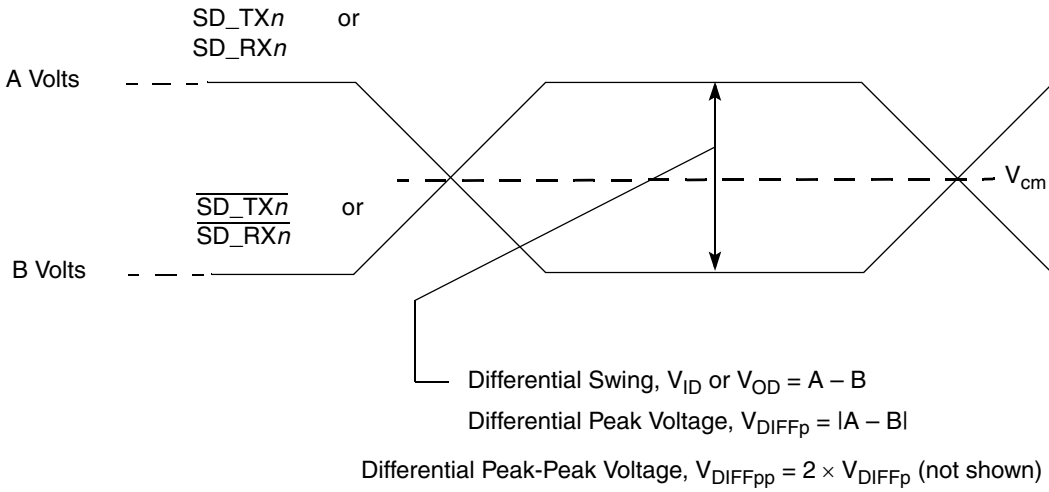


Figure 35. Differential voltage definitions for transmitter or receiver

Using this waveform, the definitions are as shown in the following list. To simplify the illustration, the definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signaling environment:

Single-Ended Swing
The transmitter output signals and the receiver input signals SD_TX*n*, $\overline{\text{SD\_TX}n}$, SD_RX*n* and $\overline{\text{SD\_RX}n}$ each have a peak-to-peak swing of A – B volts. This is also referred as each signal wire's single-ended swing.

Differential Output Voltage, V_{OD} (or **Differential Output Swing**):
The differential output voltage (or swing) of the transmitter, V_{OD}, is defined as the difference of the two complementary output voltages: $V_{SD\_TXn} - V_{\overline{SD\_TXn}}$. The V_{OD} value can be either positive or negative.

Differential Input Voltage, V_{ID} (or **Differential Input Swing**):
The differential input voltage (or swing) of the receiver, V_{ID}, is defined as the difference of the two complementary input voltages: $V_{SD\_RXn} - V_{\overline{SD\_RXn}}$. The V_{ID} value can be either positive or negative.

Differential Peak Voltage, V_{DIFFp}
The peak value of the differential transmitter output signal or the differential receiver input signal is defined as the differential peak voltage, $V_{DIFFp} = |A - B|$ volts.

Differential Peak-to-Peak, $V_{DIFFp-p}$
Since the differential output signal of the transmitter and the differential input signal of the receiver each range from A – B to –(A – B) volts, the peak-to-peak value of the differential transmitter output signal or the differential receiver input signal is defined as differential peak-to-peak voltage, $V_{DIFFp-p} = 2 \times V_{DIFFp} = 2 \times |(A - B)|$ volts, which is twice the differential swing in amplitude, or twice of the differential peak. For example, the output differential peak-peak voltage can also be calculated as $V_{TX-DIFFp-p} = 2 \times |V_{OD}|$.

Differential Waveform
The differential waveform is constructed by subtracting the inverting signal ($\overline{\text{SD\_TX}n}$, for example) from the non-inverting signal ($\overline{\text{SD\_TX}n}$, for example) within a differential pair. There is only one signal trace curve in a differential waveform. The voltage represented in the differential

2.20.6 Aurora

This section describes the Aurora clocking requirements and AC and DC electrical characteristics.

2.20.6.1 Aurora DC electrical characteristics

This section describes the DC electrical characteristics for Aurora.

2.20.6.1.1 Aurora DC clocking requirements for SD_REF_CLK*n* and $\overline{\text{SD\_REF\_CLK}n}$

Only SerDes bank 1 (SD_REF_CLK1 and $\overline{\text{SD\_REF\_CLK1}}$) may be used for SerDes Aurora configurations based on the RCW Configuration field SRDS_PRTCL. Aurora is not supported on SerDes banks 2-3.

For more information on these specifications, see Section 2.20.2, "SerDes reference clocks."

2.20.6.1.2 Aurora transmitter DC electrical characteristics

This table defines the Aurora transmitter DC electrical characteristics.

Table 75. Aurora transmitter DC electrical characteristics (XV_{DD} = 1.5 V or 1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typical	Max	Unit
Differential output voltage	V_{DIFFPP}	800	—	1600	mV p-p

2.20.6.1.3 Aurora receiver DC electrical characteristics

This table defines the Aurora receiver DC electrical characteristics for Aurora.

Table 76. Aurora receiver DC electrical characteristics (XV_{DD} = 1.5 V or 1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Differential input voltage	V_{IN}	120	900	1200	mV p-p	1

Note:

1. Measured at receiver

2.20.6.2 Aurora AC timing specifications

This section describes the AC timing specifications for Aurora.

2.20.6.2.1 Aurora AC clocking requirements for SD_REF_CLK*n* and $\overline{\text{SD\_REF\_CLK}n}$

Only SerDes bank 1 (SD_REF_CLK1 and $\overline{\text{SD\_REF\_CLK1}}$) may be used for SerDes Aurora configurations based on the RCW Configuration field SRDS_PRTCL. Aurora is not supported on SerDes banks 2–3.

Please note that the XAUI clock requirements for SD_REF_CLK*n* and $\overline{\text{SD\_REF\_CLK}n}$ are intended to be used within the clocking guidelines specified by either Section 2.20.2.3, "AC requirements for SerDes reference clocks" or Section 2.20.7.2.1, "AC requirements for SATA REF_CLK."

Table 85. Gen 2i/3 G transmitter AC specifications (continued)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typ	Max	Units	Notes
Deterministic jitter, $f_{C3dB} = f_{BAUD} \div 10$	$U_{SATA\_TXDJfB/10}$	—	—	0.17	UI p-p	1
Deterministic jitter, $f_{C3dB} = f_{BAUD} \div 500$	$U_{SATA\_TXDJfB/500}$	—	—	0.19	UI p-p	1
Deterministic jitter, $f_{C3dB} = f_{BAUD} \div 1667$	$U_{SATA\_TXDJfB/1667}$	—	—	0.35	UI p-p	1

Note:

1. Measured at transmitter output pins peak-to-peak phase variation, random data pattern

2.20.7.4 AC differential receiver Input characteristics

This table provides the Gen1i or 1.5 Gbits/s differential receiver input AC characteristics for the SATA interface. The AC timing specifications do not include RefClk jitter.

Table 86. Gen 1i/1.5G receiver AC specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typical	Max	Units	Notes
Unit Interval	T_{UI}	666.4333	666.6667	670.2333	ps	—
Total jitter data-data 5 UI	$U_{SATA\_TXTJ5UI}$	—	—	0.43	UI p-p	1
Total jitter, data-data 250 UI	$U_{SATA\_TXTJ250UI}$	—	—	0.60	UI p-p	1
Deterministic jitter, data-data 5 UI	$U_{SATA\_TXDJ5UI}$	—	—	0.25	UI p-p	1
Deterministic jitter, data-data 250 UI	$U_{SATA\_TXDJ250UI}$	—	—	0.35	UI p-p	1

Note:

1. Measured at receiver

This table provides the differential receiver input AC characteristics for the SATA interface at Gen2i or 3.0 Gbits/s transmission. The AC timing specifications do not include RefClk jitter.

Table 87. Gen 2i/3G receiver AC specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typical	Max	Units	Notes
Unit Interval	T_{UI}	333.2167	333.3333	335.1167	ps	—
Total jitter $f_{C3dB} = f_{BAUD} \div 10$	$U_{SATA\_TXTJfB/10}$	—	—	0.46	UI p-p	1
Total jitter $f_{C3dB} = f_{BAUD} \div 500$	$U_{SATA\_TXTJfB/500}$	—	—	0.60	UI p-p	1
Total jitter $f_{C3dB} = f_{BAUD} \div 1667$	$U_{SATA\_TXTJfB/1667}$	—	—	0.65	UI p-p	1

Note that “PCI Express link width” in the above equation refers to the negotiated link width as the result of PCI Express link training, which may or may not be the same as the link width POR selection.

3.1.7 SerDes PLL ratio

The clock ratio between each of the four SerDes PLLs and their respective externally supplied SD_REF_CLK*n*/$\overline{\text{SD\_REF\_CLK}n}$ inputs is determined by the binary value of the RCW Configuration field SRDS_RATIO_B*n* as shown in this table. Furthermore, each SerDes lane grouping can be run at a SerDes PLL frequency divider determined by the binary value of the RCW field SRDS_DIV_B*n* as shown in Table 103 and Table 104.

This table lists the supported SerDes PLL Bank *n* to SD_REF_CLK*n* ratios.

Table 102. SerDes PLL bank *n* to SD_REF_CLK*n* ratios

Binary value of SRDS_RATIO_B*n*	SRDS_PLL_*n*:SD_REF_CLK*n* ratio			
	***n* = 1 (bank 1)**	***n* = 2 (bank 2)**	***n* = 3 (bank 3)**	***n* = 4(bank 4)**
001	Reserved	20:1	20:1	Reserved
010	25:1	25:1	25:1	Reserved
011	40:1	40:1	40:1	Reserved
100	50:1	50:1	50:1	Reserved
101	Reserved	Reserved	24:1	24:1
110	Reserved	Reserved	30:1	30:1
All Others	Reserved	Reserved	Reserved	Reserved

This table shows the PLL divider support for each pair of lanes on SerDes Bank 1.

Table 103. SerDes bank 1 PLL dividers

Binary value of SRDS_DIV_B1[0:4]	SerDes bank 1 PLL divider
0b0	Divide by 1 off Bank 1 PLL
0b1	Divide by 2 off Bank 1 PLL

Note:

1. 1 bit (of 5 total SRDS_DIV_B1 bits) controls each pair of lanes, where the first bit controls configuration of lanes A/B (or 0/1) and the last bit controls configuration of lanes I/J (or 8/9).

This table shows the PLL dividers supported for each 4 lane group for SerDes Banks 2, 3, and 4.

Table 104. SerDes banks 2, 3, and 4 PLL dividers

Binary value of SRDS_DIV_B*n*	SerDes Bank *n* PLL divider
0b0	Divide by 1 off Bank *n* PLL
0b1	Divide by 2 off Bank *n* PLL

Notes:

1. One bit controls all 4 lanes of each bank.
2. n = 2 or 3 (SerDes bank 2 or bank 3)

3.1.8 Frame Manager (FMan) clock select

The Frame Managers (FM) can each be synchronous with or asynchronous to the platform, depending on configuration.

This table describes the clocking options that may be applied to each FM. The clock selection is determined by the binary value of the RCW Clocking Configuration fields FM1_CLK_SEL and FM2_CLK_SEL.

Table 105. Frame Manager (FMan) clock select

Binary value of FM*n*_CLK_SEL	FM frequency
0b0	Platform Clock Frequency /2
0b1	FMan PLL Frequency /2 [1,2]

Notes:

1. For asynchronous mode, max frequency see Table 94.
2. For PLL settings, see Table 96.

3.2 Supply power default setting

This chip is capable of supporting multiple power supply levels on its I/O supplies. The I/O voltage select inputs, shown in the following table, properly configure the receivers and drivers of the I/Os associated with the BVDD, CVDD, and LVDD power planes, respectively.

WARNING

Incorrect voltage select settings can lead to irreversible device damage.

Table 106. I/O voltage selection

Signals	Value (binary)	VDD voltage selection		
		BVDD	CVDD	LVDD
IO_VSEL[0:4] Default (0_0000)	0_0000	3.3 V	3.3 V	3.3 V
	0_0001	3.3 V	3.3 V	2.5 V
	0_0011	3.3 V	2.5 V	3.3 V
	0_0100	3.3 V	2.5 V	2.5 V
	0_0110	3.3 V	1.8 V	3.3 V
	0_0111	3.3 V	1.8 V	2.5 V
	0_1001	2.5 V	3.3 V	3.3 V
	0_1010	2.5 V	3.3 V	2.5 V
	0_1100	2.5 V	2.5 V	3.3 V
	0_1101	2.5 V	2.5 V	2.5 V
	0_1111	2.5 V	1.8 V	3.3 V
	1_0000	2.5 V	1.8 V	2.5 V
	1_0010	1.8 V	3.3 V	3.3 V
	1_0011	1.8 V	3.3 V	2.5 V
	1_0101	1.8 V	2.5 V	3.3 V
	1_0110	1.8 V	2.5 V	2.5 V
	1_1000	1.8 V	1.8 V	3.3 V
	1_1001	1.8 V	1.8 V	2.5 V
	1_1011	3.3 V	3.3 V	3.3 V
	1_1100	3.3 V	3.3 V	3.3 V
	1_1101	3.3 V	3.3 V	3.3 V
	1_1110	3.3 V	3.3 V	3.3 V
	1_1111	3.3 V	3.3 V	3.3 V
	All Others	Reserved		

3.3 Power supply design

3.3.1 PLL power supply filtering

Each of the PLLs described in Section 3.1, "System clocking," is provided with power through independent power supply pins (AV_{DD_PLAT}, AV_{DD_CCn}, AV_{DD_DDR}, AV_{DD_FM}, and AV_{DD_SRDSn}). AV_{DD_PLAT}, AV_{DD_CCn}, AV_{DD_FM}, and AV_{DD_DDR} voltages must be derived directly from the V_{DD_PL} source through a low frequency filter scheme. AV_{DD_SRDSn} voltages must be derived directly from the SV_{DD} source through a low frequency filter scheme.

The recommended solution for PLL filtering is to provide independent filter circuits per PLL power supply, as illustrated in Figure 51, one for each of the AV_{DD} pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLL's resonant frequency range from a 500-kHz to 10-MHz range.

3.7 Recommended thermal model

Information about Flotherm models of the package or thermal data not available in this document can be obtained from your local Freescale sales office.

3.8 Thermal management information

This section provides thermal management information for the flip-chip, plastic-ball, grid array (FC-PBGA) package for air-cooled applications. Proper thermal control design is primarily dependent on the system-level design—the heat sink, airflow, and thermal interface material.

The recommended attachment method to the heat sink is illustrated in this figure. The heat sink should be attached to the printed-circuit board with the spring force centered over the die. This spring force should not exceed 10 pounds force (45 Newton).

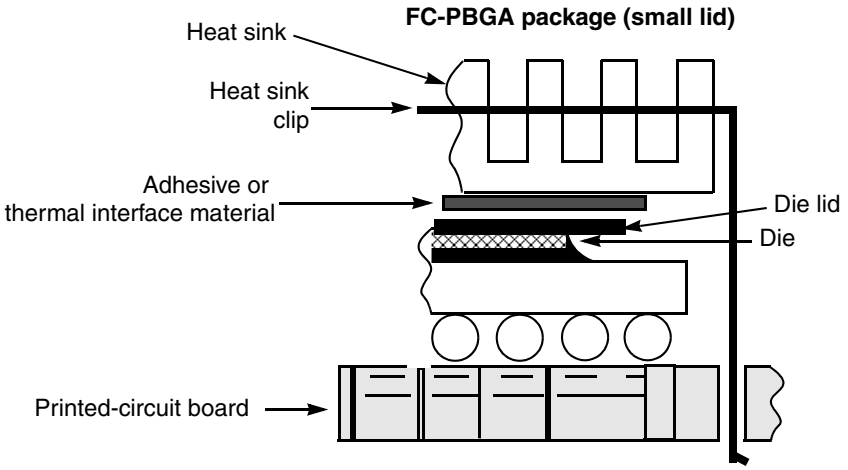


Figure 62. Exploded cross-sectional view—FC-PBGA (with lid) package

The system board designer can choose between several types of heat sinks to place on the device. There are several commercially-available thermal interfaces to choose from in the industry. Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost.

3.8.1 Internal package conduction resistance

For the package, the intrinsic internal conduction thermal resistance paths are as follows:

- The die junction-to-case thermal resistance
- The die junction-to-lid-top thermal resistance
- The die junction-to-board thermal resistance

5 Security fuse processor

This chip implements the QorIQ platform's Trust Architecture, supporting capabilities such as secure boot. Use of the Trust Architecture features is dependent on programming fuses in the Security Fuse Processor (SFP). The details of the Trust Architecture and SFP can be found in the applicable chip reference manual.

To program SFP fuses, the user is required to supply 1.5 V to the POV_{DD} pin per Section 2.2, "Power-up sequencing." POV_{DD} should only be powered for the duration of the fuse programming cycle, with a per device limit of two fuse programming cycles. All other times, connect POV_{DD} to GND. The sequencing requirements for raising and lowering POV_{DD} are shown in Figure 8. To ensure device reliability, fuse programming must be performed within the recommended fuse programming temperature range per Table 3.

Users not implementing the QorIQ platform's Trust Architecture features are not required to program fuses and should connect POV_{DD} to GND.

6 Ordering information

Please contact your local Freescale sales office or regional marketing team for ordering information.

6.1 Part numbering nomenclature

This table provides the Freescale QorIQ platform part numbering nomenclature.

Table 108. Part Numbering Nomenclature

p	*n*	*nn*	*n*	*x*	*t*	*e*	*n*	*c*	*d*	*r*
Generation	**Platform**	**Number of Cores**	**Derivative**	**Qual Status**	**Temperature Range**	**Encryption**	**Package Type**	**CPU Speed**	**DDR Speed**	**Die Revision**
P = 45 nm	5	• 01 = 1 core • 02 = 2 cores • 04 = 4 cores	0–9	P = Prototype N = Qualified	• S = Std temp (0 °C to 105 °C • X = Ext temp (–40 °C to 105 °C)	• E = SEC present • N = SEC not present	1 = FC-PBGA lead-free 7 = FC-PBGA C4/C5 lead-free	• T = 1800 MHz • V = 2000 MHz • 2 = 2200 MHz	• M = 1200 MHz • N = 1333 MHz • Q = 1600 MHz	A = Rev 1.0 B = Rev 2.0 C = Rev 2.1