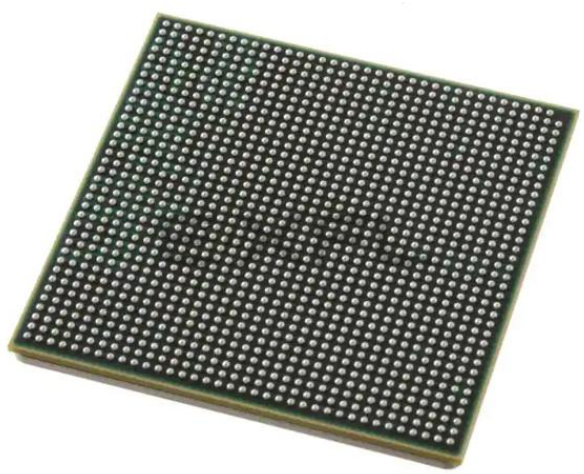

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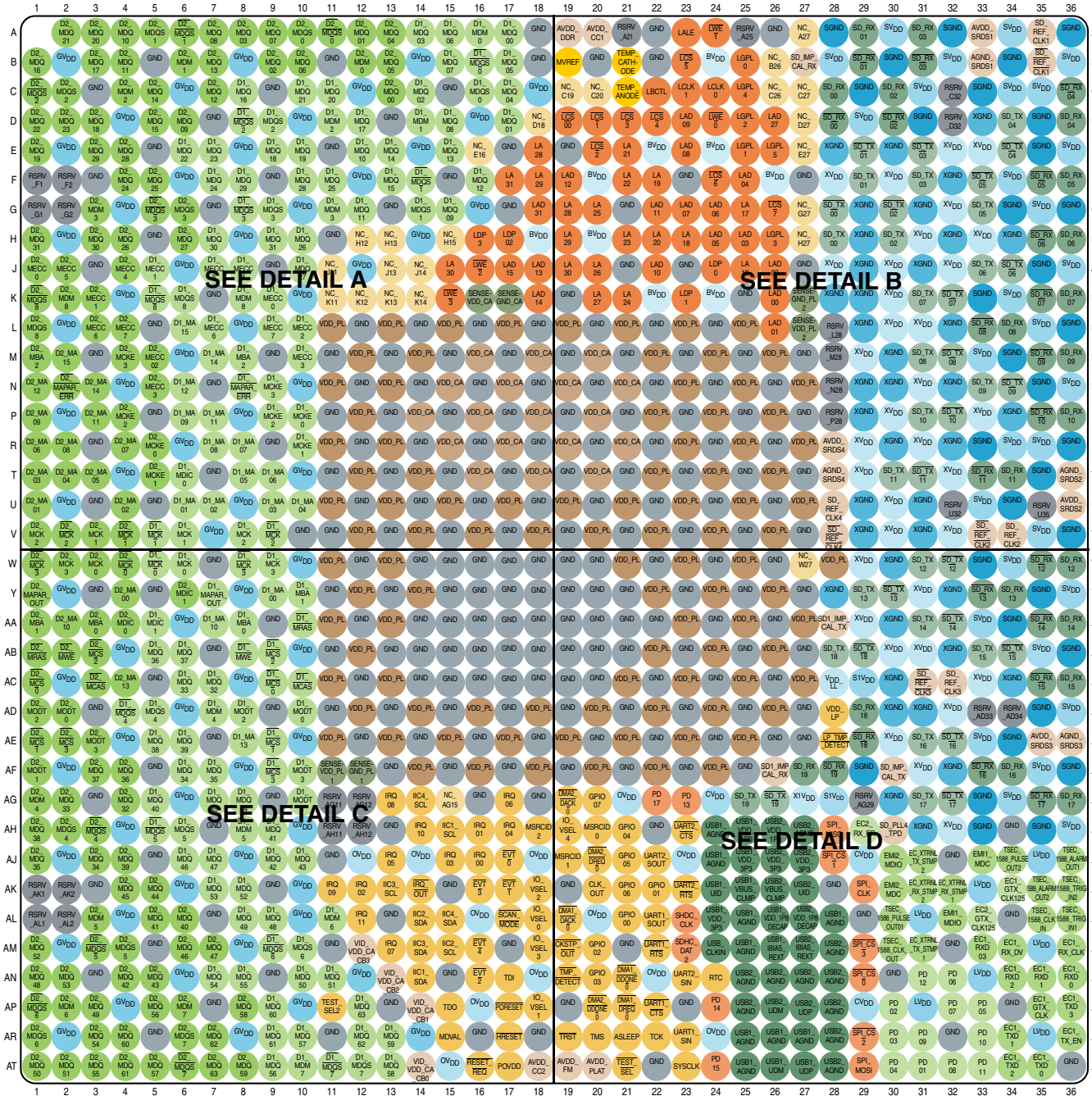
Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e5500
Number of Cores/Bus Width	2 Core, 64-Bit
Speed	2.2GHz
Co-Processors/DSP	-
RAM Controllers	DDR3, DDR3L
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	1Gbps (10), 10Gbps (2)
SATA	SATA 3Gbps (2)
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.0V, 1.2V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	Boot Security, Cryptography, Secure Fusebox, Secure Debug, Tamper Detection, Volatile key Storage
Package / Case	1295-BBGA, FCBGA
Supplier Device Package	1295-FCPBGA (37.5x37.5)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p5021nxe72qc



Signal Groups

- OV_{DD} I/O Supply Voltage
- LV_{DD} I/O Supply Voltage
- GV_{DD} DDR DRAM I/O Supply
- CV_{DD} SPI Voltage Supply
- BV_{DD} Local Bus I/O Supply
- SV_{DD} SerDes Core Power Supply
- XV_{DD} SerDes Transcvr Pad Supply
- VDD_{PL} Platform Supply Voltage
- VDD_{CA} Core Group A Supply Voltage
- $AVDD_{SRDS1}$ SerDes 1 PLL Supply Voltage
- $AVDD_{SRDS2}$ SerDes 2 PLL Supply Voltage
- $AVDD_{PLAT}$ Platform PLL Supply Voltage
- $AVDD_{CC}$ Core PLL Supply Voltage
- $SENSE_{VDD\_PL}$ Platform Voltage Sense
- $SENSE_{VDD}$ Core Group A Voltage Sense
- $SENSE_{VDD\_CB}$ Core Group B Voltage Sense
- RSRV Reserved
- POVDD Fuse Programming Override Supply

Figure 2. 1295 BGA ball map diagram (top view)

DETAIL D

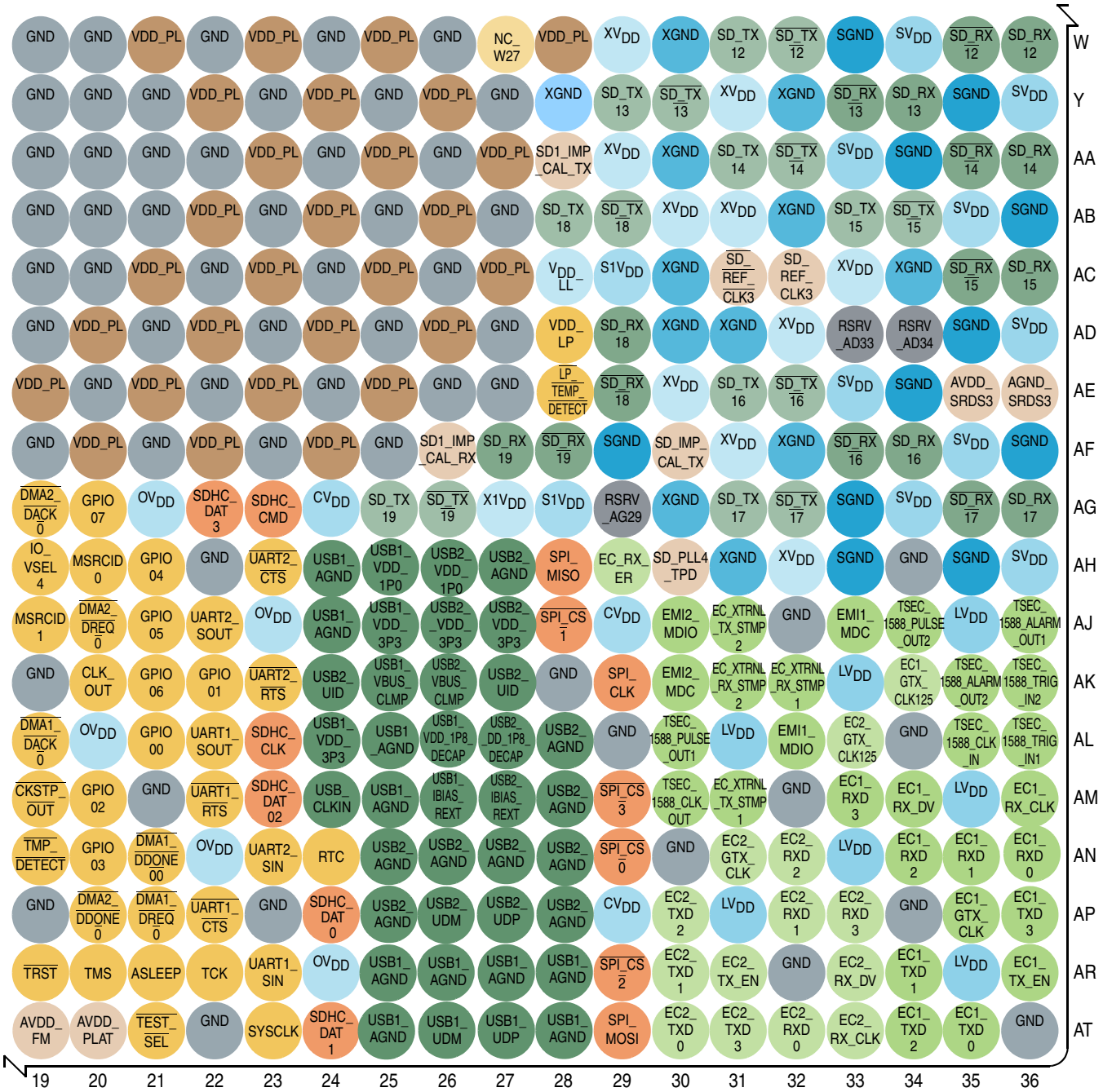


Figure 6. 1295 BGA ball map diagram (detail view D)

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
D1_MDQ31	Data	H9	I/O	GV_{DD}	—
D1_MDQ32	Data	AC7	I/O	GV_{DD}	—
D1_MDQ33	Data	AC6	I/O	GV_{DD}	—
D1_MDQ34	Data	AF6	I/O	GV_{DD}	—
D1_MDQ35	Data	AF7	I/O	GV_{DD}	—
D1_MDQ36	Data	AB5	I/O	GV_{DD}	—
D1_MDQ37	Data	AB6	I/O	GV_{DD}	—
D1_MDQ38	Data	AE5	I/O	GV_{DD}	—
D1_MDQ39	Data	AE6	I/O	GV_{DD}	—
D1_MDQ40	Data	AG5	I/O	GV_{DD}	—
D1_MDQ41	Data	AH9	I/O	GV_{DD}	—
D1_MDQ42	Data	AJ9	I/O	GV_{DD}	—
D1_MDQ43	Data	AJ10	I/O	GV_{DD}	—
D1_MDQ44	Data	AG8	I/O	GV_{DD}	—
D1_MDQ45	Data	AG7	I/O	GV_{DD}	—
D1_MDQ46	Data	AJ6	I/O	GV_{DD}	—
D1_MDQ47	Data	AJ7	I/O	GV_{DD}	—
D1_MDQ48	Data	AL9	I/O	GV_{DD}	—
D1_MDQ49	Data	AL8	I/O	GV_{DD}	—
D1_MDQ50	Data	AN10	I/O	GV_{DD}	—
D1_MDQ51	Data	AN11	I/O	GV_{DD}	—
D1_MDQ52	Data	AK8	I/O	GV_{DD}	—
D1_MDQ53	Data	AK7	I/O	GV_{DD}	—
D1_MDQ54	Data	AN7	I/O	GV_{DD}	—
D1_MDQ55	Data	AN8	I/O	GV_{DD}	—
D1_MDQ56	Data	AT9	I/O	GV_{DD}	—
D1_MDQ57	Data	AR10	I/O	GV_{DD}	—
D1_MDQ58	Data	AT13	I/O	GV_{DD}	—
D1_MDQ59	Data	AR13	I/O	GV_{DD}	—
D1_MDQ60	Data	AP9	I/O	GV_{DD}	—
D1_MDQ61	Data	AR9	I/O	GV_{DD}	—
D1_MDQ62	Data	AR12	I/O	GV_{DD}	—
D1_MDQ63	Data	AP12	I/O	GV_{DD}	—
D1_MECC0	Error Correcting Code	K9	I/O	GV_{DD}	—

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
D1_MCK2	Clock	V8	O	GV_{DD}	—
D1_MCK3	Clock	W9	O	GV_{DD}	—
$\overline{\text{D1\_MCK0}}$	Clock Complements	W5	O	GV_{DD}	—
$\overline{\text{D1\_MCK1}}$	Clock Complements	V5	O	GV_{DD}	—
$\overline{\text{D1\_MCK2}}$	Clock Complements	V9	O	GV_{DD}	—
$\overline{\text{D1\_MCK3}}$	Clock Complements	W8	O	GV_{DD}	—
D1_MODT0	On Die Termination	AD10	O	GV_{DD}	—
D1_MODT1	On Die Termination	AG10	O	GV_{DD}	—
D1_MODT2	On Die Termination	AD8	O	GV_{DD}	—
D1_MODT3	On Die Termination	AF10	O	GV_{DD}	—
D1_MDIC0	Driver Impedance Calibration	T6	I/O	GV_{DD}	16
D1_MDIC1	Driver Impedance Calibration	AA5	I/O	GV_{DD}	16
DDR SDRAM Memory interface 2					
D2_MDQ00	Data	C13	I/O	GV_{DD}	—
D2_MDQ01	Data	A12	I/O	GV_{DD}	—
D2_MDQ02	Data	B9	I/O	GV_{DD}	—
D2_MDQ03	Data	A8	I/O	GV_{DD}	—
D2_MDQ04	Data	A13	I/O	GV_{DD}	—
D2_MDQ05	Data	B13	I/O	GV_{DD}	—
D2_MDQ06	Data	B10	I/O	GV_{DD}	—
D2_MDQ07	Data	A9	I/O	GV_{DD}	—
D2_MDQ08	Data	A7	I/O	GV_{DD}	—
D2_MDQ09	Data	D6	I/O	GV_{DD}	—
D2_MDQ10	Data	A4	I/O	GV_{DD}	—
D2_MDQ11	Data	B4	I/O	GV_{DD}	—
D2_MDQ12	Data	C7	I/O	GV_{DD}	—
D2_MDQ13	Data	B7	I/O	GV_{DD}	—
D2_MDQ14	Data	C5	I/O	GV_{DD}	—
D2_MDQ15	Data	D5	I/O	GV_{DD}	—
D2_MDQ16	Data	B1	I/O	GV_{DD}	—
D2_MDQ17	Data	B3	I/O	GV_{DD}	—
D2_MDQ18	Data	D3	I/O	GV_{DD}	—
D2_MDQ19	Data	E1	I/O	GV_{DD}	—
D2_MDQ20	Data	A3	I/O	GV_{DD}	—

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
SDHC_DAT0	Data	AP24	I/O	CV_{DD}	—
SDHC_DAT1	Data	AT24	I/O	CV_{DD}	—
SDHC_DAT2	Data	AM23	I/O	CV_{DD}	—
SDHC_DAT3	Data	AG22	I/O	CV_{DD}	—
SDHC_DAT4/$\overline{\text{SPI\_CS0}}$	Data	AN29	I/O	CV_{DD}	26, 31
SDHC_DAT5/$\overline{\text{SPI\_CS1}}$	Data	AJ28	I/O	CV_{DD}	26, 31
SDHC_DAT6/$\overline{\text{SPI\_CS2}}$	Data	AR29	I/O	CV_{DD}	26, 31
SDHC_DAT7/$\overline{\text{SPI\_CS3}}$	Data	AM29	I/O	CV_{DD}	26, 31
SDHC_CLK	Host to Card Clock	AL23	O	CV_{DD}	—
$\overline{\text{SDHC\_CD}}$/IIC3_SCL/GPIO16	Card Detection	AK13	I	OV_{DD}	26,27,31
SDHC_WP/IIC3_SDA/GPIO17	Card Write Protection	AM14	I	OV_{DD}	26,27,31
eSPI					
SPI_MOSI	Master Out Slave In	AT29	I/O	CV_{DD}	—
SPI_MISO	Master In Slave Out	AH28	I	CV_{DD}	—
SPI_CLK	eSPI clock	AK29	O	CV_{DD}	—
$\overline{\text{SPI\_CS0}}$/SDHC_DAT4	eSPI chip select	AN29	O	CV_{DD}	26
$\overline{\text{SPI\_CS1}}$/SDHC_DAT5	eSPI chip select	AJ28	O	CV_{DD}	26
$\overline{\text{SPI\_CS2}}$/SDHC_DAT6	eSPI chip select	AR29	O	CV_{DD}	26
$\overline{\text{SPI\_CS3}}$/SDHC_DAT7	eSPI chip select	AM29	O	CV_{DD}	26
IEEE 1588					
TSEC_1588_CLK_IN	Clock In	AL35	I	LV_{DD}	—
TSEC_1588_TRIG_IN1	Trigger In 1	AL36	I	LV_{DD}	—
TSEC_1588_TRIG_IN2/EC1_RX_ER	Trigger In 2	AK36	I	LV_{DD}	—
TSEC_1588_ALARM_OUT1	Alarm Out 1	AJ36	O	LV_{DD}	—
TSEC_1588_ALARM_OUT2/EC1_COL/GPIO30	Alarm Out 2	AK35	O	LV_{DD}	26
TSEC_1588_CLK_OUT	Clock Out	AM30	O	LV_{DD}	—
TSEC_1588_PULSE_OUT1	Pulse Out1	AL30	O	LV_{DD}	—
TSEC_1588_PULSE_OUT2/EC1_CRS/GPIO31	Pulse Out2	AJ34	O	LV_{DD}	26
Ethernet Management interface 1					
EMI1_MDC	Management Data Clock	AJ33	O	LV_{DD}	—
EMI1_MDIO	Management Data In/Out	AL32	I/O	LV_{DD}	—
Ethernet Management interface 2					
EMI2_MDC	Management Data Clock	AK30	O	1.2 V	2, 18, 22

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GND	Ground	T13	—	—	—
GND	Ground	V13	—	—	—
GND	Ground	Y13	—	—	—
GND	Ground	AB13	—	—	—
GND	Ground	AD13	—	—	—
GND	Ground	AE14	—	—	—
GND	Ground	AC14	—	—	—
GND	Ground	AA14	—	—	—
GND	Ground	W14	—	—	—
GND	Ground	U14	—	—	—
GND	Ground	R14	—	—	—
GND	Ground	N14	—	—	—
GND	Ground	L14	—	—	—
GND	Ground	M15	—	—	—
GND	Ground	P15	—	—	—
GND	Ground	T15	—	—	—
GND	Ground	V15	—	—	—
GND	Ground	Y15	—	—	—
GND	Ground	AB15	—	—	—
GND	Ground	AD15	—	—	—
GND	Ground	AF15	—	—	—
GND	Ground	W16	—	—	—
GND	Ground	AC16	—	—	—
GND	Ground	AA16	—	—	—
GND	Ground	AE16	—	—	—
GND	Ground	U16	—	—	—
GND	Ground	R16	—	—	—
GND	Ground	N16	—	—	—
GND	Ground	M17	—	—	—
GND	Ground	P17	—	—	—
GND	Ground	T17	—	—	—
GND	Ground	N18	—	—	—
GND	Ground	R18	—	—	—
GND	Ground	U18	—	—	—

Table 15. RESET initialization timing specifications (continued)

Parameter	Min	Max	Unit[1]	Notes
Input hold time for all POR configurations with respect to negation of $\overline{\text{PORESET}}$	2	—	SYSCLKs	1
Maximum valid-to-high impedance time for actively driven POR configurations with respect to negation of $\overline{\text{PORESET}}$	—	5	SYSCLKs	1

Notes:
1. SYSCLK is the primary clock input for the chip.
2. The device asserts $\overline{\text{HRESET}}$ as an output when $\overline{\text{PORESET}}$ is asserted to initiate the power-on reset process. The device releases $\overline{\text{HRESET}}$ sometime after $\overline{\text{PORESET}}$ is negated. The exact sequencing of HRESET negation is documented in Section 4.4.1 “Power-On Reset Sequence,” of the applicable chip reference manual.
3. $\overline{\text{PORESET}}$ must be driven asserted before the core and platform power supplies are powered up , see Section 2.2, “Power-up sequencing.”

This table provides the PLL lock times.

Table 16. PLL lock times

Parameter	Min	Max	Unit	Notes
PLL lock times	—	100	µs	—

2.8 Power-on ramp rate

This section describes the AC electrical specifications for the power-on ramp rate requirements. Controlling the maximum Power-On Ramp Rate is required to avoid falsely triggering the ESD circuitry. This table provides the power supply ramp rate specifications.

Table 17. Power supply ramp rate

Parameter	Min	Max	Unit	Notes
Required ramp rate for all voltage supplies (including OV_{DD}/CV_{DD}/ GV_{DD}/BV_{DD}/SV_{DD}/XV_{DD}/LV_{DD} all V_{DD} supplies, MVREF and all AV_{DD} supplies.)	—	36000	V/s	1, 2

Notes:
1. Ramp rate is specified as a linear ramp from 10 to 90%. If non-linear (for example, exponential), the maximum rate of change from 200 to 500 mV is the most critical as this range might falsely trigger the ESD circuitry.
2. Over full recommended operating temperature range (see Table 3).

2.9 DDR3 and DDR3L SDRAM controller

This section describes the DC and AC electrical specifications for the DDR3 and DDR3L SDRAM controller interface. Note that the required GV_{DD}(typ) voltage is 1.5 V when interfacing to DDR3 SDRAM and GV_{DD}(typ) voltage is 1.35 V when interfacing to DDR3L SDRAM.

NOTE

When operating at DDR data rates of 1600 MT/s only one dual-ranked module per memory controller is supported.

Table 25. DDR3 and DDR3L SDRAM interface output AC timing specifications (continued)

For recommended operating conditions, see Table 3.

Parameter	Symbol[1]	Min	Max	Unit	Notes
MDQ/MECC/MDM output setup with respect to MDQS	t_{DDKHDS}, t_{DDKLDS}			ps	5
1600 MT/s data rate		200	—		
1333 MT/s data rate		250	—		
1200 MT/s data rate		275	—		
1066 MT/s data rate		300	—		
800 MT/s data rate		375	—		
MDQ/MECC/MDM output hold with respect to MDQS	t_{DDKHDX}, t_{DDKLDX}			ps	5
1600 MT/s data rate		200	—		
1333 MT/s data rate		250	—		
1200 MT/s data rate		275	—		
1066 MT/s data rate		300	—		
800 MT/s data rate		375	—		
MDQS preamble	t_{DDKHMP}	$0.9 \times t_{MCK}$	—	ns	—
MDQS post-amble	t_{DDKHME}	$0.4 \times t_{MCK}$	$0.6 \times t_{MCK}$	ns	—

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{\text{MCK}}$ and MDQS/$\overline{\text{MDQS}}$ referenced measurements are made from the crossing of the two signals.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{\text{MCK}}$, $\overline{\text{MCS}}$, and MDQ/MECC/MDM/MDQS.
4. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the MDQS override bits (called WR_DATA_DELAY) in the TIMING_CFG_2 register. This is typically set to the same delay as in DDR_SDRAM_CLK_CNTL[CLK_ADJUST]. The timing parameters listed in the table assume that these two parameters have been set to the same adjustment value. See the applicable chip reference manual for a description and explanation of the timing modifications enabled by use of these bits.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.

NOTE

For the ADDR/CMD setup and hold specifications in Table 25, it is assumed that the clock control register is set to adjust the memory clocks by ½ applied cycle.

This table provides the DC electrical characteristics for the eSPI interface operating at CV_{DD} = 1.8 V.

Table 28. eSPI DC electrical characteristics (CV_{DD} = 1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	1.25	—	V	1
Input low voltage	V_{IL}	—	0.6	V	1
Input current (V_{IN} = 0 V or V_{IN} = CV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (CV_{DD} = min, I_{OH} = –0.5 mA)	V_{OH}	1.35	—	V	—
Output low voltage (CV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	—	0.4	V	—

Notes:

1. The min $V_{IL}$and max V_{IH} values are based on the respective min and max CV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the CV_{IN} symbol referenced in Section 2.1.2, “Recommended operating conditions.”

2.10.2 eSPI AC timing specifications

This table provides the eSPI input and output AC timing specifications.

Table 29. eSPI AC timing specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol[1]	Min	Max	Unit	Note
SPI_MOSI output—Master data (internal clock) hold time	t_{NIKHOX}	2.36 + ($t_{PLATFORM\_CLK}$ * SPMODE[HO_ADJ])	— —	ns	2, 3
SPI_MOSI output—Master data (internal clock) delay	t_{NIKHOV}	—	5.24 + ($t_{PLATFORM\_CLK}$ * SPMODE[HO_ADJ])	ns	2, 3
SPI_CS outputs—Master data (internal clock) hold time	$t_{NIKHOX2}$	0	—	ns	2
SPI_CS outputs—Master data (internal clock) delay	$t_{NIKHOV2}$	—	6.0	ns	2
eSPI inputs—Master data (internal clock) input setup time	t_{NIIVKH}	5	—	ns	—
eSPI inputs—Master data (internal clock) input hold time	t_{NIIXKH}	0	—	ns	—

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{NIKHOV} symbolizes the NMSI outputs internal timing (NI) for the time t_{SPI} memory clock reference (K) goes from the high state (H) until outputs (O) are valid (V).
2. Output specifications are measured from the 50% level of the rising edge of CLKIN to the 50% level of the signal. Timings are measured at the pin.
3. See the applicable chip reference manual for details on the SPMODE register.

This figure provides the JTAG clock input timing diagram.

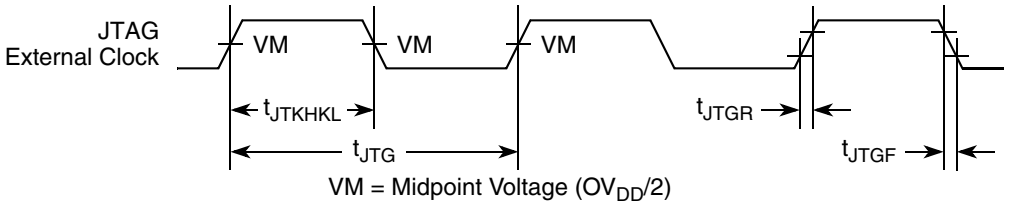


Figure 29. JTAG clock input timing diagram

This figure provides the $\overline{\text{TRST}}$ timing diagram.

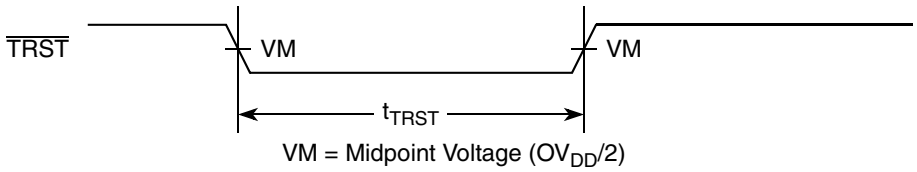


Figure 30. $\overline{\text{TRST}}$ timing diagram

This figure provides the boundary-scan timing diagram.

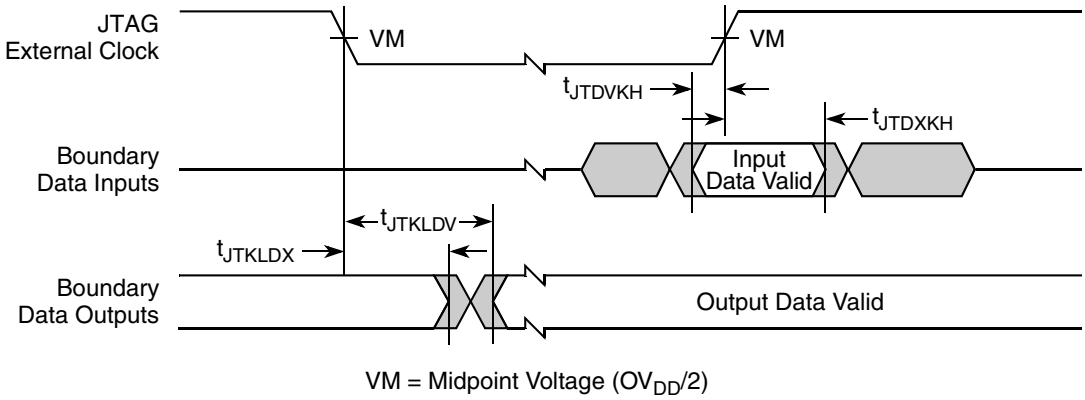


Figure 31. Boundary-scan timing diagram

2.18 I^2C

This section describes the DC and AC electrical characteristics for the I^2C interface.

2.19.2 GPIO AC timing specifications

This table provides the GPIO input and output AC timing specifications.

Table 60. GPIO Input AC timing specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Unit	Notes
GPIO inputs—minimum pulse width	t_{PIWID}	20	ns	1
Trust inputs—minimum pulse width	t_{TIWID}	3	SYSCLK	2

Note:

1. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least t_{PIWID} to ensure proper operation.
2. Trust inputs are asynchronous to any visible clock. Trust inputs are required to be valid for at least t_{TIWID} to ensure proper operation. For low power trust input pin LP_TMP_DETECT, the voltage is VDD_LP and see Table 3.for the voltage requirement.

This figure provides the AC test load for the GPIO.

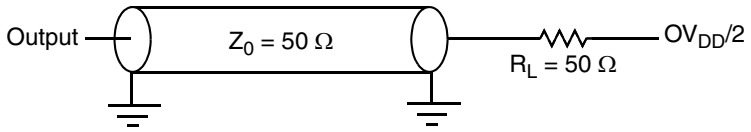


Figure 34. GPIO AC test load

2.20 High-speed serial interfaces (HSSI)

The chip features a serializer/deserializer (SerDes) interface to be used for high-speed serial interconnect applications. The SerDes interface can be used for PCI Express, XAUI, Aurora and SGMII data transfers.

This section describes the common portion of SerDes DC electrical specifications: the DC requirement for SerDes reference clocks. The SerDes data lane's transmitter and receiver reference circuits are also shown.

2.20.1 Signal terms definition

The SerDes utilizes differential signaling to transfer data across the serial link. This section defines terms used in the description and specification of differential signals.

2.20.4 PCI Express

This section describes the clocking dependencies, DC and AC electrical specifications for the PCI Express bus.

2.20.4.1 Clocking dependencies

The ports on the two ends of a link must transmit data at a rate that is within 600 parts per million (ppm) of each other at all times. This is specified to allow bit rate clock sources with a ±300 ppm tolerance.

2.20.4.2 PCI Express clocking requirements for SD_REF_CLK*n* and $\overline{\text{SD\_REF\_CLK}n}$

SerDes banks 1–2 (SD_REF_CLK[1:2] and $\overline{\text{SD\_REF\_CLK[1:2]}}$) may be used for various SerDes PCI Express configurations based on the RCW Configuration field SRDS_PRTCL. PCI Express is not supported on SerDes bank 3.

For more information on these specifications, see Section 2.20.2, "SerDes reference clocks."

2.20.4.3 PCI Express DC physical layer specifications

This section contains the DC specifications for the physical layer of PCI Express on this device.

2.20.4.3.1 PCI Express DC physical layer transmitter specifications

This section discusses the PCI Express DC physical layer transmitter specifications for 2.5 GT/s and 5 GT/s.

This table defines the PCI Express 2.0 (2.5 GT/s) DC specifications for the differential output at all transmitters. The parameters are specified at the component pins.

Table 62. PCI Express 2.0 (2.5 GT/s) differential transmitter output DC specifications (XV_{DD} = 1.5 V or 1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typical	Max	Units	Notes
Differential peak-to-peak output voltage	$V_{TX\text{-}DIFFp\text{-}p}$	800	—	1200	mV	$V_{TX\text{-}DIFFp\text{-}p} = 2 \times \lvert V_{TX\text{-}D+} - V_{TX\text{-}D-} \rvert$ See Note 1.
De-emphasized differential output voltage (ratio)	$V_{TX\text{-}DE\text{-}RATIO}$	3.0	3.5	4.0	dB	Ratio of the $V_{TX\text{-}DIFFp\text{-}p}$ of the second and following bits after a transition divided by the $V_{TX\text{-}DIFFp\text{-}p}$ of the first bit after a transition. See Note 1.
DC differential transmitter impedance	$Z_{TX\text{-}DIFF\text{-}DC}$	80	100	120	Ω	Transmitter DC differential mode low Impedance
Transmitter DC impedance	$Z_{TX\text{-}DC}$	40	50	60	Ω	Required transmitter D+ as well as D– DC Impedance during all states

Note:
1. Measured at the package pins with a test load of 50Ω to GND on each pin.

This table defines the AC specifications for the PCI Express 2.0 (5 GT/s) differential input at all receivers (RXs). The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 69. PCI Express 2.0 (5 GT/s) differential receiver Input AC specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typ	Max	Units	Notes
Unit Interval	UI	199.94	200.00	200.06	ps	Each UI is 400 ps ±300 ppm. UI does not account for spread spectrum clock dictated variations. See Note 1.
Max receiver inherent timing error	$T_{RX-TJ-CC}$	—	—	0.4	UI	The maximum inherent total timing error for common RefClk receiver architecture
Maximum time between the jitter median and maximum deviation from the median	$T_{RX-TJ-DC}$	—	—	0.34	UI	Max receiver inherent total timing error
Max receiver inherent deterministic timing error	$T_{RX-DJ-DD-CC}$	—	—	0.30	UI	The maximum inherent deterministic timing error for common RefClk receiver architecture
Max receiver inherent deterministic timing error	$T_{RX-DJ-DD-DC}$	—	—	0.24	UI	The maximum inherent deterministic timing error for common RefClk receiver architecture

Note:
1. No test load is necessarily associated with this value.

2.20.4.6 Test and measurement load

The AC timing and voltage parameters must be verified at the measurement point. The package pins of the device must be connected to the test/measurement load within 0.2 inches of that load, as shown in Figure 43.

NOTE

The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/board routing may benefit from D+ and D– not being exactly matched in length at the package pin boundary. If the vendor does not explicitly state where the measurement point is located, the measurement point is assumed to be the D+ and D– package pins.

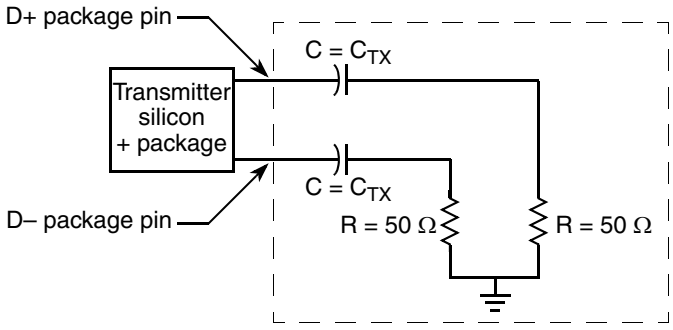


Figure 43. Test/Measurement load

2.20.6 Aurora

This section describes the Aurora clocking requirements and AC and DC electrical characteristics.

2.20.6.1 Aurora DC electrical characteristics

This section describes the DC electrical characteristics for Aurora.

2.20.6.1.1 Aurora DC clocking requirements for SD_REF_CLK*n* and $\overline{\text{SD\_REF\_CLK}n}$

Only SerDes bank 1 (SD_REF_CLK1 and $\overline{\text{SD\_REF\_CLK1}}$) may be used for SerDes Aurora configurations based on the RCW Configuration field SRDS_PRTCL. Aurora is not supported on SerDes banks 2-3.

For more information on these specifications, see Section 2.20.2, "SerDes reference clocks."

2.20.6.1.2 Aurora transmitter DC electrical characteristics

This table defines the Aurora transmitter DC electrical characteristics.

Table 75. Aurora transmitter DC electrical characteristics (XV_{DD} = 1.5 V or 1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typical	Max	Unit
Differential output voltage	V_{DIFFPP}	800	—	1600	mV p-p

2.20.6.1.3 Aurora receiver DC electrical characteristics

This table defines the Aurora receiver DC electrical characteristics for Aurora.

Table 76. Aurora receiver DC electrical characteristics (XV_{DD} = 1.5 V or 1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Differential input voltage	V_{IN}	120	900	1200	mV p-p	1

Note:

1. Measured at receiver

2.20.6.2 Aurora AC timing specifications

This section describes the AC timing specifications for Aurora.

2.20.6.2.1 Aurora AC clocking requirements for SD_REF_CLK*n* and $\overline{\text{SD\_REF\_CLK}n}$

Only SerDes bank 1 (SD_REF_CLK1 and $\overline{\text{SD\_REF\_CLK1}}$) may be used for SerDes Aurora configurations based on the RCW Configuration field SRDS_PRTCL. Aurora is not supported on SerDes banks 2–3.

Please note that the XAUI clock requirements for SD_REF_CLK*n* and $\overline{\text{SD\_REF\_CLK}n}$ are intended to be used within the clocking guidelines specified by either Section 2.20.2.3, "AC requirements for SerDes reference clocks" or Section 2.20.7.2.1, "AC requirements for SATA REF_CLK."

This figure shows the reference clock timing waveform.

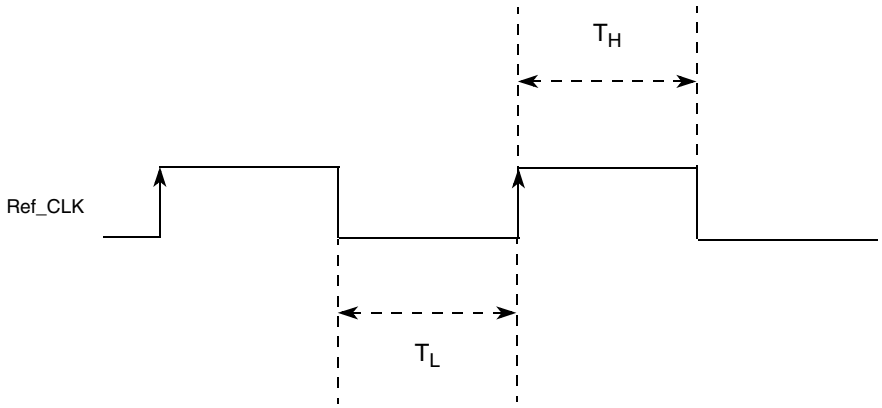


Figure 45. Reference clock timing waveform

2.20.7.3 AC transmitter Output Characteristics

This table provides the differential transmitter output AC characteristics for the SATA interface at Gen1i or 1.5 Gbits/s transmission. The AC timing specifications do not include RefClk jitter.

Table 84. Gen1i/1.5 G transmitter AC specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typ	Max	Units	Notes
Channel speed	t_{CH_SPEED}	—	1.5	—	Gbps	—
Unit Interval	T_{UI}	666.4333	666.6667	670.2333	ps	—
Total jitter data-data 5 UI	$U_{SATA\_TXTJ5UI}$	—	—	0.355	UI p-p	1
Total jitter, data-data 250 UI	$U_{SATA\_TXTJ250UI}$	—	—	0.47	UI p-p	1
Deterministic jitter, data-data 5 UI	$U_{SATA\_TXDJ5UI}$	—	—	0.175	UI p-p	1
Deterministic jitter, data-data 250 UI	$U_{SATA\_TXDJ250UI}$	—	—	0.22	UI p-p	1

Note:

1. Measured at transmitter output pins peak to peak phase variation, random data pattern

This table provides the differential transmitter output AC characteristics for the SATA interface at Gen2i or 3.0 Gbits/s transmission. The AC timing specifications do not include RefClk jitter.

Table 85. Gen 2i/3 G transmitter AC specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typ	Max	Units	Notes
Channel speed	t_{CH_SPEED}	—	3.0	—	Gbps	—
Unit Interval	T_{UI}	333.2167	333.3333	335.1167	ps	—
Total jitter $f_{C3dB} = f_{BAUD} \div 10$	$U_{SATA\_TXTJfB/10}$	—	—	0.3	UI p-p	1
Total jitter $f_{C3dB} = f_{BAUD} \div 500$	$U_{SATA\_TXTJfB/500}$	—	—	0.37	UI p-p	1
Total jitter $f_{C3dB} = f_{BAUD} \div 1667$	$U_{SATA\_TXTJfB/1667}$	—	—	0.55	UI p-p	1

Table 85. Gen 2i/3 G transmitter AC specifications (continued)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typ	Max	Units	Notes
Deterministic jitter, $f_{C3dB} = f_{BAUD} \div 10$	$U_{SATA\_TXDJfB/10}$	—	—	0.17	UI p-p	1
Deterministic jitter, $f_{C3dB} = f_{BAUD} \div 500$	$U_{SATA\_TXDJfB/500}$	—	—	0.19	UI p-p	1
Deterministic jitter, $f_{C3dB} = f_{BAUD} \div 1667$	$U_{SATA\_TXDJfB/1667}$	—	—	0.35	UI p-p	1

Note:

1. Measured at transmitter output pins peak-to-peak phase variation, random data pattern

2.20.7.4 AC differential receiver Input characteristics

This table provides the Gen1i or 1.5 Gbits/s differential receiver input AC characteristics for the SATA interface. The AC timing specifications do not include RefClk jitter.

Table 86. Gen 1i/1.5G receiver AC specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typical	Max	Units	Notes
Unit Interval	T_{UI}	666.4333	666.6667	670.2333	ps	—
Total jitter data-data 5 UI	$U_{SATA\_TXTJ5UI}$	—	—	0.43	UI p-p	1
Total jitter, data-data 250 UI	$U_{SATA\_TXTJ250UI}$	—	—	0.60	UI p-p	1
Deterministic jitter, data-data 5 UI	$U_{SATA\_TXDJ5UI}$	—	—	0.25	UI p-p	1
Deterministic jitter, data-data 250 UI	$U_{SATA\_TXDJ250UI}$	—	—	0.35	UI p-p	1

Note:

1. Measured at receiver

This table provides the differential receiver input AC characteristics for the SATA interface at Gen2i or 3.0 Gbits/s transmission. The AC timing specifications do not include RefClk jitter.

Table 87. Gen 2i/3G receiver AC specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typical	Max	Units	Notes
Unit Interval	T_{UI}	333.2167	333.3333	335.1167	ps	—
Total jitter $f_{C3dB} = f_{BAUD} \div 10$	$U_{SATA\_TXTJfB/10}$	—	—	0.46	UI p-p	1
Total jitter $f_{C3dB} = f_{BAUD} \div 500$	$U_{SATA\_TXTJfB/500}$	—	—	0.60	UI p-p	1
Total jitter $f_{C3dB} = f_{BAUD} \div 1667$	$U_{SATA\_TXTJfB/1667}$	—	—	0.65	UI p-p	1

Table 87. Gen 2i/3G receiver AC specifications (continued)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typical	Max	Units	Notes
Deterministic jitter, $f_{C3dB} = f_{BAUD} \div 10$	$U_{SATA\_TXDJfB/10}$	—	—	0.35	UI p-p	1
Deterministic jitter, $f_{C3dB} = f_{BAUD} \div 500$	$U_{SATA\_TXDJfB/500}$	—	—	0.42	UI p-p	1
Deterministic jitter, $f_{C3dB} = f_{BAUD} \div 1667$	$U_{SATA\_TXDJfB/1667}$	—	—	0.35	UI p-p	1

Note:

1. Measured at receiver

2.20.8 SGMII interface

Each SGMII port features a 4-wire AC-coupled serial link from the SerDes interface of the chip, as shown in Figure 46, where C_{TX} is the external (on board) AC-coupled capacitor. Each output pin of the SerDes transmitter differential pair features 50-Ω output impedance. Each input of the SerDes receiver differential pair features 50-Ω on-die termination to XGND. The reference circuit of the SerDes transmitter and receiver is shown in Figure 42.

2.20.8.0.1 SGMII clocking requirements for SD_REF_CLK*n* and $\overline{\text{SD\_REF\_CLK}n}$

When operating in SGMII mode, the EC_GTX_CLK125 clock is not required for this port. Instead, a SerDes reference clock is required on SD_REF_CLK[1:3] and $\overline{\text{SD\_REF\_CLK}[1:3]}$ pins. SerDes banks 1-3 may be used for SerDes SGMII configurations based on the RCW Configuration field SRDS_PRTCL.

For more information on these specifications, see Section 2.20.2, "SerDes reference clocks."

2.20.8.1 SGMII DC electrical characteristics

This section discusses the electrical characteristics for the SGMII interface.

2.20.8.1.1 SGMII transmit DC timing specifications

This table describe the SGMII SerDes transmitter and receiver AC-coupled DC electrical characteristics for 1.25 GBaud. Transmitter DC characteristics are measured at the transmitter outputs (SD_TX*n* and $\overline{\text{SD\_TX}n}$) as shown in Figure 47.

Table 88. SGMII DC transmitter electrical characteristics (XV_{DD} = 1.5 V or 1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Output high voltage	V_{OH}	—	—	1.5 x $\lvert V_{OD}\rvert_{-max}$	mV	1
Output low voltage	V_{OL}	$\lvert V_{OD}\rvert_{-min}/2$	—	—	mV	1

2.20.8.2.1 SGMII transmit AC timing specifications

This table provides the SGMII transmit AC timing specifications. A source synchronous clock is not supported. The AC timing specifications do not include RefClk jitter.

Table 92. SGMII transmit AC timing specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Deterministic jitter	JD	—	—	0.17	UI p-p	—
Total jitter	JT	—	—	0.35	UI p-p	1
Unit Interval: 1.25 GBaud	UI	800 – 100 ppm	800	800 + 100 ppm	ps	—
Unit Interval: 3.125 GBaud	UI	320 – 100 ppm	320	320 + 100 ppm	ps	—
AC coupling capacitor	C_{TX}	10	—	200	nF	2

Notes:

1. See Figure 44 for single frequency sinusoidal jitter measurements.
2. The external AC coupling capacitor is required. It is recommended that it be placed near the device transmitter outputs.

2.20.8.2.2 SGMII AC measurement details

Transmitter and receiver AC characteristics are measured at the transmitter outputs (SD_TX*n* and $\overline{\text{SD\_TX}n}$) or at the receiver inputs (SD_RX*n* and $\overline{\text{SD\_RX}n}$) respectively, as depicted in this figure.

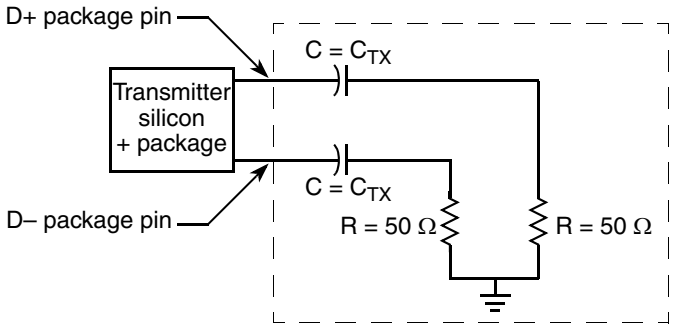


Figure 48. SGMII AC test/measurement load

2.20.8.2.3 SGMII receiver AC timing specification

This table provides the SGMII receiver AC timing specifications. The AC timing specifications do not include RefClk jitter. Source synchronous clocking is not supported. Clock is recovered from the data.

Table 93. SGMII receive AC timing specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Deterministic jitter tolerance	JD	0.37	—	—	UI p-p	1, 2
Combined deterministic and random jitter tolerance	JDR	0.55	—	—	UI p-p	1, 2
Total jitter tolerance	JT	0.65	—	—	UI p-p	1,2, 3

Each circuit should be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of the footprint, without the inductance of vias.

Figure 51 shows the PLL power supply filter circuit.

Where:

R = 5 Ω ± 5%
C1 = 10µF ± 10%, 0603, X5R, with ESL ≤ 0.5 nH
C2 = 1.0 µF ± 10%, 0402, X5R, with ESL ≤ 0.5 nH

NOTE

A higher capacitance value for C2 may be used to improve the filter as long as the other C2 parameters do not change (0402 body, X5R, ESL ≤ 0.5 nH).

Voltage for AV_{DD} is defined at the PLL supply filter and not the pin of AV_{DD}.

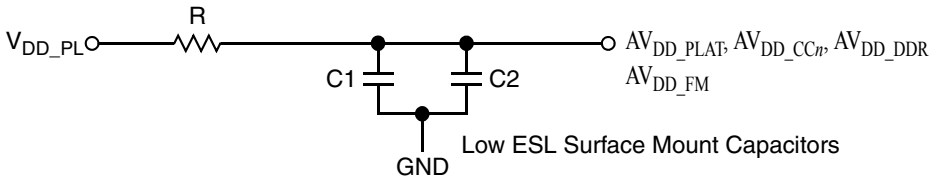


Figure 51. PLL power supply filter circuit

The AV_{DD_SRDSn} signals provides power for the analog portions of the SerDes PLL. To ensure stability of the internal clock, the power supplied to the PLL is filtered using a circuit similar to the one shown in following Figure 52. For maximum effectiveness, the filter circuit is placed as closely as possible to the AV_{DD_SRDSn} balls to ensure it filters out as much noise as possible. The ground connection should be near the AV_{DD_SRDSn} balls. The 0.003-µF capacitor is closest to the balls, followed by two 2.2-µF capacitors, and finally the 1-Ω resistor to the board supply plane. The capacitors are connected from AV_{DD_SRDSn} to the ground plane. Use ceramic chip capacitors with the highest possible self-resonant frequency. All traces should be kept short, wide, and direct.

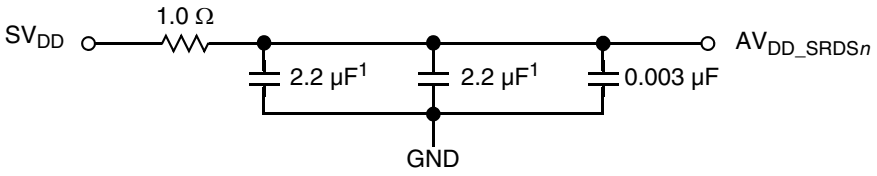


Figure 52. SerDes PLL power supply filter circuit

Note the following:

- AV_{DD_SRDSn} should be a filtered version of SV_{DD}.
- Signals on the SerDes interface are fed from the XV_{DD} power plane.
- Voltage for AV_{DD_SRDSn} is defined at the PLL supply filter and not the pin of AV_{DD_SRDSn}.
- An 0805 sized capacitor is recommended for system initial bring-up.

3.3.2 XV_{DD} power supply filtering

XV_{DD} may be supplied by a linear regulator or sourced by a filtered 1.5 V or 1.8 V voltage source. Systems may design in both options to allow flexibility to address system noise dependencies.

An example solution for XV_{DD} filtering, where 1.5 V or 1.8 V is sourced from voltage source (for example, GV_{DD} at 1.5 V when using DDR3, or CV_{DD} at 1.8 V), is illustrated in Figure 53. The component values in this example filter is system

3.6.3 Guidelines for high-speed interface termination

This section provides the guidelines for high-speed interface termination when the SerDes interface is entirely unused or when it is partly unused.

3.6.3.1 SerDes interface entirely unused

If the high-speed SerDes interface is not used at all, the unused pin should be terminated as described in this section.

The following pins must be left unconnected:

- SD_TX[19:0]
- $\overline{\text{SD\_TX}}$[19:0]
- SD_IMP_CAL_RX
- SD_IMP_CAL_TX
- SD1_IMP_CAL_RX
- SD1_IMP_CAL_TX

The following pins must be connected to SGND:

- SD_RX[19:0]
- $\overline{\text{SD\_RX}}$[19:0]
- SD_REF_CLK1, SD_REF_CLK2, SD_REF_CLK3, SD_REF_CLK4
- $\overline{\text{SD\_REF\_CLK1}}$, $\overline{\text{SD\_REF\_CLK2}}$, $\overline{\text{SD\_REF\_CLK3}}$, $\overline{\text{SD\_REF\_CLK4}}$

The RCW configuration fields SRDS_LPD_B1, SRDS_LPD_B2, SRDS_LPD_B3, and SRDS_LPD_B4, all bits must be set to power down all the lanes in each bank.

The RCW configuration field SRDS_EN may be cleared to power down the SerDes block for power saving. Setting RCW[SRDS_EN_S1] = 0 powers down the PLLs of banks 1 to 3; RCW[SRDS_EN_S2]=0 powers down the PLL of bank 4.

Additionally, software may configure SRDSB*n*RSTCTL[SDRD] = 1 for the unused banks to power down the SerDes bank PLLs to save power.

Note that both SV_{DD} and XV_{DD} must remain powered.

3.6.3.2 SerDes interface partly unused

If only part of the high speed SerDes interface pins are used, the remaining high-speed serial I/O pins should be terminated as described in this section.

The following pins must be left unconnected:

- SD_TX[*n*]
- $\overline{\text{SD\_TX}}$[*n*]

The following unused pins must be connected to SGND:

- SD_RX[*n*]
- $\overline{\text{SD\_RX}}$[*n*]
- SD_REF_CLK1, $\overline{\text{SD\_REF\_CLK1}}$ (If entire SerDes bank 1 unused)
- SD_REF_CLK2, $\overline{\text{SD\_REF\_CLK2}}$ (If entire SerDes bank 2 unused)
- SD_REF_CLK3, $\overline{\text{SD\_REF\_CLK3}}$ (If entire SerDes bank 3 unused)
- SD_REF_CLK4, $\overline{\text{SD\_REF\_CLK4}}$ (If entire SerDes bank 4 unused)