Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	PowerPC e5500
Number of Cores/Bus Width	2 Core, 64-Bit
Speed	1.8GHz
Co-Processors/DSP	-
RAM Controllers	DDR3, DDR3L
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	1Gbps (10), 10Gbps (2)
SATA	SATA 3Gbps (2)
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.0V, 1.1V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	Boot Security, Cryptography, Secure Fusebox, Secure Debug, Tamper Detection, Volatile key Storage
Package / Case	1295-BBGA, FCBGA
Supplier Device Package	1295-FCPBGA (37.5x37.5)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=p5021nxe7tmc

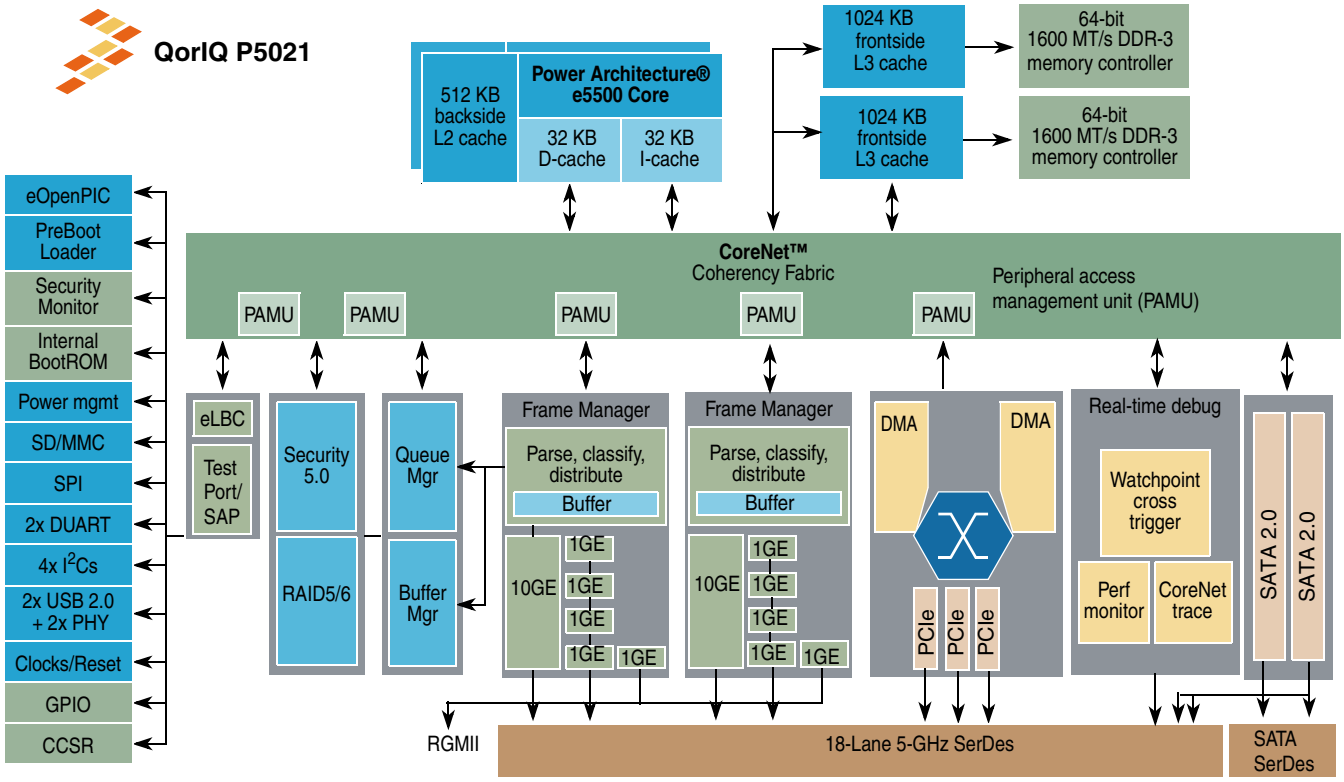


Figure 1. P5021 block diagram

1 Pin assignments and reset states

1.1 1295 FC-PBGA ball layout diagrams

These figures show the FC-PBGA ball map diagrams.

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
$\overline{\text{LCS4}}$	Chip Selects	D22	O	BV_{DD}	5
$\overline{\text{LCS5}}$	Chip Selects	B23	O	BV_{DD}	5
$\overline{\text{LCS6}}$	Chip Selects	F24	O	BV_{DD}	5
$\overline{\text{LCS7}}$	Chip Selects	G26	O	BV_{DD}	5
$\overline{\text{LWE0}}$	Write Enable	D24	O	BV_{DD}	—
$\overline{\text{LWE1}}$	Write Enable	A24	O	BV_{DD}	—
$\overline{\text{LWE2}}$	Write Enable	J16	O	BV_{DD}	—
$\overline{\text{LWE3}}$	Write Enable	K15	O	BV_{DD}	—
LBCTL	Buffer Control	C22	O	BV_{DD}	—
LALE	Address Latch Enable	A23	I/O	BV_{DD}	—
LGPL0/LFCLE	UPM General Purpose Line 0/ LFCLE—FCM	B25	O	BV_{DD}	3, 4
LGPL1/LFALE	UPM General Purpose Line 1/ LFALE—FCM	E25	O	BV_{DD}	3, 4
LGPL2/$\overline{\text{LOE}}$/$\overline{\text{LFRE}}$	UPM General Purpose Line 2/ LOE_B—Output Enable	D25	O	BV_{DD}	3, 4
LGPL3/$\overline{\text{LFWP}}$	UPM General Purpose LIne 3/ LFWP_B—FCM	H26	O	BV_{DD}	3, 4
LGPL4/$\overline{\text{LGTA}}$/LUPWAIT/LPBSE	UPM General Purpose Line 4/ LGTA_B—FCM	C25	I/O	BV_{DD}	39
LGPL5	UPM General Purpose Line 5 / Amux	E26	O	BV_{DD}	3, 4
LCLK0	Local Bus Clock	C24	O	BV_{DD}	—
LCLK1	Local Bus Clock	C23	O	BV_{DD}	—
DMA					
$\overline{\text{DMA1\_DREQ0}}$/GPIO18	DMA1 Channel 0 Request	AP21	I	OV_{DD}	26
$\overline{\text{DMA1\_DACK0}}$/GPIO19	DMA1 Channel 0 Acknowledge	AL19	O	OV_{DD}	26
$\overline{\text{DMA1\_DDONE0}}$	DMA1 Channel 0 Done	AN21	O	OV_{DD}	27
$\overline{\text{DMA2\_DREQ0}}$/GPIO20/ALT_MDVAL	DMA2 Channel 0 Request	AJ20	I	OV_{DD}	26
$\overline{\text{DMA2\_DACK0}}$/$\overline{\text{EVT7}}$/ALT_MDSRCID0	DMA2 Channel 0 Acknowledge	AG19	O	OV_{DD}	26
$\overline{\text{DMA2\_DDONE0}}$/$\overline{\text{EVT8}}$/ALT_MDSRCID1	DMA2 Channel 0 Done	AP20	O	OV_{DD}	26
USB Port 1					
USB1_UDP	USB1 PHY Data Plus	AT27	I/O	USB_V_{DD}_3P3	—
USB1_UDM	USB1 PHY Data Minus	AT26	I/O	USB_V_{DD}_3P3	—
USB1_VBUS_CLMP	USB1 PHY VBUS Divided Signal	AK25	I	USB_V_{DD}_3P3	38

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GND	Ground	Y17	—	—	—
GND	Ground	AB17	—	—	—
GND	Ground	AD17	—	—	—
GND	Ground	AF17	—	—	—
GND	Ground	W18	—	—	—
GND	Ground	AC18	—	—	—
GND	Ground	AA18	—	—	—
GND	Ground	AE18	—	—	—
GND	Ground	AF19	—	—	—
GND	Ground	AD19	—	—	—
GND	Ground	AB19	—	—	—
GND	Ground	Y19	—	—	—
GND	Ground	V19	—	—	—
GND	Ground	T19	—	—	—
GND	Ground	P19	—	—	—
GND	Ground	M19	—	—	—
GND	Ground	N20	—	—	—
GND	Ground	R20	—	—	—
GND	Ground	U20	—	—	—
GND	Ground	AE20	—	—	—
GND	Ground	AA20	—	—	—
GND	Ground	AC20	—	—	—
GND	Ground	W20	—	—	—
GND	Ground	AF21	—	—	—
GND	Ground	AD21	—	—	—
GND	Ground	AB21	—	—	—
GND	Ground	Y21	—	—	—
GND	Ground	V21	—	—	—
GND	Ground	T21	—	—	—
GND	Ground	P21	—	—	—
GND	Ground	M21	—	—	—
GND	Ground	AE22	—	—	—
GND	Ground	AC22	—	—	—
GND	Ground	AA22	—	—	—

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GVDD	DDR Supply	W10	—	GV_{DD}	—
GVDD	DDR Supply	AA6	—	GV_{DD}	—
GVDD	DDR Supply	AR2	—	GV_{DD}	—
GVDD	DDR Supply	Y2	—	GV_{DD}	—
GVDD	DDR Supply	Y8	—	GV_{DD}	—
GVDD	DDR Supply	AC2	—	GV_{DD}	—
GVDD	DDR Supply	AD6	—	GV_{DD}	—
GVDD	DDR Supply	AE10	—	GV_{DD}	—
GVDD	DDR Supply	AE4	—	GV_{DD}	—
GVDD	DDR Supply	AF2	—	GV_{DD}	—
GVDD	DDR Supply	AF8	—	GV_{DD}	—
GVDD	DDR Supply	AB4	—	GV_{DD}	—
GVDD	DDR Supply	AB10	—	GV_{DD}	—
GVDD	DDR Supply	AC8	—	GV_{DD}	—
GVDD	DDR Supply	AG6	—	GV_{DD}	—
GVDD	DDR Supply	AH10	—	GV_{DD}	—
GVDD	DDR Supply	AH4	—	GV_{DD}	—
GVDD	DDR Supply	AJ2	—	GV_{DD}	—
GVDD	DDR Supply	AJ8	—	GV_{DD}	—
GVDD	DDR Supply	AR14	—	GV_{DD}	—
GVDD	DDR Supply	AK6	—	GV_{DD}	—
GVDD	DDR Supply	AL4	—	GV_{DD}	—
GVDD	DDR Supply	AL10	—	GV_{DD}	—
GVDD	DDR Supply	AM2	—	GV_{DD}	—
GVDD	DDR Supply	AM8	—	GV_{DD}	—
GVDD	DDR Supply	AP10	—	GV_{DD}	—
GVDD	DDR Supply	AN12	—	GV_{DD}	—
GVDD	DDR Supply	AN6	—	GV_{DD}	—
GVDD	DDR Supply	AP4	—	GV_{DD}	—
BVDD	Local Bus Supply	B24	—	BV_{DD}	—
BVDD	Local Bus Supply	K22	—	BV_{DD}	—
BVDD	Local Bus Supply	F20	—	BV_{DD}	—
BVDD	Local Bus Supply	F26	—	BV_{DD}	—
BVDD	Local Bus Supply	E24	—	BV_{DD}	—

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
USB2_VDD_1P8_DECAP	USB2 PHY 1.8V Output to External Decap	AL27	—	—	37
No Connection Pins					
NC_A27	No Connection	A27	—	—	11
NC_B26	No Connection	B26	—	—	11
NC_C19	No Connection	C19	—	—	11
NC_C20	No Connection	C20	—	—	11
NC_C26	No Connection	C26	—	—	11
NC_C27	No Connection	C27	—	—	11
NC_D18	No Connection	D18	—	—	11
NC_D27	No Connection	D27	—	—	11
NC_E16	No Connection	E16	—	—	11
NC_E27	No Connection	E27	—	—	11
NC_G27	No Connection	G27	—	—	11
NC_H12	No Connection	H12	—	—	11
NC_H13	No Connection	H13	—	—	11
NC_H15	No Connection	H15	—	—	11
NC_H27	No Connection	H27	—	—	11
NC_J11	No Connection	J11	—	—	11
NC_J13	No Connection	J13	—	—	11
NC_J14	No Connection	J14	—	—	11
NC_K11	No Connection	K11	—	—	11
NC_K12	No Connection	K12	—	—	11
NC_K13	No Connection	K13	—	—	11
NC_K14	No Connection	K14	—	—	11
NC_W27	No Connection	W27	—	—	11
NC_AG15	No Connection	AG15	—	—	11
Reserved Pins					
Reserve_A21	—	A21	—	—	41
Reserve_A25	—	A25	—	—	11
Reserve_C32	—	C32	—	—	11
Reserve_D32	—	D32	—	—	11
Reserve_F1	—	F1	—	—	11
Reserve_F2	—	F2	—	—	11

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
Reserve_G1	—	G1	—	—	11
Reserve_G2	—	G2	—	—	11
Reserve_L28	—	L28	—	GND	21
Reserve_M28	—	M28	—	GND	21
Reserve_N28	—	N28	—	GND	21
Reserve_P28	—	P28	—	GND	21
Reserve_U32	—	U32	—	—	11
Reserve_U35	—	U35	—	—	11
Reserve_AD33	—	AD33	—	—	11
Reserve_AD34	—	AD34	—	—	11
Reserve_AG11	—	AG11	—	GND	21
Reserve_AG12	—	AG12	—	GND	21
Reserve_AG26	—	AG26	—	—	11
Reserve_AG29	—	AG29	—	—	11
Reserve_AH11	—	AH11	—	GND	21
Reserve_AH12	—	AH12	—	GND	21
Reserve_AH30	—	AH30	—	—	11
Reserve_AK1	—	AK1	—	—	11
Reserve_AK2	—	AK2	—	—	11
Reserve_AL1	—	AL1	—	—	11
Reserve_AL2	—	AL2	—	—	11

Table 3. Recommended operating conditions (continued)

Parameter		Symbol	Recommended value	Unit	Notes
Input voltage	DDR3 and DDR3L DRAM signals	MV_{IN}	GND to GV_{DD}	V	7
	DDR3 and DDR3L DRAM reference	MV_{REF}	$GV_{DD}/2$ ± 1%	V	7
	Ethernet signals (except EMI2)	LV_{IN}	GND to LV_{DD}	V	7
	eSPI, eSHDC	CV_{IN}	GND to CV_{DD}	V	7
	Enhanced local bus signals	BV_{IN}	GND to BV_{DD}	V	7
	DUART, I^2C, DMA, MPIC, GPIO, system control and power management, clocking, debug, I/O voltage select, and JTAG I/O voltage	OV_{IN}	GND to OV_{DD}	V	7
	SerDes signals	SV_{IN}	GND to SV_{DD}	V	7
	USB PHY Transceiver signals	$USB\_V_{IN}\_3P3$	GND to $USB\_V_{DD}\_3P3$	V	7
	Ethernet Management interface 2 (EMI2) signals	—	GND to 1.2V	V	4, 7
Operating Temperature range	Normal Operation	T_A, T_J	T_A = 0 (min) to T_J = 105 (max) (90 (max) core frequency > 2000 MHz)	°C	—
	Extended Temperature	T_A, T_J	T_A = -40 (min) to T_J = 105 (max)	°C	—
	Secure Boot Fuse Programming	T_A, T_J	T_A = 0 (min) to T_J = 70 (max)	°C	2

Notes:

1. V_{DD_PL} voltage must not exceed V_{DD_CA}.
2. POV_{DD} must be supplied 1.5 V and the chip must operate in the specified fuse programming temperature range only during secure boot fuse programming. For all other operating conditions, POV_{DD} must be tied to GND, subject to the power sequencing constraints shown in Section 2.2, "Power-up sequencing."
3. Selecting RGMII limits LV_{DD} to 2.5V.
4. Ethernet Management interface 2 pins function as open drain I/Os. The interface shall conform to 1.2 V nominal voltage levels. LV_{DD} must be powered to use this interface.6. Supply voltage specified at the voltage sense pin. Voltage input pins must be regulated to provide specified voltage at the sense pin.
7. All input signals must increase/decrease monotonically throughout the entire rise/fall duration.

WARNING

Only 100,000 POR cycles are permitted per lifetime of a device.

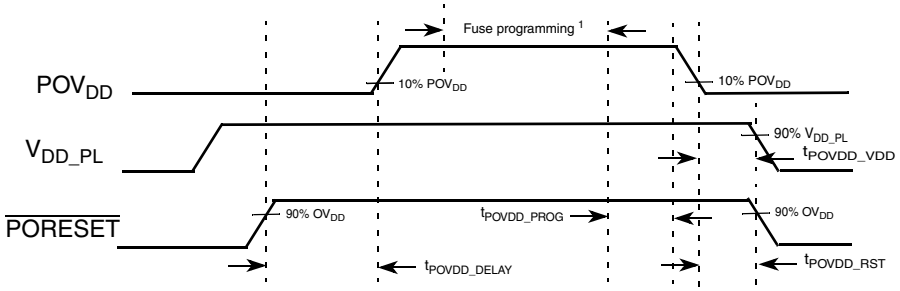
WARNING

While VDD is ramping, current may be supplied from VDD through the P5021 to GVDD. Nevertheless, GVDD from an external supply should follow the sequencing described above.

All supplies must be at their stable values within 75 ms.

Items on the same line have no ordering requirement with respect to one another. Items on separate lines must be ordered sequentially such that voltage rails on a previous step must reach 90% of their value before the voltage rails on the current step reach 10% of theirs.

This figure provides the POV_{DD} timing diagram.



NOTE: POV_{DD} must be stable at 1.5 V prior to initiating fuse programming.

Figure 8. POV_{DD} timing diagram

This table provides information on the power-down and power-up sequence parameters for POV_{DD}.

Table 5. POV_{DD} timing [5]

Driver type	Min	Max	Unit	Notes
t_{POVDD_DELAY}	100	—	SYSCLKs	1
t_{POVDD_PROG}	0	—	µs	2
t_{POVDD_VDD}	0	—	µs	3
t_{POVDD_RST}	0	—	µs	4

Notes:

1. Delay required from the negation of $\overline{\text{PORESET}}$ to driving POV_{DD} ramp up. Delay measured from $\overline{\text{PORESET}}$ negation at 90% OV_{DD} to 10% POV_{DD} ramp up.
2. Delay required from fuse programming finished to POV_{DD} ramp down start. Fuse programming must complete while POV_{DD} is stable at 1.5 V. No activity other than that required for secure boot fuse programming is permitted while POV_{DD} driven to any voltage above GND, including the reading of the fuse block. The reading of the fuse block may only occur while POV_{DD} = GND. After fuse programming is completed, it is required to return POV_{DD} = GND.
3. Delay required from POV_{DD} ramp down complete to V_{DD_PL} ramp down start. POV_{DD} must be grounded to minimum 10% POV_{DD} before V_{DD_PL} is at 90% V_{DD}.
4. Delay required from POV_{DD} ramp down complete to $\overline{\text{PORESET}}$ assertion. POV_{DD} must be grounded to minimum 10% POV_{DD} before $\overline{\text{PORESET}}$ assertion reaches 90% OV_{DD}.
5. Only two secure boot fuse programming events are permitted per lifetime of a device.

To guarantee MCKE low during power up, the above sequencing for GV_{DD} is required. If there is no concern about any of the DDR signals being in an indeterminate state during power up, the sequencing for GV_{DD} is not required.

WARNING

Incorrect voltage select settings can lead to irreversible device damage. See Section 3.2, "Supply power default setting."

NOTE

From a system standpoint, if any of the I/O power supplies ramp prior to the V_{DD_CA}, or V_{DD_PL} supplies, the I/Os associated with that I/O supply may drive a logic one or zero during power-up, and extra current may be drawn by the device.

2.3 Power-down requirements

The power-down cycle must complete such that power supply values are below 0.4 V before a new power-up cycle can be started.

If performing secure boot fuse programming per Section 2.2, "Power-up sequencing," it is required that POV_{DD} = GND before the system is power cycled ($\overline{\text{PORESET}}$ assertion) or powered down (V_{DD_PL} ramp down) per the required timing specified in Table 5.

V_{DD_PL} and USB_V_{DD}_1P0 must be ramped down simultaneously. USB_V_{DD}_1P8_DECAP should starts ramping down only after USB_V_{DD}_3P3 is below 1.65 V.

2.4 Power characteristics

This table shows the power dissipations of the V_{DD_CA}, SV_{DD}, and V_{DD_PL} supply for various operating platform clock frequencies versus the core and DDR clock frequencies for the chip.

Table 6. Power dissipation

Power Mode	Core freq (MHz)	Plat freq (MHz)	DDR data rate (MHz)	FM freq (MHz)	V_{DD_PL}, SV_{DD} (V)	V_{DD_CA} (V)	Junction temp (°C)	Core and platform power[1] (W)	V_{DD_PL} power (W)	V_{DD_CA} power (W)	SV_{DD} power (W)	Note
Typical	2200	800	1600	600	1.0	1.2	65	23	—	—	—	—
Thermal							90	33	—	—	—	—
Maximum								34	17	15	15	2.2
Typical	2000	700	1333	600	1.0	1.1	65	21	—	—	—	—
Thermal							105	30	—	—	—	—
Maximum								31	16	13	13	2.2

Table 19. DDR3L SDRAM interface DC electrical characteristics (GV_{DD} = 1.35 V)[1] (continued)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
I/O leakage current	I_{OZ}	–50	50	μA	6
Output high current (V_{OUT} = 0.641 V)	I_{OH}	—	–23.3	mA	7, 8
Output low current (V_{OUT} = 0.641 V)	I_{OL}	23.3	—	mA	7, 8

Notes:

1. GV_{DD} is expected to be within 50 mV of the DRAM's voltage supply at all times. The DRAM's and memory controller's voltage supply may or may not be from the same source.
2. MV_{REF} is expected to be equal to 0.5 × GV_{DD} and to track GV_{DD} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed the MV_{REF} DC level by more than ±1% of the DC value (that is, ±13.5 mV).
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made, and it is expected to be equal to MV_{REF} with a min value of MV_{REF} – 0.04 and a max value of MV_{REF} + 0.04. V_{TT} should track variations in the DC level of MV_{REF}
4. The voltage regulator for MV_{REF} must meet the specifications stated in Table 21.
5. Input capacitance load for DQ, DQS, and $\overline{DQS}$ are available in the IBIS models.
6. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GV_{DD}.
7. Refer to the IBIS model for the complete output IV curve characteristics.
8. I_{OH} and I_{OL} are measured at GV_{DD} = 1.283 V

This table provides the DDR controller interface capacitance for DDR3 and DDR3L.

Table 20. DDR3 and DDR3L SDRAM Capacitance

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS, $\overline{DQS}$	C_{IO}	6	8	pF	1, 2
Delta input/output capacitance: DQ, DQS, $\overline{DQS}$	C_{DIO}	—	0.5	pF	1, 2

Notes:

1. This parameter is sampled. GV_{DD} = 1.5 V ± 0.075 V (for DDR3), f = 1 MHz, T_A = 25 °C, V_{OUT} = GV_{DD}/2, V_{OUT} (peak-to-peak) = 0.150 V.
2. This parameter is sampled. GV_{DD} = 1.35 V – 0.067 V ÷ + 0.100 V (for DDR3L), f = 1 MHz, T_A = 25 °C, V_{OUT} = GV_{DD}/2, V_{OUT} (peak-to-peak) = 0.167 V.

This table provides the current draw characteristics for MVREF.

Table 21. Current Draw Characteristics for MVREF

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Notes
Current draw for DDR3 SDRAM for MVREF	MVREF	—	1250	μA	—
Current draw for DDR3L SDRAM for MVREF	MVREF	—	1250	μA	—

This figure provides the AC test load for the eSPI.

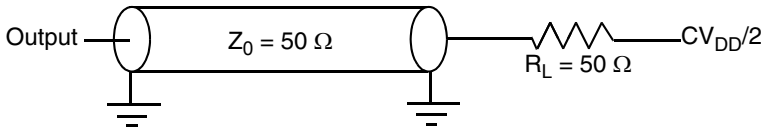


Figure 13. eSPI AC test load

This figure represents the AC timing from Table 29 in master mode (internal clock). Note that although timing specifications generally refer to the rising edge of the clock, this figure also applies when the falling edge is the active edge. Also, note that the clock edge is selectable on eSPI.

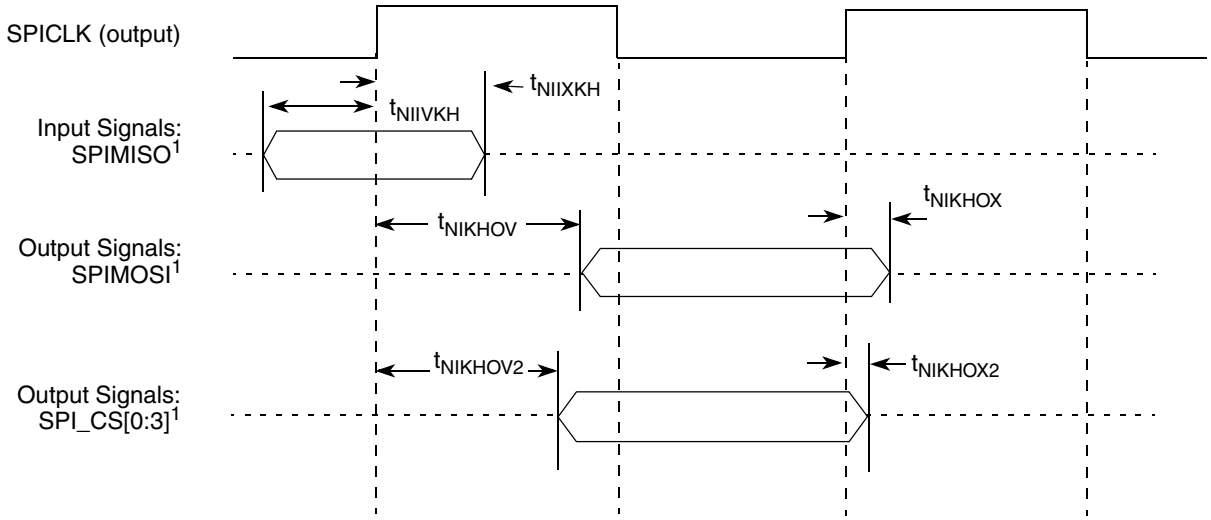


Figure 14. eSPI AC timing in master mode (Internal Clock) diagram

2.11 DUART

This section describes the DC and AC electrical specifications for the DUART interface.

2.11.1 DUART DC electrical characteristics

This table provides the DC electrical characteristics for the DUART interface.

Table 30. DUART DC electrical characteristics (OV_{DD} = 3.3 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1

This table provides the MII transmit AC timing specifications.

Table 34. MII transmit AC timing specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typ	Max	Unit
TX_CLK clock period 10 Mbps	t_{MTX}	399.96	400	400.04	ns
TX_CLK clock period 100 Mbps	t_{MTX}	39.996	40	40.004	ns
TX_CLK duty cycle	t_{MTXH}/t_{MTX}	35	—	65	%
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	t_{MTKHDX}	0	—	25	ns
TX_CLK data clock rise (20%–80%)	t_{MTXR}	1.0	—	4.0	ns
TX_CLK data clock fall (80%–20%)	t_{MTXF}	1.0	—	4.0	ns

This figure shows the MII transmit AC timing diagram.

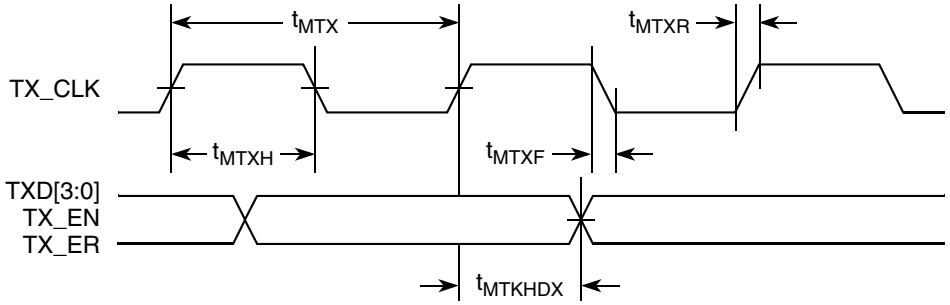


Figure 15. MII transmit AC timing diagram

This table provides the MII receive AC timing specifications.

Table 35. MII Receive AC timing specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typ	Max	Unit
RX_CLK clock period 10 Mbps	t_{MRX}	399.96	400	400.04	ns
RX_CLK clock period 100 Mbps	t_{MRX}	39.996	40	40.004	ns
RX_CLK duty cycle	t_{MRXH}/t_{MRX}	35	—	65	%
RXD[3:0], RX_DV, RX_ER setup time to RX_CLK	t_{MRDVKH}	10.0	—	—	ns
RXD[3:0], RX_DV, RX_ER hold time to RX_CLK	t_{MRDXKH}	10.0	—	—	ns
RX_CLK clock rise (20%-80%)	t_{MRXR}	1.0	—	4.0	ns
RX_CLK clock fall time (80%-20%)	t_{MRXF}	1.0	—	4.0	ns

Note: The frequency of RX_CLK should not exceed frequency of GTX_CLK125 by more than 300ppm.

The characteristics of the clock signals are as follows:

- The SerDes transceivers core power supply voltage requirements (SV_{DD}) are as specified in Section 2.1.2, "Recommended operating conditions."
- The SerDes reference clock receiver reference circuit structure is as follows:
  - The SD_REF_CLK*n* and $\overline{\text{SD\_REF\_CLK}n}$ are internally AC-coupled differential inputs as shown in Figure 36. Each differential clock input (SD_REF_CLK*n* or $\overline{\text{SD\_REF\_CLK}n}$) has on-chip 50-Ω termination to SGND followed by on-chip AC-coupling.
  - The external reference clock driver must be able to drive this termination.
  - The SerDes reference clock input can be either differential or single-ended. See the differential mode and single-ended mode descriptions below for detailed requirements.
- The maximum average current requirement also determines the common mode voltage range.
  - When the SerDes reference clock differential inputs are DC coupled externally with the clock driver chip, the maximum average current allowed for each input pin is 8 mA. In this case, the exact common mode input voltage is not critical as long as it is within the range allowed by the maximum average current of 8 mA because the input is AC-coupled on-chip.
  - This current limitation sets the maximum common mode input voltage to be less than 0.4 V (0.4 V ÷ 50 = 8 mA) while the minimum common mode input level is 0.1 V above SGND. For example, a clock with a 50/50 duty cycle can be produced by a clock driver with output driven by its current source from 0 mA to 16 mA (0–0.8 V), such that each phase of the differential input has a single-ended swing from 0 V to 800 mV with the common mode voltage at 400 mV.
  - If the device driving the SD_REF_CLK*n* and $\overline{\text{SD\_REF\_CLK}n}$ inputs cannot drive 50 Ω to SGND DC or the drive strength of the clock driver chip exceeds the maximum input current limitations, it must be AC-coupled off-chip.
- The input amplitude requirement is described in detail in the following sections.

2.20.2.2 DC-level requirement for SerDes reference clocks

The DC level requirement for the SerDes reference clock inputs is different depending on the signaling mode used to connect the clock driver chip and SerDes reference clock inputs, as described below:

- Differential Mode
  - The input amplitude of the differential clock must be between 400 mV and 1600 mV differential peak-peak (or between 200 mV and 800 mV differential peak). In other words, each signal wire of the differential pair must have a single-ended swing of less than 800 mV and greater than 200 mV. This requirement is the same for both external DC-coupled or AC-coupled connection.
  - For an external DC-coupled connection, as described in Section 2.20.2.1, "SerDes reference clock receiver characteristics," the maximum average current requirements sets the requirement for average voltage (common mode voltage) as between 100 mV and 400 mV. Figure 37 shows the SerDes reference clock input requirement for DC-coupled connection scheme.

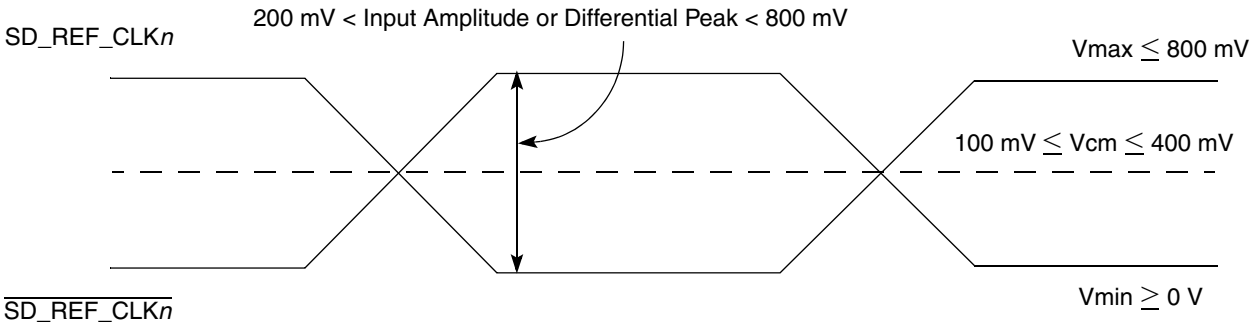


Figure 37. Differential reference clock input DC requirements (external DC-coupled)

2.20.2.3 AC requirements for SerDes reference clocks

This table lists AC requirements for the PCI Express, SGMII, Serial RapidIO and Aurora SerDes reference clocks to be guaranteed by the customer's application design.

Table 61. SD_REF_CLK*n* and $\overline{\text{SD\_REF\_CLK}n}$ input clock requirements (SV_{DD} = 1.0 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ frequency range	t_{CLK_REF}	—	100/125	—	MHz	1
SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ clock frequency tolerance	t_{CLK_TOL}	–350	—	350	ppm	—
SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ reference clock duty cycle	t_{CLK_DUTY}	40	50	60	%	4
SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ max deterministic peak-peak jitter at 10^{-6} BER	t_{CLK_DJ}	—	—	42	ps	—
SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ total reference clock jitter at 10^{-6} BER (peak-to-peak jitter at refClk input)	t_{CLK_TJ}	—	—	86	ps	2
SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ rising/falling edge rate	t_{CLKRR}/t_{CLKFR}	1	—	4	V/ns	3
Differential input high voltage	V_{IH}	200	—	—	mV	4
Differential input low voltage	V_{IL}	—	—	–200	mV	4
Rising edge rate (SD_REF_CLK*n*) to falling edge rate (SD_REF_CLK*n*) matching	Rise-Fall Matching	—	—	20	%	5, 6

Notes:

1. **Caution:** Only 100 and 125 have been tested. In-between values not work correctly with the rest of the system.
2. Limits from PCI Express CEM Rev 2.0
3. Measured from –200 mV to +200 mV on the differential waveform (derived from SD_REF_CLK*n* minus $\overline{\text{SD\_REF\_CLK}n}$). The signal must be monotonic through the measurement region for rise and fall time. The 400 mV measurement window is centered on the differential zero crossing. See Figure 40.
4. Measurement taken from differential waveform
5. Measurement taken from single-ended waveform
6. Matching applies to rising edge for SD_REF_CLK*n* and falling edge rate for $\overline{\text{SD\_REF\_CLK}n}$. It is measured using a 200 mV window centered on the median cross point where SD_REF_CLK*n* rising meets $\overline{\text{SD\_REF\_CLK}n}$ falling. The median cross point is used to calculate the voltage thresholds that the oscilloscope uses for the edge rate calculations. The rise edge rate of SD_REF_CLK*n* should be compared to the fall edge rate of $\overline{\text{SD\_REF\_CLK}n}$, the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 41.

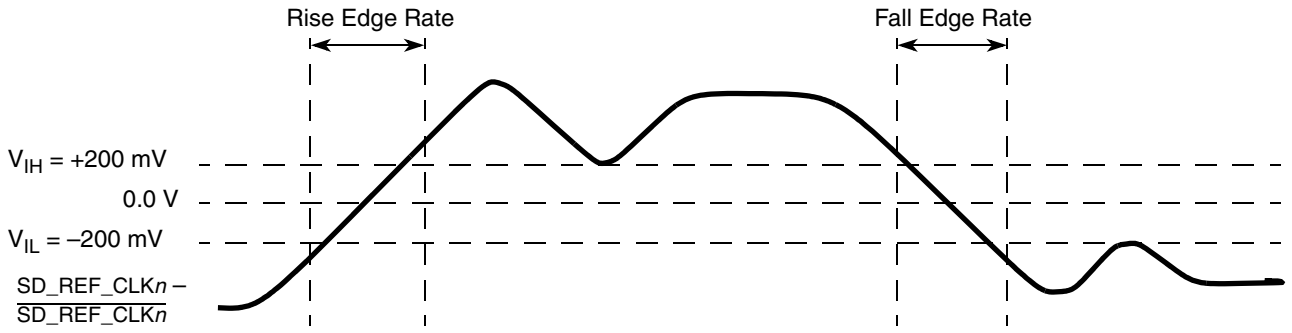


Figure 40. Differential measurement points for rise and fall time

Table 64. PCI Express 2.0 (2.5 GT/s) differential receiver input DC specifications (XV_{DD} = 1.5 V or 1.8 V) (continued)

Parameter	Symbol	Min	Typ	Max	Units	Notes
Powered down DC input impedance	$Z_{RX-HIGH-IMP-DC}$	50 k	—	—	Ω	Required receiver D+ as well as D– DC Impedance when the receiver terminations do not have power. See Note 3.
Electrical idle detect threshold	$V_{RX-IDLE-DET-DIFFp-p}$	65	—	175	mV	$V_{RX-IDLE-DET-DIFFp-p}$ = 2 × $\lvert V_{RX-D+} - V_{RX-D-} \rvert$ Measured at the package pins of the receiver

Notes:
1. Measured at the package pins with a test load of 50 Ω to GND on each pin.
2. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all unconfigured lanes of a port.
3. The receiver DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the receiver ground.

This table defines the DC specifications for the PCI Express 2.0 (5 GT/s) differential input at all receivers. The parameters are specified at the component pins.

Table 65. PCI Express 2.0 (5 GT/s) differential receiver input DC specifications (XV_{DD} = 1.5 V or 1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typ	Max	Units	Notes
Differential input peak-to-peak voltage	$V_{RX-DIFFp-p}$	120	—	1200	V	$V_{RX-DIFFp-p} = 2 \times \lvert V_{RX-D+} - V_{RX-D-} \rvert$ See Note 1.
DC differential input impedance	$Z_{RX-DIFF-DC}$	80	100	120	Ω	Receiver DC Differential mode impedance. See Note 2
DC input impedance	Z_{RX-DC}	40	50	60	Ω	Required receiver D+ as well as D– DC Impedance (50 ±20% tolerance). See Notes 1 and 2.
Powered down DC input impedance	$Z_{RX-HIGH-IMP-DC}$	50	—	—	kΩ	Required receiver D+ as well as D– DC Impedance when the receiver terminations do not have power. See Note 3.
Electrical idle detect threshold	$V_{RX-IDLE-DET-DIFFp-p}$	65	—	175	mV	$V_{RX-IDLE-DET-DIFFp-p}$ = 2 × $\lvert V_{RX-D+} - V_{RX-D-} \rvert$ Measured at the package pins of the receiver

Notes:
1. Measured at the package pins with a test load of 50Ω to GND on each pin.
2. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all unconfigured lanes of a port.
3. The receiver DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the receiver ground.

Table 85. Gen 2i/3 G transmitter AC specifications (continued)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typ	Max	Units	Notes
Deterministic jitter, $f_{C3dB} = f_{BAUD} \div 10$	$U_{SATA\_TXDJfB/10}$	—	—	0.17	UI p-p	1
Deterministic jitter, $f_{C3dB} = f_{BAUD} \div 500$	$U_{SATA\_TXDJfB/500}$	—	—	0.19	UI p-p	1
Deterministic jitter, $f_{C3dB} = f_{BAUD} \div 1667$	$U_{SATA\_TXDJfB/1667}$	—	—	0.35	UI p-p	1

Note:

1. Measured at transmitter output pins peak-to-peak phase variation, random data pattern

2.20.7.4 AC differential receiver Input characteristics

This table provides the Gen1i or 1.5 Gbits/s differential receiver input AC characteristics for the SATA interface. The AC timing specifications do not include RefClk jitter.

Table 86. Gen 1i/1.5G receiver AC specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typical	Max	Units	Notes
Unit Interval	T_{UI}	666.4333	666.6667	670.2333	ps	—
Total jitter data-data 5 UI	$U_{SATA\_TXTJ5UI}$	—	—	0.43	UI p-p	1
Total jitter, data-data 250 UI	$U_{SATA\_TXTJ250UI}$	—	—	0.60	UI p-p	1
Deterministic jitter, data-data 5 UI	$U_{SATA\_TXDJ5UI}$	—	—	0.25	UI p-p	1
Deterministic jitter, data-data 250 UI	$U_{SATA\_TXDJ250UI}$	—	—	0.35	UI p-p	1

Note:

1. Measured at receiver

This table provides the differential receiver input AC characteristics for the SATA interface at Gen2i or 3.0 Gbits/s transmission. The AC timing specifications do not include RefClk jitter.

Table 87. Gen 2i/3G receiver AC specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typical	Max	Units	Notes
Unit Interval	T_{UI}	333.2167	333.3333	335.1167	ps	—
Total jitter $f_{C3dB} = f_{BAUD} \div 10$	$U_{SATA\_TXTJfB/10}$	—	—	0.46	UI p-p	1
Total jitter $f_{C3dB} = f_{BAUD} \div 500$	$U_{SATA\_TXTJfB/500}$	—	—	0.60	UI p-p	1
Total jitter $f_{C3dB} = f_{BAUD} \div 1667$	$U_{SATA\_TXTJfB/1667}$	—	—	0.65	UI p-p	1

3.1.8 Frame Manager (FMan) clock select

The Frame Managers (FM) can each be synchronous with or asynchronous to the platform, depending on configuration.

This table describes the clocking options that may be applied to each FM. The clock selection is determined by the binary value of the RCW Clocking Configuration fields FM1_CLK_SEL and FM2_CLK_SEL.

Table 105. Frame Manager (FMan) clock select

Binary value of FM*n*_CLK_SEL	FM frequency
0b0	Platform Clock Frequency /2
0b1	FMan PLL Frequency /2 [1,2]

Notes:

1. For asynchronous mode, max frequency see Table 94.
2. For PLL settings, see Table 96.

3.2 Supply power default setting

This chip is capable of supporting multiple power supply levels on its I/O supplies. The I/O voltage select inputs, shown in the following table, properly configure the receivers and drivers of the I/Os associated with the BVDD, CVDD, and LVDD power planes, respectively.

WARNING

Incorrect voltage select settings can lead to irreversible device damage.

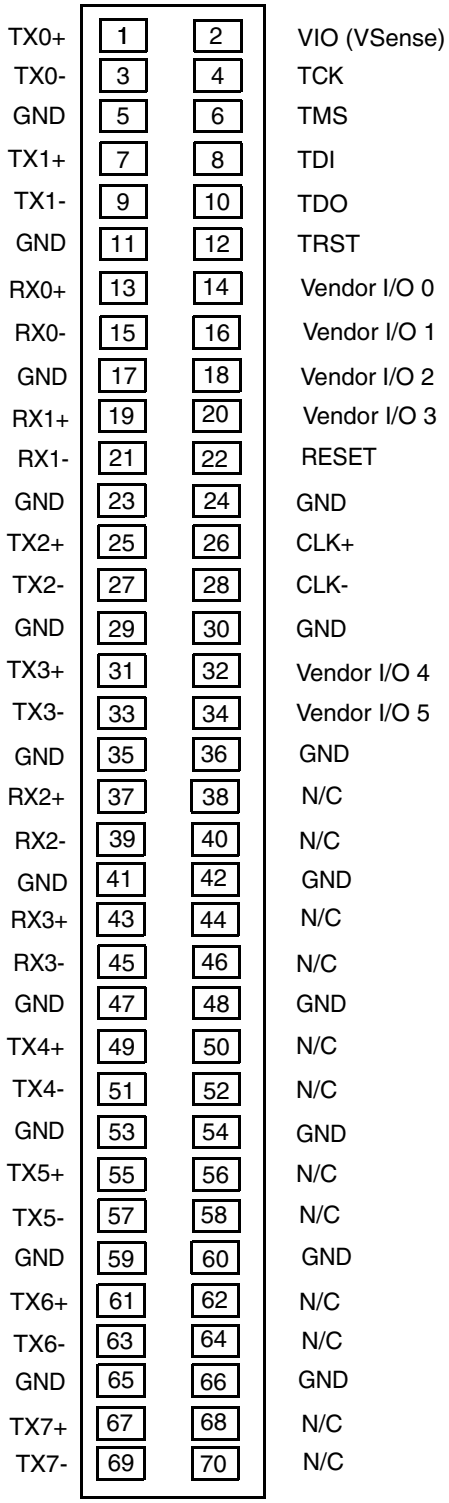
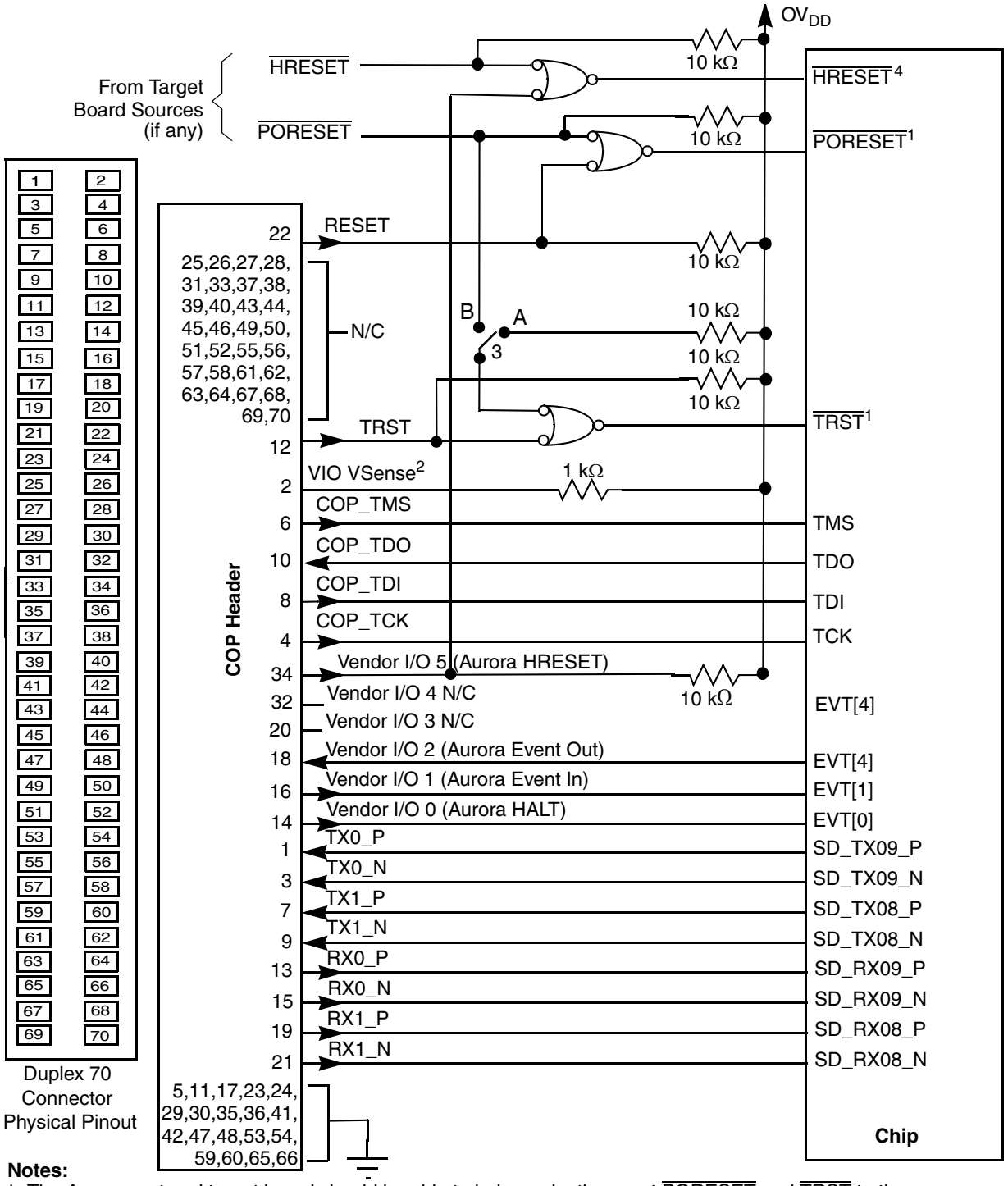


Figure 58. Aurora 70 pin connector duplex pinout



Notes:

1. The Aurora port and target board should be able to independently assert $\overline{\text{PORESET}}$ and $\overline{\text{TRST}}$ to the processor in order to fully control the processor as shown here.
2. Populate this with a 1 kΩ resistor for short-circuit/current-limiting protection.
3. This switch is included as a precaution for BSDL testing. The switch should be closed to position A during BSDL testing to avoid accidentally asserting the $\overline{\text{TRST}}$ line. If BSDL testing is not being performed, this switch should be closed to position B.
4. Asserting $\overline{\text{HRESET}}$ causes a hard reset on the device.

Figure 60. Aurora 70 pin connector duplex interface connection

5 Security fuse processor

This chip implements the QorIQ platform's Trust Architecture, supporting capabilities such as secure boot. Use of the Trust Architecture features is dependent on programming fuses in the Security Fuse Processor (SFP). The details of the Trust Architecture and SFP can be found in the applicable chip reference manual.

To program SFP fuses, the user is required to supply 1.5 V to the POV_{DD} pin per Section 2.2, "Power-up sequencing." POV_{DD} should only be powered for the duration of the fuse programming cycle, with a per device limit of two fuse programming cycles. All other times, connect POV_{DD} to GND. The sequencing requirements for raising and lowering POV_{DD} are shown in Figure 8. To ensure device reliability, fuse programming must be performed within the recommended fuse programming temperature range per Table 3.

Users not implementing the QorIQ platform's Trust Architecture features are not required to program fuses and should connect POV_{DD} to GND.

6 Ordering information

Please contact your local Freescale sales office or regional marketing team for ordering information.

6.1 Part numbering nomenclature

This table provides the Freescale QorIQ platform part numbering nomenclature.

Table 108. Part Numbering Nomenclature

p	*n*	*nn*	*n*	*x*	*t*	*e*	*n*	*c*	*d*	*r*
Generation	**Platform**	**Number of Cores**	**Derivative**	**Qual Status**	**Temperature Range**	**Encryption**	**Package Type**	**CPU Speed**	**DDR Speed**	**Die Revision**
P = 45 nm	5	• 01 = 1 core • 02 = 2 cores • 04 = 4 cores	0–9	P = Prototype N = Qualified	• S = Std temp (0 °C to 105 °C • X = Ext temp (–40 °C to 105 °C)	• E = SEC present • N = SEC not present	1 = FC-PBGA lead-free 7 = FC-PBGA C4/C5 lead-free	• T = 1800 MHz • V = 2000 MHz • 2 = 2200 MHz	• M = 1200 MHz • N = 1333 MHz • Q = 1600 MHz	A = Rev 1.0 B = Rev 2.0 C = Rev 2.1