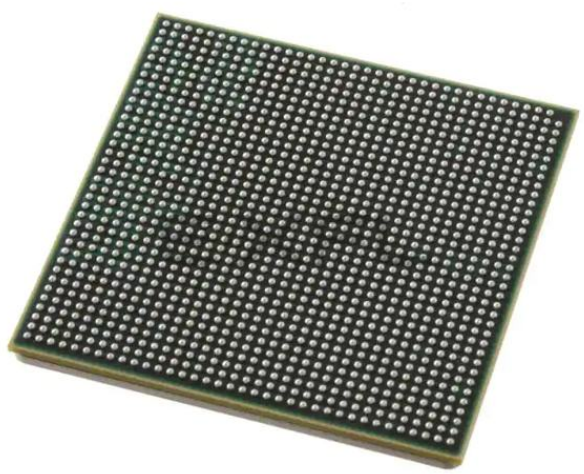

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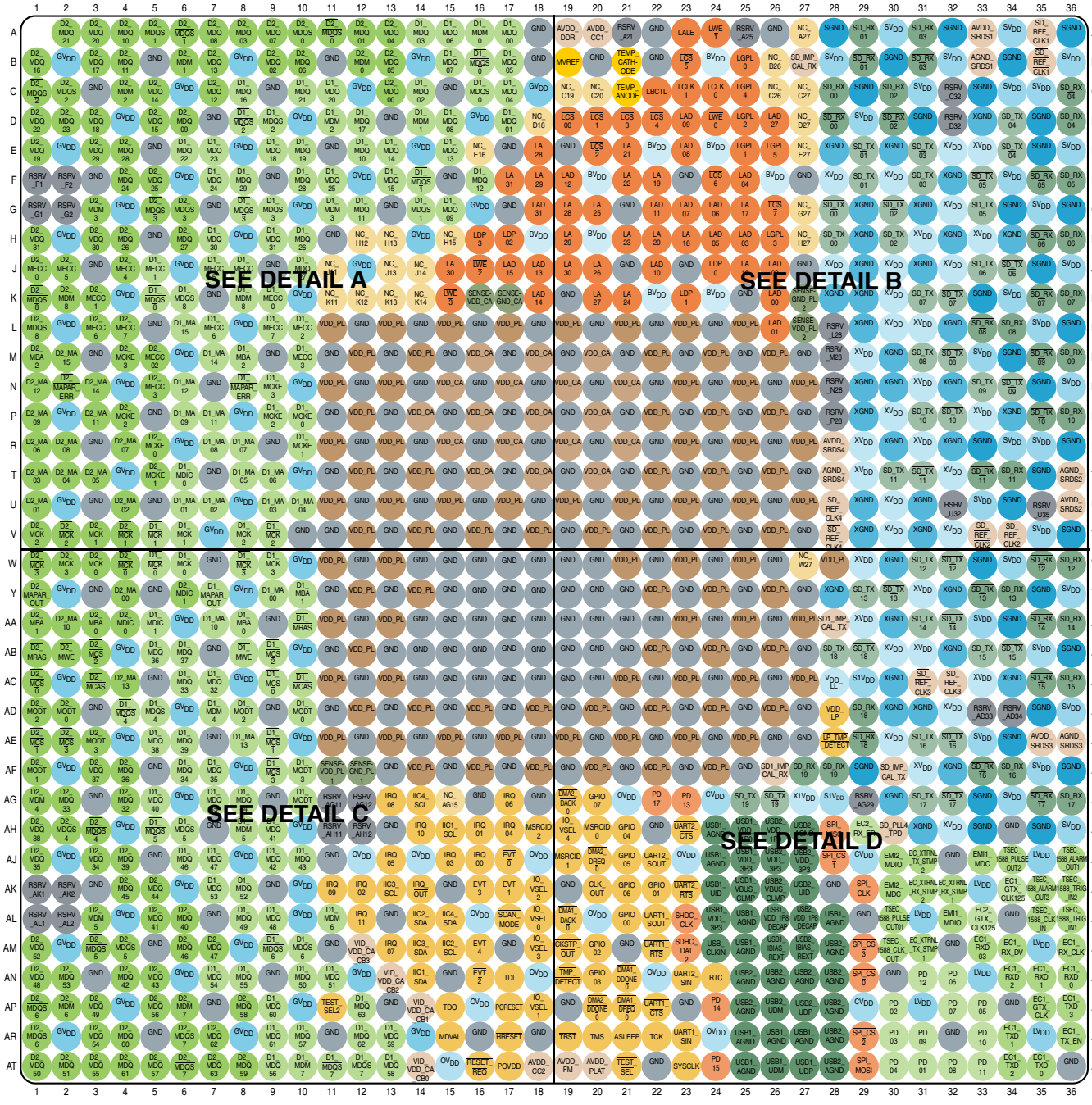
## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | PowerPC e5500 |
| Number of Cores/Bus Width | 2 Core, 64-Bit |
| Speed | 2.0GHz |
| Co-Processors/DSP | - |
| RAM Controllers | DDR3, DDR3L |
| Graphics Acceleration | No |
| Display & Interface Controllers | - |
| Ethernet | 1Gbps (10), 10Gbps (2) |
| SATA | SATA 3Gbps (2) |
| USB | USB 2.0 + PHY (2) |
| Voltage - I/O | 1.0V, 1.1V |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Security Features | Boot Security, Cryptography, Secure Fusebox, Secure Debug, Tamper Detection, Volatile key Storage |
| Package / Case | 1295-BBGA, FCBGA |
| Supplier Device Package | 1295-FCPBGA (37.5x37.5) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/p5021nxe7vnc |




***Signal Groups***

- $OV_{DD}$ I/O Supply Voltage
- $LV_{DD}$ I/O Supply Voltage
- $GV_{DD}$ DDR DRAM I/O Supply
- $CV_{DD}$ SPI Voltage Supply
- $BV_{DD}$ Local Bus I/O Supply
- $SV_{DD}$ SerDes Core Power Supply
- $XV_{DD}$ SerDes Transcvr Pad Supply
- $VDD_{PL}$ Platform Supply Voltage
- $VDD_{CA}$ Core Group A Supply Voltage
- $AVDD_{SRDS1}$ SerDes 1 PLL Supply Voltage
- $AVDD_{SRDS2}$ SerDes 2 PLL Supply Voltage
- $AVDD_{PLAT}$ Platform PLL Supply Voltage
- $AVDD_{CC}$ Core PLL Supply Voltage
- $SENSE_{VDD\_PL}$ Platform Voltage Sense
- $SENSE_{VDD}$ Core Group A Voltage Sense
- $SENSE_{VDD\_CB}$ Core Group B Voltage Sense
- RSRV Reserved
- POVDD Fuse Programming Override Supply

**Figure 2. 1295 BGA ball map diagram (top view)**

## 1.2 Pinout list

This table provides the pinout listing for the 1295 FC-PBGA package by bus.

**Table 1. Pins listed by bus**

| Signal | Signal description | Package pin number | Pin type | Power supply | Notes |
|---|---|---|---|---|---|
| **DDR SDRAM Memory interface 1** | | | | | |
| D1_MDQ00 | Data | A17 | I/O | $GV_{DD}$ | — |
| D1_MDQ01 | Data | D17 | I/O | $GV_{DD}$ | — |
| D1_MDQ02 | Data | C14 | I/O | $GV_{DD}$ | — |
| D1_MDQ03 | Data | A14 | I/O | $GV_{DD}$ | — |
| D1_MDQ04 | Data | C17 | I/O | $GV_{DD}$ | — |
| D1_MDQ05 | Data | B17 | I/O | $GV_{DD}$ | — |
| D1_MDQ06 | Data | A15 | I/O | $GV_{DD}$ | — |
| D1_MDQ07 | Data | B15 | I/O | $GV_{DD}$ | — |
| D1_MDQ08 | Data | D15 | I/O | $GV_{DD}$ | — |
| D1_MDQ09 | Data | G15 | I/O | $GV_{DD}$ | — |
| D1_MDQ10 | Data | E12 | I/O | $GV_{DD}$ | — |
| D1_MDQ11 | Data | G12 | I/O | $GV_{DD}$ | — |
| D1_MDQ12 | Data | F16 | I/O | $GV_{DD}$ | — |
| D1_MDQ13 | Data | E15 | I/O | $GV_{DD}$ | — |
| D1_MDQ14 | Data | E13 | I/O | $GV_{DD}$ | — |
| D1_MDQ15 | Data | F13 | I/O | $GV_{DD}$ | — |
| D1_MDQ16 | Data | C8 | I/O | $GV_{DD}$ | — |
| D1_MDQ17 | Data | D12 | I/O | $GV_{DD}$ | — |
| D1_MDQ18 | Data | E9 | I/O | $GV_{DD}$ | — |
| D1_MDQ19 | Data | E10 | I/O | $GV_{DD}$ | — |
| D1_MDQ20 | Data | C11 | I/O | $GV_{DD}$ | — |
| D1_MDQ21 | Data | C10 | I/O | $GV_{DD}$ | — |
| D1_MDQ22 | Data | E6 | I/O | $GV_{DD}$ | — |
| D1_MDQ23 | Data | E7 | I/O | $GV_{DD}$ | — |
| D1_MDQ24 | Data | F7 | I/O | $GV_{DD}$ | — |
| D1_MDQ25 | Data | F11 | I/O | $GV_{DD}$ | — |
| D1_MDQ26 | Data | H10 | I/O | $GV_{DD}$ | — |
| D1_MDQ27 | Data | J10 | I/O | $GV_{DD}$ | — |
| D1_MDQ28 | Data | F10 | I/O | $GV_{DD}$ | — |
| D1_MDQ29 | Data | F8 | I/O | $GV_{DD}$ | — |
| D1_MDQ30 | Data | H7 | I/O | $GV_{DD}$ | — |

**Table 1. Pins listed by bus (continued)**

| Signal | Signal description | Package pin number | Pin type | Power supply | Notes |
|---|---|---|---|---|---|
| SD_TX15 | Transmit Data (positive) | AB33 | O | $XV_{DD}$ | — |
| SD_TX14 | Transmit Data (positive) | AA31 | O | $XV_{DD}$ | — |
| SD_TX13 | Transmit Data (positive) | Y29 | O | $XV_{DD}$ | — |
| SD_TX12 | Transmit Data (positive) | W31 | O | $XV_{DD}$ | — |
| SD_TX11 | Transmit Data (positive) | T30 | O | $XV_{DD}$ | — |
| SD_TX10 | Transmit Data (positive) | P31 | O | $XV_{DD}$ | — |
| SD_TX09 | Transmit Data (positive) | N33 | O | $XV_{DD}$ | — |
| SD_TX08 | Transmit Data (positive) | M31 | O | $XV_{DD}$ | — |
| SD_TX07 | Transmit Data (positive) | K31 | O | $XV_{DD}$ | — |
| SD_TX06 | Transmit Data (positive) | J33 | O | $XV_{DD}$ | — |
| SD_TX05 | Transmit Data (positive) | G33 | O | $XV_{DD}$ | — |
| SD_TX04 | Transmit Data (positive) | D34 | O | $XV_{DD}$ | — |
| SD_TX03 | Transmit Data (positive) | F31 | O | $XV_{DD}$ | — |
| SD_TX02 | Transmit Data (positive) | H30 | O | $XV_{DD}$ | — |
| SD_TX01 | Transmit Data (positive) | F29 | O | $XV_{DD}$ | — |
| SD_TX00 | Transmit Data (positive) | H28 | O | $XV_{DD}$ | — |
| $\overline{\text{SD\_TX19}}$ | Transmit Data (negative) | AG26 | O | $XV_{DD}$ | — |
| $\overline{\text{SD\_TX18}}$ | Transmit Data (negative) | AB29 | O | $XV_{DD}$ | — |
| $\overline{\text{SD\_TX17}}$ | Transmit Data (negative) | AG32 | O | $XV_{DD}$ | — |
| $\overline{\text{SD\_TX16}}$ | Transmit Data (negative) | AE32 | O | $XV_{DD}$ | — |
| $\overline{\text{SD\_TX15}}$ | Transmit Data (negative) | AB34 | O | $XV_{DD}$ | — |
| $\overline{\text{SD\_TX14}}$ | Transmit Data (negative) | AA32 | O | $XV_{DD}$ | — |
| $\overline{\text{SD\_TX13}}$ | Transmit Data (negative) | Y30 | O | $XV_{DD}$ | — |
| $\overline{\text{SD\_TX12}}$ | Transmit Data (negative) | W32 | O | $XV_{DD}$ | — |
| $\overline{\text{SD\_TX11}}$ | Transmit Data (negative) | T31 | O | $XV_{DD}$ | — |
| $\overline{\text{SD\_TX10}}$ | Transmit Data (negative) | P32 | O | $XV_{DD}$ | — |
| $\overline{\text{SD\_TX09}}$ | Transmit Data (negative) | N34 | O | $XV_{DD}$ | — |
| $\overline{\text{SD\_TX08}}$ | Transmit Data (negative) | M32 | O | $XV_{DD}$ | — |
| $\overline{\text{SD\_TX07}}$ | Transmit Data (negative) | K32 | O | $XV_{DD}$ | — |
| $\overline{\text{SD\_TX06}}$ | Transmit Data (negative) | J34 | O | $XV_{DD}$ | — |
| $\overline{\text{SD\_TX05}}$ | Transmit Data (negative) | F33 | O | $XV_{DD}$ | — |
| $\overline{\text{SD\_TX04}}$ | Transmit Data (negative) | E34 | O | $XV_{DD}$ | — |
| $\overline{\text{SD\_TX03}}$ | Transmit Data (negative) | E31 | O | $XV_{DD}$ | — |
| $\overline{\text{SD\_TX02}}$ | Transmit Data (negative) | G30 | O | $XV_{DD}$ | — |

**Table 1. Pins listed by bus (continued)**

| Signal | Signal description | Package pin number | Pin type | Power supply | Notes |
|---|---|---|---|---|---|
| $\overline{\text{SD\_TX01}}$ | Transmit Data (negative) | E29 | O | $XV_{DD}$ | — |
| $\overline{\text{SD\_TX00}}$ | Transmit Data (negative) | G28 | O | $XV_{DD}$ | — |
| SD_RX19 | Receive Data (positive) | AF27 | I | $XV_{DD}$ | — |
| SD_RX18 | Receive Data (positive) | AD29 | I | $XV_{DD}$ | — |
| SD_RX17 | Receive Data (positive) | AG36 | I | $XV_{DD}$ | — |
| SD_RX16 | Receive Data (positive) | AF34 | I | $XV_{DD}$ | — |
| SD_RX15 | Receive Data (positive) | AC36 | I | $XV_{DD}$ | — |
| SD_RX14 | Receive Data (positive) | AA36 | I | $XV_{DD}$ | — |
| SD_RX13 | Receive Data (positive) | Y34 | I | $XV_{DD}$ | — |
| SD_RX12 | Receive Data (positive) | W36 | I | $XV_{DD}$ | — |
| SD_RX11 | Receive Data (positive) | T34 | I | $XV_{DD}$ | — |
| SD_RX10 | Receive Data (positive) | P36 | I | $XV_{DD}$ | — |
| SD_RX09 | Receive Data (positive) | M36 | I | $XV_{DD}$ | — |
| SD_RX08 | Receive Data (positive) | L34 | I | $XV_{DD}$ | — |
| SD_RX07 | Receive Data (positive) | K36 | I | $XV_{DD}$ | — |
| SD_RX06 | Receive Data (positive) | H36 | I | $XV_{DD}$ | — |
| SD_RX05 | Receive Data (positive) | F36 | I | $XV_{DD}$ | — |
| SD_RX04 | Receive Data (positive) | D36 | I | $XV_{DD}$ | — |
| SD_RX03 | Receive Data (positive) | A31 | I | $XV_{DD}$ | — |
| SD_RX02 | Receive Data (positive) | C30 | I | $XV_{DD}$ | — |
| SD_RX01 | Receive Data (positive) | A29 | I | $XV_{DD}$ | — |
| SD_RX00 | Receive Data (positive) | C28 | I | $XV_{DD}$ | — |
| $\overline{\text{SD\_RX19}}$ | Receive Data (negative) | AF28 | I | $XV_{DD}$ | — |
| $\overline{\text{SD\_RX18}}$ | Receive Data (negative) | AE29 | I | $XV_{DD}$ | — |
| $\overline{\text{SD\_RX17}}$ | Receive Data (negative) | AG35 | I | $XV_{DD}$ | — |
| $\overline{\text{SD\_RX16}}$ | Receive Data (negative) | AF33 | I | $XV_{DD}$ | — |
| $\overline{\text{SD\_RX15}}$ | Receive Data (negative) | AC35 | I | $XV_{DD}$ | — |
| $\overline{\text{SD\_RX14}}$ | Receive Data (negative) | AA35 | I | $XV_{DD}$ | — |
| $\overline{\text{SD\_RX13}}$ | Receive Data (negative) | Y33 | I | $XV_{DD}$ | — |
| $\overline{\text{SD\_RX12}}$ | Receive Data (negative) | W35 | I | $XV_{DD}$ | — |
| $\overline{\text{SD\_RX11}}$ | Receive Data (negative) | T33 | I | $XV_{DD}$ | — |
| $\overline{\text{SD\_RX10}}$ | Receive Data (negative) | P35 | I | $XV_{DD}$ | — |
| $\overline{\text{SD\_RX09}}$ | Receive Data (negative) | M35 | I | $XV_{DD}$ | — |
| $\overline{\text{SD\_RX08}}$ | Receive Data (negative) | L33 | I | $XV_{DD}$ | — |

**Table 1. Pins listed by bus (continued)**

| Signal | Signal description | Package pin number | Pin type | Power supply | Notes |
|---|---|---|---|---|---|
| $\overline{\text{SD\_RX07}}$ | Receive Data (negative) | K35 | I | $XV_{DD}$ | — |
| $\overline{\text{SD\_RX06}}$ | Receive Data (negative) | H35 | I | $XV_{DD}$ | — |
| $\overline{\text{SD\_RX05}}$ | Receive Data (negative) | F35 | I | $XV_{DD}$ | — |
| $\overline{\text{SD\_RX04}}$ | Receive Data (negative) | C36 | I | $XV_{DD}$ | — |
| $\overline{\text{SD\_RX03}}$ | Receive Data (negative) | B31 | I | $XV_{DD}$ | — |
| $\overline{\text{SD\_RX02}}$ | Receive Data (negative) | D30 | I | $XV_{DD}$ | — |
| $\overline{\text{SD\_RX01}}$ | Receive Data (negative) | B29 | I | $XV_{DD}$ | — |
| $\overline{\text{SD\_RX00}}$ | Receive Data (negative) | D28 | I | $XV_{DD}$ | — |
| SD_REF_CLK1 | SerDes Bank 1 PLL Reference Clock | A35 | I | $XV_{DD}$ | — |
| $\overline{\text{SD\_REF\_CLK1}}$ | SerDes Bank 1 PLL Reference Clock Complement | B35 | I | $XV_{DD}$ | — |
| SD_REF_CLK2 | SerDes Bank 2 PLL Reference Clock | V34 | I | $XV_{DD}$ | — |
| $\overline{\text{SD\_REF\_CLK2}}$ | SerDes Bank 2 PLL Reference Clock Complement | V33 | I | $XV_{DD}$ | — |
| SD_REF_CLK3 | SerDes Bank 3 PLL Reference Clock | AC32 | I | XVDD | — |
| $\overline{\text{SD\_REF\_CLK3}}$ | SerDes Bank 3 PLL Reference Clock Complement | AC31 | I | XVDD | — |
| SD_REF_CLK4 | SerDes Bank 4 PLL Reference Clock | U28 | I | XVDD | — |
| $\overline{\text{SD\_REF\_CLK4}}$ | SerDes Bank 4 PLL Reference Clock Complement | V28 | I | XVDD | — |
| **General-Purpose Input/Output** | | | | | |
| GPIO00 | General Purpose Input / Output | AL21 | I/O | $OV_{DD}$ | — |
| GPIO01 | General Purpose Input / Output | AK22 | I/O | $OV_{DD}$ | — |
| GPIO02 | General Purpose Input / Output | AM20 | I/O | $OV_{DD}$ | — |
| GPIO03 | General Purpose Input / Output | AN20 | I/O | $OV_{DD}$ | — |
| GPIO04/USB1_DRVVBUS | General Purpose Input / Output | AH21 | I/O | $OV_{DD}$ | — |
| GPIO05/USB1_PWRFAULT | General Purpose Input / Output | AJ21 | I/O | $OV_{DD}$ | — |
| GPIO06/USB2_DRVVBUS | General Purpose Input / Output | AK21 | I/O | $OV_{DD}$ | — |
| GPIO07/USB2_PWRFAULT | General Purpose Input / Output | AG20 | I/O | $OV_{DD}$ | — |
| GPIO08/UART1_SOUT | General Purpose Input / Output | AL22 | I/O | $OV_{DD}$ | — |
| GPIO09/UART2_SOUT | General Purpose Input / Output | AJ22 | I/O | $OV_{DD}$ | — |
| GPIO10/UART1_SIN | General Purpose Input / Output | AR23 | I/O | $OV_{DD}$ | — |
| GPIO11/UART2_SIN | General Purpose Input / Output | AN23 | I/O | $OV_{DD}$ | — |

**Table 1. Pins listed by bus (continued)**

| Signal | Signal description | Package pin number | Pin type | Power supply | Notes |
|---|---|---|---|---|---|
| GND | Ground | T13 | — | — | — |
| GND | Ground | V13 | — | — | — |
| GND | Ground | Y13 | — | — | — |
| GND | Ground | AB13 | — | — | — |
| GND | Ground | AD13 | — | — | — |
| GND | Ground | AE14 | — | — | — |
| GND | Ground | AC14 | — | — | — |
| GND | Ground | AA14 | — | — | — |
| GND | Ground | W14 | — | — | — |
| GND | Ground | U14 | — | — | — |
| GND | Ground | R14 | — | — | — |
| GND | Ground | N14 | — | — | — |
| GND | Ground | L14 | — | — | — |
| GND | Ground | M15 | — | — | — |
| GND | Ground | P15 | — | — | — |
| GND | Ground | T15 | — | — | — |
| GND | Ground | V15 | — | — | — |
| GND | Ground | Y15 | — | — | — |
| GND | Ground | AB15 | — | — | — |
| GND | Ground | AD15 | — | — | — |
| GND | Ground | AF15 | — | — | — |
| GND | Ground | W16 | — | — | — |
| GND | Ground | AC16 | — | — | — |
| GND | Ground | AA16 | — | — | — |
| GND | Ground | AE16 | — | — | — |
| GND | Ground | U16 | — | — | — |
| GND | Ground | R16 | — | — | — |
| GND | Ground | N16 | — | — | — |
| GND | Ground | M17 | — | — | — |
| GND | Ground | P17 | — | — | — |
| GND | Ground | T17 | — | — | — |
| GND | Ground | N18 | — | — | — |
| GND | Ground | R18 | — | — | — |
| GND | Ground | U18 | — | — | — |

**Table 1. Pins listed by bus (continued)**

| Signal | Signal description | Package pin number | Pin type | Power supply | Notes |
|---|---|---|---|---|---|
| GND | Ground | Y17 | — | — | — |
| GND | Ground | AB17 | — | — | — |
| GND | Ground | AD17 | — | — | — |
| GND | Ground | AF17 | — | — | — |
| GND | Ground | W18 | — | — | — |
| GND | Ground | AC18 | — | — | — |
| GND | Ground | AA18 | — | — | — |
| GND | Ground | AE18 | — | — | — |
| GND | Ground | AF19 | — | — | — |
| GND | Ground | AD19 | — | — | — |
| GND | Ground | AB19 | — | — | — |
| GND | Ground | Y19 | — | — | — |
| GND | Ground | V19 | — | — | — |
| GND | Ground | T19 | — | — | — |
| GND | Ground | P19 | — | — | — |
| GND | Ground | M19 | — | — | — |
| GND | Ground | N20 | — | — | — |
| GND | Ground | R20 | — | — | — |
| GND | Ground | U20 | — | — | — |
| GND | Ground | AE20 | — | — | — |
| GND | Ground | AA20 | — | — | — |
| GND | Ground | AC20 | — | — | — |
| GND | Ground | W20 | — | — | — |
| GND | Ground | AF21 | — | — | — |
| GND | Ground | AD21 | — | — | — |
| GND | Ground | AB21 | — | — | — |
| GND | Ground | Y21 | — | — | — |
| GND | Ground | V21 | — | — | — |
| GND | Ground | T21 | — | — | — |
| GND | Ground | P21 | — | — | — |
| GND | Ground | M21 | — | — | — |
| GND | Ground | AE22 | — | — | — |
| GND | Ground | AC22 | — | — | — |
| GND | Ground | AA22 | — | — | — |

**Table 1. Pins listed by bus (continued)**

| Signal | Signal description | Package pin number | Pin type | Power supply | Notes |
|---|---|---|---|---|---|
| USB1_AGND | USB1 PHY Transceiver GND | AR26 | — | — | — |
| USB1_AGND | USB1 PHY Transceiver GND | AR27 | — | — | — |
| USB1_AGND | USB1 PHY Transceiver GND | AR28 | — | — | — |
| USB1_AGND | USB1 PHY Transceiver GND | AT25 | — | — | — |
| USB1_AGND | USB1 PHY Transceiver GND | AT28 | — | — | — |
| USB2_AGND | USB2 PHY Transceiver GND | AH27 | — | — | — |
| USB2_AGND | USB2 PHY Transceiver GND | AL28 | — | — | — |
| USB2_AGND | USB2 PHY Transceiver GND | AM28 | — | — | — |
| USB2_AGND | USB2 PHY Transceiver GND | AN25 | — | — | — |
| USB2_AGND | USB2 PHY Transceiver GND | AN26 | — | — | — |
| USB2_AGND | USB2 PHY Transceiver GND | AN27 | — | — | — |
| USB2_AGND | USB2 PHY Transceiver GND | AN28 | — | — | — |
| USB2_AGND | USB2 PHY Transceiver GND | AP25 | — | — | — |
| USB2_AGND | USB2 PHY Transceiver GND | AP28 | — | — | — |
| OVDD | General I/O Supply | AN22 | — | $OV_{DD}$ | — |
| OVDD | General I/O Supply | AJ14 | — | $OV_{DD}$ | — |
| OVDD | General I/O Supply | AJ18 | — | $OV_{DD}$ | — |
| OVDD | General I/O Supply | AL16 | — | $OV_{DD}$ | — |
| OVDD | General I/O Supply | AJ12 | — | $OV_{DD}$ | — |
| OVDD | General I/O Supply | AN18 | — | $OV_{DD}$ | — |
| OVDD | General I/O Supply | AG21 | — | $OV_{DD}$ | — |
| OVDD | General I/O Supply | AL20 | — | $OV_{DD}$ | — |
| OVDD | General I/O Supply | AT15 | — | $OV_{DD}$ | — |
| OVDD | General I/O Supply | AJ23 | — | $OV_{DD}$ | — |
| OVDD | General I/O Supply | AP16 | — | $OV_{DD}$ | — |
| OVDD | General I/O Supply | AR24 | — | $OV_{DD}$ | — |
| CVDD | eSPI & eSDHC Supply | AG24 | — | $CV_{DD}$ | — |
| CVDD | eSPI & eSDHC Supply | AJ29 | — | $CV_{DD}$ | — |
| CVDD | eSPI & eSDHC Supply | AP29 | — | $CV_{DD}$ | — |
| GVDD | DDR Supply | B2 | — | $GV_{DD}$ | — |
| GVDD | DDR Supply | B8 | — | $GV_{DD}$ | — |
| GVDD | DDR Supply | B14 | — | $GV_{DD}$ | — |
| GVDD | DDR Supply | C18 | — | $GV_{DD}$ | — |
| GVDD | DDR Supply | C12 | — | $GV_{DD}$ | — |

**Table 1. Pins listed by bus (continued)**

| Signal | Signal description | Package pin number | Pin type | Power supply | Notes |
|---|---|---|---|---|---|
| GVDD | DDR Supply | C6 | — | $GV_{DD}$ | — |
| GVDD | DDR Supply | D4 | — | $GV_{DD}$ | — |
| GVDD | DDR Supply | D10 | — | $GV_{DD}$ | — |
| GVDD | DDR Supply | D16 | — | $GV_{DD}$ | — |
| GVDD | DDR Supply | E14 | — | $GV_{DD}$ | — |
| GVDD | DDR Supply | E8 | — | $GV_{DD}$ | — |
| GVDD | DDR Supply | E2 | — | $GV_{DD}$ | — |
| GVDD | DDR Supply | F6 | — | $GV_{DD}$ | — |
| GVDD | DDR Supply | F12 | — | $GV_{DD}$ | — |
| GVDD | DDR Supply | AR8 | — | $GV_{DD}$ | — |
| GVDD | DDR Supply | G4 | — | $GV_{DD}$ | — |
| GVDD | DDR Supply | G10 | — | $GV_{DD}$ | — |
| GVDD | DDR Supply | G16 | — | $GV_{DD}$ | — |
| GVDD | DDR Supply | H14 | — | $GV_{DD}$ | — |
| GVDD | DDR Supply | H8 | — | $GV_{DD}$ | — |
| GVDD | DDR Supply | H2 | — | $GV_{DD}$ | — |
| GVDD | DDR Supply | J6 | — | $GV_{DD}$ | — |
| GVDD | DDR Supply | K10 | — | $GV_{DD}$ | — |
| GVDD | DDR Supply | K4 | — | $GV_{DD}$ | — |
| GVDD | DDR Supply | L2 | — | $GV_{DD}$ | — |
| GVDD | DDR Supply | L8 | — | $GV_{DD}$ | — |
| GVDD | DDR Supply | M6 | — | $GV_{DD}$ | — |
| GVDD | DDR Supply | N4 | — | $GV_{DD}$ | — |
| GVDD | DDR Supply | N10 | — | $GV_{DD}$ | — |
| GVDD | DDR Supply | P8 | — | $GV_{DD}$ | — |
| GVDD | DDR Supply | P2 | — | $GV_{DD}$ | — |
| GVDD | DDR Supply | R6 | — | $GV_{DD}$ | — |
| GVDD | DDR Supply | T10 | — | $GV_{DD}$ | — |
| GVDD | DDR Supply | T4 | — | $GV_{DD}$ | — |
| GVDD | DDR Supply | J12 | — | $GV_{DD}$ | — |
| GVDD | DDR Supply | U2 | — | $GV_{DD}$ | — |
| GVDD | DDR Supply | U8 | — | $GV_{DD}$ | — |
| GVDD | DDR Supply | V7 | — | $GV_{DD}$ | — |
| GVDD | DDR Supply | AK10 | — | $GV_{DD}$ | — |

**Table 1. Pins listed by bus (continued)**

| Signal | Signal description | Package pin number | Pin type | Power supply | Notes |
|---|---|---|---|---|---|
| BVDD | Local Bus Supply | E22 | — | $BV_{DD}$ | — |
| BVDD | Local Bus Supply | K24 | — | $BV_{DD}$ | — |
| BVDD | Local Bus Supply | H20 | — | $BV_{DD}$ | — |
| BVDD | Local Bus Supply | H18 | — | $BV_{DD}$ | — |
| SVDD | SerDes Core Logic Supply | A30 | — | $SV_{DD}$ | — |
| SVDD | SerDes Core Logic Supply | A34 | — | $SV_{DD}$ | — |
| SVDD | SerDes Core Logic Supply | AA33 | — | $SV_{DD}$ | — |
| SVDD | SerDes Core Logic Supply | AB35 | — | $SV_{DD}$ | — |
| SVDD | SerDes Core Logic Supply | AD36 | — | $SV_{DD}$ | — |
| SVDD | SerDes Core Logic Supply | AE33 | — | $SV_{DD}$ | — |
| SVDD | SerDes Core Logic Supply | AF35 | — | $SV_{DD}$ | — |
| SVDD | SerDes Core Logic Supply | AG34 | — | $SV_{DD}$ | — |
| SVDD | SerDes Core Logic Supply | B28 | — | $SV_{DD}$ | — |
| SVDD | SerDes Core Logic Supply | B32 | — | $SV_{DD}$ | — |
| SVDD | SerDes Core Logic Supply | B36 | — | $SV_{DD}$ | — |
| SVDD | SerDes Core Logic Supply | C31 | — | $SV_{DD}$ | — |
| SVDD | SerDes Core Logic Supply | C34 | — | $SV_{DD}$ | — |
| SVDD | SerDes Core Logic Supply | C35 | — | $SV_{DD}$ | — |
| SVDD | SerDes Core Logic Supply | D29 | — | $SV_{DD}$ | — |
| SVDD | SerDes Core Logic Supply | E36 | — | $SV_{DD}$ | — |
| SVDD | SerDes Core Logic Supply | F34 | — | $SV_{DD}$ | — |
| SVDD | SerDes Core Logic Supply | G35 | — | $SV_{DD}$ | — |
| SVDD | SerDes Core Logic Supply | J36 | — | $SV_{DD}$ | — |
| SVDD | SerDes Core Logic Supply | K34 | — | $SV_{DD}$ | — |
| SVDD | SerDes Core Logic Supply | L35 | — | $SV_{DD}$ | — |
| SVDD | SerDes Core Logic Supply | M33 | — | $SV_{DD}$ | — |
| SVDD | SerDes Core Logic Supply | N36 | — | $SV_{DD}$ | — |
| SVDD | SerDes Core Logic Supply | R34 | — | $SV_{DD}$ | — |
| SVDD | SerDes Core Logic Supply | R35 | — | $SV_{DD}$ | — |
| SVDD | SerDes Core Logic Supply | U33 | — | $SV_{DD}$ | — |
| SVDD | SerDes Core Logic Supply | V35 | — | $SV_{DD}$ | — |
| SVDD | SerDes Core Logic Supply | W34 | — | $SV_{DD}$ | — |
| SVDD | SerDes Core Logic Supply | Y36 | — | $SV_{DD}$ | — |
| SVDD | SerDes Core Logic Supply | AH36 | — | $SV_{DD}$ | — |

**Table 1. Pins listed by bus (continued)**

| Signal | Signal description | Package pin number | Pin type | Power supply | Notes |
|---|---|---|---|---|---|
| AVDD_SRDS2 | SerDes PLL2 Supply | U36 | — | — | 13 |
| AVDD_SRDS3 | SerDes PLL3 Supply | AE35 | — | — | 13 |
| AVDD_SRDS4 | SerDes PLL4 Supply | R28 | — | — | 13 |
| SENSEVDD_PL1 | Platform Vdd Sense | AF11 | — | — | 8 |
| SENSEVDD_PL2 | Platform Vdd Sense | L27 | — | — | 8 |
| SENSEVDD_CA | Core Group A Vdd Sense | K16 | — | — | 8 |
| USB1_VDD_3P3 | USB1 PHY Transceiver 3.3V Supply | AL24 | — | — | — |
| USB1_VDD_3P3 | USB1 PHY Transceiver 3.3V Supply | AJ25 | — | — | — |
| USB2_VDD_3P3 | USB2 PHY Transceiver 3.3V Supply | AJ26 | — | — | — |
| USB2_VDD_3P3 | USB2 PHY Transceiver 3.3V Supply | AJ27 | — | — | — |
| USB1_VDD_1P0 | USB1 PHY PLL 1.0V Supply | AH25 | — | — | — |
| USB2_VDD_1P0 | USB2 PHY PLL 1.0V Supply | AH26 | — | — | — |
| **Analog Signals** | | | | | |
| MVREF | SSTL_1.5/1.35 Reference Voltage | B19 | I | $GV_{DD}/2$ | — |
| SD_IMP_CAL_TX | SerDes transmitter Impedance Calibration | AF30 | I | 200Ω (±1%) to $XV_{DD}$ | 23 |
| SD1_IMP_CAL_TX | SerDes transmitter Impedance Calibration | AA28 | I | 200Ω (±1%) to $XV_{DD}$ | 23 |
| SD_IMP_CAL_RX | SerDes receiver Impedance Calibration | B27 | I | 200Ω (±1%) to $SV_{DD}$ | 24 |
| SD1_IMP_CAL_RX | SerDes receiver Impedance Calibration | AF26 | I | 200Ω (±1%) to $SV_{DD}$ | 24 |
| TEMP_ANODE | Temperature Diode Anode | C21 | — | internal diode | 9 |
| TEMP_CATHODE | Temperature Diode Cathode | B21 | — | internal diode | 9 |
| USB1_IBIAS_REXT | USB PHY1 Reference Bias Current Generation | AM26 | — | — | 36 |
| USB2_IBIAS_REXT | USB PHY2 Reference Bias Current Generation | AM27 | — | — | 36 |
| USB1_VDD_1P8_DECAP | USB1 PHY 1.8V Output to External Decap | AL26 | — | — | 37 |

## 2.1.2 Recommended operating conditions

This table provides the recommended operating conditions for this device. Note that proper device operation outside these conditions is not guaranteed.

**Table 3. Recommended operating conditions**

| Parameter | | Symbol | Recommended value | Unit | Notes |
|---|---|---|---|---|---|
| Core group A (core 0,1) supply voltage | | $V_{DD\_CA}$ | 1.1 ± 50mV (core frequency ≤ 2000 MHz)<br>1.2V ± 30mV (core frequency > 2000 MHz) | V | 1,6 |
| Platform supply voltage | | $V_{DD\_PL}$ | 1.0 ± 50mV | V | 1,6 |
| PLL supply voltage (core, platform, DDR, FMan) | | $AV_{DD}$ | 1.0 ± 50mV | V | — |
| PLL supply voltage (SerDes) | | $AV_{DD\_SRDS}$ | 1.0 ± 50mV | V | — |
| Fuse programming override supply | | $POV_{DD}$ | 1.5 ± 75mV | V | 2 |
| DUART, $I^2C$, DMA, MPIC, GPIO, system control and power management, clocking, debug, I/O voltage select, and JTAG I/O voltage | | $OV_{DD}$ | 3.3 ± 165mV | V | — |
| eSPI, eSDHC | | $CV_{DD}$ | 3.3 ± 165mV<br>2.5 ± 125mV<br>1.8 ± 90mV | V | — |
| DDR DRAM I/O voltage | DDR3 | $GV_{DD}$ | 1.5 ± 75mV | V | — |
| | DDR3L | | 1.35 ± 67mV | | |
| Enhanced local bus I/O voltage | | $BV_{DD}$ | 3.3 ± 165mV<br>2.5 ± 125mV<br>1.8 ± 90mV | V | — |
| Main power supply for internal circuitry of SerDes and pad power supply for SerDes receiver | | $SV_{DD}$ | 1.0 + 50mV<br>1.0 – 30mV | V | — |
| Pad power supply for SerDes transmitter | | $XV_{DD}$ | 1.8 ± 90mV<br>1.5 ± 75mV | V | — |
| Ethernet I/O, Ethernet Management interface 1 (EMI1), 1588, GPIO | | $LV_{DD}$ | 3.3 ± 165mV<br>2.5 ± 125mV | V | 3 |
| USB PHY transceiver supply voltage | | $USB\_V_{DD}\_3P3$ | 3.3 ± 165mV | V | — |
| USB PHY PLL supply voltage | | $USB\_V_{DD}\_1P0$ | 1.0 ± 50mV | V | — |
| Low-power security monitor supply | | $V_{DD\_LP}$ | 1.0 ± 50mV | V | — |

**Table 3. Recommended operating conditions (continued)**

| Parameter | | Symbol | Recommended value | Unit | Notes |
|---|---|---|---|---|---|
| Input voltage | DDR3 and DDR3L DRAM signals | $MV_{IN}$ | GND to $GV_{DD}$ | V | 7 |
| | DDR3 and DDR3L DRAM reference | $MV_{REF}$ | $GV_{DD}/2$ ± 1% | V | 7 |
| | Ethernet signals (except EMI2) | $LV_{IN}$ | GND to $LV_{DD}$ | V | 7 |
| | eSPI, eSHDC | $CV_{IN}$ | GND to $CV_{DD}$ | V | 7 |
| | Enhanced local bus signals | $BV_{IN}$ | GND to $BV_{DD}$ | V | 7 |
| | DUART, $I^2C$, DMA, MPIC, GPIO, system control and power management, clocking, debug, I/O voltage select, and JTAG I/O voltage | $OV_{IN}$ | GND to $OV_{DD}$ | V | 7 |
| | SerDes signals | $SV_{IN}$ | GND to $SV_{DD}$ | V | 7 |
| | USB PHY Transceiver signals | $USB\_V_{IN}\_3P3$ | GND to $USB\_V_{DD}\_3P3$ | V | 7 |
| | Ethernet Management interface 2 (EMI2) signals | — | GND to 1.2V | V | 4, 7 |
| Operating Temperature range | Normal Operation | $T_A$, $T_J$ | $T_A$ = 0 (min) to $T_J$ = 105 (max) (90 (max) core frequency > 2000 MHz) | °C | — |
| | Extended Temperature | $T_A$, $T_J$ | $T_A$ = -40 (min) to $T_J$ = 105 (max) | °C | — |
| | Secure Boot Fuse Programming | $T_A$, $T_J$ | $T_A$ = 0 (min) to $T_J$ = 70 (max) | °C | 2 |

**Notes:**

1. $V_{DD\_PL}$ voltage must not exceed $V_{DD\_CA}$.
2. $POV_{DD}$ must be supplied 1.5 V and the chip must operate in the specified fuse programming temperature range only during secure boot fuse programming. For all other operating conditions, $POV_{DD}$ must be tied to GND, subject to the power sequencing constraints shown in Section 2.2, "Power-up sequencing."
3. Selecting RGMII limits $LV_{DD}$ to 2.5V.
4. Ethernet Management interface 2 pins function as open drain I/Os. The interface shall conform to 1.2 V nominal voltage levels. $LV_{DD}$ must be powered to use this interface.6. Supply voltage specified at the voltage sense pin. Voltage input pins must be regulated to provide specified voltage at the sense pin.
7. All input signals must increase/decrease monotonically throughout the entire rise/fall duration.

This table provides the system clock (SYSCLK) AC timing specifications.

**Table 12. SYSCLK AC timing specifications**

For recommended operating conditions, see Table 3.

| Parameter/Condition | Symbol | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| SYSCLK frequency | $f_{SYSCLK}$ | 100 | — | 166 | MHz | 1, 2 |
| SYSCLK cycle time | $t_{SYSCLK}$ | 6 | — | 10 | ns | 1, 2 |
| SYSCLK duty cycle | $t_{KHK}$ / $t_{SYSCLK}$ | 40 | — | 60 | % | 2 |
| SYSCLK slew rate | — | 1 | — | 4 | V/ns | 3 |
| SYSCLK peak period jitter | — | — | — | 150 | ps | — |
| SYSCLK jitter phase noise | — | — | — | 500 | KHz | 4 |
| AC Input Swing Limits at 3.3 V $OV_{DD}$ | $\Delta V_{AC}$ | 1.9 | — | — | V | — |

**Notes:**
1. **Caution:** The relevant clock ratio settings must be chosen such that the resulting SYSCLK frequency, do not exceed their respective maximum or minimum operating frequencies.
2. Measured at the rising edge and/or the falling edge at $OV_{DD}/2$.
3. Slew rate as measured from ±0.3 $\Delta \mathbf{V_{AC}}$ at center of peak to peak voltage at clock input.
4. Phase noise is calculated as FFT of TIE jitter.

## 2.6.2 Spread-spectrum sources recommendations

Spread-spectrum clock sources is an increasingly popular way to control electromagnetic interference emissions (EMI) by spreading the emitted noise to a wider spectrum and reducing the peak noise magnitude in order to meet industry and government requirements. These clock sources intentionally add long-term jitter to diffuse the EMI spectral content. The jitter specification given in Table 13 considers short-term (cycle-to-cycle) jitter only. The clock generator's cycle-to-cycle output jitter should meet the chip's input cycle-to-cycle jitter requirement. Frequency modulation and spread are separate concerns; the chip is compatible with spread spectrum sources if the recommendations listed in Table 13 are observed.

**Table 13. Spread-spectrum clock source recommendations**

For recommended operating conditions, see Table 3.

| Parameter | Min | Max | Unit | Notes |
|---|---|---|---|---|
| Frequency modulation | — | 60 | kHz | — |
| Frequency spread | — | 1.0 | % | 1, 2 |

**Notes:**
1. SYSCLK frequencies that result from frequency spreading and the resulting core frequency must meet the minimum and maximum specifications given in Table 12.
2. Maximum spread spectrum frequency may not result in exceeding any maximum operating frequency of the device.

**CAUTION**

The processor's minimum and maximum SYSCLK and core/platform/DDR frequencies must not be exceeded regardless of the type of clock source. Therefore, systems in which the processor is operated at its maximum rated core/platform/DDR frequency should avoid violating the stated limits by using down-spreading only.

This table provides the MII transmit AC timing specifications.

**Table 34. MII transmit AC timing specifications**

For recommended operating conditions, see Table 3.

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| TX_CLK clock period 10 Mbps | $t_{MTX}$ | 399.96 | 400 | 400.04 | ns |
| TX_CLK clock period 100 Mbps | $t_{MTX}$ | 39.996 | 40 | 40.004 | ns |
| TX_CLK duty cycle | $t_{MTXH}/t_{MTX}$ | 35 | — | 65 | % |
| TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay | $t_{MTKHDX}$ | 0 | — | 25 | ns |
| TX_CLK data clock rise (20%–80%) | $t_{MTXR}$ | 1.0 | — | 4.0 | ns |
| TX_CLK data clock fall (80%–20%) | $t_{MTXF}$ | 1.0 | — | 4.0 | ns |

This figure shows the MII transmit AC timing diagram.

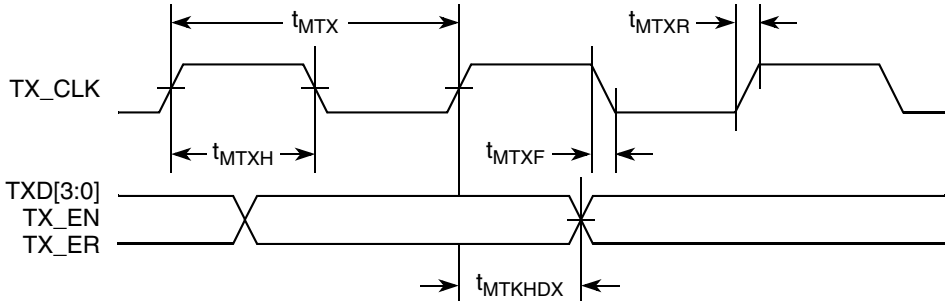



**Figure 15. MII transmit AC timing diagram**

This table provides the MII receive AC timing specifications.

**Table 35. MII Receive AC timing specifications**

For recommended operating conditions, see Table 3.

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| RX_CLK clock period 10 Mbps | $t_{MRX}$ | 399.96 | 400 | 400.04 | ns |
| RX_CLK clock period 100 Mbps | $t_{MRX}$ | 39.996 | 40 | 40.004 | ns |
| RX_CLK duty cycle | $t_{MRXH}/t_{MRX}$ | 35 | — | 65 | % |
| RXD[3:0], RX_DV, RX_ER setup time to RX_CLK | $t_{MRDVKH}$ | 10.0 | — | — | ns |
| RXD[3:0], RX_DV, RX_ER hold time to RX_CLK | $t_{MRDXKH}$ | 10.0 | — | — | ns |
| RX_CLK clock rise (20%-80%) | $t_{MRXR}$ | 1.0 | — | 4.0 | ns |
| RX_CLK clock fall time (80%-20%) | $t_{MRXF}$ | 1.0 | — | 4.0 | ns |

**Note:** The frequency of RX_CLK should not exceed frequency of GTX_CLK125 by more than 300ppm.

**Table 41. Ethernet management interface 2 AC timing specifications (continued)**

For recommended operating conditions, see Table 3.

| Parameter/Condition | Symbol[1] | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|
| MDIO to MDC hold time | $t_{MDDXKH}$ | 0 | — | — | ns | — |

**Note:**

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{MDKHDX}$ symbolizes management data timing (MD) for the time $t_{MDC}$ from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, $t_{MDDVKH}$ symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the $t_{MDC}$ clock reference (K) going to the high (H) state or setup time.
2. This parameter is dependent on the frame manager clock frequency (MIIMCFG [MgmtClk] field determines the clock frequency of the MgmtClk Clock EC_MDC).
3. This parameter is dependent on the management data clock frequency, $f_{MDC}$. The delay is equal to 0.5 management data clock period ±6 ns. For example, with a management data clock of 2.5 MHz, the min/max delay is 200 ns ± 6 ns.

This figure shows the Ethernet management interface timing diagram.

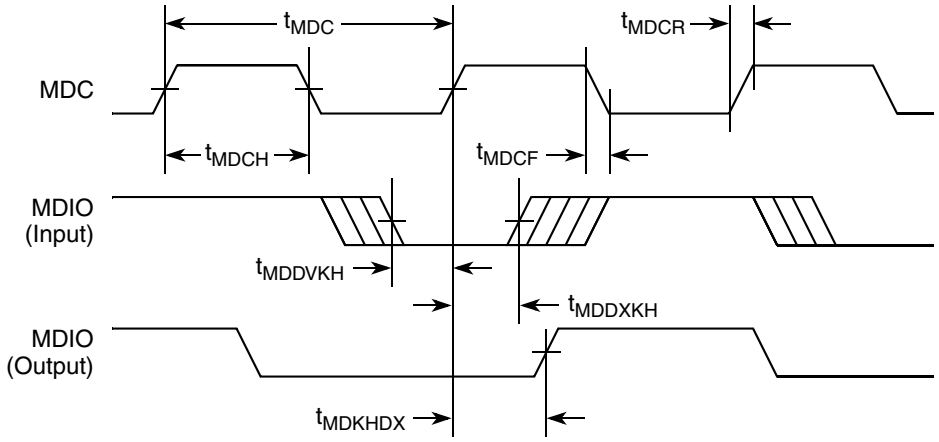



**Figure 19. Ethernet management interface timing diagram**

## 2.12.4 eTSEC IEEE Std 1588 timing specifications

This section discusses the electrical characteristics for the eTSEC IEEE Std 1588 interfaces.

### 2.12.4.1 eTSEC IEEE Std 1588 DC electrical characteristics

This table shows eTSEC IEEE Std 1588 DC electrical characteristics when operating at $LV_{DD}$ = 3.3 V supply.

**Table 42. eTSEC IEEE 1588 DC electrical characteristics ($LV_{DD}$ = 3.3 V)**

For recommended operating conditions, see Table 3.

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Input high voltage | $V_{IH}$ | 2.0 | — | V | 2 |
| Input low voltage | $V_{IL}$ | — | 0.9 | V | 2 |
| Input high current ($LV_{DD}$ = Max, $V_{IN}$ = 2.1 V) | $I_{IH}$ | — | 40 | μA | 1 |

— For an external AC-coupled connection, there is no common mode voltage requirement for the clock driver. Because the external AC-coupling capacitor blocks the DC level, the clock driver and the SerDes reference clock receiver operate in different common mode voltages. The SerDes reference clock receiver in this connection scheme has its common mode voltage set to SGND. Each signal wire of the differential inputs is allowed to swing below and above the common mode voltage (SGND). Figure 38 shows the SerDes reference clock input requirement for AC-coupled connection scheme.

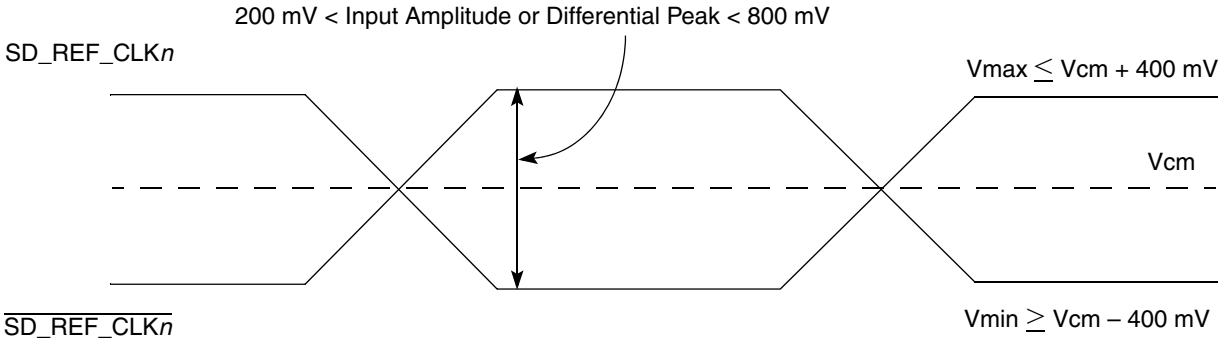



**Figure 38. Differential reference clock input DC requirements (external AC-coupled)**

- Single-Ended Mode
  — The reference clock can also be single-ended. The SD_REF_CLK*n* input amplitude (single-ended swing) must be between 400 mV and 800 mV peak-peak (from $V_{MIN}$ to $V_{MAX}$) with $\overline{\text{SD\_REF\_CLK}n}$ either left unconnected or tied to ground.
  — The SD_REF_CLK*n* input average voltage must be between 200 and 400 mV. Figure 39 shows the SerDes reference clock input requirement for single-ended signaling mode.
  — To meet the input amplitude requirement, the reference clock inputs may need to be DC- or AC-coupled externally. For the best noise performance, the reference of the clock could be DC- or AC-coupled into the unused phase ($\overline{\text{SD\_REF\_CLK}n}$) through the same source impedance as the clock input (SD_REF_CLK*n*) in use.

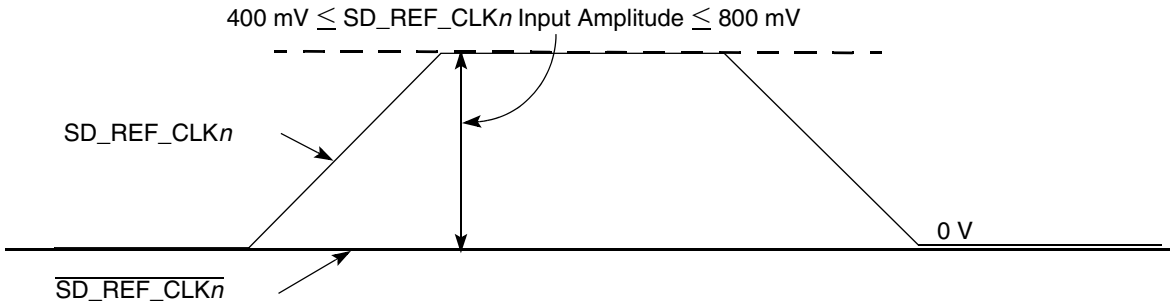



**Figure 39. Single-ended reference clock input DC requirements**

### 2.20.2.3 AC requirements for SerDes reference clocks

This table lists AC requirements for the PCI Express, SGMII, Serial RapidIO and Aurora SerDes reference clocks to be guaranteed by the customer's application design.

**Table 61. SD_REF_CLK*n* and $\overline{\text{SD\_REF\_CLK}n}$ input clock requirements ($SV_{DD}$ = 1.0 V)**

For recommended operating conditions, see Table 3.

| Parameter | Symbol | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ frequency range | $t_{CLK\_REF}$ | — | 100/125 | — | MHz | 1 |
| SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ clock frequency tolerance | $t_{CLK\_TOL}$ | –350 | — | 350 | ppm | — |
| SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ reference clock duty cycle | $t_{CLK\_DUTY}$ | 40 | 50 | 60 | % | 4 |
| SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ max deterministic peak-peak jitter at $10^{-6}$ BER | $t_{CLK\_DJ}$ | — | — | 42 | ps | — |
| SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ total reference clock jitter at $10^{-6}$ BER (peak-to-peak jitter at refClk input) | $t_{CLK\_TJ}$ | — | — | 86 | ps | 2 |
| SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ rising/falling edge rate | $t_{CLKRR}/t_{CLKFR}$ | 1 | — | 4 | V/ns | 3 |
| Differential input high voltage | $V_{IH}$ | 200 | — | — | mV | 4 |
| Differential input low voltage | $V_{IL}$ | — | — | –200 | mV | 4 |
| Rising edge rate (SD_REF_CLK*n*) to falling edge rate (SD_REF_CLK*n*) matching | Rise-Fall Matching | — | — | 20 | % | 5, 6 |

**Notes:**

1. **Caution:** Only 100 and 125 have been tested. In-between values not work correctly with the rest of the system.
2. Limits from PCI Express CEM Rev 2.0
3. Measured from –200 mV to +200 mV on the differential waveform (derived from SD_REF_CLK*n* minus $\overline{\text{SD\_REF\_CLK}n}$). The signal must be monotonic through the measurement region for rise and fall time. The 400 mV measurement window is centered on the differential zero crossing. See Figure 40.
4. Measurement taken from differential waveform
5. Measurement taken from single-ended waveform
6. Matching applies to rising edge for SD_REF_CLK*n* and falling edge rate for $\overline{\text{SD\_REF\_CLK}n}$. It is measured using a 200 mV window centered on the median cross point where SD_REF_CLK*n* rising meets $\overline{\text{SD\_REF\_CLK}n}$ falling. The median cross point is used to calculate the voltage thresholds that the oscilloscope uses for the edge rate calculations. The rise edge rate of SD_REF_CLK*n* should be compared to the fall edge rate of $\overline{\text{SD\_REF\_CLK}n}$, the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 41.

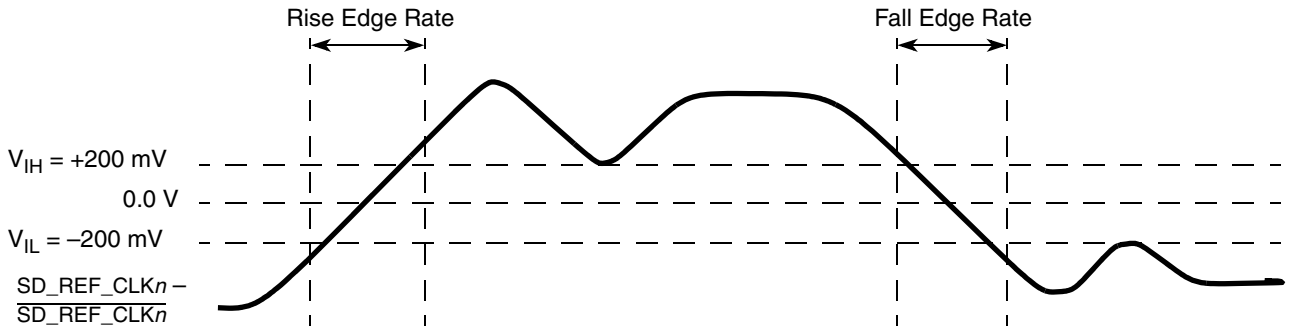



**Figure 40. Differential measurement points for rise and fall time**

This table defines the PCI Express 2.0 (5 GT/s) DC specifications for the differential output at all transmitters. The parameters are specified at the component pins.

**Table 63. PCI Express 2.0 (5 GT/s) differential transmitter output DC specifications ($XV_{DD}$ = 1.5 V or 1.8 V)**

For recommended operating conditions, see Table 3.

| Parameter | Symbol | Min | Typical | Max | Units | Notes |
|---|---|---|---|---|---|---|
| Differential peak-to-peak output voltage | $V_{TX-DIFFp-p}$ | 800 | — | 1200 | mV | $V_{TX-DIFFp-p} = 2 \times \lvert V_{TX-D+} - V_{TX-D-} \rvert$ See Note 1. |
| Low Power differential peak-to-peak output voltage | $V_{TX-DIFFp-p\_low}$ | 400 | 500 | 1200 | mV | $V_{TX-DIFFp-p} = 2 \times \lvert V_{TX-D+} - V_{TX-D-} \rvert$ See Note 1. |
| De-emphasized differential output voltage (ratio) | $V_{TX-DE-RATIO-3.5dB}$ | 3.0 | 3.5 | 4.0 | dB | Ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition. See Note 1. |
| De-emphasized differential output voltage (ratio) | $V_{TX-DE-RATIO-6.0dB}$ | 5.5 | 6.0 | 6.5 | dB | Ratio of the $V_{TX-DIFFp-p}$ of the second and following bits after a transition divided by the $V_{TX-DIFFp-p}$ of the first bit after a transition. See Note 1. |
| DC differential transmitter impedance | $Z_{TX-DIFF-DC}$ | 80 | 100 | 120 | Ω | Transmitter DC differential mode low impedance |
| Transmitter DC Impedance | $Z_{TX-DC}$ | 40 | 50 | 60 | Ω | Required transmitter D+ as well as D– DC impedance during all states |

**Note:**
1. Measured at the package pins with a test load of 50Ω to GND on each pin.

## 2.20.4.4 PCI Express DC physical layer receiver specifications

This section discusses the PCI Express DC physical layer receiver specifications 2.5 GT/s, and 5 GT/s.

This table defines the DC specifications for the PCI Express 2.0 (2.5 GT/s) differential input at all receivers. The parameters are specified at the component pins.

**Table 64. PCI Express 2.0 (2.5 GT/s) differential receiver input DC specifications ($XV_{DD}$ = 1.5 V or 1.8 V)**

For recommended operating conditions, see Table 3.

| Parameter | Symbol | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| Differential input peak-to-peak voltage | $V_{RX-DIFFp-p}$ | 120 | — | 1200 | mV | $V_{RX-DIFFp-p} = 2 \times \lvert V_{RX-D+} - V_{RX-D-} \rvert$ See Note 1. |
| DC differential input impedance | $Z_{RX-DIFF-DC}$ | 80 | 100 | 120 | Ω | Receiver DC differential mode impedance. See Note 2 |
| DC input impedance | $Z_{RX-DC}$ | 40 | 50 | 60 | Ω | Required receiver D+ as well as D– DC Impedance (50 ±20% tolerance). See Notes 1 and 2. |

**Table 88. SGMII DC transmitter electrical characteristics ($XV_{DD}$ = 1.5 V or 1.8 V) (continued)**

For recommended operating conditions, see Table 3.

| Parameter | Symbol | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| Output differential voltage[2, 3, 4] ($XV_{DD-Typ}$ at 1.5 V and 1.8 V) | $\|V_{OD}\|$ | 320 | 500.0 | 725.0 | mV | B(1-3)TECR(lane)0[AMP_RED] =0b000000 |
| | | 293.8 | 459.0 | 665.6 | | B(1-3)TECR(lane)0[AMP_RED] =0b000010 |
| | | 266.9 | 417.0 | 604.7 | | B(1-3)TECR(lane)0[AMP_RED] =0b000101 |
| | | 240.6 | 376.0 | 545.2 | | B(1-3)TECR(lane)0[AMP_RED] =0b001000 |
| | | 213.1 | 333.0 | 482.9 | | B(1-3)TECR(lane)0[AMP_RED] =0b001100 |
| | | 186.9 | 292.0 | 423.4 | | B(1-3)TECR(lane)0[AMP_RED] =0b001111 |
| | | 160.0 | 250.0 | 362.5 | | B(1-3)TECR(lane)0[AMP_RED] =0b010011 |
| Output impedance (single-ended) | $R_O$ | 40 | 50 | 60 | Ω | — |

**Notes:**

1. This does not align to DC-coupled SGMII.
2. $|V_{OD}| = |V_{SD\_TXn} - V_{\overline{SD\_TXn}}|$. $|V_{OD}|$ is also referred to as output differential peak voltage. $V_{TX-DIFFp-p} = 2*|V_{OD}|$.
3. Example amplitude reduction setting for SGMII on SerDes bank 1 lane E: B1TECRE0[AMP_RED] = 0b000010 for an output differential voltage of 459 mV typical.
4. The $|V_{OD}|$ value shown in the Typ column is based on the condition of XVDD_SRDSn-Typ = 1.5 V or 1.8 V, no common mode offset variation. SerDes transmitter is terminated with 100-Ω differential load between SD_TX*n* and $\overline{\text{SD\_TX}n}$.