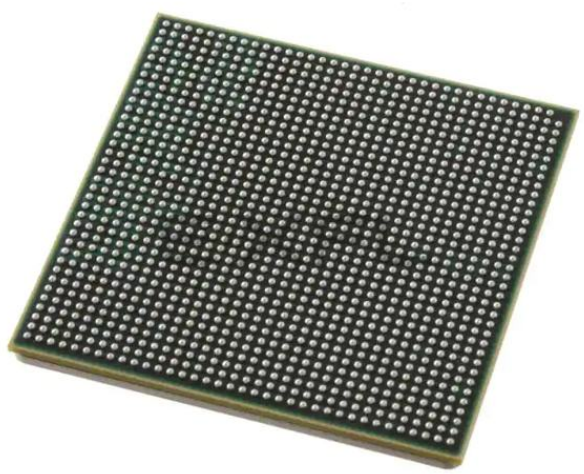

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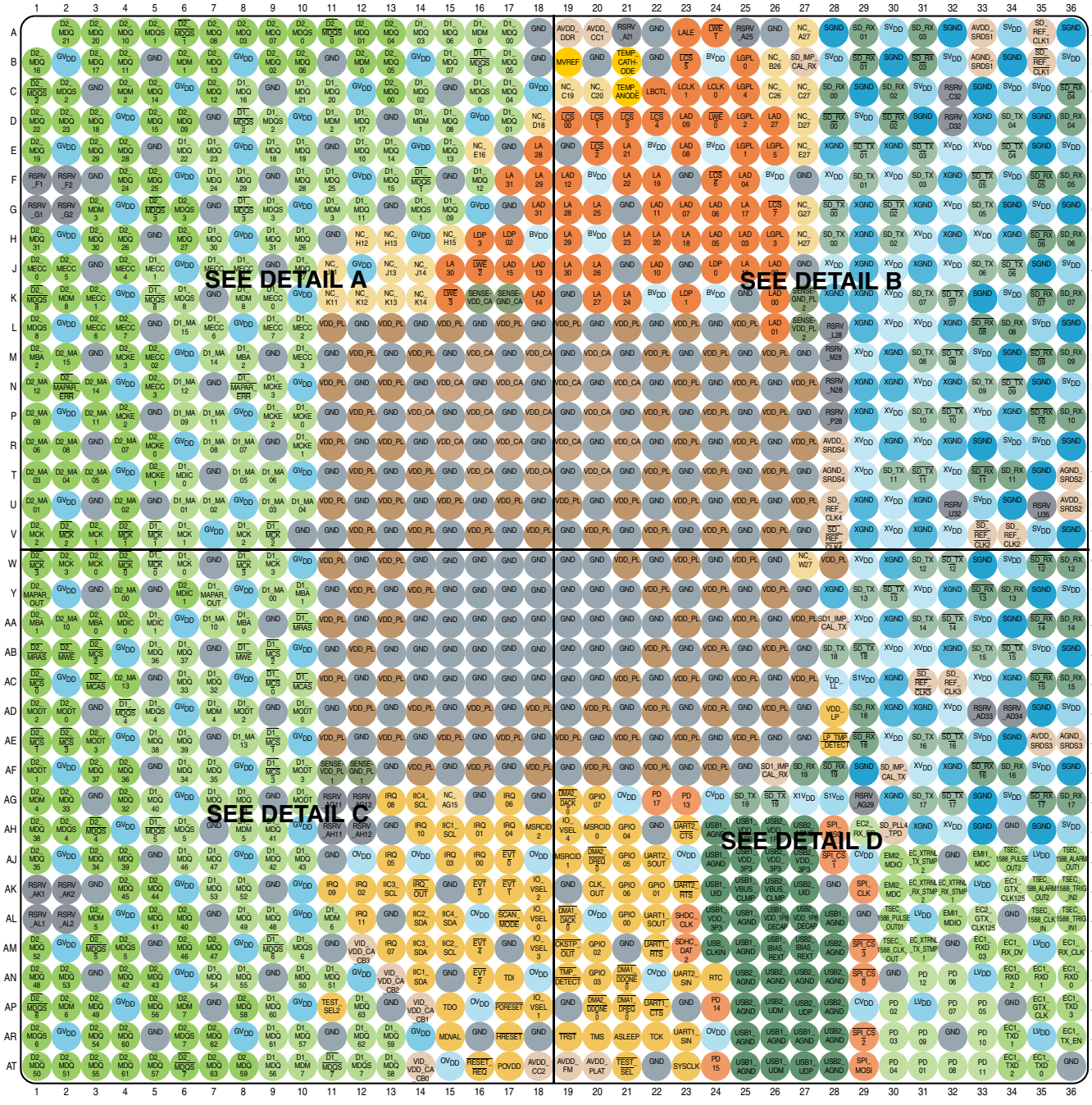
Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e5500
Number of Cores/Bus Width	2 Core, 64-Bit
Speed	2.2GHz
Co-Processors/DSP	-
RAM Controllers	DDR3, DDR3L
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	1Gbps (10), 10Gbps (2)
SATA	SATA 3Gbps (2)
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.0V, 1.2V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	1295-BBGA, FCBGA
Supplier Device Package	1295-FCPBGA (37.5x37.5)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p5021nxn72qc



Signal Groups

- OV_{DD} I/O Supply Voltage
- LV_{DD} I/O Supply Voltage
- GV_{DD} DDR DRAM I/O Supply
- CV_{DD} SPI Voltage Supply
- BV_{DD} Local Bus I/O Supply
- SV_{DD} SerDes Core Power Supply
- XV_{DD} SerDes Transcvr Pad Supply
- VDD_{PL} Platform Supply Voltage
- VDD_{CA} Core Group A Supply Voltage
- $AVDD_{SRDS1}$ SerDes 1 PLL Supply Voltage
- $AVDD_{SRDS2}$ SerDes 2 PLL Supply Voltage
- $AVDD_{PLAT}$ Platform PLL Supply Voltage
- $AVDD_{CC}$ Core PLL Supply Voltage
- $SENSE_{VDD\_PL}$ Platform Voltage Sense
- $SENSE_{VDD}$ Core Group A Voltage Sense
- $SENSE_{VDD\_CB}$ Core Group B Voltage Sense
- RSRV Reserved
- POVDD Fuse Programming Override Supply

Figure 2. 1295 BGA ball map diagram (top view)

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
D1_MECC1	Error Correcting Code	J5	I/O	GV_{DD}	—
D1_MECC2	Error Correcting Code	L10	I/O	GV_{DD}	—
D1_MECC3	Error Correcting Code	M10	I/O	GV_{DD}	—
D1_MECC4	Error Correcting Code	J8	I/O	GV_{DD}	—
D1_MECC5	Error Correcting Code	J7	I/O	GV_{DD}	—
D1_MECC6	Error Correcting Code	L7	I/O	GV_{DD}	—
D1_MECC7	Error Correcting Code	L9	I/O	GV_{DD}	—
$\overline{\text{D1\_MAPAR\_ERR}}$	Address Parity Error	N8	I	GV_{DD}	40
D1_MAPAR_OUT	Address Parity Out	Y7	O	GV_{DD}	—
D1_MDM0	Data Mask	A16	O	GV_{DD}	—
D1_MDM1	Data Mask	D14	O	GV_{DD}	—
D1_MDM2	Data Mask	D11	O	GV_{DD}	—
D1_MDM3	Data Mask	G11	O	GV_{DD}	—
D1_MDM4	Data Mask	AD7	O	GV_{DD}	—
D1_MDM5	Data Mask	AH8	O	GV_{DD}	—
D1_MDM6	Data Mask	AL11	O	GV_{DD}	—
D1_MDM7	Data Mask	AT10	O	GV_{DD}	—
D1_MDM8	Data Mask	K8	O	GV_{DD}	—
D1_MDQS0	Data Strobe	C16	I/O	GV_{DD}	—
D1_MDQS1	Data Strobe	G14	I/O	GV_{DD}	—
D1_MDQS2	Data Strobe	D9	I/O	GV_{DD}	—
D1_MDQS3	Data Strobe	G9	I/O	GV_{DD}	—
D1_MDQS4	Data Strobe	AD5	I/O	GV_{DD}	—
D1_MDQS5	Data Strobe	AH6	I/O	GV_{DD}	—
D1_MDQS6	Data Strobe	AM10	I/O	GV_{DD}	—
D1_MDQS7	Data Strobe	AT12	I/O	GV_{DD}	—
D1_MDQS8	Data Strobe	K6	I/O	GV_{DD}	—
$\overline{\text{D1\_MDQS0}}$	Data Strobe	B16	I/O	GV_{DD}	—
$\overline{\text{D1\_MDQS1}}$	Data Strobe	F14	I/O	GV_{DD}	—
$\overline{\text{D1\_MDQS2}}$	Data Strobe	D8	I/O	GV_{DD}	—
$\overline{\text{D1\_MDQS3}}$	Data Strobe	G8	I/O	GV_{DD}	—
$\overline{\text{D1\_MDQS4}}$	Data Strobe	AD4	I/O	GV_{DD}	—
$\overline{\text{D1\_MDQS5}}$	Data Strobe	AH5	I/O	GV_{DD}	—
$\overline{\text{D1\_MDQS6}}$	Data Strobe	AM9	I/O	GV_{DD}	—

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
SDHC_DAT0	Data	AP24	I/O	CV_{DD}	—
SDHC_DAT1	Data	AT24	I/O	CV_{DD}	—
SDHC_DAT2	Data	AM23	I/O	CV_{DD}	—
SDHC_DAT3	Data	AG22	I/O	CV_{DD}	—
SDHC_DAT4/$\overline{\text{SPI\_CS0}}$	Data	AN29	I/O	CV_{DD}	26, 31
SDHC_DAT5/$\overline{\text{SPI\_CS1}}$	Data	AJ28	I/O	CV_{DD}	26, 31
SDHC_DAT6/$\overline{\text{SPI\_CS2}}$	Data	AR29	I/O	CV_{DD}	26, 31
SDHC_DAT7/$\overline{\text{SPI\_CS3}}$	Data	AM29	I/O	CV_{DD}	26, 31
SDHC_CLK	Host to Card Clock	AL23	O	CV_{DD}	—
$\overline{\text{SDHC\_CD}}$/IIC3_SCL/GPIO16	Card Detection	AK13	I	OV_{DD}	26,27,31
SDHC_WP/IIC3_SDA/GPIO17	Card Write Protection	AM14	I	OV_{DD}	26,27,31
eSPI					
SPI_MOSI	Master Out Slave In	AT29	I/O	CV_{DD}	—
SPI_MISO	Master In Slave Out	AH28	I	CV_{DD}	—
SPI_CLK	eSPI clock	AK29	O	CV_{DD}	—
$\overline{\text{SPI\_CS0}}$/SDHC_DAT4	eSPI chip select	AN29	O	CV_{DD}	26
$\overline{\text{SPI\_CS1}}$/SDHC_DAT5	eSPI chip select	AJ28	O	CV_{DD}	26
$\overline{\text{SPI\_CS2}}$/SDHC_DAT6	eSPI chip select	AR29	O	CV_{DD}	26
$\overline{\text{SPI\_CS3}}$/SDHC_DAT7	eSPI chip select	AM29	O	CV_{DD}	26
IEEE 1588					
TSEC_1588_CLK_IN	Clock In	AL35	I	LV_{DD}	—
TSEC_1588_TRIG_IN1	Trigger In 1	AL36	I	LV_{DD}	—
TSEC_1588_TRIG_IN2/EC1_RX_ER	Trigger In 2	AK36	I	LV_{DD}	—
TSEC_1588_ALARM_OUT1	Alarm Out 1	AJ36	O	LV_{DD}	—
TSEC_1588_ALARM_OUT2/EC1_COL/GPIO30	Alarm Out 2	AK35	O	LV_{DD}	26
TSEC_1588_CLK_OUT	Clock Out	AM30	O	LV_{DD}	—
TSEC_1588_PULSE_OUT1	Pulse Out1	AL30	O	LV_{DD}	—
TSEC_1588_PULSE_OUT2/EC1_CRS/GPIO31	Pulse Out2	AJ34	O	LV_{DD}	26
Ethernet Management interface 1					
EMI1_MDC	Management Data Clock	AJ33	O	LV_{DD}	—
EMI1_MDIO	Management Data In/Out	AL32	I/O	LV_{DD}	—
Ethernet Management interface 2					
EMI2_MDC	Management Data Clock	AK30	O	1.2 V	2, 18, 22

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
EC2_GTX_CLK/ EC2_TX_ER	Transmit Clock Out (RGMII) Transmit Error (MII)	AN31	O	LV_{DD}	26
EC2_RXD3	Receive Data	AP33	I	LV_{DD}	27
EC2_RXD2	Receive Data	AN32	I	LV_{DD}	27
EC2_RXD1	Receive Data	AP32	I	LV_{DD}	26, 27
EC2_RXD0	Receive Data	AT32	I	LV_{DD}	26, 27
EC2_RX_DV	Receive Data Valid	AR33	I	LV_{DD}	27
EC2_RX_CLK	Receive Clock	AT33	I	LV_{DD}	27
EC2_RX_ER	Receive Error (MII)	AH29	I	LV_{DD}	—
EC2_COL/EC_XTRNL_TX_STMP2	Collision Detect (MII)	AJ31	O	LV_{DD}	26
EC2_CRS/EC_XTRNL_RX_STMP2	Carrier Sense (MII)	AK31	O	LV_{DD}	26
UART					
UART1_SOUT/GPIO8	Transmit Data	AL22	O	OV_{DD}	26
UART2_SOUT/GPIO9	Transmit Data	AJ22	O	OV_{DD}	26
UART1_SIN/GPIO10	Receive Data	AR23	I	OV_{DD}	26
UART2_SIN/GPIO11	Receive Data	AN23	I	OV_{DD}	26
$\overline{\text{UART1\_RTS}}$/UART3_SOUT/GPIO12	Ready to Send	AM22	O	OV_{DD}	26
$\overline{\text{UART2\_RTS}}$/UART4_SOUT/GPIO13	Ready to Send	AK23	O	OV_{DD}	26
$\overline{\text{UART1\_CTS}}$/UART3_SIN/GPIO14	Clear to Send	AP22	I	OV_{DD}	26
$\overline{\text{UART2\_CTS}}$/UART4_SIN/GPIO15	Clear to Send	AH23	I	OV_{DD}	26
I^2C interface					
IIC1_SCL	Serial Clock	AH15	I/O	OV_{DD}	2, 14
IIC1_SDA	Serial Data	AN14	I/O	OV_{DD}	2, 14
IIC2_SCL	Serial Clock	AM15	I/O	OV_{DD}	2, 14
IIC2_SDA	Serial Data	AL14	I/O	OV_{DD}	2, 14
IIC3_SCL/$\overline{\text{SDHC\_CD}}$/GPIO16	Serial Clock	AK13	I/O	OV_{DD}	2, 14, 27
IIC3_SDA/SDHC_WP/GPIO17	Serial Data	AM14	I/O	OV_{DD}	2, 14, 27
IIC4_SCL/$\overline{\text{EVT5}}$	Serial Clock	AG14	I/O	OV_{DD}	2, 14
IIC4_SDA/$\overline{\text{EVT6}}$	Serial Data	AL15	I/O	OV_{DD}	2, 14
SerDes (x20) PCIe, Aurora, 10GE, 1GE, SATA					
SD_TX19	Transmit Data (positive)	AG25	O	XV_{DD}	—
SD_TX18	Transmit Data (positive)	AB28	O	XV_{DD}	—
SD_TX17	Transmit Data (positive)	AG31	O	XV_{DD}	—
SD_TX16	Transmit Data (positive)	AE31	O	XV_{DD}	—

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
$\overline{\text{SD\_RX07}}$	Receive Data (negative)	K35	I	XV_{DD}	—
$\overline{\text{SD\_RX06}}$	Receive Data (negative)	H35	I	XV_{DD}	—
$\overline{\text{SD\_RX05}}$	Receive Data (negative)	F35	I	XV_{DD}	—
$\overline{\text{SD\_RX04}}$	Receive Data (negative)	C36	I	XV_{DD}	—
$\overline{\text{SD\_RX03}}$	Receive Data (negative)	B31	I	XV_{DD}	—
$\overline{\text{SD\_RX02}}$	Receive Data (negative)	D30	I	XV_{DD}	—
$\overline{\text{SD\_RX01}}$	Receive Data (negative)	B29	I	XV_{DD}	—
$\overline{\text{SD\_RX00}}$	Receive Data (negative)	D28	I	XV_{DD}	—
SD_REF_CLK1	SerDes Bank 1 PLL Reference Clock	A35	I	XV_{DD}	—
$\overline{\text{SD\_REF\_CLK1}}$	SerDes Bank 1 PLL Reference Clock Complement	B35	I	XV_{DD}	—
SD_REF_CLK2	SerDes Bank 2 PLL Reference Clock	V34	I	XV_{DD}	—
$\overline{\text{SD\_REF\_CLK2}}$	SerDes Bank 2 PLL Reference Clock Complement	V33	I	XV_{DD}	—
SD_REF_CLK3	SerDes Bank 3 PLL Reference Clock	AC32	I	XVDD	—
$\overline{\text{SD\_REF\_CLK3}}$	SerDes Bank 3 PLL Reference Clock Complement	AC31	I	XVDD	—
SD_REF_CLK4	SerDes Bank 4 PLL Reference Clock	U28	I	XVDD	—
$\overline{\text{SD\_REF\_CLK4}}$	SerDes Bank 4 PLL Reference Clock Complement	V28	I	XVDD	—
General-Purpose Input/Output					
GPIO00	General Purpose Input / Output	AL21	I/O	OV_{DD}	—
GPIO01	General Purpose Input / Output	AK22	I/O	OV_{DD}	—
GPIO02	General Purpose Input / Output	AM20	I/O	OV_{DD}	—
GPIO03	General Purpose Input / Output	AN20	I/O	OV_{DD}	—
GPIO04/USB1_DRVVBUS	General Purpose Input / Output	AH21	I/O	OV_{DD}	—
GPIO05/USB1_PWRFAULT	General Purpose Input / Output	AJ21	I/O	OV_{DD}	—
GPIO06/USB2_DRVVBUS	General Purpose Input / Output	AK21	I/O	OV_{DD}	—
GPIO07/USB2_PWRFAULT	General Purpose Input / Output	AG20	I/O	OV_{DD}	—
GPIO08/UART1_SOUT	General Purpose Input / Output	AL22	I/O	OV_{DD}	—
GPIO09/UART2_SOUT	General Purpose Input / Output	AJ22	I/O	OV_{DD}	—
GPIO10/UART1_SIN	General Purpose Input / Output	AR23	I/O	OV_{DD}	—
GPIO11/UART2_SIN	General Purpose Input / Output	AN23	I/O	OV_{DD}	—

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GND	Ground	W22	—	—	—
GND	Ground	U22	—	—	—
GND	Ground	R22	—	—	—
GND	Ground	N22	—	—	—
GND	Ground	AF23	—	—	—
GND	Ground	AD23	—	—	—
GND	Ground	AB23	—	—	—
GND	Ground	Y23	—	—	—
GND	Ground	V23	—	—	—
GND	Ground	T23	—	—	—
GND	Ground	P23	—	—	—
GND	Ground	M23	—	—	—
GND	Ground	L24	—	—	—
GND	Ground	N24	—	—	—
GND	Ground	R24	—	—	—
GND	Ground	U24	—	—	—
GND	Ground	W24	—	—	—
GND	Ground	AA24	—	—	—
GND	Ground	AC24	—	—	—
GND	Ground	AE24	—	—	—
GND	Ground	AF25	—	—	—
GND	Ground	AD25	—	—	—
GND	Ground	AB25	—	—	—
GND	Ground	Y25	—	—	—
GND	Ground	P27	—	—	—
GND	Ground	V17	—	—	—
GND	Ground	T25	—	—	—
GND	Ground	P25	—	—	—
GND	Ground	M25	—	—	—
GND	Ground	T27	—	—	—
GND	Ground	V27	—	—	—
GND	Ground	Y27	—	—	—
GND	Ground	AD27	—	—	—
GND	Ground	L12	—	—	—

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
XVDD	SerDes Transceiver Supply	Y31	—	XV_{DD}	—
XVDD	SerDes Transceiver Supply	AH32	—	XV_{DD}	—
X1VDD	SerDes Transceiver Supply	AG27	—	XV_{DD}	—
VDD_LL	SerDes B4 Logic supply	AC28	—	VDD_PL	43
LVDD	Ethernet Controller 1 and 2 Supply	AK33	—	LV_{DD}	—
LVDD	Ethernet Controller 1 and 2 Supply	AP31	—	LV_{DD}	—
LVDD	Ethernet Controller 1 and 2 Supply	AL31	—	LV_{DD}	—
LVDD	Ethernet Controller 1 and 2 Supply	AN33	—	LV_{DD}	—
LVDD	Ethernet Controller 1 and 2 Supply	AJ35	—	LV_{DD}	—
LVDD	Ethernet Controller 1 and 2 Supply	AR35	—	LV_{DD}	—
LVDD	Ethernet Controller 1 and 2 Supply	AM35	—	LV_{DD}	—
POVDD	Fuse Programming Override Supply	AT17	—	POV_{DD}	33
VDD_PL	Platform Supply	M26	—	V_{DD_PL}	—
VDD_PL	Platform Supply	P26	—	V_{DD_PL}	—
VDD_PL	Platform Supply	T26	—	V_{DD_PL}	—
VDD_PL	Platform Supply	V26	—	V_{DD_PL}	—
VDD_PL	Platform Supply	Y26	—	V_{DD_PL}	—
VDD_PL	Platform Supply	AB26	—	V_{DD_PL}	—
VDD_PL	Platform Supply	AD26	—	V_{DD_PL}	—
VDD_PL	Platform Supply	N11	—	V_{DD_PL}	—
VDD_PL	Platform Supply	R11	—	V_{DD_PL}	—
VDD_PL	Platform Supply	W11	—	V_{DD_PL}	—
VDD_PL	Platform Supply	AA11	—	V_{DD_PL}	—
VDD_PL	Platform Supply	AE11	—	V_{DD_PL}	—
VDD_PL	Platform Supply	M12	—	V_{DD_PL}	—
VDD_PL	Platform Supply	P12	—	V_{DD_PL}	—
VDD_PL	Platform Supply	T12	—	V_{DD_PL}	—
VDD_PL	Platform Supply	V12	—	V_{DD_PL}	—
VDD_PL	Platform Supply	Y12	—	V_{DD_PL}	—
VDD_PL	Platform Supply	AB12	—	V_{DD_PL}	—
VDD_PL	Platform Supply	AD12	—	V_{DD_PL}	—
VDD_PL	Platform Supply	AE13	—	V_{DD_PL}	—
VDD_PL	Platform Supply	AE15	—	V_{DD_PL}	—

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes

Notes:

1. Recommend a weak pull-up resistor (2–10 kΩ) be placed on this pin to OV_{DD}.
2. This pin is an open drain signal.
3. This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state. This pull-up is designed such that it can be overpowered by an external 4.7-kΩ resistor. However, if the signal is intended to be high after reset, and if there is any device on the net which might pull down the value of the net at reset, then a pull up or active driver is needed.
4. Functionally, this pin is an output, but structurally it is an I/O because it either samples configuration input during reset or because it has other manufacturing test functions. This pin is therefore described as an I/O for boundary scan.
5. Recommend a weak pull-up resistor (2–10 kΩ) be placed on this pin to BV_{DD}, to ensure no random chip select assertion due to possible noise, and so forth.
6. This output is actively driven during reset rather than being three-stated during reset.
7. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
8. These pins are connected to the correspondent power and ground nets internally and may be connected as a differential pair to be used by the voltage regulators with remote sense function.
9. These pins may be connected to a thermal diode monitoring device such as the ADT7461A only with a clear understanding that proper thermal diode operation is not implied and the thermal diode feature may not be available in the production device.
11. Do not connect.
12. These are test signals for factory use only and must be pulled up (100 Ω–1 kΩ) to OV_{DD} for normal device operation.
13. Independent supplies derived from board V_{DD_PL} (Core clusters, Platform, DDR) or SV_{DD} (SerDes).
14. Recommend a pull-up resistor of 1-kΩ be placed on this pin to OV_{DD} if I2C interface is used.
15. This pin requires an external 1-kΩ pull-down resistor to prevent PHY from seeing a valid Transmit Enable before it is actively driven.
16. For DDR3 and DDR3L, D*n*_MDIC[0] is grounded through an 40.2-Ω (half-strength mode) precision 1% resistor and D*n*_MDIC[1] is connected to GV_{DD} through an 40.2-Ω (half-strength mode) precision 1% resistor. These pins are used for automatic calibration of the DDR3 and DDR3L IOs.
18. These pins should be pulled up to 1.2V through a $180\Omega \pm 1\%$ resistor for EM2_MDC and a $330\Omega \pm 1\%$ resistor for EM2_MDIO.
20. Pin has a weak internal pull-up.
21. These pins should be pulled to ground (GND).
22. Ethernet Management interface 2 pins function as open drain I/Os. The interface shall conform to 1.2 V nominal voltage levels. LV_{DD} must be powered to use this interface.
23. This pin requires a 200-Ω pull-up to XV_{DD}.
24. This pin requires a 200-Ω pull-up to SV_{DD}.
25. This GPIO pin is on LV_{DD} power plane, not OV_{DD}.
26. Functionally, this pin is an I/O, but may act as an output only or an input only depending on the pin mux configuration defined by the RCW.
27. See Section 3.6, "Connection recommendations," for additional details on this signal.
28. This signal must be pulled low to GND.
30. Warning, incorrect voltage select settings can lead to irreversible device damage. See Section 3.2, "Supply power default setting."
31. SDHC_DAT[4:7] require CV_{DD} = 3.3 V when muxed extended SDHC data signals are enabled via the RCW[SPI] field.
32. The *cfg_xvdd_sel*(LAD[26]) reset configuration pin must select the correct voltage that is being supplied on the XV_{DD} pin. Incorrect voltage select settings can lead to irreversible device damage.

This table shows the estimated power dissipation on the POV_{DD} supply for the chip, at allowable voltage levels.

Table 8. POV_{DD} power dissipation

Supply	Maximum	Unit	Notes
POV_{DD}	450	mW	1

Note:

1. To ensure device reliability, fuse programming must be performed within the recommended fuse programming temperature range per Table 3.

This table shows the estimated power dissipation on the V_{DD_LP} supply for the chip, at allowable voltage levels.

Table 9. V_{DD_LP} Power Dissipation

Supply	Maximum	Unit	Note
V_{DD_LP} (P5021 on, 105C)	1.5	mW	1
V_{DD_LP} (P5021 off, 70C)	195	uW	2
V_{DD_LP} (P5021 off, 40C)	132	uW	2

Note:

1. V_{DD_LP} = 1.0 V, T_J = 105°C.
2. When P5021 is off, V_{DD_LP} may be supplied by battery power to the Zeroizable Master Key and other Trust Architecture state. Board should implement a PMIC which switches V_{DD_LP} to battery when P5021 is powered down. See P5040 Reference Manual Trust Architecture chapter for more information.

2.5 Thermal

This table shows the thermal characteristics for the chip.

Table 10. Package thermal characteristics [6]

Rating	Board	Symbol	Value	Unit	Notes
Junction to ambient, natural convection	Single-layer board (1s)	$R_{\Theta JA}$	14	°C/W	1, 2
Junction to ambient, natural convection	Four-layer board (2s2p)	$R_{\Theta JA}$	10	°C/W	1, 2
Junction to ambient (at 200 ft./min.)	Single-layer board (1s)	$R_{\Theta JMA}$	9	°C/W	1, 2
Junction to ambient (at 200 ft./min.)	Four-layer board (2s2p)	$R_{\Theta JMA}$	7	°C/W	1, 2

Table 41. Ethernet management interface 2 AC timing specifications (continued)

For recommended operating conditions, see Table 3.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Note
MDIO to MDC hold time	t_{MDDXKH}	0	—	—	ns	—

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time.
2. This parameter is dependent on the frame manager clock frequency (MIIMCFG [MgmtClk] field determines the clock frequency of the MgmtClk Clock EC_MDC).
3. This parameter is dependent on the management data clock frequency, f_{MDC}. The delay is equal to 0.5 management data clock period ±6 ns. For example, with a management data clock of 2.5 MHz, the min/max delay is 200 ns ± 6 ns.

This figure shows the Ethernet management interface timing diagram.

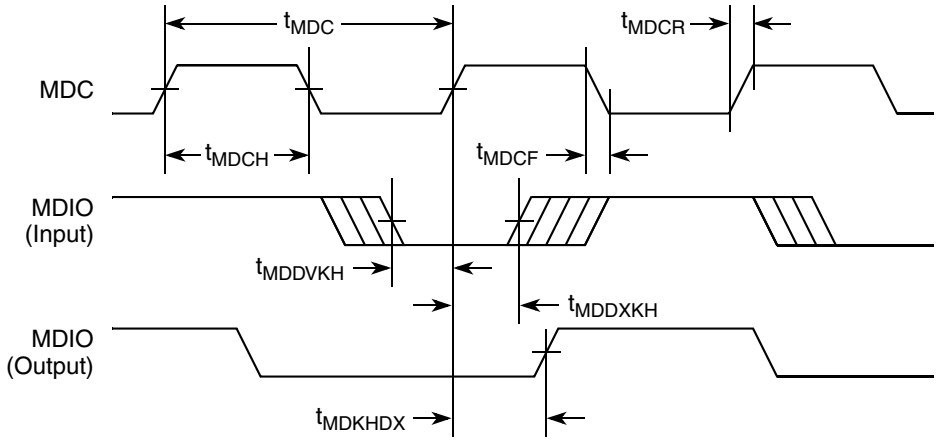


Figure 19. Ethernet management interface timing diagram

2.12.4 eTSEC IEEE Std 1588 timing specifications

This section discusses the electrical characteristics for the eTSEC IEEE Std 1588 interfaces.

2.12.4.1 eTSEC IEEE Std 1588 DC electrical characteristics

This table shows eTSEC IEEE Std 1588 DC electrical characteristics when operating at LV_{DD} = 3.3 V supply.

Table 42. eTSEC IEEE 1588 DC electrical characteristics (LV_{DD} = 3.3 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2.0	—	V	2
Input low voltage	V_{IL}	—	0.9	V	2
Input high current (LV_{DD} = Max, V_{IN} = 2.1 V)	I_{IH}	—	40	μA	1

Table 48. Enhanced local bus DC electrical characteristics (BV_{DD} = 1.8 V) (continued)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Notes
Input current (V_{IN} = 0 V or V_{IN} = BV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (BV_{DD} = min, I_{OH} = –0.5 mA)	V_{OH}	1.35	—	V	—
Output low voltage (BV_{DD} = min, I_{OL} = 0.5 mA)	V_{OL}	—	0.4	V	—

Notes:

1. The min V_{IL} and max V_{IH} values are based on the respective min and max BV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the BV_{IN} symbol referenced in Section 2.1.2, "Recommended operating conditions."

2.14.2 Enhanced local bus AC timing specifications

This section describes the AC timing specifications for the enhanced local bus interface.

2.14.2.1 Test condition

This figure provides the AC test load for the enhanced local bus.

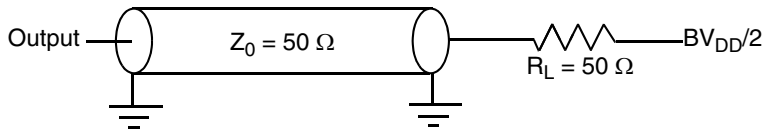


Figure 23. Enhanced local bus AC test load

2.14.2.2 Local bus AC timing specification

All output signal timings are relative to the falling edge of any LCLKs. The external circuit must use the rising edge of the LCLKs to latch the data.

All input timings except LGTA/LUPWAIT/LFRB are relative to the rising edge of LCLKs. LGTA/LUPWAIT/LFRB are relative to the falling edge of LCLKs.

This table describes the timing specifications of the local bus interface.

Table 49. Enhanced local bus timing specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol[1]	Min	Max	Unit	Notes
Local bus cycle time	t_{LBK}	10	—	ns	—
Local bus duty cycle	t_{LBKH}/t_{LBK}	45	55	%	—
LCLK[n] skew to LCLK[m]	$t_{LBKSKEW}$	—	150	ps	2
Input setup (except LGTA/LUPWAIT/LFRB)	t_{LBIVKH}	6	—	ns	—
Input hold (except LGTA/LUPWAIT/LFRB)	t_{LBIXKH}	1	—	ns	—

Table 49. Enhanced local bus timing specifications (continued)

For recommended operating conditions, see Table 3.

Parameter	Symbol[1]	Min	Max	Unit	Notes
Input setup (for LGTA/LUPWAIT/LFRB)	t_{LBIVKL}	6	—	ns	—
Input hold (for LGTA/LUPWAIT/LFRB)	t_{LBIXKL}	1	—	ns	—
Output delay (Except LALE)	t_{LBKLOV}	—	1.5	ns	—
Output hold (Except LALE)	t_{LBKLOX}	-3.5	—	ns	5
Local bus clock to output high impedance for LAD/LDP	t_{LBKLOZ}	—	2	ns	3
LALE output negation to LAD/LDP output transition (LATCH hold time)	t_{LBONOT}	2 platform clock cycles—1ns (LBCR[AHD]=1)	—	ns	4
		4 platform clock cycles—1ns (LBCR[AHD]=0)	—		

Notes:

1. All signals are measured from $BV_{DD}/2$ of rising/falling edge of LCLK to $BV_{DD}/2$ of the signal in question.
2. Skew measured between different LCLKs at $BV_{DD}/2$.
3. For purposes of active/float timing measurements, the high impedance or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
4. t_{LBONOT} is a measurement of the minimum time between the negation of LALE and any change in LAD. t_{LBONOT} is determined by LBCR[AHD]. The unit is the eLBC controller clock cycle, which is the internal clock that runs the local bus controller, not the external LCLK. LCLK cycle = eLBC controller clock cycle x LCRR[CLKDIV]. After power on reset, LBCR[AHD] defaults to 0 and eLBC runs at maximum hold time.
5. Output hold is negative. This means that output transition happens earlier than the falling edge of LCLK.

This figure provides the eSDHC clock input timing diagram.

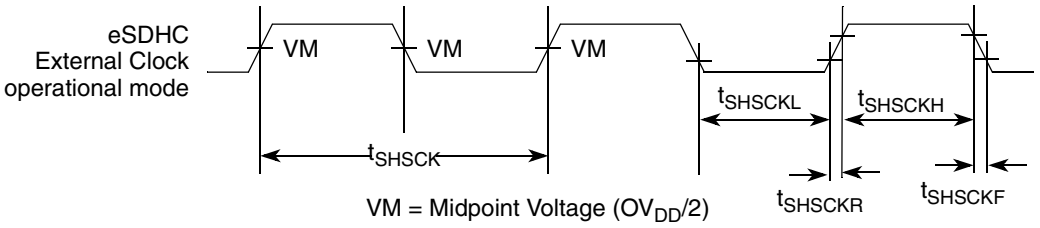


Figure 26. eSDHC clock input timing diagram

This figure provides the data and command input/output timing diagram.

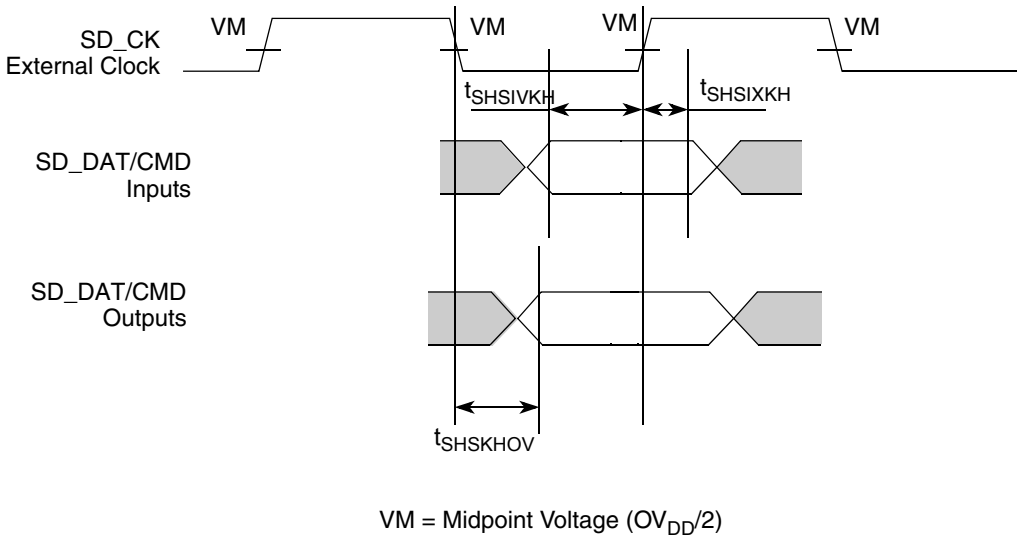


Figure 27. eSDHC data and command input/output timing diagram referenced to clock

2.16 Multicore programmable interrupt controller (MPIC) specifications

This section describes the DC and AC electrical specifications for the multicore programmable interrupt controller.

2.16.1 MPIC DC specifications

This table provides the DC electrical characteristics for the MPIC interface.

Table 52. MPIC DC electrical characteristics (OV_{DD} = 3.3 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	2.0	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (OV_{IN} = 0 V or OV_{IN} = OV_{DD})	I_{IN}	—	±40	μA	2
Output high voltage (OV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—

2.20.2.3 AC requirements for SerDes reference clocks

This table lists AC requirements for the PCI Express, SGMII, Serial RapidIO and Aurora SerDes reference clocks to be guaranteed by the customer's application design.

Table 61. SD_REF_CLK*n* and $\overline{\text{SD\_REF\_CLK}n}$ input clock requirements (SV_{DD} = 1.0 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ frequency range	t_{CLK_REF}	—	100/125	—	MHz	1
SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ clock frequency tolerance	t_{CLK_TOL}	–350	—	350	ppm	—
SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ reference clock duty cycle	t_{CLK_DUTY}	40	50	60	%	4
SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ max deterministic peak-peak jitter at 10^{-6} BER	t_{CLK_DJ}	—	—	42	ps	—
SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ total reference clock jitter at 10^{-6} BER (peak-to-peak jitter at refClk input)	t_{CLK_TJ}	—	—	86	ps	2
SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ rising/falling edge rate	t_{CLKRR}/t_{CLKFR}	1	—	4	V/ns	3
Differential input high voltage	V_{IH}	200	—	—	mV	4
Differential input low voltage	V_{IL}	—	—	–200	mV	4
Rising edge rate (SD_REF_CLK*n*) to falling edge rate (SD_REF_CLK*n*) matching	Rise-Fall Matching	—	—	20	%	5, 6

Notes:

1. **Caution:** Only 100 and 125 have been tested. In-between values not work correctly with the rest of the system.
2. Limits from PCI Express CEM Rev 2.0
3. Measured from –200 mV to +200 mV on the differential waveform (derived from SD_REF_CLK*n* minus $\overline{\text{SD\_REF\_CLK}n}$). The signal must be monotonic through the measurement region for rise and fall time. The 400 mV measurement window is centered on the differential zero crossing. See Figure 40.
4. Measurement taken from differential waveform
5. Measurement taken from single-ended waveform
6. Matching applies to rising edge for SD_REF_CLK*n* and falling edge rate for $\overline{\text{SD\_REF\_CLK}n}$. It is measured using a 200 mV window centered on the median cross point where SD_REF_CLK*n* rising meets $\overline{\text{SD\_REF\_CLK}n}$ falling. The median cross point is used to calculate the voltage thresholds that the oscilloscope uses for the edge rate calculations. The rise edge rate of SD_REF_CLK*n* should be compared to the fall edge rate of $\overline{\text{SD\_REF\_CLK}n}$, the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 41.

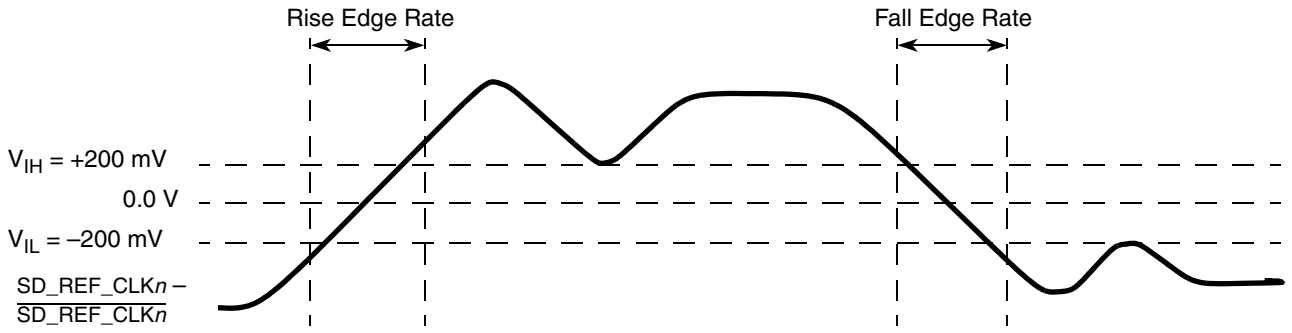


Figure 40. Differential measurement points for rise and fall time

This table defines the PCI Express 2.0 (5 GT/s) AC specifications for the differential output at all transmitters. The parameters are specified at the component pins. The AC timing specifications do not include RefClk jitter.

Table 67. PCI Express 2.0 (5 GT/s) differential transmitter Output AC specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typ	Max	Units	Notes
Unit Interval	UI	199.94	200.00	200.06	ps	Each UI is 400 ps ± 300 ppm. UI does not account for spread spectrum clock dictated variations. See Note 1.
Minimum transmitter eye width	T_{TX-EYE}	0.75	—	—	UI	The maximum transmitter jitter can be derived as: $T_{TX-MAX-JITTER} = 1 - T_{TX-EYE} = 0.25$ UI. See Notes 2 and 3.
Transmitter RMS deterministic jitter > 1.5 MHz	$T_{TX-HF-DJ-DD}$	—	—	0.15	ps	—
Transmitter RMS deterministic jitter < 1.5 MHz	$T_{TX-LF-RMS}$	—	3.0	—	ps	Reference input clock RMS jitter (< 1.5 MHz) at pin < 1 ps
AC coupling capacitor	C_{TX}	75	—	200	nF	All transmitters must be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See Note 4.

Notes:
1. No test load is necessarily associated with this value.
2. Specified at the measurement point into a timing and voltage test load as shown in Figure 43 and measured over any 250 consecutive transmitter UIs.
3. A $T_{TX-EYE} = 0.75$ UI provides for a total sum of deterministic and random jitter budget of $T_{TX-JITTER-MAX} = 0.25$ UI for the transmitter collected over any 250 consecutive transmitter UIs. The $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ median is less than half of the total transmitter jitter budget collected over any 250 consecutive transmitter UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.
4. The chip's SerDes transmitter does not have C_{TX} built-in. An external AC coupling capacitor is required.

2.20.4.5.2 PCI Express AC physical layer receiver specifications

This section discusses the PCI Express AC physical layer receiver specifications 2.5 GT/s, and 5 GT/s.

This figure shows an example of a 4-wire AC-coupled SGMII serial link connection.

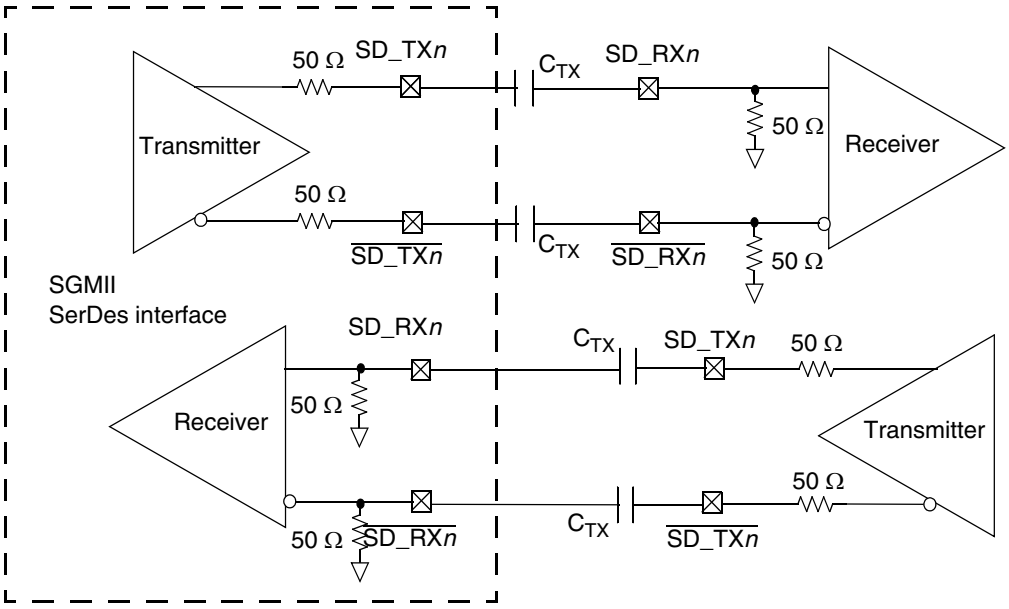


Figure 46. 4-wire, AC-coupled, SGMII serial link connection example

This figure shows the SGMII transmitter DC measurement circuit.

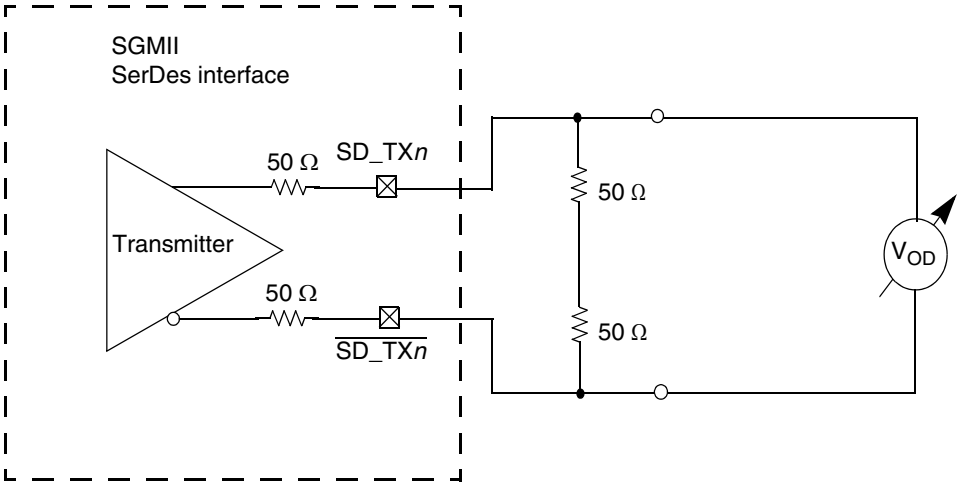


Figure 47. SGMII transmitter DC measurement circuit

3.1.2 Platform to SYSCLK PLL ratio

The allowed platform clock to SYSCLK ratios are shown in this table.

Note that in synchronous DDR mode, the DDR data rate is the determining factor for selecting the platform bus frequency because the platform frequency must equal the DDR data rate.

In asynchronous DDR mode, the memory bus clock frequency is decoupled from the platform bus frequency.

Table 95. Platform to SYSCLK PLL ratios

Binary value of SYS_PLL_RAT	Platform:SYSCLK ratio
0_0101	5:1
0_0110	6:1
0_0111	7:1
0_1000	8:1
All Others	Reserved

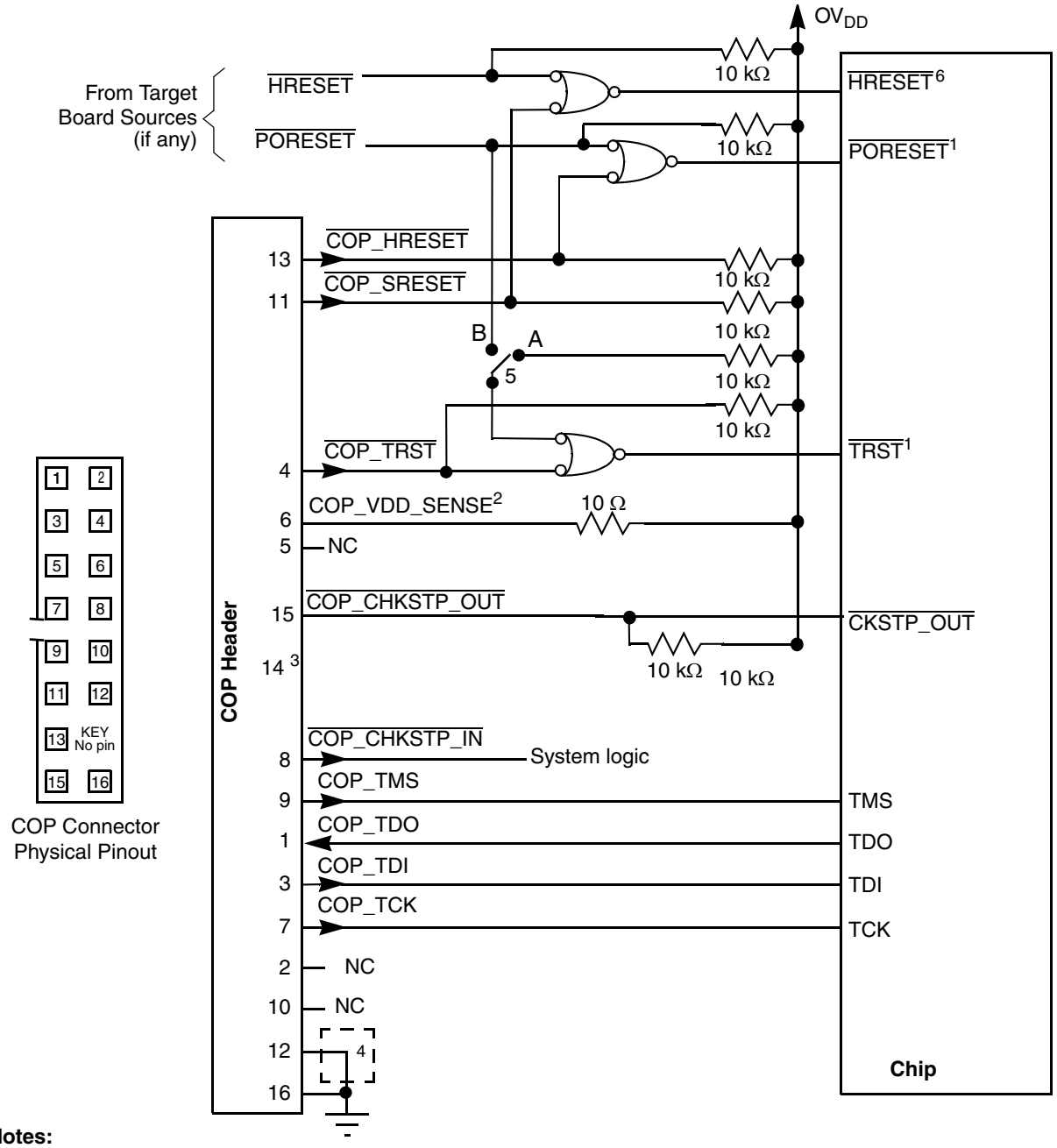
3.1.3 e5500-64 core complex/ FMan to SYSCLK PLL ratio

The clock ratio between SYSCLK and each of the two core complex PLLs and FMan PLL is determined at power up by the binary value of the RCW field CCn_PLL_RAT. (Note: *n*=1 or 2 are the core complex PLLs, *n*=3 is the FMan PLL). This table describes the supported ratios. Note that a core complex/ FMan PLL setting targeting 1 GHz and above must set RCW field CCn_PLL_CFG = 0b10, for setting targeting below 1 GHz CCn_PLL_CFG=0b00.

This table lists the supported core complex/ FMan to SYSCLK ratios.

Table 96. Core complex/ FMan PLL to SYSCLK ratios

Binary value of CC*n*_PLL_RAT	Core cluster:SYSCLK ratio
0_1000	8:1
0_1001	9:1
0_1010	10:1
0_1011	11:1
0_1100	12:1
0_1110	14:1
0_1111	15:1
1_0000	16:1
1_0001	17:1
1_0010	18:1
1_0100	20:1
1_0110	22:1
All Others	Reserved



Notes:

1. The COP port and target board should be able to independently assert $\overline{\text{PORESET}}$ and $\overline{\text{TRST}}$ to the processor in order to fully control the processor as shown here.
2. Populate this with a 10 Ω resistor for short-circuit/current-limiting protection.
3. The KEY location (pin 14) is not physically present on the COP header.
4. Although pin 12 is defined as a No-Connect, some debug tools may use pin 12 as an additional GND pin for improved signal integrity.
5. This switch is included as a precaution for BSDL testing. The switch should be closed to position A during BSDL testing to avoid accidentally asserting the $\overline{\text{TRST}}$ line. If BSDL testing is not being performed, this switch should be closed to position B.
6. Asserting $\overline{\text{HRESET}}$ causes a hard reset on the device.

Figure 56. Legacy JTAG interface connection

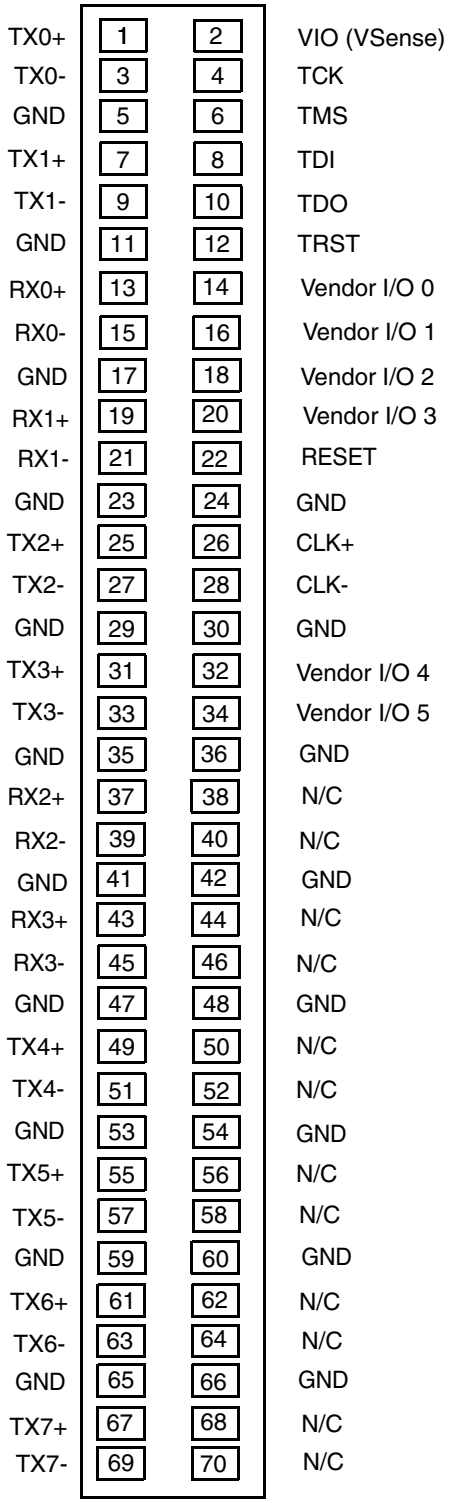


Figure 58. Aurora 70 pin connector duplex pinout

3.6.3 Guidelines for high-speed interface termination

This section provides the guidelines for high-speed interface termination when the SerDes interface is entirely unused or when it is partly unused.

3.6.3.1 SerDes interface entirely unused

If the high-speed SerDes interface is not used at all, the unused pin should be terminated as described in this section.

The following pins must be left unconnected:

- SD_TX[19:0]
- $\overline{\text{SD\_TX}}$[19:0]
- SD_IMP_CAL_RX
- SD_IMP_CAL_TX
- SD1_IMP_CAL_RX
- SD1_IMP_CAL_TX

The following pins must be connected to SGND:

- SD_RX[19:0]
- $\overline{\text{SD\_RX}}$[19:0]
- SD_REF_CLK1, SD_REF_CLK2, SD_REF_CLK3, SD_REF_CLK4
- $\overline{\text{SD\_REF\_CLK1}}$, $\overline{\text{SD\_REF\_CLK2}}$, $\overline{\text{SD\_REF\_CLK3}}$, $\overline{\text{SD\_REF\_CLK4}}$

The RCW configuration fields SRDS_LPD_B1, SRDS_LPD_B2, SRDS_LPD_B3, and SRDS_LPD_B4, all bits must be set to power down all the lanes in each bank.

The RCW configuration field SRDS_EN may be cleared to power down the SerDes block for power saving. Setting RCW[SRDS_EN_S1] = 0 powers down the PLLs of banks 1 to 3; RCW[SRDS_EN_S2]=0 powers down the PLL of bank 4.

Additionally, software may configure SRDSB*n*RSTCTL[SDRD] = 1 for the unused banks to power down the SerDes bank PLLs to save power.

Note that both SV_{DD} and XV_{DD} must remain powered.

3.6.3.2 SerDes interface partly unused

If only part of the high speed SerDes interface pins are used, the remaining high-speed serial I/O pins should be terminated as described in this section.

The following pins must be left unconnected:

- SD_TX[*n*]
- $\overline{\text{SD\_TX}}$[*n*]

The following unused pins must be connected to SGND:

- SD_RX[*n*]
- $\overline{\text{SD\_RX}}$[*n*]
- SD_REF_CLK1, $\overline{\text{SD\_REF\_CLK1}}$ (If entire SerDes bank 1 unused)
- SD_REF_CLK2, $\overline{\text{SD\_REF\_CLK2}}$ (If entire SerDes bank 2 unused)
- SD_REF_CLK3, $\overline{\text{SD\_REF\_CLK3}}$ (If entire SerDes bank 3 unused)
- SD_REF_CLK4, $\overline{\text{SD\_REF\_CLK4}}$ (If entire SerDes bank 4 unused)