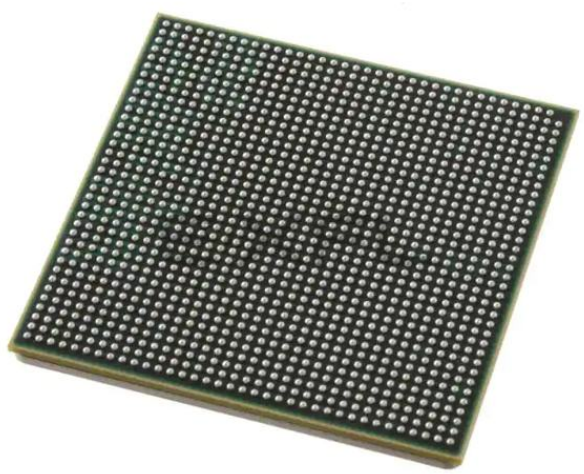

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e5500
Number of Cores/Bus Width	2 Core, 64-Bit
Speed	2.0GHz
Co-Processors/DSP	-
RAM Controllers	DDR3, DDR3L
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	1Gbps (10), 10Gbps (2)
SATA	SATA 3Gbps (2)
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.0V, 1.1V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	1295-BBGA, FCBGA
Supplier Device Package	1295-FCPBGA (37.5x37.5)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p5021nxn7vnc

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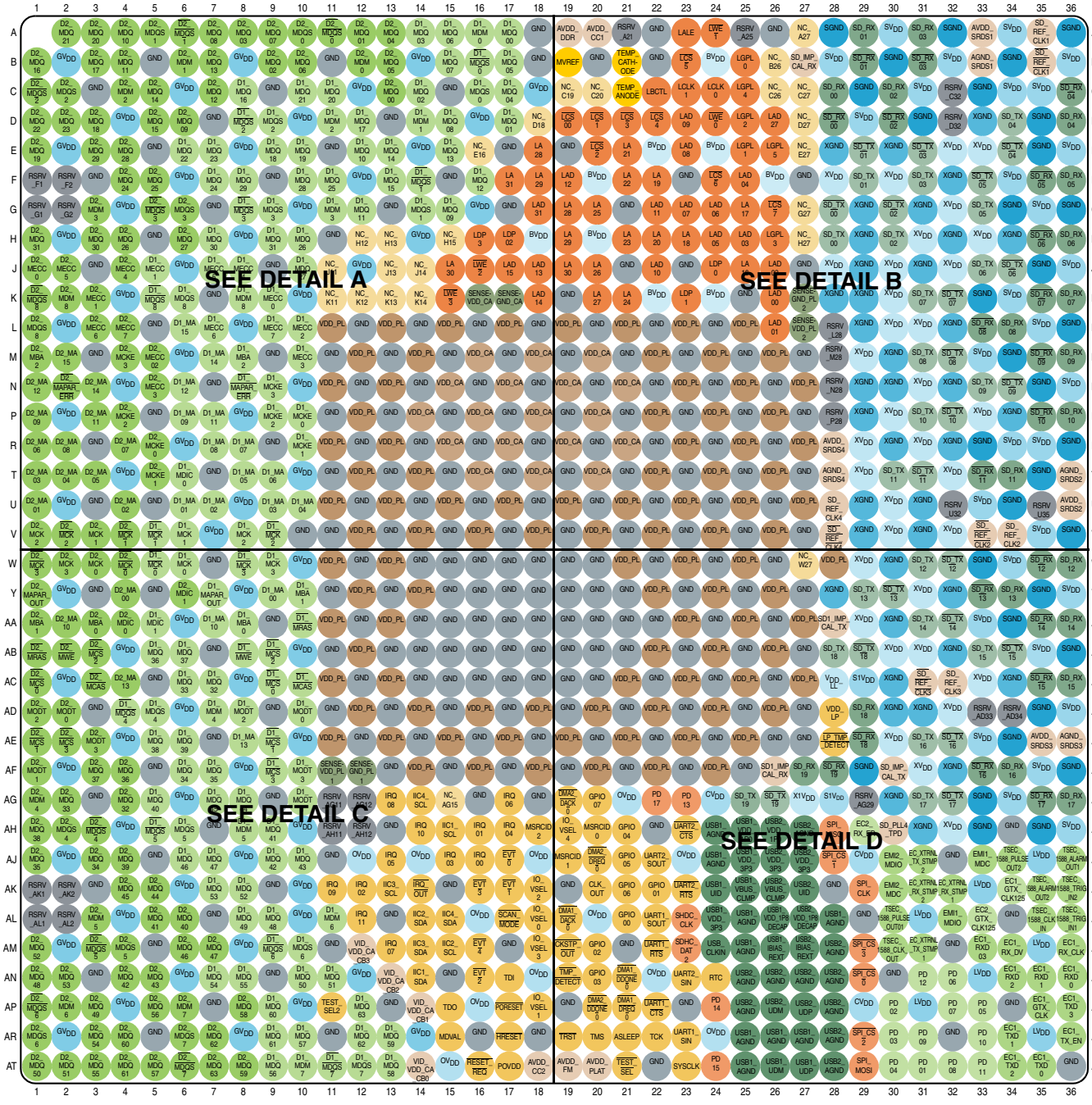

Signal Groups

- OV_{DD} I/O Supply Voltage
- LV_{DD} I/O Supply Voltage
- GV_{DD} DDR DRAM I/O Supply
- CV_{DD} SPI Voltage Supply
- BV_{DD} Local Bus I/O Supply
- SV_{DD} SerDes Core Power Supply
- XV_{DD} SerDes Transcvr Pad Supply
- VDD_{PL} Platform Supply Voltage
- VDD_{CA} Core Group A Supply Voltage
- $AVDD_{SRDS1}$ SerDes 1 PLL Supply Voltage
- $AVDD_{SRDS2}$ SerDes 2 PLL Supply Voltage
- $AVDD_{PLAT}$ Platform PLL Supply Voltage
- $AVDD_{CC}$ Core PLL Supply Voltage
- $SENSE_{VDD\_PL}$ Platform Voltage Sense
- $SENSE_{VDD}$ Core Group A Voltage Sense
- $SENSE_{VDD\_CB}$ Core Group B Voltage Sense
- RSRV Reserved
- POVDD Fuse Programming Override Supply

Figure 2. 1295 BGA ball map diagram (top view)

DETAIL C

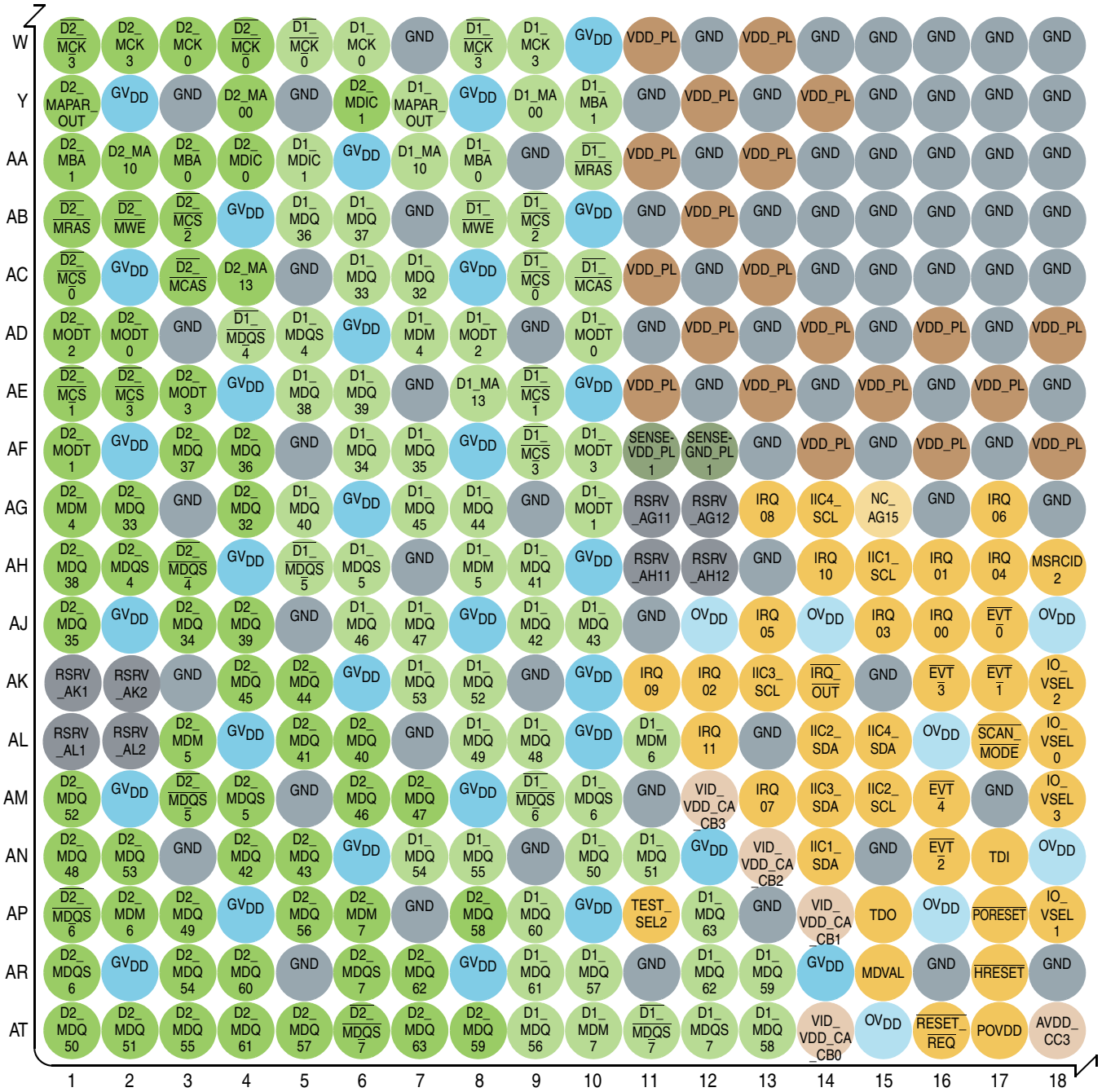

Figure 5. 1295 BGA ball map diagram (detail view C)

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
D1_MECC1	Error Correcting Code	J5	I/O	GV_{DD}	—
D1_MECC2	Error Correcting Code	L10	I/O	GV_{DD}	—
D1_MECC3	Error Correcting Code	M10	I/O	GV_{DD}	—
D1_MECC4	Error Correcting Code	J8	I/O	GV_{DD}	—
D1_MECC5	Error Correcting Code	J7	I/O	GV_{DD}	—
D1_MECC6	Error Correcting Code	L7	I/O	GV_{DD}	—
D1_MECC7	Error Correcting Code	L9	I/O	GV_{DD}	—
$\overline{\text{D1\_MAPAR\_ERR}}$	Address Parity Error	N8	I	GV_{DD}	40
D1_MAPAR_OUT	Address Parity Out	Y7	O	GV_{DD}	—
D1_MDM0	Data Mask	A16	O	GV_{DD}	—
D1_MDM1	Data Mask	D14	O	GV_{DD}	—
D1_MDM2	Data Mask	D11	O	GV_{DD}	—
D1_MDM3	Data Mask	G11	O	GV_{DD}	—
D1_MDM4	Data Mask	AD7	O	GV_{DD}	—
D1_MDM5	Data Mask	AH8	O	GV_{DD}	—
D1_MDM6	Data Mask	AL11	O	GV_{DD}	—
D1_MDM7	Data Mask	AT10	O	GV_{DD}	—
D1_MDM8	Data Mask	K8	O	GV_{DD}	—
D1_MDQS0	Data Strobe	C16	I/O	GV_{DD}	—
D1_MDQS1	Data Strobe	G14	I/O	GV_{DD}	—
D1_MDQS2	Data Strobe	D9	I/O	GV_{DD}	—
D1_MDQS3	Data Strobe	G9	I/O	GV_{DD}	—
D1_MDQS4	Data Strobe	AD5	I/O	GV_{DD}	—
D1_MDQS5	Data Strobe	AH6	I/O	GV_{DD}	—
D1_MDQS6	Data Strobe	AM10	I/O	GV_{DD}	—
D1_MDQS7	Data Strobe	AT12	I/O	GV_{DD}	—
D1_MDQS8	Data Strobe	K6	I/O	GV_{DD}	—
$\overline{\text{D1\_MDQS0}}$	Data Strobe	B16	I/O	GV_{DD}	—
$\overline{\text{D1\_MDQS1}}$	Data Strobe	F14	I/O	GV_{DD}	—
$\overline{\text{D1\_MDQS2}}$	Data Strobe	D8	I/O	GV_{DD}	—
$\overline{\text{D1\_MDQS3}}$	Data Strobe	G8	I/O	GV_{DD}	—
$\overline{\text{D1\_MDQS4}}$	Data Strobe	AD4	I/O	GV_{DD}	—
$\overline{\text{D1\_MDQS5}}$	Data Strobe	AH5	I/O	GV_{DD}	—
$\overline{\text{D1\_MDQS6}}$	Data Strobe	AM9	I/O	GV_{DD}	—

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
EC2_GTX_CLK/ EC2_TX_ER	Transmit Clock Out (RGMII) Transmit Error (MII)	AN31	O	LV_{DD}	26
EC2_RXD3	Receive Data	AP33	I	LV_{DD}	27
EC2_RXD2	Receive Data	AN32	I	LV_{DD}	27
EC2_RXD1	Receive Data	AP32	I	LV_{DD}	26, 27
EC2_RXD0	Receive Data	AT32	I	LV_{DD}	26, 27
EC2_RX_DV	Receive Data Valid	AR33	I	LV_{DD}	27
EC2_RX_CLK	Receive Clock	AT33	I	LV_{DD}	27
EC2_RX_ER	Receive Error (MII)	AH29	I	LV_{DD}	—
EC2_COL/EC_XTRNL_TX_STMP2	Collision Detect (MII)	AJ31	O	LV_{DD}	26
EC2_CRS/EC_XTRNL_RX_STMP2	Carrier Sense (MII)	AK31	O	LV_{DD}	26
UART					
UART1_SOUT/GPIO8	Transmit Data	AL22	O	OV_{DD}	26
UART2_SOUT/GPIO9	Transmit Data	AJ22	O	OV_{DD}	26
UART1_SIN/GPIO10	Receive Data	AR23	I	OV_{DD}	26
UART2_SIN/GPIO11	Receive Data	AN23	I	OV_{DD}	26
$\overline{\text{UART1\_RTS}}$/UART3_SOUT/GPIO12	Ready to Send	AM22	O	OV_{DD}	26
$\overline{\text{UART2\_RTS}}$/UART4_SOUT/GPIO13	Ready to Send	AK23	O	OV_{DD}	26
$\overline{\text{UART1\_CTS}}$/UART3_SIN/GPIO14	Clear to Send	AP22	I	OV_{DD}	26
$\overline{\text{UART2\_CTS}}$/UART4_SIN/GPIO15	Clear to Send	AH23	I	OV_{DD}	26
I^2C interface					
IIC1_SCL	Serial Clock	AH15	I/O	OV_{DD}	2, 14
IIC1_SDA	Serial Data	AN14	I/O	OV_{DD}	2, 14
IIC2_SCL	Serial Clock	AM15	I/O	OV_{DD}	2, 14
IIC2_SDA	Serial Data	AL14	I/O	OV_{DD}	2, 14
IIC3_SCL/$\overline{\text{SDHC\_CD}}$/GPIO16	Serial Clock	AK13	I/O	OV_{DD}	2, 14, 27
IIC3_SDA/SDHC_WP/GPIO17	Serial Data	AM14	I/O	OV_{DD}	2, 14, 27
IIC4_SCL/$\overline{\text{EVT5}}$	Serial Clock	AG14	I/O	OV_{DD}	2, 14
IIC4_SDA/$\overline{\text{EVT6}}$	Serial Data	AL15	I/O	OV_{DD}	2, 14
SerDes (x20) PCIe, Aurora, 10GE, 1GE, SATA					
SD_TX19	Transmit Data (positive)	AG25	O	XV_{DD}	—
SD_TX18	Transmit Data (positive)	AB28	O	XV_{DD}	—
SD_TX17	Transmit Data (positive)	AG31	O	XV_{DD}	—
SD_TX16	Transmit Data (positive)	AE31	O	XV_{DD}	—

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
$\overline{\text{SD\_RX07}}$	Receive Data (negative)	K35	I	XV_{DD}	—
$\overline{\text{SD\_RX06}}$	Receive Data (negative)	H35	I	XV_{DD}	—
$\overline{\text{SD\_RX05}}$	Receive Data (negative)	F35	I	XV_{DD}	—
$\overline{\text{SD\_RX04}}$	Receive Data (negative)	C36	I	XV_{DD}	—
$\overline{\text{SD\_RX03}}$	Receive Data (negative)	B31	I	XV_{DD}	—
$\overline{\text{SD\_RX02}}$	Receive Data (negative)	D30	I	XV_{DD}	—
$\overline{\text{SD\_RX01}}$	Receive Data (negative)	B29	I	XV_{DD}	—
$\overline{\text{SD\_RX00}}$	Receive Data (negative)	D28	I	XV_{DD}	—
SD_REF_CLK1	SerDes Bank 1 PLL Reference Clock	A35	I	XV_{DD}	—
$\overline{\text{SD\_REF\_CLK1}}$	SerDes Bank 1 PLL Reference Clock Complement	B35	I	XV_{DD}	—
SD_REF_CLK2	SerDes Bank 2 PLL Reference Clock	V34	I	XV_{DD}	—
$\overline{\text{SD\_REF\_CLK2}}$	SerDes Bank 2 PLL Reference Clock Complement	V33	I	XV_{DD}	—
SD_REF_CLK3	SerDes Bank 3 PLL Reference Clock	AC32	I	XVDD	—
$\overline{\text{SD\_REF\_CLK3}}$	SerDes Bank 3 PLL Reference Clock Complement	AC31	I	XVDD	—
SD_REF_CLK4	SerDes Bank 4 PLL Reference Clock	U28	I	XVDD	—
$\overline{\text{SD\_REF\_CLK4}}$	SerDes Bank 4 PLL Reference Clock Complement	V28	I	XVDD	—
General-Purpose Input/Output					
GPIO00	General Purpose Input / Output	AL21	I/O	OV_{DD}	—
GPIO01	General Purpose Input / Output	AK22	I/O	OV_{DD}	—
GPIO02	General Purpose Input / Output	AM20	I/O	OV_{DD}	—
GPIO03	General Purpose Input / Output	AN20	I/O	OV_{DD}	—
GPIO04/USB1_DRVVBUS	General Purpose Input / Output	AH21	I/O	OV_{DD}	—
GPIO05/USB1_PWRFAULT	General Purpose Input / Output	AJ21	I/O	OV_{DD}	—
GPIO06/USB2_DRVVBUS	General Purpose Input / Output	AK21	I/O	OV_{DD}	—
GPIO07/USB2_PWRFAULT	General Purpose Input / Output	AG20	I/O	OV_{DD}	—
GPIO08/UART1_SOUT	General Purpose Input / Output	AL22	I/O	OV_{DD}	—
GPIO09/UART2_SOUT	General Purpose Input / Output	AJ22	I/O	OV_{DD}	—
GPIO10/UART1_SIN	General Purpose Input / Output	AR23	I/O	OV_{DD}	—
GPIO11/UART2_SIN	General Purpose Input / Output	AN23	I/O	OV_{DD}	—

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GND	Ground	AF5	—	—	—
GND	Ground	AG3	—	—	—
GND	Ground	AG9	—	—	—
GND	Ground	AH7	—	—	—
GND	Ground	AJ5	—	—	—
GND	Ground	AK3	—	—	—
GND	Ground	AN3	—	—	—
GND	Ground	AM5	—	—	—
GND	Ground	AL7	—	—	—
GND	Ground	AK9	—	—	—
GND	Ground	AJ11	—	—	—
GND	Ground	AH13	—	—	—
GND	Ground	AR5	—	—	—
GND	Ground	AP7	—	—	—
GND	Ground	AN9	—	—	—
GND	Ground	AM11	—	—	—
GND	Ground	AL13	—	—	—
GND	Ground	AK15	—	—	—
GND	Ground	AG18	—	—	—
GND	Ground	AR11	—	—	—
GND	Ground	AP13	—	—	—
GND	Ground	AN15	—	—	—
GND	Ground	AM17	—	—	—
GND	Ground	AK19	—	—	—
GND	Ground	AF13	—	—	—
GND	Ground	AR18	—	—	—
GND	Ground	AB27	—	—	—
GND	Ground	AP19	—	—	—
GND	Ground	AH22	—	—	—
GND	Ground	AM21	—	—	—
GND	Ground	AL29	—	—	—
GND	Ground	AR16	—	—	—
GND	Ground	AT22	—	—	—
GND	Ground	AP23	—	—	—

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
SGND	SerDes Core Logic GND	C29	—	—	—
SGND	SerDes Core Logic GND	C33	—	—	—
SGND	SerDes Core Logic GND	D31	—	—	—
SGND	SerDes Core Logic GND	D35	—	—	—
SGND	SerDes Core Logic GND	E35	—	—	—
SGND	SerDes Core Logic GND	G34	—	—	—
SGND	SerDes Core Logic GND	G36	—	—	—
SGND	SerDes Core Logic GND	J35	—	—	—
SGND	SerDes Core Logic GND	K33	—	—	—
SGND	SerDes Core Logic GND	L36	—	—	—
SGND	SerDes Core Logic GND	M34	—	—	—
SGND	SerDes Core Logic GND	N35	—	—	—
SGND	SerDes Core Logic GND	R33	—	—	—
SGND	SerDes Core Logic GND	R36	—	—	—
SGND	SerDes Core Logic GND	T35	—	—	—
SGND	SerDes Core Logic GND	U34	—	—	—
SGND	SerDes Core Logic GND	V36	—	—	—
SGND	SerDes Core Logic GND	W33	—	—	—
SGND	SerDes Core Logic GND	Y35	—	—	—
SGND	SerDes Core Logic GND	AH35	—	—	—
SGND	SerDes Core Logic GND	AH33	—	—	—
SGND	SerDes Core Logic GND	AF29	—	—	—
AGND_SRDS1	SerDes PLL1 GND	B33	—	—	—
AGND_SRDS2	SerDes PLL2 GND	T36	—	—	—
AGND_SRDS3	SerDes PLL3 GND	AE36	—	—	—
AGND_SRDS4	SerDes PLL4 GND	T28	—	—	—
SENSEGND_PL1	Platform GND Sense 1	AF12	—	—	8
SENSEGND_PL2	Platform GND Sense 2	K27	—	—	8
SENSEGND_CA	Core Group A GND Sense	K17	—	—	8
USB1_AGND	USB1 PHY Transceiver GND	AH24	—	—	—
USB1_AGND	USB1 PHY Transceiver GND	AJ24	—	—	—
USB1_AGND	USB1 PHY Transceiver GND	AL25	—	—	—
USB1_AGND	USB1 PHY Transceiver GND	AM25	—	—	—
USB1_AGND	USB1 PHY Transceiver GND	AR25	—	—	—

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GVDD	DDR Supply	C6	—	GV_{DD}	—
GVDD	DDR Supply	D4	—	GV_{DD}	—
GVDD	DDR Supply	D10	—	GV_{DD}	—
GVDD	DDR Supply	D16	—	GV_{DD}	—
GVDD	DDR Supply	E14	—	GV_{DD}	—
GVDD	DDR Supply	E8	—	GV_{DD}	—
GVDD	DDR Supply	E2	—	GV_{DD}	—
GVDD	DDR Supply	F6	—	GV_{DD}	—
GVDD	DDR Supply	F12	—	GV_{DD}	—
GVDD	DDR Supply	AR8	—	GV_{DD}	—
GVDD	DDR Supply	G4	—	GV_{DD}	—
GVDD	DDR Supply	G10	—	GV_{DD}	—
GVDD	DDR Supply	G16	—	GV_{DD}	—
GVDD	DDR Supply	H14	—	GV_{DD}	—
GVDD	DDR Supply	H8	—	GV_{DD}	—
GVDD	DDR Supply	H2	—	GV_{DD}	—
GVDD	DDR Supply	J6	—	GV_{DD}	—
GVDD	DDR Supply	K10	—	GV_{DD}	—
GVDD	DDR Supply	K4	—	GV_{DD}	—
GVDD	DDR Supply	L2	—	GV_{DD}	—
GVDD	DDR Supply	L8	—	GV_{DD}	—
GVDD	DDR Supply	M6	—	GV_{DD}	—
GVDD	DDR Supply	N4	—	GV_{DD}	—
GVDD	DDR Supply	N10	—	GV_{DD}	—
GVDD	DDR Supply	P8	—	GV_{DD}	—
GVDD	DDR Supply	P2	—	GV_{DD}	—
GVDD	DDR Supply	R6	—	GV_{DD}	—
GVDD	DDR Supply	T10	—	GV_{DD}	—
GVDD	DDR Supply	T4	—	GV_{DD}	—
GVDD	DDR Supply	J12	—	GV_{DD}	—
GVDD	DDR Supply	U2	—	GV_{DD}	—
GVDD	DDR Supply	U8	—	GV_{DD}	—
GVDD	DDR Supply	V7	—	GV_{DD}	—
GVDD	DDR Supply	AK10	—	GV_{DD}	—

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes
GVDD	DDR Supply	W10	—	GV_{DD}	—
GVDD	DDR Supply	AA6	—	GV_{DD}	—
GVDD	DDR Supply	AR2	—	GV_{DD}	—
GVDD	DDR Supply	Y2	—	GV_{DD}	—
GVDD	DDR Supply	Y8	—	GV_{DD}	—
GVDD	DDR Supply	AC2	—	GV_{DD}	—
GVDD	DDR Supply	AD6	—	GV_{DD}	—
GVDD	DDR Supply	AE10	—	GV_{DD}	—
GVDD	DDR Supply	AE4	—	GV_{DD}	—
GVDD	DDR Supply	AF2	—	GV_{DD}	—
GVDD	DDR Supply	AF8	—	GV_{DD}	—
GVDD	DDR Supply	AB4	—	GV_{DD}	—
GVDD	DDR Supply	AB10	—	GV_{DD}	—
GVDD	DDR Supply	AC8	—	GV_{DD}	—
GVDD	DDR Supply	AG6	—	GV_{DD}	—
GVDD	DDR Supply	AH10	—	GV_{DD}	—
GVDD	DDR Supply	AH4	—	GV_{DD}	—
GVDD	DDR Supply	AJ2	—	GV_{DD}	—
GVDD	DDR Supply	AJ8	—	GV_{DD}	—
GVDD	DDR Supply	AR14	—	GV_{DD}	—
GVDD	DDR Supply	AK6	—	GV_{DD}	—
GVDD	DDR Supply	AL4	—	GV_{DD}	—
GVDD	DDR Supply	AL10	—	GV_{DD}	—
GVDD	DDR Supply	AM2	—	GV_{DD}	—
GVDD	DDR Supply	AM8	—	GV_{DD}	—
GVDD	DDR Supply	AP10	—	GV_{DD}	—
GVDD	DDR Supply	AN12	—	GV_{DD}	—
GVDD	DDR Supply	AN6	—	GV_{DD}	—
GVDD	DDR Supply	AP4	—	GV_{DD}	—
BVDD	Local Bus Supply	B24	—	BV_{DD}	—
BVDD	Local Bus Supply	K22	—	BV_{DD}	—
BVDD	Local Bus Supply	F20	—	BV_{DD}	—
BVDD	Local Bus Supply	F26	—	BV_{DD}	—
BVDD	Local Bus Supply	E24	—	BV_{DD}	—

Table 1. Pins listed by bus (continued)

Signal	Signal description	Package pin number	Pin type	Power supply	Notes

Notes:

1. Recommend a weak pull-up resistor (2–10 kΩ) be placed on this pin to OV_{DD}.
2. This pin is an open drain signal.
3. This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state. This pull-up is designed such that it can be overpowered by an external 4.7-kΩ resistor. However, if the signal is intended to be high after reset, and if there is any device on the net which might pull down the value of the net at reset, then a pull up or active driver is needed.
4. Functionally, this pin is an output, but structurally it is an I/O because it either samples configuration input during reset or because it has other manufacturing test functions. This pin is therefore described as an I/O for boundary scan.
5. Recommend a weak pull-up resistor (2–10 kΩ) be placed on this pin to BV_{DD}, to ensure no random chip select assertion due to possible noise, and so forth.
6. This output is actively driven during reset rather than being three-stated during reset.
7. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
8. These pins are connected to the correspondent power and ground nets internally and may be connected as a differential pair to be used by the voltage regulators with remote sense function.
9. These pins may be connected to a thermal diode monitoring device such as the ADT7461A only with a clear understanding that proper thermal diode operation is not implied and the thermal diode feature may not be available in the production device.
11. Do not connect.
12. These are test signals for factory use only and must be pulled up (100 Ω–1 kΩ) to OV_{DD} for normal device operation.
13. Independent supplies derived from board V_{DD_PL} (Core clusters, Platform, DDR) or SV_{DD} (SerDes).
14. Recommend a pull-up resistor of 1-kΩ be placed on this pin to OV_{DD} if I2C interface is used.
15. This pin requires an external 1-kΩ pull-down resistor to prevent PHY from seeing a valid Transmit Enable before it is actively driven.
16. For DDR3 and DDR3L, D*n*_MDIC[0] is grounded through an 40.2-Ω (half-strength mode) precision 1% resistor and D*n*_MDIC[1] is connected to GV_{DD} through an 40.2-Ω (half-strength mode) precision 1% resistor. These pins are used for automatic calibration of the DDR3 and DDR3L IOs.
18. These pins should be pulled up to 1.2V through a $180\Omega \pm 1\%$ resistor for EM2_MDC and a $330\Omega \pm 1\%$ resistor for EM2_MDIO.
20. Pin has a weak internal pull-up.
21. These pins should be pulled to ground (GND).
22. Ethernet Management interface 2 pins function as open drain I/Os. The interface shall conform to 1.2 V nominal voltage levels. LV_{DD} must be powered to use this interface.
23. This pin requires a 200-Ω pull-up to XV_{DD}.
24. This pin requires a 200-Ω pull-up to SV_{DD}.
25. This GPIO pin is on LV_{DD} power plane, not OV_{DD}.
26. Functionally, this pin is an I/O, but may act as an output only or an input only depending on the pin mux configuration defined by the RCW.
27. See Section 3.6, "Connection recommendations," for additional details on this signal.
28. This signal must be pulled low to GND.
30. Warning, incorrect voltage select settings can lead to irreversible device damage. See Section 3.2, "Supply power default setting."
31. SDHC_DAT[4:7] require CV_{DD} = 3.3 V when muxed extended SDHC data signals are enabled via the RCW[SPI] field.
32. The *cfg_xvdd_sel*(LAD[26]) reset configuration pin must select the correct voltage that is being supplied on the XV_{DD} pin. Incorrect voltage select settings can lead to irreversible device damage.

Table 2. Absolute maximum operating conditions[1] (continued)

Parameter		Symbol	Maximum value	Unit	Notes
Input voltage[7]	DDR3 and DDR3L DRAM signals	MV_{IN}	–0.3 to (GV_{DD} + 0.3)	V	2, 7
	DDR3 and DDR3L DRAM reference	MV_{REF}	–0.3 to (GV_{DD}/2+ 0.3)	V	2, 7
	Ethernet signals (except EMI2)	LV_{IN}	–0.3 to (LV_{DD} + 0.3)	V	3, 7
	eSPI, eSHDC	CV_{IN}	–0.3 to (CV_{DD} + 0.3)	V	4, 7
	Enhanced local bus signals	BV_{IN}	–0.3 to (BV_{DD} + 0.3)	V	5, 7
	DUART, I^2C, DMA, MPIC, GPIO, system control and power management, clocking, debug, I/O voltage select, and JTAG I/O voltage	OV_{IN}	–0.3 to (OV_{DD} + 0.3)	V	6, 7
	SerDes signals	XV_{IN}	–0.4 to (XV_{DD} + 0.3)	V	7
	USB PHY transceiver signals	$USB\_V_{IN}\_3P3$	–0.3 to ($USB\_V_{DD}\_3P3$ + 0.3)	V	7
	Ethernet management interface 2 (EMI2) signals	—	–0.3 to (1.2 + 0.3)	V	7
Storage junction temperature range		T_{stg}	–55 to 150	°C	—

Notes:

1. Functional operating conditions are given in Table 3. Absolute maximum ratings are stress ratings only; functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. **Caution:** MV_{IN} must not exceed GV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
3. **Caution:** LV_{IN} must not exceed LV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. **Caution:** CV_{IN} must not exceed CV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
5. **Caution:** BV_{IN} must not exceed BV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
6. **Caution:** OV_{IN} must not exceed OV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
7. (C,X,B,G,L,O)V_{IN} may overshoot (for V_{IH}) or undershoot (for V_{IL}) to the voltages and maximum duration shown in Figure 7.
8. Ethernet Management interface 2 pins function as open drain I/Os. The interface shall conform to 1.2 V nominal voltage levels. LV_{DD} must be powered to use this interface.
9. Supply voltage specified at the voltage sense pin. Voltage input pins should be regulated to provide specified voltage at the sense pin.
10. Implementation may choose either V_{DD_PL} pin for feedback loop. If the platform and core groups are supplied by a single regulator, it is recommended that V_{DD_CA} be used.
11. V_{DD_PL} voltage must not exceed V_{DD_CA}.

Table 3. Recommended operating conditions (continued)

Parameter		Symbol	Recommended value	Unit	Notes
Input voltage	DDR3 and DDR3L DRAM signals	MV_{IN}	GND to GV_{DD}	V	7
	DDR3 and DDR3L DRAM reference	MV_{REF}	$GV_{DD}/2$ ± 1%	V	7
	Ethernet signals (except EMI2)	LV_{IN}	GND to LV_{DD}	V	7
	eSPI, eSHDC	CV_{IN}	GND to CV_{DD}	V	7
	Enhanced local bus signals	BV_{IN}	GND to BV_{DD}	V	7
	DUART, I^2C, DMA, MPIC, GPIO, system control and power management, clocking, debug, I/O voltage select, and JTAG I/O voltage	OV_{IN}	GND to OV_{DD}	V	7
	SerDes signals	SV_{IN}	GND to SV_{DD}	V	7
	USB PHY Transceiver signals	$USB\_V_{IN}\_3P3$	GND to $USB\_V_{DD}\_3P3$	V	7
	Ethernet Management interface 2 (EMI2) signals	—	GND to 1.2V	V	4, 7
Operating Temperature range	Normal Operation	T_A, T_J	T_A = 0 (min) to T_J = 105 (max) (90 (max) core frequency > 2000 MHz)	°C	—
	Extended Temperature	T_A, T_J	T_A = -40 (min) to T_J = 105 (max)	°C	—
	Secure Boot Fuse Programming	T_A, T_J	T_A = 0 (min) to T_J = 70 (max)	°C	2

Notes:

1. V_{DD_PL} voltage must not exceed V_{DD_CA}.
2. POV_{DD} must be supplied 1.5 V and the chip must operate in the specified fuse programming temperature range only during secure boot fuse programming. For all other operating conditions, POV_{DD} must be tied to GND, subject to the power sequencing constraints shown in Section 2.2, "Power-up sequencing."
3. Selecting RGMII limits LV_{DD} to 2.5V.
4. Ethernet Management interface 2 pins function as open drain I/Os. The interface shall conform to 1.2 V nominal voltage levels. LV_{DD} must be powered to use this interface.6. Supply voltage specified at the voltage sense pin. Voltage input pins must be regulated to provide specified voltage at the sense pin.
7. All input signals must increase/decrease monotonically throughout the entire rise/fall duration.

Table 15. RESET initialization timing specifications (continued)

Parameter	Min	Max	Unit[1]	Notes
Input hold time for all POR configurations with respect to negation of $\overline{\text{PORESET}}$	2	—	SYSCLKs	1
Maximum valid-to-high impedance time for actively driven POR configurations with respect to negation of $\overline{\text{PORESET}}$	—	5	SYSCLKs	1

Notes:
1. SYSCLK is the primary clock input for the chip.
2. The device asserts $\overline{\text{HRESET}}$ as an output when $\overline{\text{PORESET}}$ is asserted to initiate the power-on reset process. The device releases $\overline{\text{HRESET}}$ sometime after $\overline{\text{PORESET}}$ is negated. The exact sequencing of HRESET negation is documented in Section 4.4.1 “Power-On Reset Sequence,” of the applicable chip reference manual.
3. $\overline{\text{PORESET}}$ must be driven asserted before the core and platform power supplies are powered up , see Section 2.2, “Power-up sequencing.”

This table provides the PLL lock times.

Table 16. PLL lock times

Parameter	Min	Max	Unit	Notes
PLL lock times	—	100	µs	—

2.8 Power-on ramp rate

This section describes the AC electrical specifications for the power-on ramp rate requirements. Controlling the maximum Power-On Ramp Rate is required to avoid falsely triggering the ESD circuitry. This table provides the power supply ramp rate specifications.

Table 17. Power supply ramp rate

Parameter	Min	Max	Unit	Notes
Required ramp rate for all voltage supplies (including OV_{DD}/CV_{DD}/ GV_{DD}/BV_{DD}/SV_{DD}/XV_{DD}/LV_{DD} all V_{DD} supplies, MVREF and all AV_{DD} supplies.)	—	36000	V/s	1, 2

Notes:
1. Ramp rate is specified as a linear ramp from 10 to 90%. If non-linear (for example, exponential), the maximum rate of change from 200 to 500 mV is the most critical as this range might falsely trigger the ESD circuitry.
2. Over full recommended operating temperature range (see Table 3).

2.9 DDR3 and DDR3L SDRAM controller

This section describes the DC and AC electrical specifications for the DDR3 and DDR3L SDRAM controller interface. Note that the required GV_{DD}(typ) voltage is 1.5 V when interfacing to DDR3 SDRAM and GV_{DD}(typ) voltage is 1.35 V when interfacing to DDR3L SDRAM.

NOTE

When operating at DDR data rates of 1600 MT/s only one dual-ranked module per memory controller is supported.

Table 25. DDR3 and DDR3L SDRAM interface output AC timing specifications (continued)

For recommended operating conditions, see Table 3.

Parameter	Symbol[1]	Min	Max	Unit	Notes
MDQ/MECC/MDM output setup with respect to MDQS	t_{DDKHDS}, t_{DDKLDS}			ps	5
1600 MT/s data rate		200	—		
1333 MT/s data rate		250	—		
1200 MT/s data rate		275	—		
1066 MT/s data rate		300	—		
800 MT/s data rate		375	—		
MDQ/MECC/MDM output hold with respect to MDQS	t_{DDKHDX}, t_{DDKLDX}			ps	5
1600 MT/s data rate		200	—		
1333 MT/s data rate		250	—		
1200 MT/s data rate		275	—		
1066 MT/s data rate		300	—		
800 MT/s data rate		375	—		
MDQS preamble	t_{DDKHMP}	$0.9 \times t_{MCK}$	—	ns	—
MDQS post-amble	t_{DDKHME}	$0.4 \times t_{MCK}$	$0.6 \times t_{MCK}$	ns	—

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{\text{MCK}}$ and MDQS/$\overline{\text{MDQS}}$ referenced measurements are made from the crossing of the two signals.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{\text{MCK}}$, $\overline{\text{MCS}}$, and MDQ/MECC/MDM/MDQS.
4. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the MDQS override bits (called WR_DATA_DELAY) in the TIMING_CFG_2 register. This is typically set to the same delay as in DDR_SDRAM_CLK_CNTL[CLK_ADJUST]. The timing parameters listed in the table assume that these two parameters have been set to the same adjustment value. See the applicable chip reference manual for a description and explanation of the timing modifications enabled by use of these bits.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.

NOTE

For the ADDR/CMD setup and hold specifications in Table 25, it is assumed that the clock control register is set to adjust the memory clocks by ½ applied cycle.

This figure shows the DDR3 and DDR3L SDRAM interface output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).

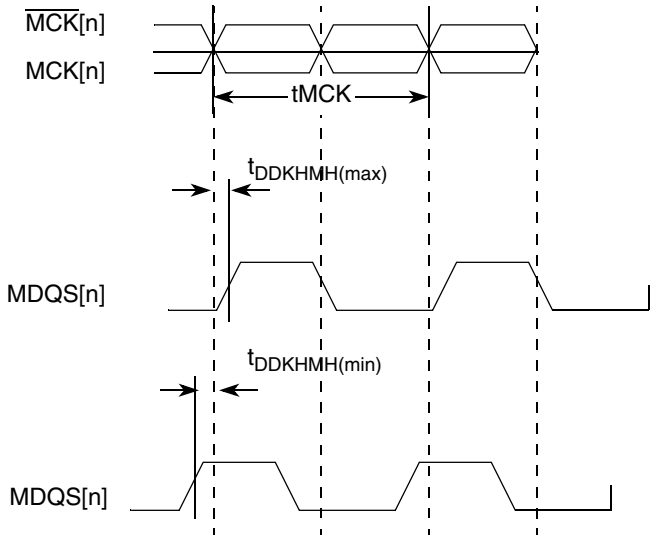

Figure 10. t_{DDKHMH} timing diagram

This figure shows the DDR3 and DDR3L SDRAM output timing diagram.

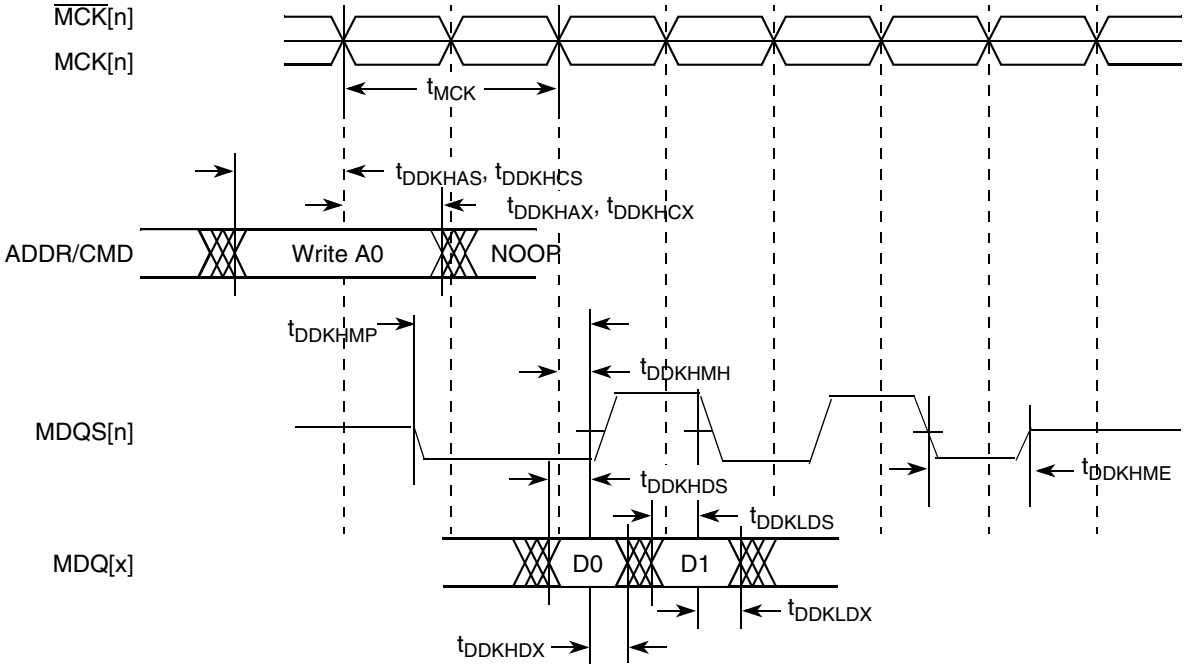

Figure 11. DDR3 and DDR3L output timing diagram

This table provides the Gen2i or 3 Gbits/s differential receiver input DC characteristics for the SATA interface.

Table 82. Gen2i/3 G receiver Input DC specifications (XV_{DD} = 1.5 V or 1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typical	Max	Units	Notes
Differential input voltage	V_{SATA_RXDIFF}	275	—	750	mV p-p	1
Differential receiver input impedance	Z_{SATA_RXSEIM}	85	100	115	Ω	2
OOB signal detection threshold	V_{SATA_OOB}	75	120	240	mV p-p	2

Notes:
1. Voltage relative to common of either signal comprising a differential pair
2. DC impedance

2.20.7.2 SATA AC timing specifications

This section discusses the SATA AC timing specifications.

2.20.7.2.1 AC requirements for SATA REF_CLK

The AC requirements for the SATA reference clock are listed in this table to be guaranteed by the customer's application design.

Table 83. SATA reference clock input requirements

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ frequency range	t_{CLK_REF}	—	100/125	—	MHz	1
SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ clock frequency tolerance	t_{CLK_TOL}	–350	—	+350	ppm	—
SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ reference clock duty cycle	t_{CLK_DUTY}	40	50	60	%	5
SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ cycle-to-cycle clock jitter (period jitter)	t_{CLK_CJ}	—	—	100	ps	2
SD_REF_CLK/$\overline{\text{SD\_REF\_CLK}}$ total reference clock jitter, phase jitter (peak-peak)	t_{CLK_PJ}	–50	—	+50	ps	2, 3, 4

Notes:
1. **Caution:** Only 100, and 125 MHz have been tested. In-between values do not work correctly with the rest of the system.
2. At RefClk input
3. In a frequency band from 150 kHz to 15 MHz at BER of 10^{-12}
4. Total peak-to-peak deterministic jitter should be less than or equal to 50 ps.
5. Measurement taken from differential waveform

Table 98. Asynchronous DDR clock ratio (continued)

Binary value of MEM_PLL_RAT[10:14]	DDR:SYSCLK ratio
0_1100	12:1
0_1101	13:1
1_0000	16:1
1_0010	18:1
1_0011	19:1
1_0100	20:1
1_1000	24:1
All Others	Reserved

Note:
1. RCW[MEM_PLL_CFG] is set dependant on the DDR clock ratio used. See Table 99 for valid setttings of DDR clock ratio and MEM_PLL_CFG.

Table 99. Supported DDR ratios and RCW MEM_PLL_CFG settings

MEM:SYSCLK Ratio	SYSCLK (MHz)			
	100	125	133.3	150
	DDR Rate (MT/s)/MEM_PLL_CFG			
1 (Sync Mode)	Platform Clock/01			
6	Reserved		800/11	900/11[3]
8	800/10[1]	1000/01[1]	1067/01	1200/01
9	900/10[2]	1125/01[2]	1200/01	1350/01
10	1000/01	1250/01	1333/01	1500/01
12	1200/11	1500/11	1600/11	Reserved
13	1300/11	Reserved		
16	1600/11	Reserved		

Notes:
1. For MEM SYSYCLK RATIO = 8, MEM_PLL_CFG changes from 10 to 01 when SYSCLK is greater than or equal to 120.9MHz
2. For MEM SYSYCLK RATIO = 9, MEM_PLL_CFG changes from 10 to 01 when SYSCLK is greater than or equal to 107.4MHz
3. Maximum SYSCLK is 161.2MHz when MEM:SYSCLK ratio = 6

In synchronous mode, the DDR data rate to platform clock ratios supported are listed in this table. This ratio is determined by the binary value of the RCW Configuration field MEM_PLL_RAT[10:14].

3.1.8 Frame Manager (FMan) clock select

The Frame Managers (FM) can each be synchronous with or asynchronous to the platform, depending on configuration.

This table describes the clocking options that may be applied to each FM. The clock selection is determined by the binary value of the RCW Clocking Configuration fields FM1_CLK_SEL and FM2_CLK_SEL.

Table 105. Frame Manager (FMan) clock select

Binary value of FM*n*_CLK_SEL	FM frequency
0b0	Platform Clock Frequency /2
0b1	FMan PLL Frequency /2 [1,2]

Notes:

1. For asynchronous mode, max frequency see Table 94.
2. For PLL settings, see Table 96.

3.2 Supply power default setting

This chip is capable of supporting multiple power supply levels on its I/O supplies. The I/O voltage select inputs, shown in the following table, properly configure the receivers and drivers of the I/Os associated with the BVDD, CVDD, and LVDD power planes, respectively.

WARNING

Incorrect voltage select settings can lead to irreversible device damage.

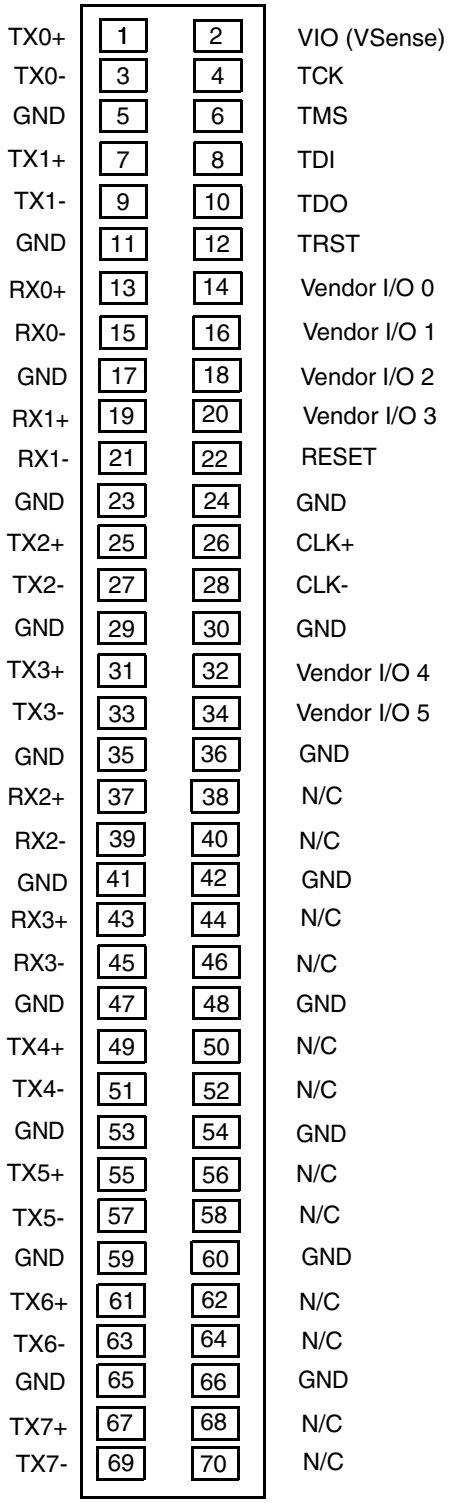

Figure 58. Aurora 70 pin connector duplex pinout