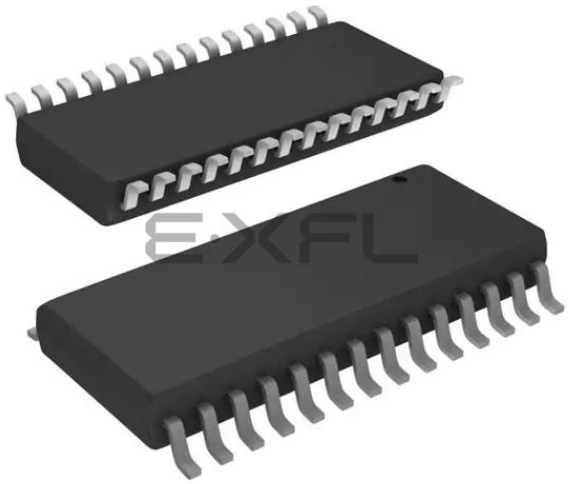

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Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	40MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVD, Power Control PWM, QEI, POR, PWM, WDT
Number of I/O	24
Program Memory Size	8KB (4K x 16)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	4.2V ~ 5.5V
Data Converters	A/D 5x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18f2331-e-so

TABLE 1-3: PIC18F4331/4431 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	PDIP	TQFP	QFN			
						PORTB is a bidirectional I/O port. PORTB can be software programmed for internal weak pull-ups on all inputs.
RB0/PWM0	33	8	9			
RB0				I/O	TTL	Digital I/O.
PWM0				O	TTL	PWM Output 0.
RB1/PWM1	34	9	10			
RB1				I/O	TTL	Digital I/O.
PWM1				O	TTL	PWM Output 1.
RB2/PWM2	35	10	11			
RB2				I/O	TTL	Digital I/O.
PWM2				O	TTL	PWM Output 2.
RB3/PWM3	36	11	12			
RB3				I/O	TTL	Digital I/O.
PWM3				O	TTL	PWM Output 3.
RB4/KBI0/PWM5	37	14	14			
RB4				I/O	TTL	Digital I/O.
KBI0				I	TTL	Interrupt-on-change pin.
PWM5				O	TTL	PWM Output 5.
RB5/KBI1/PWM4/ PGM	38	15	15			
RB5				I/O	TTL	Digital I/O.
KBI1				I	TTL	Interrupt-on-change pin.
PWM4				O	TTL	PWM Output 4.
PGM				I/O	ST	Single-Supply ICSP™ Programming entry pin.
RB6/KBI2/PGC	39	16	16			
RB6				I/O	TTL	Digital I/O.
KBI2				I	TTL	Interrupt-on-change pin.
PGC				I/O	ST	In-Circuit Debugger and ICSP programming clock pin.
RB7/KBI3/PGD	40	17	17			
RB7				I/O	TTL	Digital I/O.
KBI3				I	TTL	Interrupt-on-change pin.
PGD				I/O	ST	In-Circuit Debugger and ICSP programming data pin.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; I = Input; O = Output; P = Power

Note 1: RC3 is the alternate pin for T0CKI/T5CKI; RC4 is the alternate pin for SDI/SDA; RC5 is the alternate pin for SCK/SCL; RC7 is the alternate pin for SDO.

2: RD4 is the alternate pin for $\overline{\text{FLTA}}$.

3: RD5 is the alternate pin for PWM4.

FIGURE 5-5: TIME-OUT SEQUENCE ON POWER-UP (MCLR NOT TIED TO VDD): CASE 2

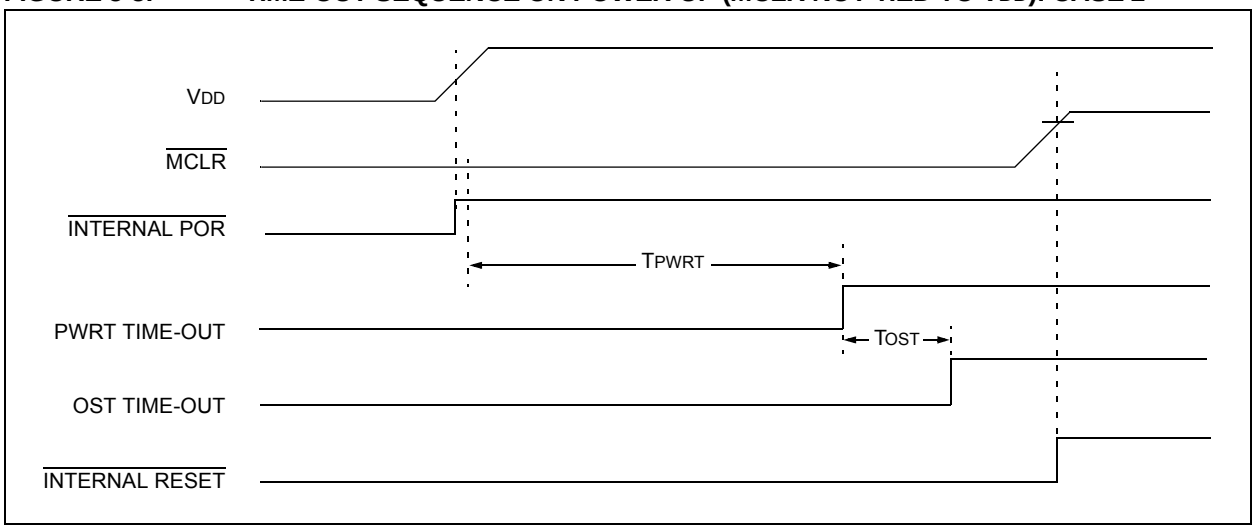
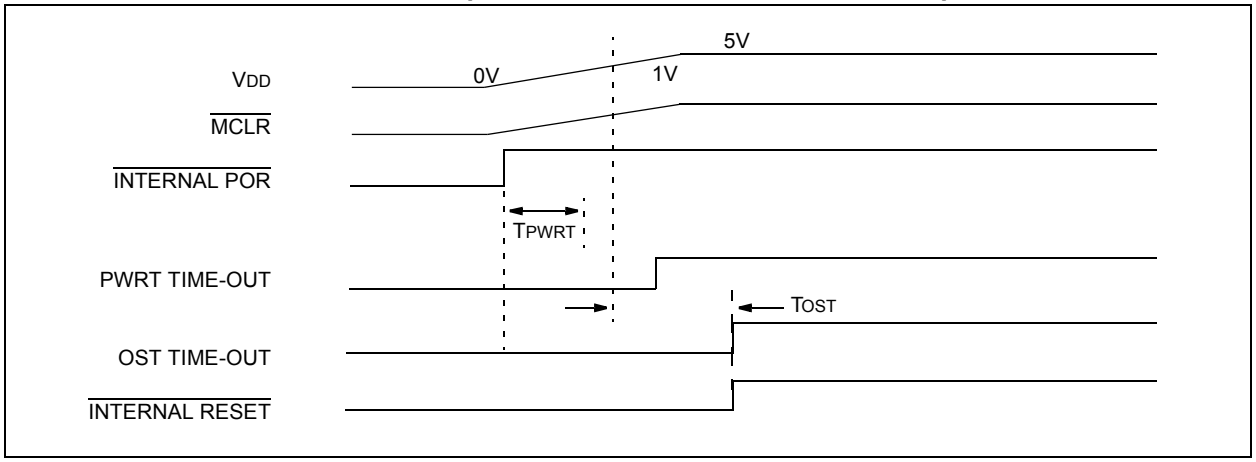


FIGURE 5-6: SLOW RISE TIME (MCLR TIED TO VDD, VDD RISE > TPWRT)



The PLUSW register can be used to implement a form of Indexed Addressing in the data memory space. By manipulating the value in the W register, users can reach addresses that are fixed offsets from pointer addresses. In some applications, this can be used to implement some powerful program control structure, such as software stacks, inside of data memory.

6.7.3.3 Operations by FSRs on FSRs

Indirect Addressing operations that target other FSRs or virtual registers represent special cases. For example, using an FSR to point to one of the virtual registers will not result in successful operations. As a specific case, assume that FSR0H:FSR0L contain FE7h, the address of INDF1. Attempts to read the value of the INDF1 using INDF0 as an operand will return 00h. Attempts to write to INDF1 using INDF0 as the operand will result in a NOP.

On the other hand, using the virtual registers to write to an FSR pair may not occur as planned. In these cases, the value will be written to the FSR pair but without any incrementing or decrementing. Thus, writing to INDF2 or POSTDEC2 will write the same value to the FSR2H:FSR2L.

Since the FSRs are physical registers mapped in the SFR space, they can be manipulated through all direct operations. Users should proceed cautiously when working on these registers, particularly if their code uses Indirect Addressing.

Similarly, operations by Indirect Addressing are generally permitted on all other SFRs. Users should exercise the appropriate caution that they do not inadvertently change settings that might affect the operation of the device.

REGISTER 10-6: PIR3: PERIPHERAL INTERRUPT REQUEST (FLAG) REGISTER 3

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	PTIF	IC3DRIF	IC2QEIF	IC1IF	TMR5IF
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-5 **Unimplemented:** Read as '0'

bit 4 **PTIF:** PWM Time Base Interrupt bit
- 1 = PWM time base matched the value in the PTPER registers. Interrupt is issued according to the postscaler settings. PTIF must be cleared in software.
- 0 = PWM time base has not matched the value in the PTPER registers

bit 3 **IC3DRIF:** IC3 Interrupt Flag/Direction Change Interrupt Flag bit

IC3 Enabled (CAP3CON<3:0>):
- 1 = TMR5 value was captured by the active edge on CAP3 input (must be cleared in software)
- 0 = TMR5 capture has not occurred

QEI Enabled (QEIM<2:0>):
- 1 = Direction of rotation has changed (must be cleared in software)
- 0 = Direction of rotation has not changed

bit 2 **IC2QEIF:** IC2 Interrupt Flag/QEI Interrupt Flag bit

IC2 Enabled (CAP2CON<3:0>):
- 1 = TMR5 value was captured by the active edge on CAP2 input (must be cleared in software)
- 0 = TMR5 capture has not occurred

QEI Enabled (QEIM<2:0>):
- 1 = The QEI position counter has reached the MAXCNT value, or the index pulse, INDX, has been detected. Depends on the QEI operating mode enabled. Must be cleared in software.
- 0 = The QEI position counter has not reached the MAXCNT value or the index pulse has not been detected

bit 1 IC1 Enabled (CAP1CON<3:0>):
- 1 = TMR5 value was captured by the active edge on CAP1 input (must be cleared in software)
- 0 = TMR5 capture has not occurred

QEI Enabled (QEIM<2:0>), Velocity Measurement Mode Enabled ($\overline{\text{VELM}}$ = 0 in QEICON register):
- 1 = Timer5 value was captured by the active velocity edge (based on PHA or PHB input). CAP1REN bit must be set in CAP1CON register. IC1IF must be cleared in software.
- 0 = Timer5 value was not captured by the active velocity edge

bit 0 **TMR5IF:** Timer5 Interrupt Flag bit
- 1 = Timer5 time base matched the PR5 value (must be cleared in software)
- 0 = Timer5 time base did not match the PR5 value

11.0 I/O PORTS

Depending on the device selected and features enabled, there are up to five ports available. Some pins of the I/O ports are multiplexed with an alternate function from the peripheral features on the device. In general, when a peripheral is enabled, that pin may not be used as a general purpose I/O pin.

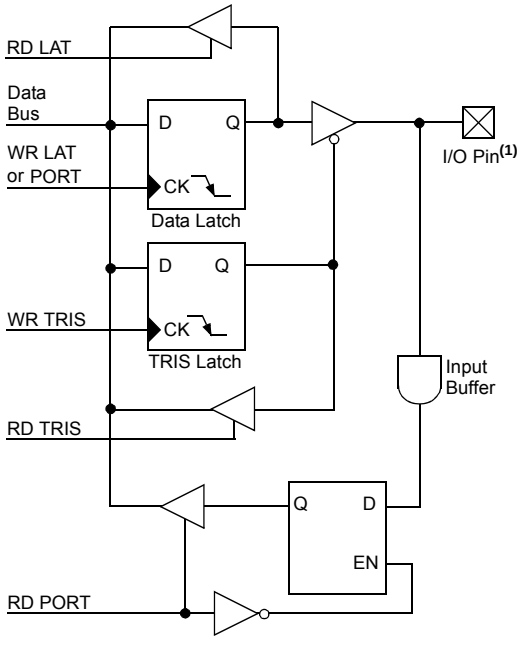
Each port has three registers for its operation. These registers are:

- TRIS register (Data Direction register)
- PORT register (reads the levels on the pins of the device)
- LAT register (Data Latch)

The Data Latch (LAT register) is useful for read-modify-write operations on the value that the I/O pins are driving.

A simplified model of a generic I/O port without the interfaces to other peripherals is shown in Figure 11-1.

FIGURE 11-1: GENERIC I/O PORT OPERATION



Note 1: I/O pins have diode protection to VDD and VSS.

11.1 PORTA, TRISA and LATA Registers

PORTA is an 8-bit wide, bidirectional port. The corresponding data direction register is TRISA. Setting a TRISA bit (= 1) will make the corresponding PORTA pin an input (i.e., put the corresponding output driver in a high-impedance mode). Clearing a TRISA bit (= 0) will make the corresponding PORTA pin an output (i.e., put the contents of the output latch on the selected pin).

Reading the PORTA register reads the status of the pins, whereas writing to it, will write to the port latch.

The Data Latch register (LATA) is also memory mapped. Read-modify-write operations on the LATA register read and write the latched output value for PORTA.

The RA<4:2> pins are multiplexed with three input capture pins and Quadrature Encoder Interface pins. Pins, RA6 and RA7, are multiplexed with the main oscillator pins. They are enabled as oscillator or I/O pins by the selection of the main oscillator in Configuration Register 1H (see **Section 23.1 "Configuration Bits"** for details). When they are not used as port pins, RA6 and RA7 and their associated TRIS and LAT bits are read as '0'.

The other PORTA pins are multiplexed with analog inputs, the analog VREF+ and VREF- inputs and the comparator voltage reference output. The operation of pins RA<3:0> and RA5 as A/D Converter inputs is selected by clearing/setting the control bits in the ANSEL0 and ANSEL1 registers.

Note 1: On a Power-on Reset, RA<5:0> are configured as analog inputs and read as '0'.

2: RA5 I/F is available only on 40-pin devices (PIC18F4331/4431).

The TRISA register controls the direction of the RA pins, even when they are being used as analog inputs. The user must ensure the bits in the TRISA register are maintained set when using them as analog inputs.

EXAMPLE 11-1: INITIALIZING PORTA

```
CLRF    PORTA   ; Initialize PORTA by
                ; clearing output
                ; data latches
CLRF    LATA    ; Alternate method
                ; to clear output
                ; data latches
MOVLW   0x3F    ; Configure A/D
MOVWF   ANSEL0  ; for digital inputs
MOVLW   0xCF    ; Value used to
                ; initialize data
                ; direction
MOVWF   TRISA   ; Set RA<3:0> as inputs
                ; RA<5:4> as outputs
```

When in Counter mode, the counter must be configured as the synchronous counter only ($\overline{T5SYNC}$ = 0). When configured in Asynchronous mode, the IC module will not work properly.

Note 1: Input capture prescalers are reset (cleared) when the input capture module is disabled (CAPxM = 0000).

2: When the Input Capture mode is changed, without first disabling the module and entering the new Input Capture mode, a false interrupt (or Special Event Trigger on IC1) may be generated. The user should either: (1) disable the input capture before entering another mode, or (2) disable IC interrupts to avoid false interrupts during IC mode changes.

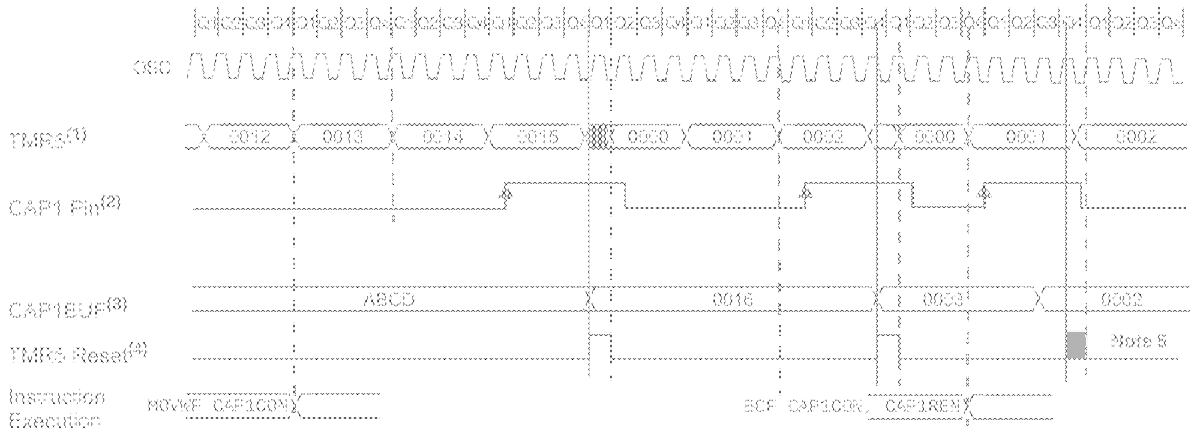
3: During IC mode changes, the prescaler count will not be cleared, therefore, the first capture in the new IC mode may be from the non-zero prescaler.

17.1.1 EDGE CAPTURE MODE

In this mode, the value of the time base is captured either on every rising edge, every falling edge, every 4th rising edge, or every 16th rising edge. The edge present on the input capture pin (CAP1, CAP2 or CAP3) is sampled by the synchronizing latch. The signal is used to load the Input Capture Buffer (ICxBUF register) on the following Q1 clock (see Figure 17-4). Consequently, Timer5 is either reset to '0' (Q1 immediately following the capture event) or left free running, depending on the setting of the Capture Reset Enable bit, CAPxREN, in the CAPxCON register.

Note: On the first capture edge following the setting of the Input Capture mode (i.e., MOVWF CAP1CON), Timer5 contents are always captured into the corresponding Input Capture Buffer (i.e., CAPxBUF). Timer5 can optionally be reset; however, this is dependent on the setting of the Capture Reset Enable bit, CAPxREN (see Figure 17-4).

FIGURE 17-4: EDGE CAPTURE MODE TIMING



Note 1: TMR5 is a synchronous time base input to the input capture; prescaler = 1:1. It increments on the Q1 rising edge.

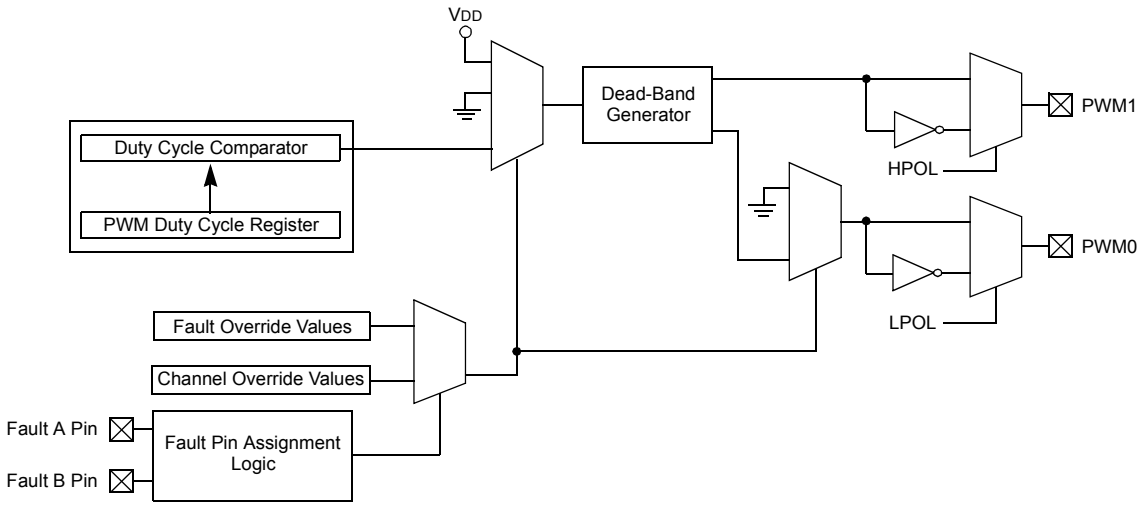
2: IC1 is configured in Edge Capture mode (CAP1M<3:0> = 0010) with the time base reset upon edge capture (CAP1REN = 1) and no noise filter.

3: TMR5 value is latched by CAP1BUF on TCY. In the event that a write to TMR5 coincides with an input capture event, the write will always take precedence. All Input Capture Buffers, CAP1BUF, CAP2BUF and CAP3BUF, are updated with the incremented value of the time base on the next TCY clock edge when the capture event takes place (see Note 4 when Reset occurs).

4: TMR5 Reset is normally an asynchronous Reset signal to TMR5. When used with the input capture, it is active immediately after the time base value is captured.

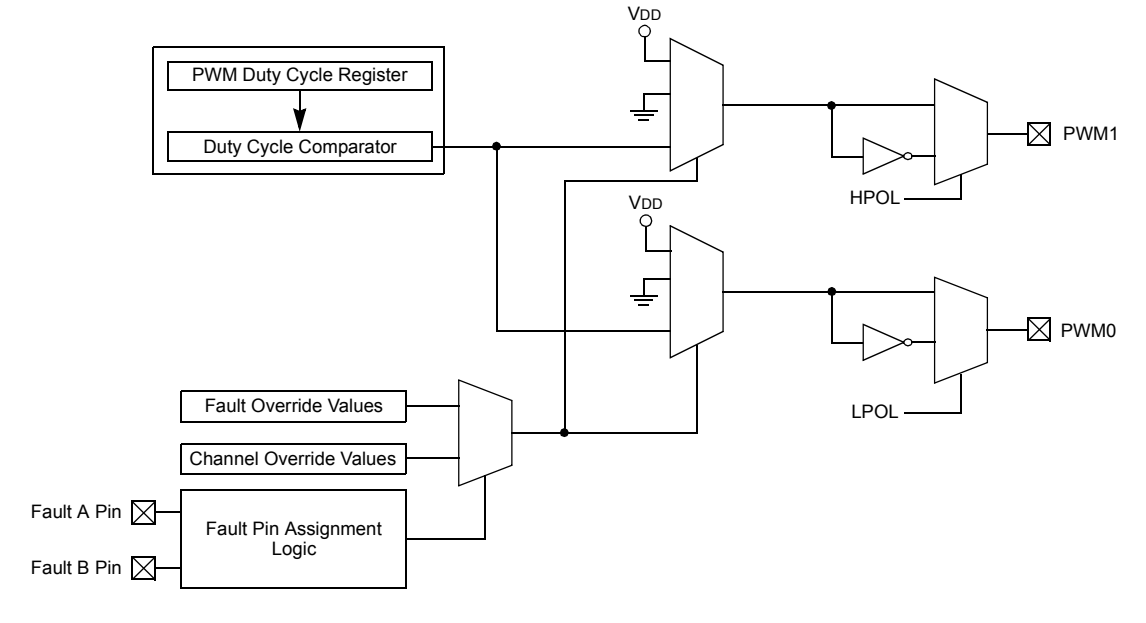
5: TMR5 Reset pulse is disabled by clearing the CAP1REN bit (e.g., BCF CAP1CON, CAP1REN).

FIGURE 18-2: PWM MODULE BLOCK DIAGRAM, ONE OUTPUT PAIR, COMPLEMENTARY MODE



Note: In Complementary mode, the even channel cannot be forced active by a Fault or override event when the odd channel is active. The even channel is always the complement of the odd channel and is inactive, with dead time inserted, before the odd channel is driven to its active state.

FIGURE 18-3: PWM MODULE BLOCK DIAGRAM, ONE OUTPUT PAIR, INDEPENDENT MODE



This module contains four duty cycle generators, numbered 0 through 3. The module has eight PWM output pins, numbered 0 through 7. The eight PWM outputs are grouped into output pairs of even and odd numbered outputs. In Complementary modes, the even PWM pins must always be the complement of the corresponding odd PWM pin. For example, PWM0 will be the complement of PWM1, PWM2 will be the complement of PWM3 and so on. The dead-time generator inserts an OFF period called “dead time” between the going OFF of one pin to the going ON of the complementary pin of the paired pins. This is to prevent damage to the power switching devices that will be connected to the PWM output pins.

The time base for the PWM module is provided by its own 12-bit timer, which also incorporates selectable prescaler and postscaler options.

18.4.4 INTERRUPTS IN DOUBLE UPDATE MODE

This mode is available in Continuous Up/Down Count mode. In the Double Update mode (PTMOD<1:0> = 11), an interrupt event is generated each time the PTMR register is equal to zero and each time the PTMR matches with PTPER register. Figure 18-8 shows the interrupts in Continuous Up/Down Count mode with double updates.

The Double Update mode provides two additional functions to the user in Center-Aligned mode.

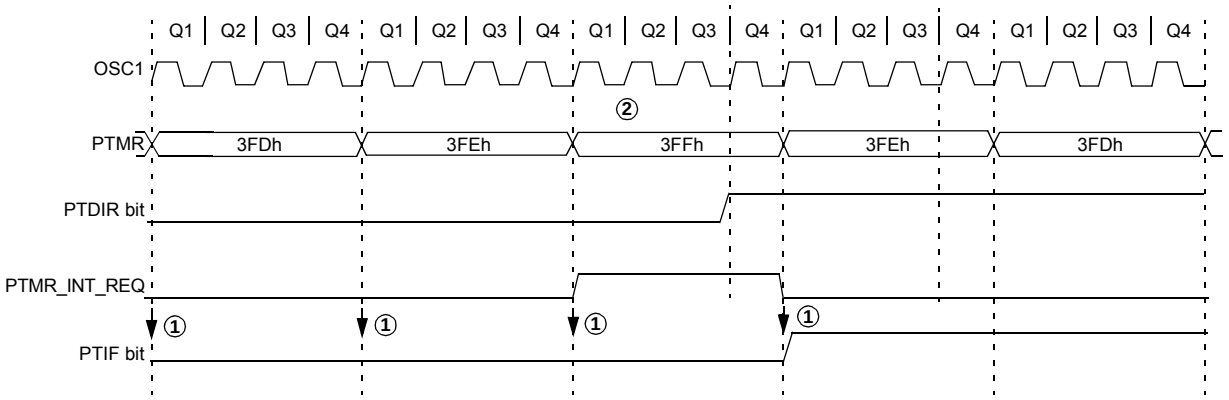
1. The control loop bandwidth is doubled because the PWM duty cycles can be updated twice per period.
2. Asymmetrical center-aligned PWM waveforms can be generated, which are useful for minimizing output waveform distortion in certain motor control applications.

Note:	Do not change the PTMOD bits while PTEN is active; it will yield unexpected results. To change the PWM Timer mode of operation, first clear the PTEN bit, load the PTMOD bits with the required data and then set PTEN.

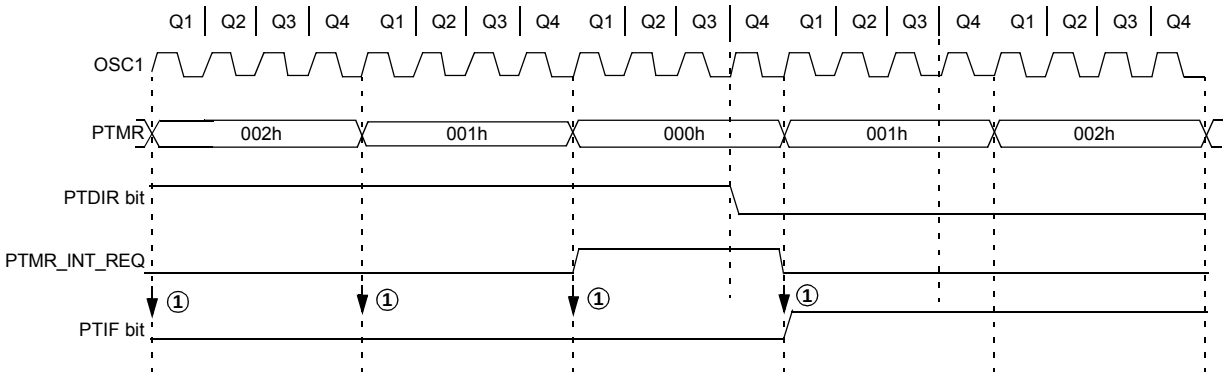
FIGURE 18-8: PWM TIME BASE INTERRUPT, CONTINUOUS UP/DOWN COUNT MODE WITH DOUBLE UPDATES

A: PRESCALER = 1:1

Case 1: PTMR Counting Upwards



Case 2: PTMR Counting Downwards



Note 1: Interrupt flag bit, PTIF, is sampled here (every Q1).

2: PWM Time Base Period register, PTPER, is loaded with the value, 3FFh, for this example.

18.12.3 PWM OUTPUTS WHILE IN FAULT CONDITION

While in the Fault state (i.e., one or both $\overline{\text{FLTA}}$ and $\overline{\text{FLTB}}$ inputs are active), the PWM output signals are driven into their inactive states. The selection of which PWM outputs are deactivated (while in the Fault state) is determined by the FLTCON bit in the FLTCONFIG register as follows:

- FLTCON = 1: When $\overline{\text{FLTA}}$ or $\overline{\text{FLTB}}$ is asserted, the PWM outputs (i.e., PWM<7:0>) are driven into their inactive state.
- FLTCON = 0: When $\overline{\text{FLTA}}$ or $\overline{\text{FLTB}}$ is asserted, only PWM<5:0> outputs are driven inactive, leaving PWM<7:6> activated.

Note:	Disabling only three PWM channels and leaving one PWM channel enabled when in the Fault state, allows the flexibility to have at least one PWM channel enabled. None of the PWM outputs can be enabled (driven with the PWM Duty Cycle registers) while FLTCON = 1 and the Fault condition is present.

18.12.4 PWM OUTPUTS IN DEBUG MODE

The BRFEN bit in the FLTCONFIG register controls the simulation of a Fault condition, when a breakpoint is hit, while debugging the application using an In-Circuit Emulator (ICE) or an In-Circuit Debugger (ICD). Setting the BRFEN to high, enables the Fault condition on breakpoint, thus driving the PWM outputs to the inactive state. This is done to avoid any continuous keeping of status on the PWM pin, which may result in damage of the power devices connected to the PWM outputs.

If BRFEN = 0, the Fault condition on breakpoint is disabled.

Note:	It is highly recommended to enable the Fault condition on breakpoint if a debugging tool is used while developing the firmware and high-power circuitry. When the device is ready to program after debugging the firmware, the BRFEN bit can be disabled.

TABLE 18-6: REGISTERS ASSOCIATED WITH THE POWER CONTROL PWM MODULE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on Page:
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	54
IPR3	—	—	—	PTIP	IC3DRIP	IC2QEIP	IC1IP	TMR5IP	56
PIE3	—	—	—	PTIE	IC3DRIE	IC2QEIE	IC1IE	TMR5IE	56
PIR3	—	—	—	PTIF	IC3DRIF	IC2QEIF	IC1IF	TMR5IF	56
PTCON0	PTOPS3	PTOPS2	PTOPS1	PTOPS0	PTCKPS1	PTCKPS0	PTMOD1	PTMOD0	58
PTCON1	PTEN	PTDIR	—	—	—	—	—	—	58
PTMRL(1)	PWM Time Base Register (lower 8 bits)								58
PTMRH(1)	**UNUSED**				PWM Time Base Register (upper 4 bits)				58
PTPERL(1)	PWM Time Base Period Register (lower 8 bits)								58
PTPERH(1)	**UNUSED**				PWM Time Base Period Register (upper 4 bits)				58
SEVTCMPL(1)	PWM Special Event Compare Register (lower 8 bits)								58
SEVTCMPH(1)	**UNUSED**				PWM Special Event Compare Register (upper 4 bits)				58
PWMCON0	—	PWMEN2	PWMEN1	PWMEN0	PMOD3(2)	PMOD2	PMOD1	PMOD0	58
PWMCON1	SEVOPS3	SEVOPS2	SEVOPS1	SEVOPS0	SEVTDIR	—	UDIS	OSYNC	58
DTCON	DTPS1	DTPS0	DT5	DT4	DT3	DT2	DT1	DT0	58
FLTCONFIG	BRFEN	FLTBS(2)	FLTBMOD(2)	FLTBEN(2)	FLTCON	FLTAS	FLTAMOD	FLTAEN	58
OVDCOND	POVD7(2)	POVD6(2)	POVD5	POVD4	POVD3	POVD2	POVD1	POVD0	58
OVDCONS	POUT7(2)	POUT6(2)	POUT5	POUT4	POUT3	POUT2	POUT1	POUT0	58
PDC0L(1)	PWM Duty Cycle #0L Register (lower 8 bits)								58
PDC0H(1)	**UNUSED**		PWM Duty Cycle #0H Register (upper 6 bits)						58
PDC1L(1)	PWM Duty Cycle #1L register (lower 8 bits)								58
PDC1H(1)	**UNUSED**		PWM Duty Cycle #1H Register (upper 6 bits)						58
PDC2L(1)	PWM Duty Cycle #2L Register (lower 8 bits)								58
PDC2H(1)	**UNUSED**		PWM Duty Cycle #2H Register (upper 6 bits)						58
PDC3L(1,2)	PWM Duty Cycle #3L Register (lower 8 bits)								58
PDC3H(1,2)	**UNUSED**		PWM Duty Cycle #3H Register (upper 6 bits)						58

Legend: — = Unimplemented, read as '0'. Shaded cells are not used with the power control PWM.

Note 1: Double-buffered register pairs. Refer to text for explanation of how these registers are read and written to.

2: Unimplemented in PIC18F2331/2431 devices; maintain these bits clear. Reset values shown are for PIC18F4331/4431 devices.

NOTES:

20.3.5 BREAK CHARACTER SEQUENCE

The Enhanced USART module has the capability of sending the special Break character sequences that are required by the LIN/J2602 bus standard. The Break character transmit consists of a Start bit, followed by twelve '0' bits and a Stop bit. The Frame Break character is sent whenever the SENDB and TXEN bits (TXSTA<3> and TXSTA<5>) are set while the Transmit Shift register is loaded with data. Note that the value of data written to TXREG will be ignored and all '0's will be transmitted.

The SENDB bit is automatically reset by hardware after the corresponding Stop bit is sent. This allows the user to preload the transmit FIFO with the next transmit byte following the Break character (typically, the Sync character in the LIN/J2602 specification).

Note that the data value written to the TXREG for the Break character is ignored. The write simply serves the purpose of initiating the proper sequence.

The TRMT bit indicates when the transmit operation is active or Idle, just as it does during normal transmission. See Figure 20-9 for the timing of the Break character sequence.

20.3.5.1 Break and Sync Transmit Sequence

The following sequence will send a message frame header made up of a Break, followed by an Auto-Baud Sync byte. This sequence is typical of a LIN/J2602 bus master.

1. Configure the EUSART for the desired mode.
2. Set the TXEN and SENDB bits to setup the Break character.
3. Load the TXREG with a dummy character to initiate transmission (the value is ignored).
4. Write '55h' to TXREG to load the Sync character into the transmit FIFO buffer.
5. After the Break has been sent, the SENDB bit is reset by hardware. The Sync character now transmits in the preconfigured mode.

When the TXREG becomes empty, as indicated by the TXIF, the next data byte can be written to TXREG.

20.3.6 RECEIVING A BREAK CHARACTER

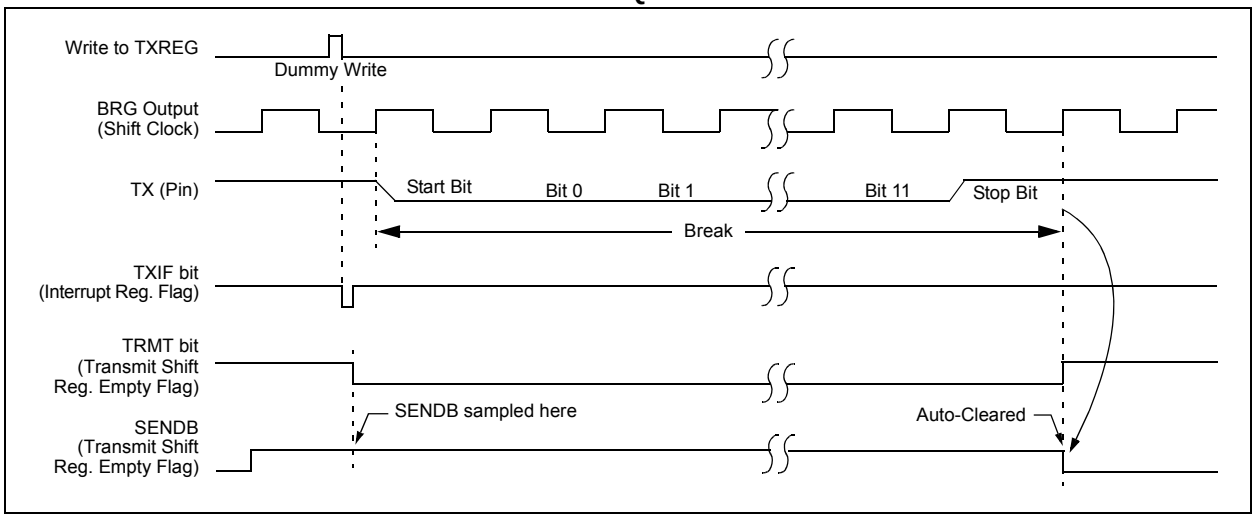
The Enhanced USART module can receive a Break character in two ways.

The first method forces configuration of the baud rate at a frequency of 9/13 of the typical speed. This allows for the Stop bit transition to be at the correct sampling location (13 bits for Break versus Start bit and 8 data bits for typical data).

The second method uses the auto-wake-up feature described in **Section 20.3.4 "Auto-Wake-up on Sync Break Character"**. By enabling this feature, the EUSART will sample the next two transitions on RX/DT, cause an RCIF interrupt and receive the next data byte followed by another interrupt.

Note that following a Break character, the user will typically want to enable the Auto-Baud Rate Detect feature. For both methods, the user can set the ABD bit before placing the EUSART in its Sleep mode.

FIGURE 20-9: SEND BREAK CHARACTER SEQUENCE



20.4 EUSART Synchronous Master Mode

The Synchronous Master mode is entered by setting the CSRC bit (TXSTA<7>). In this mode, the data is transmitted in a half-duplex manner (i.e., transmission and reception do not occur at the same time). When transmitting data, the reception is inhibited and vice versa. Synchronous mode is entered by setting bit SYNC (TXSTA<4>). In addition, enable bit SPEN (RCSTA<7>) is set in order to configure the RC6/TX/CK/$\overline{SS}$ and RC7/RX/DT/SDO I/O pins to CK (clock) and DT (data) lines, respectively.

The Master mode indicates that the processor transmits the master clock on the CK line. Clock polarity is selected with the SCKP bit (BAUDCON<4>). Setting SCKP sets the Idle state on CK as high, while clearing the bit, sets the Idle state low. This option is provided to support Microwire devices with this module.

20.4.1 EUSART SYNCHRONOUS MASTER TRANSMISSION

The EUSART transmitter block diagram is shown in Figure 20-2. The heart of the transmitter is the Transmit (Serial) Shift Register (TSR). The Shift register obtains its data from the Read/Write Transmit Buffer register, TXREG. The TXREG register is loaded with data in software. The TSR register is not loaded until the last bit has been transmitted from the previous load. As soon as the last bit is transmitted, the TSR is loaded with new data from the TXREG (if available).

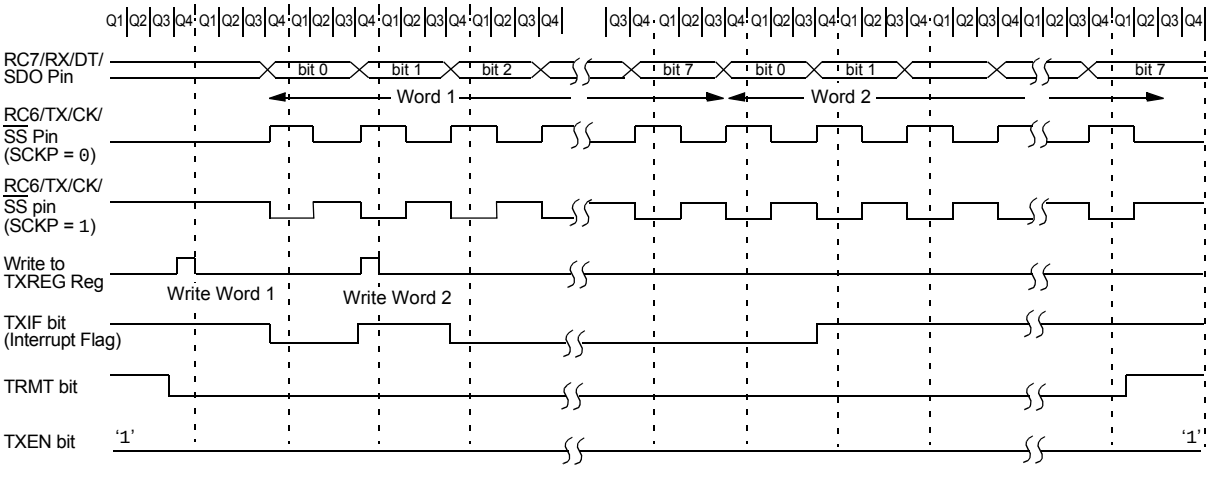
Once the TXREG register transfers the data to the TSR register (occurs in one TCYCLE), the TXREG is empty and interrupt bit, TXIF (PIR1<4>), is set. The interrupt can be enabled/disabled by setting/clearing enable bit, TXIE (PIE1<4>). Flag bit, TXIF, will be set, regardless of the state of enable bit, TXIE, and cannot be cleared in software. It will reset only when new data is loaded into the TXREG register.

While flag bit, TXIF, indicates the status of the TXREG register, another bit, TRMT (TXSTA<1>), shows the status of the TSR register. TRMT is a read-only bit which is set when the TSR is empty. No interrupt logic is tied to this bit, so the user must poll this bit in order to determine if the TSR register is empty. The TSR is not mapped in data memory, so it is not available to the user.

To set up a Synchronous Master Transmission:

1. Initialize the SPBRGH:SPBRG registers for the appropriate baud rate. Set or clear the BRGH and BRG16 bits, as required, to achieve the desired baud rate.
2. Enable the synchronous master serial port by setting bits, SYNC, SPEN and CSRC.
3. If interrupts are desired, set enable bit, TXIE.
4. If 9-bit transmission is desired, set bit, TX9.
5. Enable the transmission by setting bit, TXEN.
6. If 9-bit transmission is selected, the ninth bit should be loaded in bit, TX9D.
7. Start transmission by loading data to the TXREG register.
8. If using interrupts, ensure that the GIE and PEIE bits in the INTCON register (INTCON<7:6>) are set.

FIGURE 20-10: SYNCHRONOUS TRANSMISSION



Note: Sync Master mode, SPBRG = 0, continuous transmission of two 8-bit words.

21.9 A/D Conversions

Figure 21-3 shows the operation of the A/D Converter after the GO/$\overline{\text{DONE}}$ bit has been set and the ACQT<2:0> bits are cleared. A conversion is started after the following instruction to allow entry into Sleep mode before the conversion begins. The internal A/D RC oscillator must be selected to perform a conversion in Sleep.

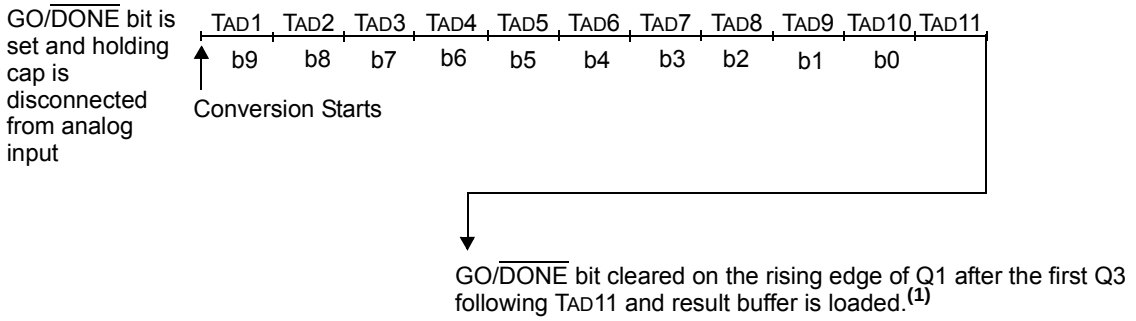
Figure 21-4 shows the operation of the A/D Converter after the GO/$\overline{\text{DONE}}$ bit has been set, the ACQT<3:0> bits are set to '010' and a 4 TAD acquisition time is selected before the conversion starts.

Clearing the GO/$\overline{\text{DONE}}$ bit during a conversion will abort the current conversion. The resulting buffer location will contain the partially completed A/D conversion sample. This will not set the ADIF flag, therefore, the user must read the buffer location before a conversion sequence overwrites it.

After the A/D conversion is completed or aborted, a 2 TAD wait is required before the next acquisition can be started. After this wait, acquisition on the selected channel is automatically started.

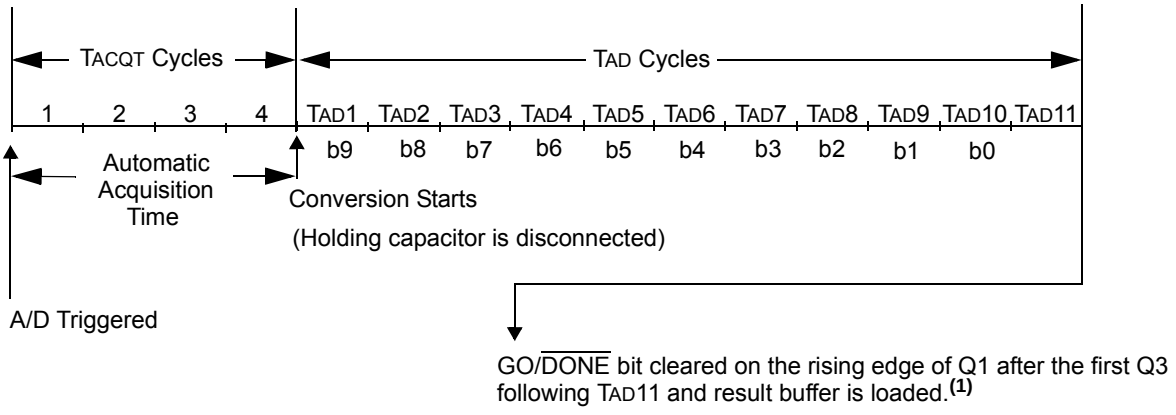
Note:	The GO/$\overline{\text{DONE}}$ bit should **NOT** be set in the same instruction that turns on the A/D.

FIGURE 21-3: A/D CONVERSION TAD CYCLES (ACQT<2:0> = 000, TACQ = 0)



Note 1: Conversion time is a minimum of 11 TAD + 2 TCY and a maximum of 11 TAD + 6 TCY.

FIGURE 21-4: A/D CONVERSION TAD CYCLES (ACQT<3:0> = 0010, TACQ = 4 TAD)



Note 1: In Continuous modes, next conversion starts at the end of TAD12.

RRNCF **Rotate Right f (No Carry)**

Syntax: [*label*] RRNCF f [,d [,a]]

Operands: $0 \le f \le 255$
$d \in [0,1]$
$a \in [0,1]$

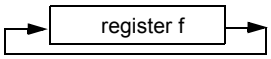
Operation: (f<n>) → dest<n – 1>,
(f<0>) → dest<7>

Status Affected: N, Z

Encoding:

0100	00da	ffff	ffff

Description: The contents of register, 'f', are rotated one bit to the right. If 'd' is '0', the result is placed in W. If 'd' is '1', the result is placed back in register, 'f'. If 'a' is '0', the Access Bank will be selected, overriding the BSR value. If 'a' is '1', then the bank will be selected as per the BSR value.



Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	Write to destination

Example 1:
```
RRNCF   REG, 1, 0
```
Before Instruction
REG = 1101 0111
After Instruction
REG = 1110 1011

Example 2:
```
RRNCF   REG, W
```
Before Instruction
W = ?
REG = 1101 0111
After Instruction
W = 1110 1011
REG = 1101 0111

SETF **Set f**

Syntax: [*label*] SETF f [,a]

Operands: $0 \le f \le 255$
$a \in [0,1]$

Operation: FFh → f

Status Affected: None

Encoding:

0110	100a	ffff	ffff

Description: The contents of the specified register are set to FFh. If 'a' is '0', the Access Bank will be selected, overriding the BSR value. If 'a' is '1', then the bank will be selected as per the BSR value.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	Write register 'f'

Example:
```
SETF    REG
```
Before Instruction
REG = 0x5A
After Instruction
REG = 0xFF

XORWF **Exclusive OR W with f**

Syntax: [*label*] XORWF f [,d [,a]]

Operands: $0 \le f \le 255$
$d \in [0,1]$
$a \in [0,1]$

Operation: (W) .XOR. (f) → dest

Status Affected: N, Z

Encoding:

0001	10da	ffff	ffff

Description: Exclusive OR the contents of W with register, 'f'. If 'd' is '0', the result is stored in W. If 'd' is '1', the result is stored back in the register, 'f'. If 'a' is '0', the Access Bank will be selected, overriding the BSR value. If 'a' is '1', then the bank will be selected as per the BSR value.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	Write to destination

Example: XORWF REG

Before Instruction
REG = 0xAF
W = 0xB5

After Instruction
REG = 0x1A
W = 0xB5

TABLE 26-8: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER AND BROWN-OUT RESET REQUIREMENTS

Param. No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
30	TMCL	$\overline{\text{MCLR}}$ Pulse Width (low)	2	—	—	μs	
31	TWDT	Watchdog Timer Time-out Period (no postscaler)	—	4.00	—	ms	
32	TOST	Oscillation Start-up Timer Period	1024 TOSC	—	1024 TOSC	—	TOSC = OSC1 period
33	TPWRT	Power-up Timer Period	—	65.5	—	ms	
34	TIOZ	I/O High-impedance from $\overline{\text{MCLR}}$ Low or Watchdog Timer Reset	—	2	—	μs	
35	TBOR	Brown-out Reset Pulse Width	200	—	—	μs	VDD ≤ BVDD (see D005)
36	TIRVST	Time for Internal Reference Voltage to become Stable	—	20	50	μs	
37	TLVD	Low-Voltage Detect Pulse Width	200	—	—	μs	VDD ≤ VLVD
38	TCSD	CPU Start-up Time	—	10	—	μs	
39	TIOBST	Time for INTOSC to Stabilize	—	1	—	ms	

FIGURE 26-15: I²C™ BUS START/STOP BITS TIMING

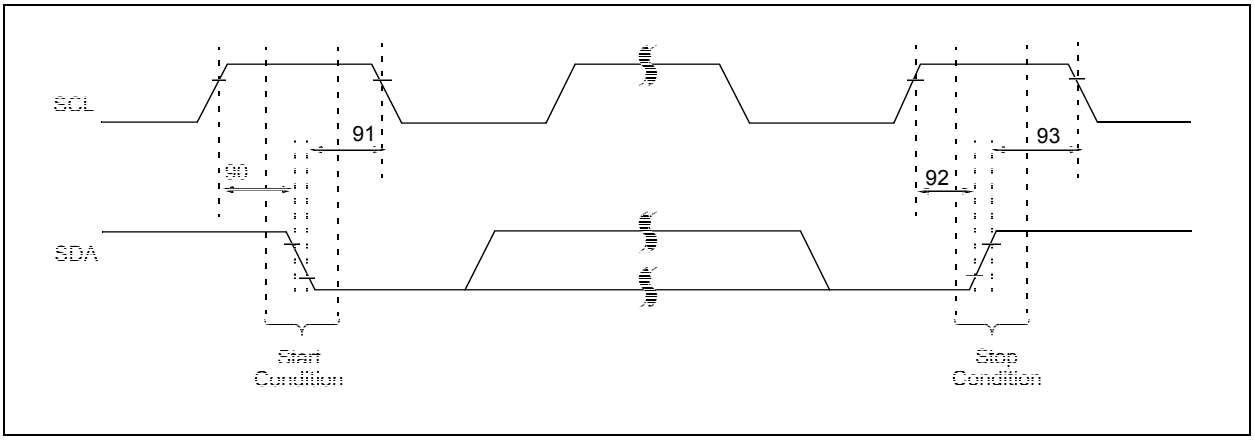
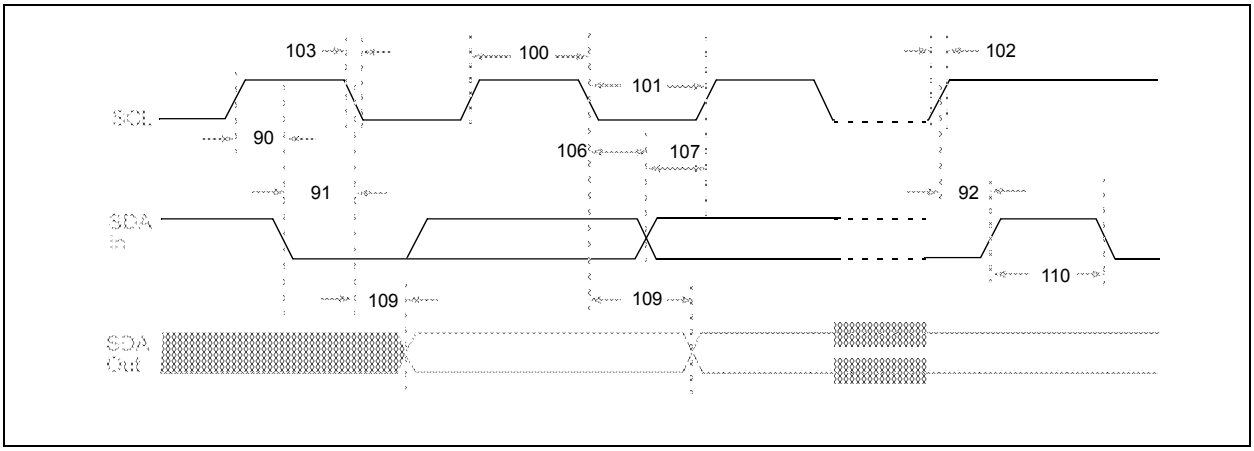


TABLE 26-15: I²C™ BUS START/STOP BITS REQUIREMENTS (SLAVE MODE)

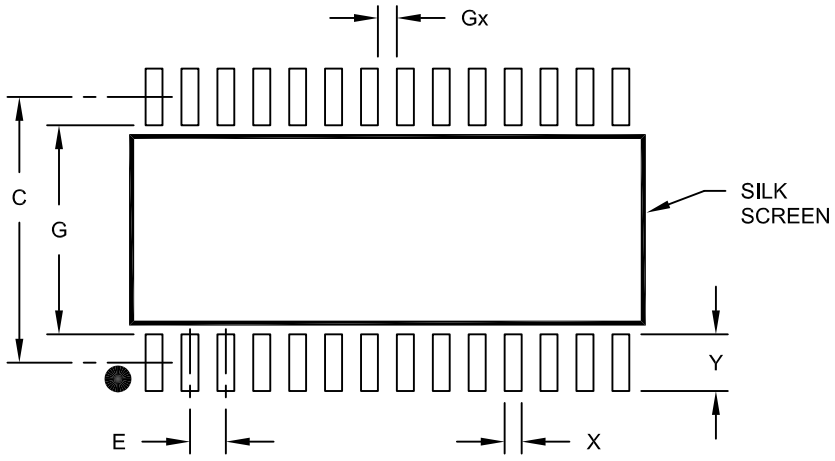
Param. No.	Symbol	Characteristic		Min	Max	Units	Conditions
90	TSU:STA	Start Condition	100 kHz mode	4700	—	ns	Only relevant for repeated Start condition
		Setup Time	400 kHz mode	600	—		
91	THD:STA	Start Condition	100 kHz mode	4000	—	ns	After this period, the first clock pulse is generated
		Hold Time	400 kHz mode	600	—		
92	TSU:STO	Stop Condition	100 kHz mode	4000	—	ns	
		Setup Time	400 kHz mode	600	—		
93	THD:STO	Stop Condition	100 kHz mode	4700	—	ns	
		Hold Time	400 kHz mode	600	—		

FIGURE 26-16: I²C™ BUS DATA TIMING



28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		9.40	
Contact Pad Width (X28)	X			0.60
Contact Pad Length (X28)	Y			2.00
Distance Between Pads	Gx	0.67		
Distance Between Pads	G	7.40		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2052A

APPENDIX E: MIGRATION FROM MID-RANGE TO ENHANCED DEVICES

A detailed discussion of the differences between the mid-range MCU devices (i.e., PIC16CXXX) and the enhanced devices (i.e., PIC18FXXX) is provided in AN716, “Migrating Designs from PIC16C74A/74B to PIC18F442.” The changes discussed, while device-specific, are generally applicable to all mid-range to enhanced device migrations.

This Application Note is available on Microchip’s web site: www.Microchip.com.

APPENDIX F: MIGRATION FROM HIGH-END TO ENHANCED DEVICES

A detailed discussion of the migration pathway and differences between the high-end MCU devices (i.e., PIC17CXXX) and the enhanced devices (i.e., PIC18FXXX) is provided in AN726, “PIC17CXXX to PIC18FXXX Migration.”

This Application Note is available on Microchip’s web site: www.Microchip.com.