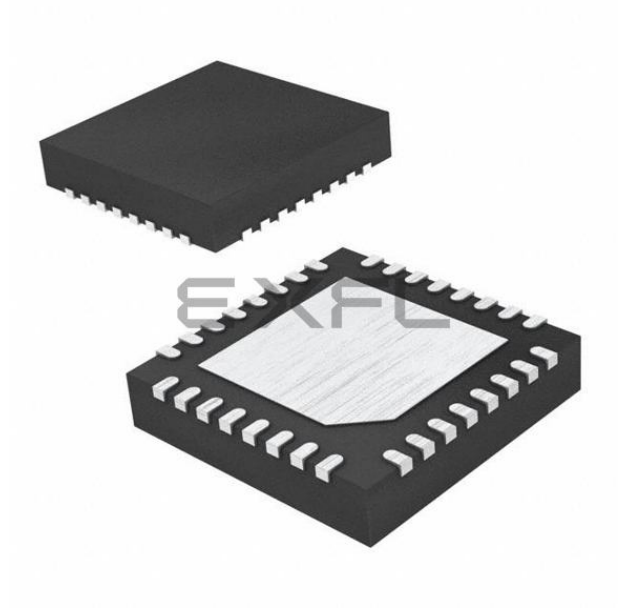

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Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	768 x 8
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Oscillator Type	Internal
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TABLE 1-2: PIC18F2331/2431 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	SPDIP, SOIC	QFN			
					PORTB is a bidirectional I/O port. PORTB can be software programmed for internal weak pull-ups on all inputs.
RB0/PWM0	21	18			
RB0			I/O	TTL	Digital I/O.
PWM0			O	TTL	PWM Output 0.
RB1/PWM1	22	19			
RB1			I/O	TTL	Digital I/O.
PWM1			O	TTL	PWM Output 1.
RB2/PWM2	23	20			
RB2			I/O	TTL	Digital I/O.
PWM2			O	TTL	PWM Output 2.
RB3/PWM3	24	21			
RB3			I/O	TTL	Digital I/O.
PWM3			O	TTL	PWM Output 3.
RB4/KBI0/PWM5	25	22			
RB4			I/O	TTL	Digital I/O.
KBI0			I	TTL	Interrupt-on-change pin.
PWM5			O	TTL	PWM Output 5.
RB5/KBI1/PWM4/PGM	26	23			
RB5			I/O	TTL	Digital I/O.
KBI1			I	TTL	Interrupt-on-change pin.
PWM4			O	TTL	PWM Output 4.
PGM			I/O	ST	Single-Supply ICSP™ Programming entry pin.
RB6/KBI2/PGC	27	24			
RB6			I/O	TTL	Digital I/O.
KBI2			I	TTL	Interrupt-on-change pin.
PGC			I/O	ST	In-Circuit Debugger and ICSP programming clock pin.
RB7/KBI3/PGD	28	25			
RB7			I/O	TTL	Digital I/O.
KBI3			I	TTL	Interrupt-on-change pin.
PGD			I/O	ST	In-Circuit Debugger and ICSP programming data pin.

Legend: TTL = TTL compatible input
CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels
I = Input
O = Output
P = Power

TABLE 1-3: PIC18F4331/4431 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	PDIP	TQFP	QFN			
						PORTD is a bidirectional I/O port.
RD0/T0CKI/T5CKI	19	38	38			
RD0				I/O	ST	Digital I/O.
T0CKI				I	ST	Timer0 external clock input.
T5CKI				I	ST	Timer5 input clock.
RD1/SDO	20	39	39			
RD1				I/O	ST	Digital I/O.
SDO(1)				O	—	SPI data out.
RD2/SDI/SDA	21	40	40			
RD2				I/O	ST	Digital I/O.
SDI(1)				I	ST	SPI data in.
SDA(1)				I/O	ST	I^2C™ data I/O.
RD3/SCK/SCL	22	41	41			
RD3				I/O	ST	Digital I/O.
SCK(1)				I/O	ST	Synchronous serial clock input/output for SPI mode.
SCL(1)				I/O	ST	Synchronous serial clock input/output for I^2C mode.
RD4/$\overline{\text{FLTA}}$	27	2	2			
RD4				I/O	ST	Digital I/O.
$\overline{\text{FLTA}}$(2)				I	ST	Fault interrupt input pin.
RD5/PWM4	28	3	3			
RD5				I/O	ST	Digital I/O.
PWM4(3)				O	TTL	PWM Output 4.
RD6/PWM6	29	4	4			
RD6				I/O	ST	Digital I/O.
PWM6				O	TTL	PWM Output 6.
RD7/PWM7	30	5	5			
RD7				I/O	ST	Digital I/O.
PWM7				O	TTL	PWM Output 7.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; I = Input; O = Output; P = Power

Note 1: RC3 is the alternate pin for T0CKI/T5CKI; RC4 is the alternate pin for SDI/SDA; RC5 is the alternate pin for SCK/SCL; RC7 is the alternate pin for SDO.

2: RD4 is the alternate pin for $\overline{\text{FLTA}}$.

3: RD5 is the alternate pin for PWM4.

6.5.4 SPECIAL FUNCTION REGISTERS

The Special Function Registers (SFRs) are registers used by the CPU and peripheral modules for controlling the desired operation of the device. These registers are implemented as static RAM. A list of these registers is given in Table 6-1 and Table 6-2.

The SFRs can be classified into two sets: those associated with the "core" function and those related to the peripheral functions. Those registers related to the "core" are described in this section, while those related to the operation of the peripheral features are described in the section of that peripheral feature.

The SFRs are typically distributed among the peripherals whose functions they control.

The unused SFR locations will be unimplemented and read as '0's.

TABLE 6-1: SPECIAL FUNCTION REGISTER MAP FOR PIC18F2331/2431/4331/4431 DEVICES

Address	Name	Address	Name	Address	Name	Address	Name	Address	Name
FFFh	TOSU	FDFh	INDF2(1)	FBFh	CCPR1H	F9Fh	IPR1	F7Fh	PTCON0
FFEh	TOSH	FDEh	POSTINC2(1)	FBEh	CCPR1L	F9Eh	PIR1	F7Eh	PTCON1
FFDh	TOSL	FDDh	POSTDEC2(1)	FBDh	CCP1CON	F9Dh	PIE1	F7Dh	PTMRL
FFCh	STKPTR	FDCh	PREINC2(1)	FBCh	CCPR2H	F9Ch	—(2)	F7Ch	PTMRH
FFBh	PCLATU	FDBh	PLUSW2(1)	FBBh	CCPR2L	F9Bh	OSCTUNE	F7Bh	PTPERL
FFAh	PCLATH	FDAh	FSR2H	FBAh	CCP2CON	F9Ah	ADCON3	F7Ah	PTPERH
FF9h	PCL	FD9h	FSR2L	FB9h	ANSEL1	F99h	ADCHS	F79h	PDC0L
FF8h	TBLPTRU	FD8h	STATUS	FB8h	ANSEL0	F98h	—(2)	F78h	PDC0H
FF7h	TBLPTRH	FD7h	TMR0H	FB7h	T5CON	F97h	—(2)	F77h	PDC1L
FF6h	TBLPTRL	FD6h	TMR0L	FB6h	QEICON	F96h	TRISE(3)	F76h	PDC1H
FF5h	TABLAT	FD5h	T0CON	FB5h	—(2)	F95h	TRISD(3)	F75h	PDC2L
FF4h	PRODH	FD4h	—(2)	FB4h	—(2)	F94h	TRISC	F74h	PDC2H
FF3h	PRODL	FD3h	OSCCON	FB3h	—(2)	F93h	TRISB	F73h	PDC3L(3)
FF2h	INTCON	FD2h	LVDCON	FB2h	—(2)	F92h	TRISA	F72h	PDC3H(3)
FF1h	INTCON2	FD1h	WDTCON	FB1h	—(2)	F91h	PR5H	F71h	SEVTCMPL
FF0h	INTCON3	FD0h	RCON	FB0h	SPBRGH	F90h	PR5L	F70h	SEVTCMPH
FEFh	INDF0(1)	FCFh	TMR1H	FAFh	SPBRG	F8Fh	—(2)	F6Fh	PWMCON0
FEEh	POSTINC0(1)	FCEh	TMR1L	FAEh	RCREG	F8Eh	—(2)	F6Eh	PWMCON1
FEDh	POSTDEC0(1)	FCDh	T1CON	FADh	TXREG	F8Dh	LATE(3)	F6Dh	DTCON
FECh	PREINC0(1)	FCCh	TMR2	FACh	TXSTA	F8Ch	LATD(3)	F6Ch	FLTCONFIG
FEBh	PLUSW0(1)	FCBh	PR2	FABh	RCSTA	F8Bh	LATC	F6Bh	OVDCOND
FEAh	FSR0H	FCAh	T2CON	FAAh	BAUDCON	F8Ah	LATB	F6Ah	OVDCONS
FE9h	FSR0L	FC9h	SSPBUF	FA9h	EEADR	F89h	LATA	F69h	CAP1BUFH
FE8h	WREG	FC8h	SSPADD	FA8h	EEDATA	F88h	TMR5H	F68h	CAP1BUFL
FE7h	INDF1(1)	FC7h	SSPSTAT	FA7h	EECON2	F87h	TMR5L	F67h	CAP2BUFH
FE6h	POSTINC1(1)	FC6h	SSPCON	FA6h	EECON1	F86h	—(2)	F66h	CAP2BUFL
FE5h	POSTDEC1(1)	FC5h	—(2)	FA5h	IPR3	F85h	—(2)	F65h	CAP3BUFH
FE4h	PREINC1(1)	FC4h	ADRESH	FA4h	PIR3	F84h	PORTE	F64h	CAP3BUFL
FE3h	PLUSW1(1)	FC3h	ADRESL	FA3h	PIE3	F83h	PORTD(3)	F63h	CAP1CON
FE2h	FSR1H	FC2h	ADCON0	FA2h	IPR2	F82h	PORTC	F62h	CAP2CON
FE1h	FSR1L	FC1h	ADCON1	FA1h	PIR2	F81h	PORTB	F61h	CAP3CON
FE0h	BSR	FC0h	ADCON2	FA0h	PIE2	F80h	PORTA	F60h	DFLTCON

Note 1: This is not a physical register.
2: Unimplemented registers are read as '0'.
3: This register is not available on 28-pin devices.

7.3 Reading the Data EEPROM Memory

To read a data memory location, the user must write the address to the EEADR register, clear the EEPGD control bit (EECON1<7>) and then set control bit, RD (EECON1<0>). The data is available for the very next instruction cycle; therefore, the EEDATA register can be read by the next instruction. EEDATA will hold this value until another read operation, or until it is written to by the user (during a write operation).The basic process is shown in Example 7-1.

7.4 Writing to the Data EEPROM Memory

To write an EEPROM data location, the address must first be written to the EEADR register and the data written to the EEDATA register. The sequence in Example 7-2 must be followed to initiate the write cycle.

The write will not begin if this sequence is not exactly followed (write 55h to EECON2, write 0AAh to EECON2, then set WR bit) for each byte. It is strongly recommended that interrupts be disabled during this code segment.

Additionally, the WREN bit in EECON1 must be set to enable writes. This mechanism prevents accidental writes to data EEPROM due to unexpected code execution (i.e., runaway programs). The WREN bit should be kept clear at all times, except when updating the EEPROM. The WREN bit is not cleared by hardware.

After a write sequence has been initiated, EECON1, EEADR and EEDATA cannot be modified. The WR bit will be inhibited from being set unless the WREN bit is set. The WREN bit must be set on a previous instruction. Both WR and WREN cannot be set with the same instruction.

At the completion of the write cycle, the WR bit is cleared in hardware and the EEPROM Interrupt Flag bit (EEIF) is set. The user may either enable this interrupt or poll this bit. EEIF must be cleared by software.

7.5 Write Verify

Depending on the application, good programming practice may dictate that the value written to the memory should be verified against the original value. This should be used in applications where excessive writes can stress bits near the specification limit.

7.6 Protection Against Spurious Write

There are conditions when the device may not want to write to the data EEPROM memory. To protect against spurious EEPROM writes, various mechanisms have been built-in. On power-up, the WREN bit is cleared. Also, the Power-up Timer (72 ms duration) prevents EEPROM write.

The write initiate sequence and the WREN bit together help prevent an accidental write during brown-out, power glitch, or software malfunction.

EXAMPLE 7-1: DATA EEPROM READ

```
        MOVLW   DATA_EE_ADDR      ;
        MOVWF   EEADR             ; Data Memory Address to read
        BCF     EECON1, EEPGD     ; Point to DATA memory
        BSF     EECON1, RD        ; EEPROM Read
        MOVF    EEDATA, W         ; W = EEDATA
```

EXAMPLE 7-2: DATA EEPROM WRITE

```
                MOVLW   DATA_EE_ADDR      ;
                MOVWF   EEADR             ; Data Memory Address to write
                MOVLW   DATA_EE_DATA      ;
                MOVWF   EEDATA            ; Data Memory Value to write
                BCF     EECON1, EEPGD     ; Point to DATA memory
                BCF     EECON1, CFGS      ; Access EEPROM
                BSF     EECON1, WREN      ; Enable writes
                BCF     INTCON, GIE       ; Disable Interrupts
                MOVLW   55h               ;
Required        MOVWF   EECON2            ; Write 55h
Sequence        MOVLW   0AAh              ;
                MOVWF   EECON2            ; Write 0AAh
                BSF     EECON1, WR        ; Set WR bit to begin write
                BTFSC   EECON1, WR        ; Wait for write to complete

                GOTO    $-2               ;
                BSF     INTCON, GIE       ; Enable interrupts
```

REGISTER 8-1: EECON1: DATA EEPROM CONTROL REGISTER 1

R/W-x	R/W-x	U-0	R/W-0	R/W-x	R/W-0	R/S-0	R/S-0
EEPGD	CFGS	—	FREE	WRERR(1)	WREN	WR	RD
bit 7							bit 0

Legend:	S = Settable bit (cannot be cleared in software)		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **EEPGD:** Flash Program or Data EEPROM Memory Select bit
- 1 = Access Flash program memory
- 0 = Access data EEPROM memory

bit 6 **CFGS:** Flash Program/Data EEPROM or Configuration Select bit
- 1 = Access Configuration registers
- 0 = Access Flash program or data EEPROM memory

bit 5 **Unimplemented:** Read as '0'

bit 4 **FREE:** Flash Row Erase Enable bit
- 1 = Erase the program memory row addressed by TBLPTR on the next WR command (cleared by completion of erase operation)
- 0 = Perform write only

bit 3 **WRERR:** Flash Program/Data EEPROM Error Flag bit(1)
- 1 = A write operation is prematurely terminated (any Reset during self-timed programming in normal operation, or an improper write attempt)
- 0 = The write operation completed

bit 2 **WREN:** Flash Program/Data EEPROM Write Enable bit
- 1 = Allows write cycles to Flash program/data EEPROM
- 0 = Inhibits write cycles to Flash program/data EEPROM

bit 1 **WR:** Write Control bit
- 1 = Initiates a data EEPROM erase/write cycle or a program memory erase cycle or write cycle (The operation is self-timed and the bit is cleared by hardware once write is complete. The WR bit can only be set (not cleared) in software.)
- 0 = Write cycle to the EEPROM is complete

bit 0 **RD:** Read Control bit
- 1 = Initiates an EEPROM read (Read takes one cycle. RD is cleared in hardware. The RD bit can only be set (not cleared) in software. RD bit cannot be set when EEPGD = 1 or CFGS = 1.)
- 0 = Does not initiate an EEPROM read

Note 1: When a WRERR occurs, the EEPGD and CFGS bits are not cleared. This allows tracing of the error condition.

11.0 I/O PORTS

Depending on the device selected and features enabled, there are up to five ports available. Some pins of the I/O ports are multiplexed with an alternate function from the peripheral features on the device. In general, when a peripheral is enabled, that pin may not be used as a general purpose I/O pin.

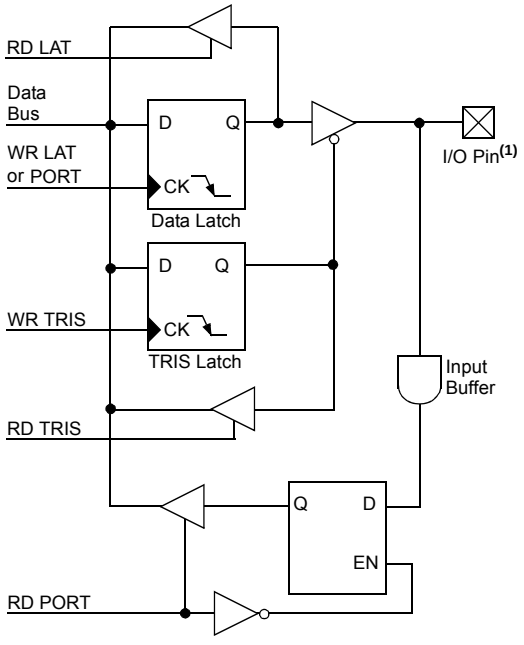
Each port has three registers for its operation. These registers are:

- TRIS register (Data Direction register)
- PORT register (reads the levels on the pins of the device)
- LAT register (Data Latch)

The Data Latch (LAT register) is useful for read-modify-write operations on the value that the I/O pins are driving.

A simplified model of a generic I/O port without the interfaces to other peripherals is shown in Figure 11-1.

FIGURE 11-1: GENERIC I/O PORT OPERATION



Note 1: I/O pins have diode protection to VDD and VSS.

11.1 PORTA, TRISA and LATA Registers

PORTA is an 8-bit wide, bidirectional port. The corresponding data direction register is TRISA. Setting a TRISA bit (= 1) will make the corresponding PORTA pin an input (i.e., put the corresponding output driver in a high-impedance mode). Clearing a TRISA bit (= 0) will make the corresponding PORTA pin an output (i.e., put the contents of the output latch on the selected pin).

Reading the PORTA register reads the status of the pins, whereas writing to it, will write to the port latch.

The Data Latch register (LATA) is also memory mapped. Read-modify-write operations on the LATA register read and write the latched output value for PORTA.

The RA<4:2> pins are multiplexed with three input capture pins and Quadrature Encoder Interface pins. Pins, RA6 and RA7, are multiplexed with the main oscillator pins. They are enabled as oscillator or I/O pins by the selection of the main oscillator in Configuration Register 1H (see **Section 23.1 "Configuration Bits"** for details). When they are not used as port pins, RA6 and RA7 and their associated TRIS and LAT bits are read as '0'.

The other PORTA pins are multiplexed with analog inputs, the analog VREF+ and VREF- inputs and the comparator voltage reference output. The operation of pins RA<3:0> and RA5 as A/D Converter inputs is selected by clearing/setting the control bits in the ANSEL0 and ANSEL1 registers.

Note 1: On a Power-on Reset, RA<5:0> are configured as analog inputs and read as '0'.

2: RA5 I/F is available only on 40-pin devices (PIC18F4331/4431).

The TRISA register controls the direction of the RA pins, even when they are being used as analog inputs. The user must ensure the bits in the TRISA register are maintained set when using them as analog inputs.

EXAMPLE 11-1: INITIALIZING PORTA

```
CLRF    PORTA   ; Initialize PORTA by
                ; clearing output
                ; data latches
CLRF    LATA    ; Alternate method
                ; to clear output
                ; data latches
MOVLW   0x3F    ; Configure A/D
MOVWF   ANSEL0  ; for digital inputs
MOVLW   0xCF    ; Value used to
                ; initialize data
                ; direction
MOVWF   TRISA   ; Set RA<3:0> as inputs
                ; RA<5:4> as outputs
```

TABLE 11-3: PORTB I/O SUMMARY

Pin	Function	TRIS Setting	I/O	I/O Type	Description
RB0/PWM0	RB0	0	O	DIG	LATB<0> data output; not affected by analog input.
		1	I	TTL	PORTB<0> data input; weak pull-up when $\overline{\text{RBPU}}$ bit is cleared. Disabled when analog input is enabled.
	PWM0	0	O	DIG	PWM Output 0.
RB1/PWM1	RB1	0	O	DIG	LATB<1> data output; not affected by analog input.
		1	I	TTL	PORTB<1> data input; weak pull-up when $\overline{\text{RBPU}}$ bit is cleared. Disabled when analog input is enabled.
	PWM1	0	O	DIG	PWM Output 1.
RB2/PWM2	RB2	0	O	DIG	LATB<2> data output; not affected by analog input.
		1	I	TTL	PORTB<2> data input; weak pull-up when $\overline{\text{RBPU}}$ bit is cleared. Disabled when analog input is enabled.
	PWM2	0	O	DIG	PWM Output 2.
RB3/PWM3	RB3	0	O	DIG	LATB<3> data output; not affected by analog input.
		1	I	TTL	PORTB<3> data input; weak pull-up when $\overline{\text{RBPU}}$ bit is cleared. Disabled when analog input is enabled.
	PWM3	0	O	DIG	PWM Output 3.
RB4/KBI0/PWM5	RB4	0	O	DIG	LATB<4> data output; not affected by analog input.
		1	I	TTL	PORTB<4> data input; weak pull-up when $\overline{\text{RBPU}}$ bit is cleared. Disabled when analog input is enabled.
	KBI0	1	I	TTL	Interrupt-on-change pin.
	PWM5	0	O	DIG	PWM Output 5.
RB5/KBI1/ PWM4/PGM	RB5	0	O	DIG	LATB<5> data output.
		1	I	TTL	PORTB<5> data input; weak pull-up when $\overline{\text{RBPU}}$ bit is cleared.
	KBI1	1	I	TTL	Interrupt-on-change pin.
	PWM4(3)	0	O	DIG	PWM Output 4; takes priority over port data.
	PGM(2)	x	I	ST	Single-Supply Programming mode entry (ICSP™). Enabled by LVP Configuration bit; all other pin functions are disabled.
RB6/KBI2/PGC	RB6	0	O	DIG	LATB<6> data output.
		1	I	TTL	PORTB<6> data input; weak pull-up when $\overline{\text{RBPU}}$ bit is cleared.
	KBI2	1	I	TTL	Interrupt-on-change pin.
	PGC	x	I	ST	Serial execution (ICSP™) clock input for ICSP and ICD operation.(1)
RB7/KBI3/PGD	RB7	0	O	DIG	LATB<7> data output.
		1	I	TTL	PORTB<7> data input; weak pull-up when $\overline{\text{RBPU}}$ bit is cleared.
	KBI3	1	I	TTL	Interrupt-on-change pin.
	PGD	x	O	DIG	Serial execution data output for ICSP and ICD operation.(1)
		x	I	ST	Serial execution data input for ICSP and ICD operation.(1)

Legend: DIG = Digital level output; TTL = TTL input buffer; ST = Schmitt Trigger input buffer; ANA = Analog level input/output; x = Don't care (TRIS bit does not affect port direction or is overridden for this option).

Note 1: All other pin functions are disabled when ICSP or ICD is enabled.

2: Single-Supply Programming must be enabled.

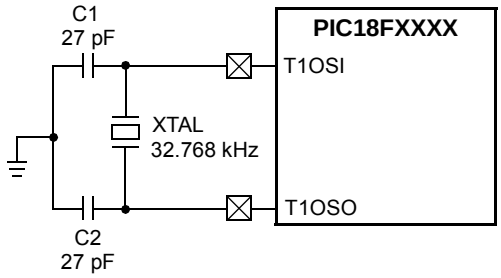
3: RD5 is the alternate pin for PWM4.

13.2 Timer1 Oscillator

A crystal oscillator circuit is built in-between pins, T1OSI (input) and T1OSO (amplifier output). It is enabled by setting control bit, T1OSCEN (T1CON<3>). The oscillator is a low-power oscillator rated for 32 kHz crystals. It will continue to run during all power-managed modes. The circuit for a typical LP oscillator is shown in Figure 13-3. Table 13-1 shows the capacitor selection for the Timer1 oscillator.

The user must provide a software time delay to ensure proper start-up of the Timer1 oscillator.

FIGURE 13-3: EXTERNAL COMPONENTS FOR THE TIMER1 LP OSCILLATOR



Note: See the notes with Table 13-1 for additional information about capacitor selection.

TABLE 13-1: CAPACITOR SELECTION FOR THE TIMER OSCILLATOR

Osc Type	Freq	C1	C2
LP	32 kHz	27 pF(1)	27 pF(1)

Note 1: Microchip suggests this value as a starting point in validating the oscillator circuit.

2: Higher capacitance increases the stability of the oscillator, but also increases the start-up time.

3: Since each resonator/crystal has its own characteristics, the user should consult the resonator/crystal manufacturer for appropriate values of external components.

4: Capacitor values are for design guidance only.

13.3 Timer1 Oscillator Layout Considerations

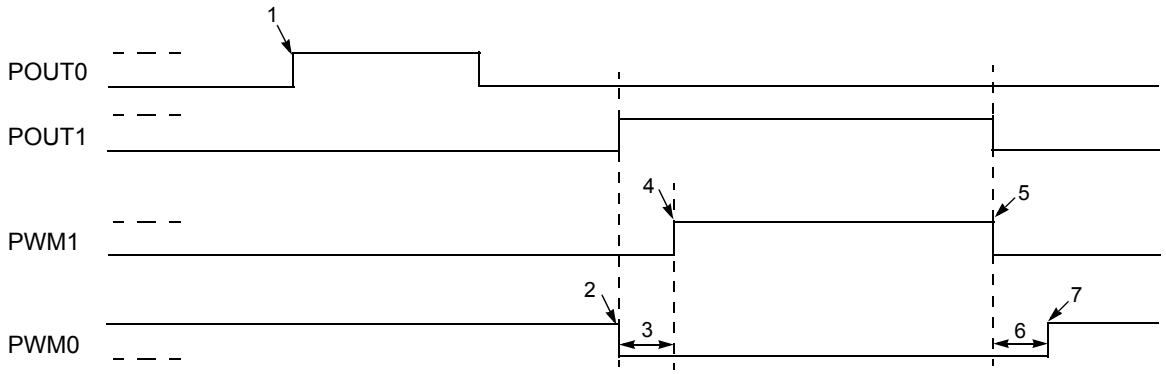
The Timer1 oscillator for PIC18F2331/2431/4331/4431 devices incorporates an additional low-power feature. When this option is selected, it allows the oscillator to automatically reduce its power consumption when the microcontroller is in Sleep mode. During normal device operation, the oscillator draws full current. As high noise environments may cause excessive oscillator instability in Sleep mode, this option is best suited for low noise applications, where power conservation is an important design consideration.

The low-power option is enabled by clearing the T1OSCMX bit (CONFIG3L<5>). By default, the option is disabled, which results in a more or less constant current draw for the Timer1 oscillator.

Due to the low-power nature of the oscillator, it may also be sensitive to rapidly changing signals in close proximity.

The oscillator circuit, shown in Figure 13-3, should be located as close as possible to the microcontroller. There should be no circuits passing within the oscillator circuit boundaries other than VSS or VDD. Refer to **Section 2.0 "Guidelines for Getting Started with PIC18F Microcontrollers"** for additional information

FIGURE 18-20: PWM OVERRIDE BITS IN COMPLEMENTARY MODE



Assume: POVD0 = 0; POVD1 = 0; PMOD0 = 0

1. Even override bits have no effect in Complementary mode.
2. Odd override bit is activated, which causes the even PWM to deactivate.
3. Dead-time insertion.
4. Odd PWM activated after the dead time.
5. Odd override bit is deactivated, which causes the odd PWM to deactivate.
6. Dead-time insertion.
7. Even PWM is activated after the dead time.

REGISTER 19-1: SSPSTAT: SYNCHRONOUS SERIAL PORT STATUS REGISTER

R/W-0	R/W-0	R-0	R-0	R-0	R-0	R-0	R-0
SMP	CKE	D/$\overline{A}$	P	S	R/$\overline{W}$	UA	BF
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **SMP:** Sample bit

SPI Master mode:
1 = Input data sampled at end of data output time
0 = Input data sampled at middle of data output time

SPI Slave mode:
SMP must be cleared when SPI is used in Slave mode.

bit 6 **CKE**: SPI Clock Edge Select bit (Figure 19-2, Figure 19-3 and Figure 19-4)

SPI mode, CKP = 0:
1 = Data transmitted on rising edge of SCK
0 = Data transmitted on falling edge of SCK

SPI mode, CKP = 1:
1 = Data transmitted on falling edge of SCK
0 = Data transmitted on rising edge of SCK

I^2C™ mode:
This bit must be maintained clear.

bit 5 **D/$\overline{A}$**: Data/$\overline{Address}$ bit (I^2C mode only)
1 = Indicates that the last byte received or transmitted was data
0 = Indicates that the last byte received or transmitted was address

bit 4 **P**: Stop bit (I^2C mode only)
This bit is cleared when the SSP module is disabled or when the Start bit is detected last; SSPEN is cleared.
1 = Indicates that a Stop bit has been detected last (this bit is '0' on Reset)
0 = Stop bit was not detected last

bit 3 **S**: Start bit (I^2C mode only)
This bit is cleared when the SSP module is disabled or when the Stop bit is detected last; SSPEN is cleared.
1 = Indicates that a Start bit has been detected last (this bit is '0' on Reset)
0 = Start bit was not detected last

bit 2 **R/$\overline{W}$**: Read/$\overline{Write}$ Information bit (I^2C mode only)
This bit holds the R/$\overline{W}$ bit information following the last address match. This bit is only valid from the address match to the next Start bit, Stop bit or $\overline{ACK}$ bit.
1 = Read
0 = Write

bit 1 **UA**: Update Address bit (10-Bit I^2C mode only)
1 = Indicates that the user needs to update the address in the SSPADD register
0 = Address does not need to be updated

bit 0 **BF**: Buffer Full Status bit

Receive (SPI and I^2C modes):
1 = Receive complete, SSPBUF is full
0 = Receive not complete, SSPBUF is empty

Transmit (I^2C mode only):
1 = Transmit in progress, SSPBUF is full
0 = Transmit complete, SSPBUF is empty

REGISTER 20-1: TXSTA: TRANSMIT STATUS AND CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-1	R/W-0
CSRC	TX9	TXEN(1)	SYNC	SENDB	BRGH	TRMT	TX9D
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **CSRC:** Clock Source Select bit
Asynchronous mode:
Don't care.
Synchronous mode:
1 = Master mode (clock generated internally from BRG)
0 = Slave mode (clock from external source)

bit 6 **TX9:** 9-Bit Transmit Enable bit
1 = Selects 9-bit transmission
0 = Selects 8-bit transmission

bit 5 **TXEN:** Transmit Enable bit(1)
1 = Transmit enabled
0 = Transmit disabled

bit 4 **SYNC:** EUSART Mode Select bit
1 = Synchronous mode
0 = Asynchronous mode

bit 3 **SENDB:** Send Break Character bit
Asynchronous mode:
1 = Send Sync Break on next transmission (cleared by hardware upon completion)
0 = Sync Break transmission completed
Synchronous mode:
Don't care.

bit 2 **BRGH:** High Baud Rate Select bit
Asynchronous mode:
1 = High speed
0 = Low speed
Synchronous mode:
Unused in this mode.

bit 1 **TRMT:** Transmit Shift Register Status bit
1 = TSR is empty
0 = TSR is full

bit 0 **TX9D:** 9th Bit of Transmit Data
Can be address/data bit or a parity bit.

Note 1: SREN/CREN overrides TXEN in Sync mode.

20.5 EUSART Synchronous Slave Mode

Synchronous Slave mode is entered by clearing bit, CSRC (TXSTA<7>). This mode differs from the Synchronous Master mode in that the shift clock is supplied externally at the RC6/TX/CK/SS pin (instead of being supplied internally in Master mode). This allows the device to transfer or receive data while in any low-power mode.

20.5.1 EUSART SYNCHRONOUS SLAVE TRANSMIT

The operation of the Synchronous Master and Slave modes are identical, except in the case of Sleep mode.

If two words are written to the TXREG and then the SLEEP instruction is executed, the following will occur:

a) The first word will immediately transfer to the TSR register and transmit.
b) The second word will remain in TXREG register.
c) Flag bit, TXIF, will not be set.
d) When the first word has been shifted out of TSR, the TXREG register will transfer the second word to the TSR and flag bit, TXIF, will now be set.
e) If enable bit, TXIE, is set, the interrupt will wake the chip from Sleep. If the global interrupt is enabled, the program will branch to the interrupt vector.

To set up a Synchronous Slave Transmission:

1. Enable the synchronous slave serial port by setting bits, SYNC and SPEN, and clearing bit, CSRC.
2. Clear bits, CREN and SREN.
3. If interrupts are desired, set enable bit, TXIE.
4. If 9-bit transmission is desired, set bit, TX9.
5. Enable the transmission by setting enable bit, TXEN.
6. If 9-bit transmission is selected, the ninth bit should be loaded in bit, TX9D.
7. Start transmission by loading data to the TXREG register.
8. If using interrupts, ensure that the GIE and PEIE bits in the INTCON register (INTCON<7:6>) are set.

TABLE 20-9: REGISTERS ASSOCIATED WITH SYNCHRONOUS SLAVE TRANSMISSION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on Page:
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	54
PIR1	—	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	57
PIE1	—	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	57
IPR1	—	ADIP	RCIP	TXIP	SSPIP	CCP1IP	TMR2IP	TMR1IP	57
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	56
TXREG	EUSART Transmit Register								56
TXSTA	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	56
BAUDCON	—	RCIDL	—	SCKP	BRG16	—	WUE	ABDEN	56
SPBRGH	EUSART Baud Rate Generator Register High Byte								56
SPBRG	EUSART Baud Rate Generator Register Low Byte								56

Legend: — = unimplemented, read as '0'. Shaded cells are not used for synchronous slave transmission.

REGISTER 21-4: ADCON3: A/D CONTROL REGISTER 3

R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADRS1	ADRS0	—	SSRC4(1)	SSRC3(1)	SSRC2(1)	SSRC1(1)	SSRC0(1)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **ADRS<1:0>**: A/D Result Buffer Depth Interrupt Select Control for Continuous Loop Mode bits
The ADRS bits are ignored in Single-Shot mode.
00 = Interrupt is generated when each word is written to the buffer
01 = Interrupt is generated when the 2nd and 4th words are written to the buffer
10 = Interrupt is generated when the 4th word is written to the buffer
11 = Unimplemented

bit 5 **Unimplemented:** Read as '0'

bit 4-0 **SSRC<4:0>:** A/D Trigger Source Select bits(1)
00000 = All triggers disabled
xxxx1 = External interrupt RC3/INT0 starts A/D sequence
xxx1x = Timer5 starts A/D sequence
xx1xx = Input Capture 1 (IC1) starts A/D sequence
x1xxx = CCP2 compare match starts A/D sequence
1xxxx = Power Control PWM module rising edge starts A/D sequence

Note 1: The SSRC<4:0> bits can be set such that any of the triggers will start a conversion (e.g., SSRC<4:0> = 00101 will trigger the A/D conversion sequence when RC3/INT0 or Input Capture 1 event occurs).

21.1.3 CONVERSION SEQUENCING

The ACMOD<1:0> bits control the sequencing of the A/D conversions. When ACSCH = 0, the A/D is configured to sample and convert a single channel. The ACMOD bits select which group to perform the conversions and the GxSEL<1:0> bits select which channel in the group is to be converted. If Single-Shot mode is enabled, the A/D interrupt flag will be set after the channel is converted. If Continuous Loop mode is enabled, the A/D interrupt flag will be set according to the ADRS<1:0> bits.

When ACSCH = 1, multiple channel sequencing is enabled and two submodes can be selected. The first mode is Sequential mode with two settings. The first setting is called SEQM1, and first samples and converts the selected Group A channel, and then samples and converts the selected Group B channel. The second mode is called SEQM2, and it samples and converts a Group A channel, Group B channel, Group C channel and finally, a Group D channel.

The second multiple channel sequencing submode is Simultaneous Sampling mode. In this mode, there are also two settings. The first setting is called STNM1, and uses the two sample and hold circuits on the A/D module. The selected Group A and B channels are simultaneously sampled and then the Group A channel is converted followed by the conversion of the Group B channel. The second setting is called STNM2, and starts the same as STNM1, but follows it with a simultaneous sample of Group C and D channels. The A/D module will then convert the Group C channel followed by the Group D channel.

21.1.4 TRIGGERING A/D CONVERSIONS

The PIC18F2331/2431/4331/4431 devices are capable of triggering conversions from many different sources. The same method used by all other microcontrollers of setting the GO/$\overline{\text{DONE}}$ bit still works. The other trigger sources are:

- RC3/INT0 Pin
- Timer5 Overflow
- Input Capture 1 (IC1)
- CCP2 Compare Match
- Power Control PWM Rising Edge

These triggers are enabled using the SSRC<4:0> bits (ADCON3<4:0>). Any combination of the five sources can trigger a conversion by simply setting the corresponding bit in ADCON3. When the trigger occurs, the GO/$\overline{\text{DONE}}$ bit is automatically set by the hardware and then cleared once the conversion completes.

21.1.5 A/D MODULE INITIALIZATION STEPS

The following steps should be followed to initialize the A/D module:

1. Configure the A/D module:
   a) Configure the analog pins, voltage reference and digital I/O.
   b) Select the A/D input channels.
   c) Select the A/D Auto-Conversion mode (Single-Shot or Continuous Loop).
   d) Select the A/D conversion clock.
   e) Select the A/D conversion trigger.
2. Configure the A/D interrupt (if required):
   a) Set the GIE bit.
   b) Set the PEIE bit.
   c) Set the ADIE bit.
   d) Clear the ADIF bit.
   e) Select the A/D trigger setting.
   f) Select the A/D interrupt priority.
3. Turn on ADC:
   a) Set the ADON bit in the ADCON0 register.
   b) Wait the required power-up setup time, about 5-10 μs.
4. Start the sample/conversion sequence:
   a) Sample for a minimum of 2 T_{AD} and start the conversion by setting the GO/$\overline{\text{DONE}}$ bit. The GO/$\overline{\text{DONE}}$ bit is set by the user in software or by the module if initiated by a trigger.
   b) If T_{ACQ} is assigned a value (multiple of T_{AD}), then setting the GO/$\overline{\text{DONE}}$ bit starts a sample period of the T_{ACQ} value, then starts a conversion.
5. Wait for A/D conversion/conversions to complete using one of the following options:
   a) Poll for the GO/$\overline{\text{DONE}}$ bit to be cleared if in Single-Shot mode.
   b) Wait for the A/D Interrupt Flag (ADIF) to be set.
   c) Poll for the BFEMT bit to be cleared to signify that at least the first conversion has completed.
6. Read the A/D results, clear the ADIF flag, reconfigure the trigger.

CLRF **Clear f**

Syntax: [*label*] CLRF f [,a]

Operands: $0 \le f \le 255$
$a \in [0,1]$

Operation: 000h → f,
1 → Z

Status Affected: Z

Encoding:

0110	101a	ffff	ffff

Description: Clears the contents of the specified register. If 'a' is '0', the Access Bank will be selected, overriding the BSR value. If 'a' = 1, then the bank will be selected as per the BSR value.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	Write register 'f'

Example: CLRF FLAG_REG

Before Instruction
FLAG_REG = 0x5A

After Instruction
FLAG_REG = 0x00

CLRWDT **Clear Watchdog Timer**

Syntax: [*label*] CLRWDT

Operands: None

Operation: 000h → WDT,
000h → WDT postscaler,
1 → $\overline{TO}$,
1 → $\overline{PD}$

Status Affected: $\overline{TO}$, $\overline{PD}$

Encoding:

0000	0000	0000	0100

Description: CLRWDT instruction resets the Watchdog Timer. It also resets the postscaler of the WDT. Status bits $\overline{TO}$ and $\overline{PD}$ are set.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	No operation	Process Data	No operation

Example: CLRWDT

Before Instruction
WDT Counter = ?

After Instruction
WDT Counter = 0x00
WDT Postscaler = 0
$\overline{TO}$ = 1
$\overline{PD}$ = 1

IORLW **Inclusive OR Literal with W**

Syntax: [*label*] IORLW k

Operands: $0 \le k \le 255$

Operation: (W) .OR. k → W

Status Affected: N, Z

Encoding:

0000	1001	kkkk	kkkk

Description: The contents of W are ORed with the 8-bit literal, 'k'. The result is placed in W.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read literal 'k'	Process Data	Write to W

Example: IORLW 0x35

Before Instruction
W = 0x9A

After Instruction
W = 0xBF

IORWF **Inclusive OR W with f**

Syntax: [*label*] IORWF f [,d [,a]]

Operands: $0 \le f \le 255$
$d \in [0,1]$
$a \in [0,1]$

Operation: (W) .OR. (f) → dest

Status Affected: N, Z

Encoding:

0001	00da	ffff	ffff

Description: Inclusive OR W with register, 'f'. If 'd' is '0', the result is placed in W. If 'd' is '1', the result is placed back in register, 'f'. If 'a' is '0', the Access Bank will be selected, overriding the BSR value. If 'a' = 1, then the bank will be selected as per the BSR value.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	Write to destination

Example: IORWF RESULT, W

Before Instruction
RESULT = 0x13
W = 0x91

After Instruction
RESULT = 0x13
W = 0x93

TABLE 26-20: A/D CONVERTER CHARACTERISTICS

PIC18LF2331/2431/4331/4431 (Industrial)			**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial				
PIC18F2331/2431/4331/4431 (Industrial)			**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Device Supply							
	AVDD	Analog VDD Supply	VDD – 0.3	—	VDD + 0.3	V	
	AVSS	Analog VSS Supply	VSS – 0.3	—	VSS + 0.3	V	
	IAD	Module Current (during conversion)	— —	500 250	— —	μA μA	VDD = 5V VDD = 2.5V
	IADO	Module Current Off	—	—	1.0	μA	
AC Timing Parameters							
A10	FTHR	Throughput Rate	— —	— —	200 75	ksps ksps	VDD = 5V, single channel VDD < 3V, single channel
A11	TAD	A/D Clock Period	385 1000	— —	20,000 20,000	ns ns	VDD = 5V VDD = 3V
A12	TRC	A/D Internal RC Oscillator Period	— — —	500 750 10000	1500 2250 20000	ns ns ns	PIC18F parts PIC18LF parts AVDD < 3.0V
A13	TCNV	Conversion Time(1)	12	12	12	TAD	
A14	TACQ	Acquisition Time(2)	2(2)	—	—	TAD	
A16	TTC	Conversion Start from External	1/4 TCY	—	—		
Reference Inputs							
A20	VREF	Reference Voltage for 10-Bit Resolution (VREF+ – VREF-)	1.5 1.8	— —	AVDD – AVSS AVDD – AVSS	V V	VDD ≥ 3V VDD < 3V
A21	VREFH	Reference Voltage High (AVDD or VREF+)	1.5V	—	AVDD	V	VDD ≥ 3V
A22	VREFL	Reference Voltage Low (AVSS or VREF-)	AVSS	—	VREFH – 1.5V	V	
A23	IREF	Reference Current	— —	150 μA 75 μA	— —		VDD = 5V VDD = 2.5V
Analog Input Characteristics							
A26	VAIN	Input Voltage(3)	AVSS – 0.3	—	AVDD + 0.3	V	
A30	ZAIN	Recommended Impedance of Analog Voltage Source	—	—	2.5	kΩ	
A31	ZCHIN	Analog Channel Input Impedance	—	—	10.0	kΩ	VDD = 3.0V
DC Performance							
A41	NR	Resolution	10 bits			—	
A42	EIL	Integral Nonlinearity	—	—	<±1	LSb	VDD ≥ 3.0V VREFH ≥ 3.0V
A43	EIL	Differential Nonlinearity	—	—	<±1	LSb	VDD ≥ 3.0V VREFH ≥ 3.0V
A45	EOFF	Offset Error	—	±0.5	<±1.5	LSb	VDD ≥ 3.0V VREFH ≥ 3.0V
A46	EGA	Gain Error	—	±0.5	<±1.5	LSb	VDD ≥ 3.0V VREFH ≥ 3.0V
A47	—	Monotonicity(4)	guaranteed			—	VDD ≥ 3.0V VREFH ≥ 3.0V

Note 1: Conversion time does not include acquisition time. See **Section 21.0 "10-Bit High-Speed Analog-to-Digital Converter (A/D) Module"** for a full discussion of acquisition time requirements.

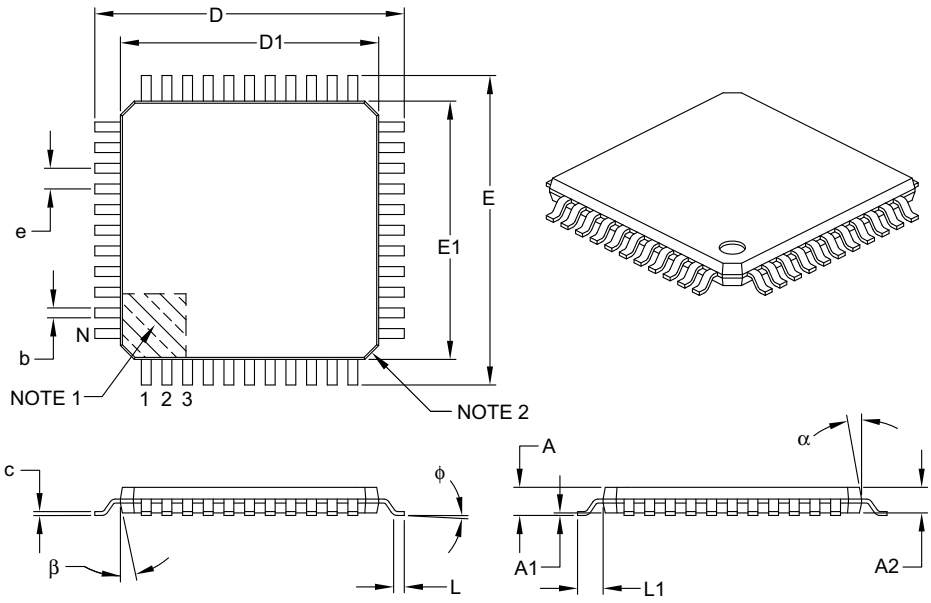
2: In Sequential modes, TACQ should be 12 TAD or greater.

3: For VDD < 2.7V and temperature below 0°C, VAIN should be limited to range < VDD/2.

4: The A/D conversion result never decreases with an increase in the input voltage and has no missing codes.

44-Lead Plastic Thin Quad Flatpack (PT) – 10x10x1 mm Body, 2.00 mm [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N		44	
Lead Pitch	e		0.80 BSC	
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.95	1.00	1.05
Standoff	A1	0.05	–	0.15
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	φ	0°	3.5°	7°
Overall Width	E		12.00 BSC	
Overall Length	D		12.00 BSC	
Molded Package Width	E1		10.00 BSC	
Molded Package Length	D1		10.00 BSC	
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.30	0.37	0.45
Mold Draft Angle Top	α	11°	12°	13°
Mold Draft Angle Bottom	β	11°	12°	13°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Chamfers at corners are optional; size may vary.
3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

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