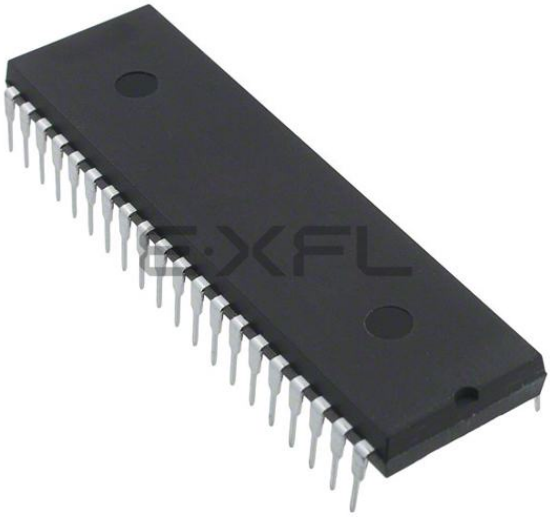

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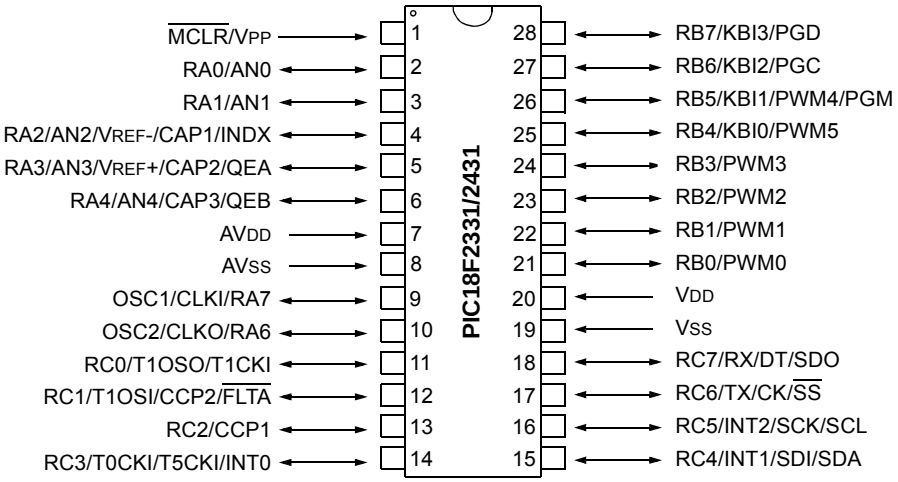
Applications of "Embedded - Microcontrollers"

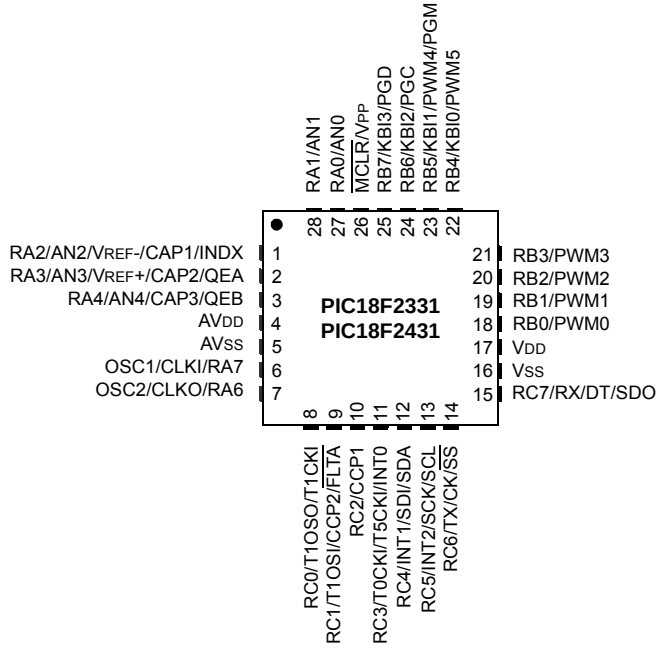
Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	40MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVD, Power Control PWM, QEI, POR, PWM, WDT
Number of I/O	36
Program Memory Size	16KB (8K x 16)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	4.2V ~ 5.5V
Data Converters	A/D 9x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.600", 15.24mm)
Supplier Device Package	40-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18f4431-e-p

Pin Diagrams

28-Pin SPDIP, SOIC



28-Pin QFN(1)



Note 1: For the QFN package, it is recommended that the bottom pad be connected to VSS.

TABLE 1-3: PIC18F4331/4431 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	PDIP	TQFP	QFN			
						PORTA is a bidirectional I/O port.
RA0/AN0	2	19	19			
RA0				I/O	TTL	Digital I/O.
AN0				I	Analog	Analog Input 0.
RA1/AN1	3	20	20			
RA1				I/O	TTL	Digital I/O.
AN1				I	Analog	Analog Input 1.
RA2/AN2/VREF-/CAP1/INDX	4	21	21			
RA2				I/O	TTL	Digital I/O.
AN2				I	Analog	Analog Input 2.
VREF-				I	Analog	A/D reference voltage (low) input.
CAP1				I	ST	Input Capture Pin 1.
INDX				I	ST	Quadrature Encoder Interface index input pin.
RA3/AN3/VREF+/CAP2/QEA	5	22	22			
RA3				I/O	TTL	Digital I/O.
AN3				I	Analog	Analog Input 3.
VREF+				I	Analog	A/D reference voltage (high) input.
CAP2				I	ST	Input Capture Pin 2.
QEA				I	ST	Quadrature Encoder Interface Channel A input pin.
RA4/AN4/CAP3/QEB	6	23	23			
RA4				I/O	TTL	Digital I/O.
AN4				I	Analog	Analog Input 4.
CAP3				I	ST	Input Capture Pin 3.
QEB				I	ST	Quadrature Encoder Interface Channel B input pin.
RA5/AN5/LVDIN	7	24	24			
RA5				I/O	TTL	Digital I/O.
AN5				I	Analog	Analog Input 5.
LVDIN				I	Analog	Low-Voltage Detect input.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; I = Input; O = Output; P = Power

Note 1: RC3 is the alternate pin for T0CKI/T5CKI; RC4 is the alternate pin for SDI/SDA; RC5 is the alternate pin for SCK/SCL; RC7 is the alternate pin for SDO.

2: RD4 is the alternate pin for $\overline{\text{FLTA}}$.

3: RD5 is the alternate pin for PWM4.

TABLE 1-3: PIC18F4331/4431 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	PDIP	TQFP	QFN			
						PORTC is a bidirectional I/O port.
RC0/T1OSO/T1CKI	15	32	34			
RC0				I/O	ST	Digital I/O.
T1OSO				O	—	Timer1 oscillator output.
T1CKI				I	ST	Timer1 external clock input.
RC1/T1OSI/CCP2/$\overline{\text{FLTA}}$	16	35	35			
RC1				I/O	ST	Digital I/O.
T1OSI				I	CMOS	Timer1 oscillator input.
CCP2				I/O	ST	Capture 2 input, Compare 2 output, PWM2 output.
$\overline{\text{FLTA}}$				I	ST	Fault interrupt input pin.
RC2/CCP1/$\overline{\text{FLTB}}$	17	36	36			
RC2				I/O	ST	Digital I/O.
CCP1				I/O	ST	Capture 1 input/Compare 1 output/PWM1 output.
$\overline{\text{FLTB}}$				I	ST	Fault interrupt input pin.
RC3/T0CKI/T5CKI/INT0	18	37	37			
RC3				I/O	ST	Digital I/O.
T0CKI(1)				I	ST	Timer0 alternate clock input.
T5CKI(1)				I	ST	Timer5 alternate clock input.
INT0				I	ST	External Interrupt 0.
RC4/INT1/SDI/SDA	23	42	42			
RC4				I/O	ST	Digital I/O.
INT1				I	ST	External Interrupt 1.
SDI(1)				I	ST	SPI data in.
SDA(1)				I/O	I^2C	I^2C™ data I/O.
RC5/INT2/SCK/SCL	24	43	43			
RC5				I/O	ST	Digital I/O.
INT2				I	ST	External Interrupt 2.
SCK(1)				I/O	ST	Synchronous serial clock input/output for SPI mode.
SCL(1)				I/O	I^2C	Synchronous serial clock input/output for I^2C mode.
RC6/TX/CK/$\overline{\text{SS}}$	25	44	44			
RC6				I/O	ST	Digital I/O.
TX				O	—	EUSART asynchronous transmit.
CK				I/O	ST	EUSART synchronous clock (see related RX/DT).
$\overline{\text{SS}}$				I	ST	SPI slave select input.
RC7/RX/DT/SDO	26	1	1			
RC7				I/O	ST	Digital I/O.
RX				I	ST	EUSART asynchronous receive.
DT				I/O	ST	EUSART synchronous data (see related TX/CK).
SDO(1)				O	—	SPI data out.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; I = Input; O = Output; P = Power

Note 1: RC3 is the alternate pin for T0CKI/T5CKI; RC4 is the alternate pin for SDI/SDA; RC5 is the alternate pin for SCK/SCL; RC7 is the alternate pin for SDO.

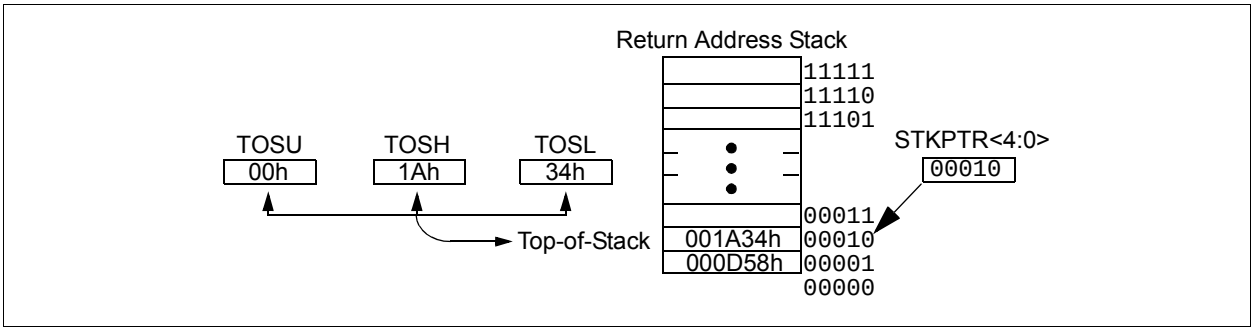
2: RD4 is the alternate pin for $\overline{\text{FLTA}}$.

3: RD5 is the alternate pin for PWM4.

When the stack has been popped enough times to unload the stack, the next pop will return a value of zero to the PC and set the STKUNF bit, while the Stack Pointer remains at zero. The STKUNF bit will remain set until cleared by software or a POR occurs.

Note:	Returning a value of zero to the PC on an underflow has the effect of vectoring the program to the Reset vector, where the stack conditions can be verified and appropriate actions can be taken. This is not the same as a Reset as the contents of the SFRs are not affected.

FIGURE 6-3: RETURN ADDRESS STACK AND ASSOCIATED REGISTERS



REGISTER 6-1: STKPTR: STACK POINTER REGISTER

R/C-0	R/C-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STKFUL(1)	STKUNF(1)	—	SP4	SP3	SP2	SP1	SP0
bit 7							bit 0

Legend:	C = Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **STKFUL:** Stack Full Flag bit(1)
1 = Stack became full or overflowed
0 = Stack has not become full or overflowed

bit 6 **STKUNF:** Stack Underflow Flag bit(1)
1 = Stack underflow occurred
0 = Stack underflow did not occur

bit 5 **Unimplemented:** Read as ‘0’

bit 4-0 **SP<4:0>:** Stack Pointer Location bits

Note 1: Bit 7 and bit 6 are cleared by user software or by a POR.

17.2 Quadrature Encoder Interface

The Quadrature Encoder Interface (QEI) decodes speed and motion sensor information. It can be used in any application that uses a quadrature encoder for feedback. The interface implements these features:

- Three QEI inputs: two phase signals (QEA and QEB) and one index signal (INDX)
- Direction of movement detection with a direction change interrupt (IC3DRIF)
- 16-bit up/down position counter
- Standard and High-Precision Position Tracking modes
- Two Position Update modes (x2 and x4)
- Velocity measurement with a programmable postscaler for high-speed velocity measurement
- Position counter interrupt (IC2QEIF in the PIR3 register)
- Velocity control interrupt (IC1IF in the PIR3 register)

The QEI submodule has three main components: the QEI control logic block, the position counter and velocity postscaler.

The QEI control logic detects the leading edge on the QEA or QEB phase input pins and generates the count pulse, which is sent to the position counter logic. It also samples the index input signal (INDX) and generates the direction of the rotation signal (up/down) and the velocity event signals.

The position counter acts as an integrator for tracking distance traveled. The QEA and QEB input edges serve as the stimulus to create the input clock which advances the Position Counter register (POSCNT). The register is incremented on either the QEA input edge, or the QEA and QEB input edges, depending on the operating mode. It is reset either by a rollover on match to the Period register, MAXCNT, or on the external index pulse input signal (INDX). An interrupt is generated on a Reset of POSCNT if the position counter interrupt is enabled.

The velocity postscaler down samples the velocity pulses used to increment the velocity counter by a specified ratio. It essentially divides down the number of velocity pulses to one output per so many inputs, preserving the pulse width in the process.

A simplified block-diagram of the QEI module is shown in Figure 17-8.

FIGURE 17-8: QEI BLOCK DIAGRAM

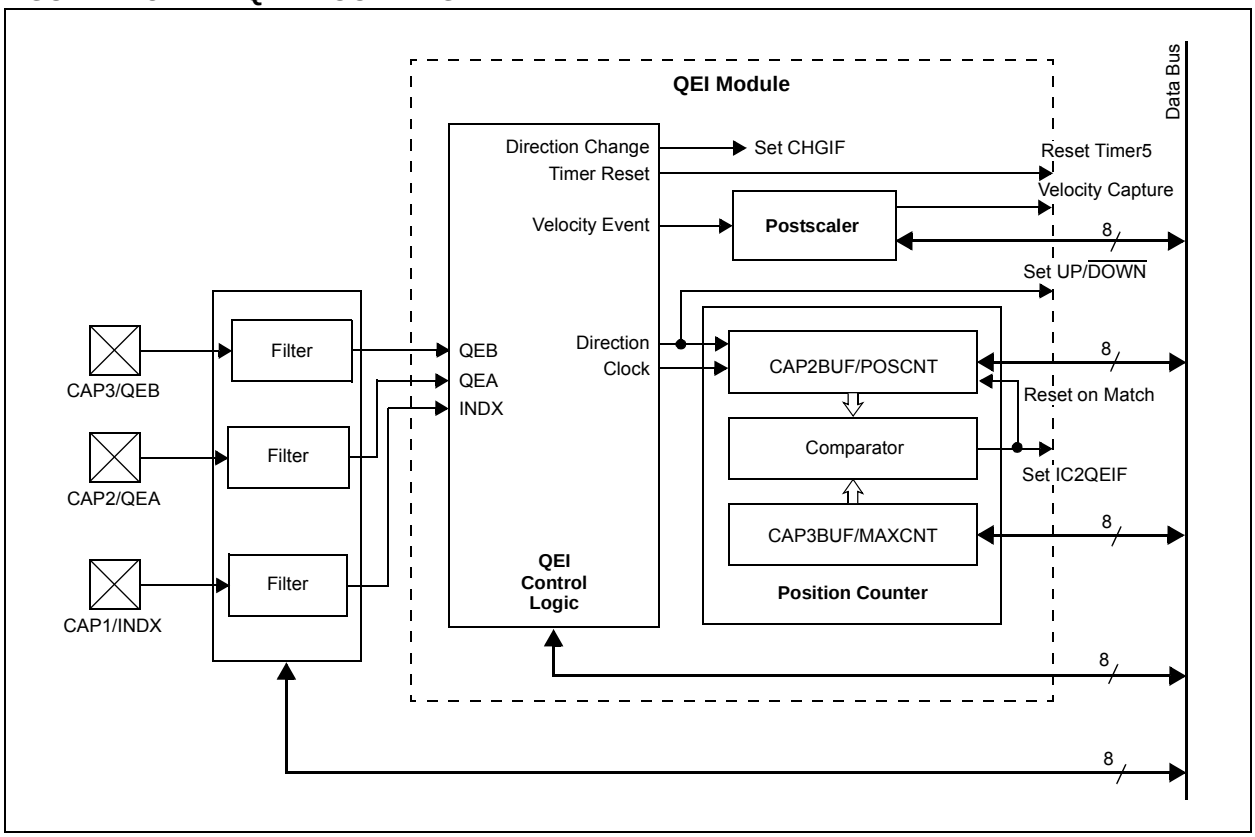
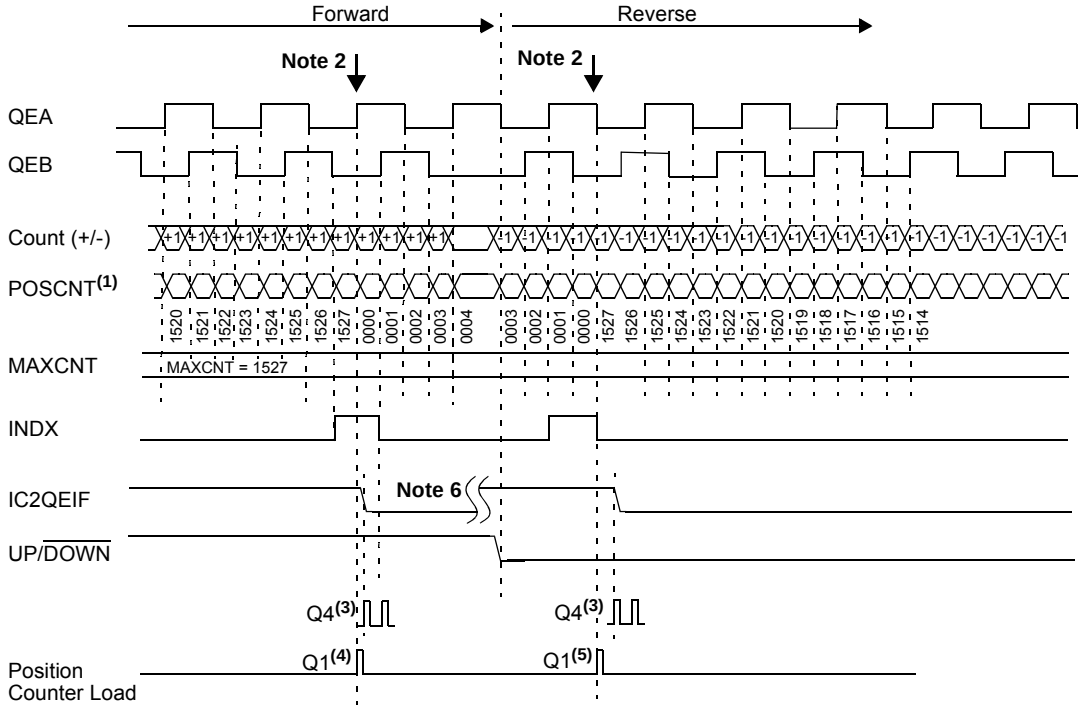


FIGURE 17-11: QEI MODULE RESET TIMING WITH THE INDEX INPUT



Note 1: POSCNT register is shown in QEI x4 Update mode (POSCNT increments on every rising and every falling edge of QEA and QEB input signals).

2: When an INDX Reset pulse is detected, POSCNT is reset to '0' on the next QEA or QEB edge. POSCNT is set to MAXCNT when POSCNT = 0 (when decrementing), which occurs on the next QEA or QEB edge. a similar Reset sequence occurs for the reverse direction, except that the INDX signal is recognized on its falling edge. The Reset is generated on the next QEA or QEB edge.

3: IC2QEIF is enabled for one TCY clock cycle.

4: The position counter is loaded with 0000h (i.e., Reset) on the next QEA or QEB edge when the INDX is high.

5: The position counter is loaded with a MAXCNT value (e.g., 1527h) on the next QEA or QEB edge following the INDX falling edge input signal detect).

6: IC2QEIF must be cleared in software.

REGISTER 18-1: PTCON0: PWM TIMER CONTROL REGISTER 0

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTOPS3	PTOPS2	PTOPS1	PTOPS0	PTCKPS1	PTCKPS0	PTMOD1	PTMOD0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-4 **PTOPS<3:0>:** PWM Time Base Output Postscale Select bits
0000 = 1:1 Postscale
0001 = 1:2 Postscale
.
.
.
1111 = 1:16 Postscale

bit 3-2 **PTCKPS<1:0>:** PWM Time Base Input Clock Prescale Select bits
00 = PWM time base input clock is FOSC/4 (1:1 prescale)
01 = PWM time base input clock is FOSC/16 (1:4 prescale)
10 = PWM time base input clock is FOSC/64 (1:16 prescale)
11 = PWM time base input clock is FOSC/256 (1:64 prescale)

bit 1-0 **PTMOD<1:0>:** PWM Time Base Mode Select bits
11 = PWM time base operates in a Continuous Up/Down Count mode with interrupts for double PWM updates
10 = PWM time base operates in a Continuous Up/Down Count mode
01 = PWM time base configured for Single-Shot mode
00 = PWM time base operates in a Free-Running mode

REGISTER 18-2: PTCON1: PWM TIMER CONTROL REGISTER 1

R/W-0	R-0	U-0	U-0	U-0	U-0	U-0	U-0
PTEN	PTDIR	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **PTEN:** PWM Time Base Timer Enable bit
1 = PWM time base is on
0 = PWM time base is off

bit 6 **PTDIR:** PWM Time Base Count Direction Status bit
1 = PWM time base counts down
0 = PWM time base counts up

bit 5-0 **Unimplemented:** Read as ‘0’

REGISTER 18-3: PWMCON0: PWM CONTROL REGISTER 0

U-0	R/W-1(1)	R/W-1(1)	R/W-1(1)	R/W-0	R/W-0	R/W-0	R/W-0
—	PWMEN2	PWMEN1	PWMEN0	PMOD3(3)	PMOD2	PMOD1	PMOD0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **Unimplemented:** Read as '0'

bit 6-4 **PWMEN<2:0>:** PWM Module Enable bits(1)

111 = All odd PWM I/O pins are enabled for PWM output(2)
110 = PWM1, PWM3 pins are enabled for PWM output
101 = All PWM I/O pins are enabled for PWM output(2)
100 = PWM0, PWM1, PWM2, PWM3, PWM4 and PWM5 pins are enabled for PWM output
011 = PWM0, PWM1, PWM2 and PWM3 I/O pins are enabled for PWM output
010 = PWM0 and PWM1 pins are enabled for PWM output
001 = PWM1 pin is enabled for PWM output
000 = PWM module is disabled; all PWM I/O pins are general purpose I/O

bit 3-0 **PMOD<3:0>:** PWM Output Pair Mode bits

For PMOD0:
1 = PWM I/O pin pair (PWM0, PWM1) is in the Independent mode
0 = PWM I/O pin pair (PWM0, PWM1) is in the Complementary mode

For PMOD1:
1 = PWM I/O pin pair (PWM2, PWM3) is in the Independent mode
0 = PWM I/O pin pair (PWM2, PWM3) is in the Complementary mode

For PMOD2:
1 = PWM I/O pin pair (PWM4, PWM5) is in the Independent mode
0 = PWM I/O pin pair (PWM4, PWM5) is in the Complementary mode

For PMOD3:(3)
1 = PWM I/O pin pair (PWM6, PWM7) is in the Independent mode
0 = PWM I/O pin pair (PWM6, PWM7) is in the Complementary mode

Note 1: Reset condition of the PWMEN bits depends on the PWMPIN Configuration bit.

2: When PWMEN<2:0> = 101, PWM<5:0> outputs are enabled for PIC18F2331/2431 devices; PWM<7:0> outputs are enabled for PIC18F4331/4431 devices.
When PWMEN<2:0> = 111, PWM Outputs 1, 3 and 5 are enabled in PIC18F2331/2431 devices; PWM Outputs 1, 3, 5 and 7 are enabled in PIC18F4331/4431 devices.

3: Unimplemented in PIC18F2331/2431 devices; maintain these bits clear.

19.0 SYNCHRONOUS SERIAL PORT (SSP) MODULE

19.1 SSP Module Overview

The Synchronous Serial Port (SSP) module is a serial interface useful for communicating with other peripheral or microcontroller devices. These peripheral devices may be serial EEPROMs, shift registers, display drivers, A/D Converters, etc. The SSP module can operate in one of two modes:

- Serial Peripheral Interface (SPI)
- Inter-Integrated Circuit (I^2C™)

An overview of I^2C operations and additional information on the SSP module can be found in the *"PIC® Mid-Range MCU Family Reference Manual"* (DS33023).

Refer to application note *AN578, "Use of the SSP Module in the I^2C™ Multi-Master Environment"* (DS00578).

19.2 SPI Mode

This section contains register definitions and operational characteristics of the SPI module. Additional information on the SPI module can be found in the *"PIC® Mid-Range MCU Family Reference Manual"* (DS33023).

SPI mode allows 8 bits of data to be synchronously transmitted and received simultaneously. To accomplish communication, typically three pins are used:

- Serial Data Out (SDO)
- Serial Data In (SDI)
- Serial Clock (SCK)

Additionally, a fourth pin may be used when in a Slave mode of operation:

- Slave Select ($\overline{SS}$)

When initializing the SPI, several options need to be specified. This is done by programming the appropriate control bits in the SSPCON (SSPCON<5:0>) and SSPSTAT<7:6> registers. These control bits allow the following to be specified:

- Master mode (SCK is the clock output)
- Slave mode (SCK is the clock input)
- Clock polarity (Idle state of SCK)
- Clock edge (output data on rising/falling edge of SCK)
- Clock rate (Master mode only)
- Slave Select mode (Slave mode only)

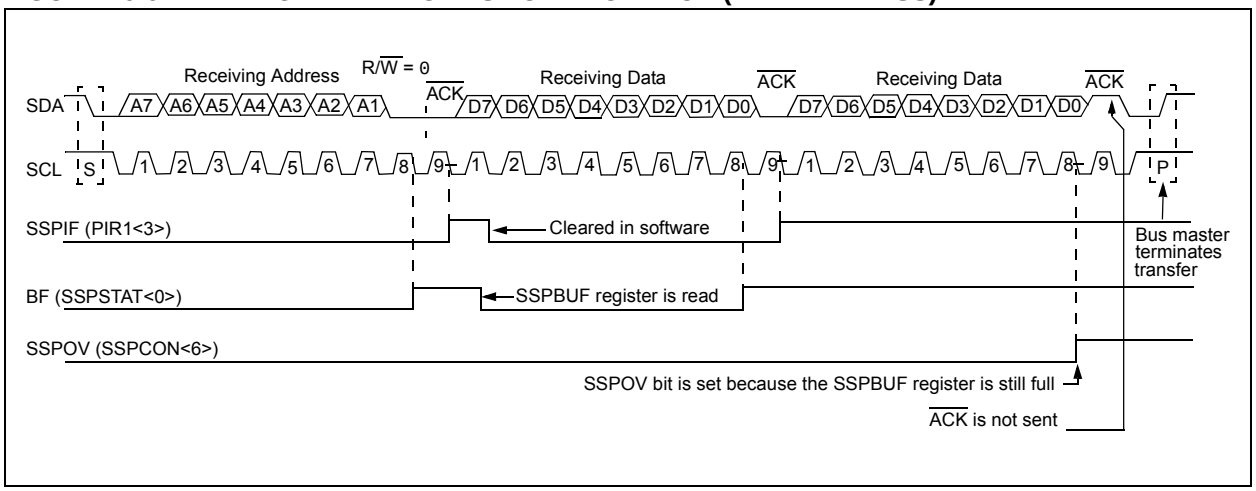
19.3.1.2 Reception

When the R/$\overline{W}$ bit of the address byte is clear and an address match occurs, the R/$\overline{W}$ bit of the SSPSTAT register is cleared. The received address is loaded into the SSPBUF register.

When the address byte overflow condition exists, then the no Acknowledge ($\overline{ACK}$) pulse is given. An overflow condition is defined as either bit BF (SSPSTAT<0>) is set, or bit SSPOV (SSPCON<6>) is set. This is an error condition due to the user's firmware.

An SSP interrupt is generated for each data transfer byte. Flag bit, SSPIF (PIR1<3>), must be cleared in software. The SSPSTAT register is used to determine the status of the byte.

FIGURE 19-6: I²C™ WAVEFORMS FOR RECEPTION (7-BIT ADDRESS)



19.3.2 MASTER MODE

Master mode of operation is supported in firmware using interrupt generation on the detection of the Start and Stop conditions. The Stop (P) and Start (S) bits are cleared from a Reset or when the SSP module is disabled. The Stop (P) and Start (S) bits will toggle based on the Start and Stop conditions. Control of the I^2C bus may be taken when the P bit is set, or the bus is Idle and both the S and P bits are clear.

In Master mode, the SCL and SDA lines are manipulated by clearing the corresponding TRISC<5:4> or TRISD<3:2> bits. The output level is always low, regardless of the value(s) in PORTC<5:4> or PORTD<3:2>. So when transmitting data, a '1' data bit must have the TRISC<4> bit set (input) and a '0' data bit must have the TRISC<4> bit cleared (output). The same scenario is true for the SCL line with the TRISC<4> or TRISD<2> bit. Pull-up resistors must be provided externally to the SCL and SDA pins for proper operation of the I^2C module.

The following events will cause the SSP Interrupt Flag bit, SSPIF, to be set (SSP interrupt will occur if enabled):

- Start condition
- Stop condition
- Data transfer byte transmitted/received

Master mode of operation can be done with either the Slave mode Idle (SSPM<3:0> = 1011) or with the Slave active. When both Master and Slave modes are enabled, the software needs to differentiate the source(s) of the interrupt.

19.3.3 MULTI-MASTER MODE

In Multi-Master mode, the interrupt generation on the detection of the Start and Stop conditions allows the determination of when the bus is free. The Stop (P) and Start (S) bits are cleared from a Reset or when the SSP module is disabled. The Stop (P) and Start (S) bits will toggle based on the Start and Stop conditions. Control of the I^2C bus may be taken when bit P (SSPSTAT<4>) is set, or the bus is Idle and both the S and P bits clear. When the bus is busy, enabling the SSP interrupt will generate the interrupt when the Stop condition occurs.

In Multi-Master mode, the SDA line must be monitored to see if the signal level is the expected output level. This check only needs to be done when a high level is output. If a high level is expected and a low level is present, the device needs to release the SDA and SCL lines (set TRISC<5:4> or TRISD<3:2>). There are two stages where this arbitration can be lost, these are:

- Address Transfer
- Data Transfer

When the slave logic is enabled, the slave continues to receive. If arbitration was lost during the address transfer stage, communication to the device may be in progress. If addressed, an $\overline{ACK}$ pulse will be generated. If arbitration was lost during the data transfer stage, the device will need to retransfer the data at a later time.

TABLE 19-3: REGISTERS ASSOCIATED WITH I^2C™ OPERATION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on Page:
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	54
PIR1	—	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	57
PIE1	—	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	57
SSPBUF	SSP Receive Buffer/Transmit Register								55
SSPADD	SSP Address Register (I^2C mode)								55
SSPCON	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	55
SSPSTAT	SMP(1)	CKE(1)	D/$\overline{A}$	P	S	R/$\overline{W}$	UA	BF	55
TRISC(2)	PORTC Data Direction Register								57
TRISD(2)	PORTD Data Direction Register								57

Legend: — = unimplemented, read as '0'. Shaded cells are not used by the SSP module in I^2C mode.

Note 1: Maintain these bits clear in I^2C mode.

2: Depending upon the setting of SSPMX in CONFIG3H, these pins are multiplexed to PORTC or PORTD.

22.0 LOW-VOLTAGE DETECT (LVD)

PIC18F2331/2431/4331/4431 devices have a Low-Voltage Detect module (LVD), a programmable circuit that enables the user to specify a device voltage trip point. If the device experiences an excursion below the trip point, an interrupt flag is set. If the interrupt is enabled, the program execution will branch to the interrupt vector address and the software can then respond to the interrupt.

The Low-Voltage Detect Control register (Register 22-1) completely controls the operation of the LVD module. This allows the circuitry to be "turned off" by the user under software control, which minimizes the current consumption for the device.

The block diagram for the LVD module is shown in Figure 22-1.

The module is enabled by setting the LVDEN bit, but the circuitry requires some time to stabilize each time that it is enabled. The IRVST bit is a read-only bit used to indicate when the circuit is stable. The module can only generate an interrupt after the circuit is stable and the IRVST bit is set. The module monitors for drops in V_{DD} below a predetermined set point.

REGISTER 22-1: LVDCON: LOW-VOLTAGE DETECT CONTROL REGISTER

U-0	U-0	R-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-1
—	—	IRVST	LVDEN	LVDL3(1)	LVDL2(1)	LVDL1(1)	LVDL0(1)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented:** Read as '0'

bit 5 **IRVST:** Internal Reference Voltage Stable Flag bit
- 1 = Indicates that the Low-Voltage Detect logic will generate the interrupt flag at the specified voltage range
- 0 = Indicates that the Low-Voltage Detect logic will not generate the interrupt flag at the specified voltage range and the LVD interrupt should not be enabled

bit 4 **LVDEN:** Low-Voltage Detect Power Enable bit
- 1 = Enables LVD, powers up LVD circuit
- 0 = Disables LVD, powers down LVD circuit

bit 3-0 **LVDL<3:0>:** Low-Voltage Detection Limit bits(1)
- 1111 = External analog input is used (input comes from the LVDIN pin)
- 1110 = Maximum setting
- .
- .
- .
- 0010 = Minimum setting
- 0001 = Reserved
- 0000 = Reserved

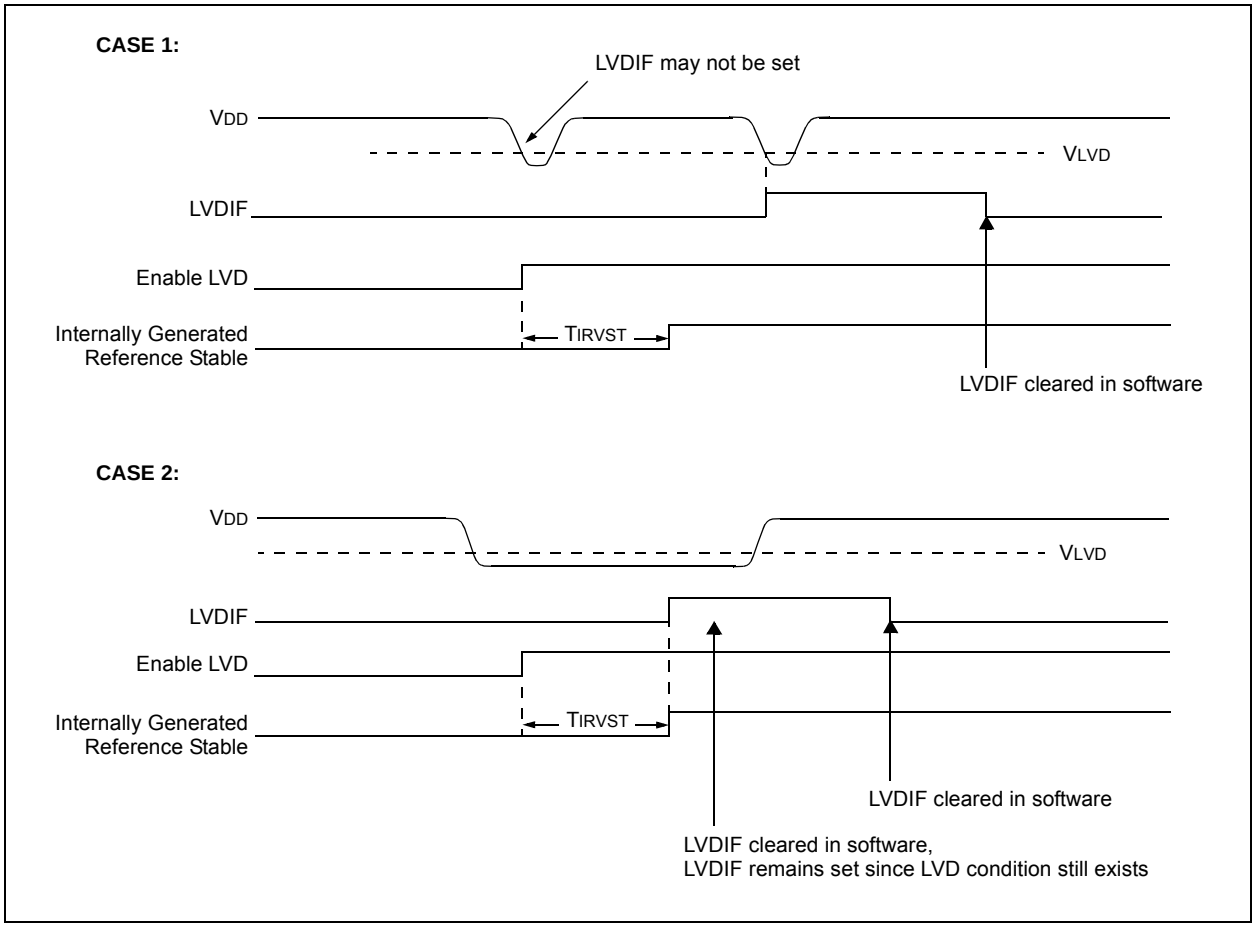
Note 1: LVDL<3:0> bit modes, which result in a trip point below the valid operating voltage of the device, are not tested.

22.4 LVD Start-up Time

The internal reference voltage of the LVD module, specified in electrical specification Parameter D420, may be used by other internal circuitry, such as the Programmable Brown-out Reset. If the LVD, or other circuits using the voltage reference, are disabled to lower the device's current consumption, the reference voltage circuit will require time to become stable before a low-voltage condition can be reliably detected. This start-up time, TIRVST, is an interval that is independent of device clock speed. It is specified in electrical specification Parameter 36.

The LVD interrupt flag is not enabled until TIRVST has expired and a stable reference voltage is reached. For this reason, brief excursions beyond the set point may not be detected during this interval (refer to Figure 22-2).

FIGURE 22-2: LOW-VOLTAGE DETECT WAVEFORMS



REGISTER 23-2: CONFIG2L: CONFIGURATION REGISTER 2 LOW (BYTE ADDRESS 300002h)

U-0	U-0	U-0	U-0	R/P-1	R/P-1	R/P-1	R/P-1
—	—	—	—	BORV1	BORV0	BOREN(1)	$\overline{\text{PWRTEN}}$(1)
bit 7							bit 0

Legend:		
R = Readable bit	P = Programmable bit	U = Unimplemented bit, read as '0'
-n = Value when device is unprogrammed		U = Unchanged from programmed state

bit 7-4 **Unimplemented:** Read as '0'

bit 3-2 **BORV<1:0>:** Brown-out Reset Voltage bits
- 11 = Reserved
- 10 = V_{BOR} set to 2.7V
- 01 = V_{BOR} set to 4.2V
- 00 = V_{BOR} set to 4.5V

bit 1 **BOREN:** Brown-out Reset Enable bit(1)
- 1 = Brown-out Reset is enabled
- 0 = Brown-out Reset is disabled

bit 0 **$\overline{\text{PWRTEN}}$:** Power-up Timer Enable bit(1)
- 1 = PWRT is disabled
- 0 = PWRT is enabled

Note 1: Having BOREN = 1 does not automatically override the $\overline{\text{PWRTEN}}$ to '0', nor automatically enables the Power-up Timer.

REGISTER 23-4: CONFIG3L: CONFIGURATION REGISTER 3 LOW (BYTE ADDRESS 300004h)

U-0	U	R/P-1	R/P-1	R/P-1	R/P-1	U	U
—	—	$\overline{\text{T1OSCMX}}$	HPOL(1)	LPOL(1)	PWMPIN(3)	—	—
bit 7							bit 0

Legend:		
R = Readable bit	P = Programmable bit	U = Unimplemented bit, read as '0'
-n = Value when device is unprogrammed		U = Unchanged from programmed state

bit 7-6 **Unimplemented:** Read as '0'

bit 5 **T1OSCMX:** Timer1 Oscillator Mode bit
1 = Low-power Timer1 operation when microcontroller is in Sleep mode
0 = Standard (legacy) Timer1 oscillator operation

bit 4 **HPOL:** High Side Transistors Polarity bit (i.e., Odd PWM Output Polarity Control bit)(1)
1 = PWM1, 3, 5 and 7 are active-high (default)(2)
0 = PWM1, 3, 5 and 7 are active-low(2)

bit 3 **LPOL:** Low Side Transistors Polarity bit (i.e., Even PWM Output Polarity Control bit)(1)
1 = PWM0, 2, 4 and 6 are active-high (default)(2)
0 = PWM0, 2, 4 and 6 are active-low(2)

bit 2 **PWMPIN:** PWM Output Pins Reset State Control bit(3)
1 = PWM outputs are disabled upon Reset (default)
0 = PWM outputs drive active states upon Reset

bit 1-0 **Unimplemented:** Read as '0'

Note 1: Polarity control bits, HPOL and LPOL, define PWM signal output active and inactive states; PWM states generated by the Fault inputs or PWM manual override.

2: PWM6 and PWM7 output channels are only available on PIC18F4331/4431 devices.

3: When PWMPIN = 0, PWMEN<2:0> = 101 if the device has eight PWM output pins (40 and 44-pin devices) and PWMEN<2:0> = 100 if the device has six PWM output pins (28-pin devices). PWM output polarity is defined by HPOL and LPOL.

23.2 Watchdog Timer (WDT)

For PIC18F2331/2431/4331/4431 devices, the WDT is driven by the INTRC source. When the WDT is enabled, the clock source is also enabled. The nominal WDT period is 4 ms and has the same stability as the INTRC oscillator.

The 4 ms period of the WDT is multiplied by a 16-bit postscaler. Any output of the WDT postscaler is selected by a multiplexer, controlled by bits in Configuration Register 2H (see Register 23-3). Available periods range from 4 ms to 131.072 seconds (2.18 minutes). The WDT and postscaler are cleared when any of the following events occur: execute a SLEEP or CLRWDT instruction, the IRCF bits (OSCCON<6:4>) are changed or a clock failure has occurred (see **Section 23.4.1 "FSCM and the Watchdog Timer"**).

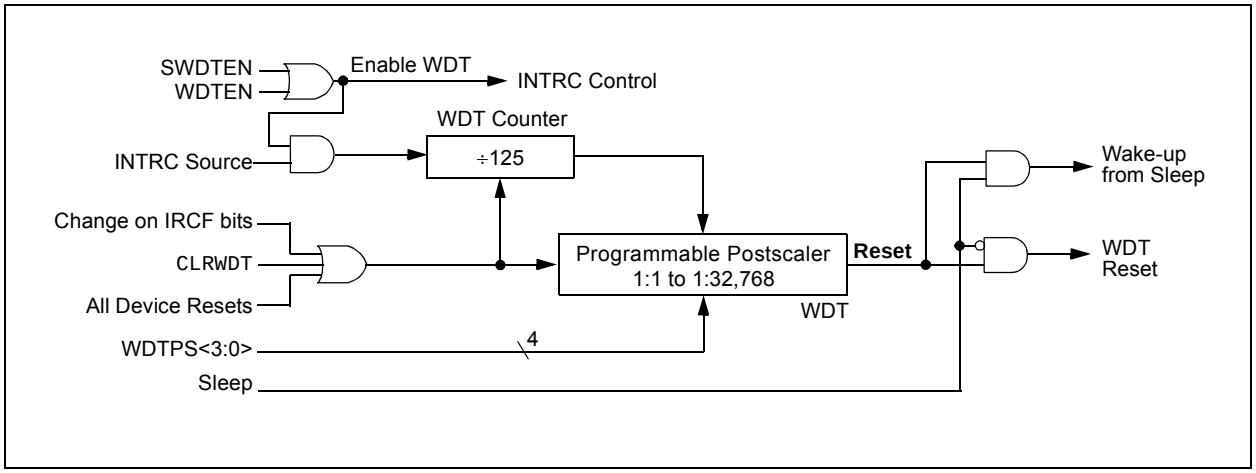
Adjustments to the internal oscillator clock period using the OSCTUNE register also affect the period of the WDT by the same factor. For example, if the INTRC period is increased by 3%, then the WDT period is increased by 3%.

Note 1:	The CLRWDT and SLEEP instructions clear the WDT and postscaler counts when executed.
2:	Changing the setting of the IRCF bits (OSCCON<6:4>) clears the WDT and postscaler counts.
3:	When a CLRWDT instruction is executed, the postscaler count will be cleared.
4:	If $\overline{\text{WINEN}}$ = 0, then CLRWDT must be executed only when WDTW = 1; otherwise, a device Reset will result.

23.2.1 CONTROL REGISTER

Register 23-15 shows the WDTCON register. This is a readable and writable register. The SWDTEN bit allows software to enable or disable the WDT, but only if the Configuration bit has disabled the WDT. The WDTW bit is a read-only bit that indicates when the WDT count is in the fourth quadrant (i.e., when the 8-bit WDT value is b'11000000' or greater).

FIGURE 23-1: WDT BLOCK DIAGRAM



23.5.2 DATA EEPROM CODE PROTECTION

The entire data EEPROM is protected from external reads and writes by two bits: CPD and WRTD. CPD inhibits external reads and writes of data EEPROM. WRTD inhibits external writes to data EEPROM. The CPU can continue to read and write data EEPROM regardless of the protection bit settings.

23.5.3 CONFIGURATION REGISTER PROTECTION

The Configuration registers can be write-protected. The WRTC bit controls protection of the Configuration registers. In normal execution mode, the WRTC bit is readable only. WRTC can only be written via ICSP or an external programmer.

23.6 ID Locations

Eight memory locations (200000h-200007h) are designated as ID locations, where the user can store checksum or other code identification numbers. These locations are both readable and writable during normal execution through the TBLRD and TBLWT instructions, or during program/verify. The ID locations can be read when the device is code-protected.

23.7 In-Circuit Serial Programming

PIC18F2331/2431/4331/4431 microcontrollers can be serially programmed while in the end application circuit. This is simply done with two lines for clock and data, and three other lines for power, ground and the programming voltage. This allows customers to manufacture boards with unprogrammed devices, and then program the microcontroller just before shipping the product. This also allows the most recent firmware or a custom firmware to be programmed.

23.8 In-Circuit Debugger

When the $\overline{\text{DEBUG}}$ bit in the CONFIG4L Configuration register is programmed to a '0', the In-Circuit Debugger functionality is enabled. This function allows simple debugging functions when used with MPLAB® IDE. When the microcontroller has this feature enabled, some resources are not available for general use. Table 23-4 shows which resources are required by the background debugger.

TABLE 23-4: DEBUGGER RESOURCES

I/O pins:	RB6, RB7
Stack:	2 levels
Program Memory:	<1 Kbytes
Data Memory:	16 bytes

To use the In-Circuit Debugger function of the microcontroller, the design must implement In-Circuit Serial Programming connections to $\overline{\text{MCLR}}$/VPP, VDD, VSS, RB7 and RB6. This will interface to the In-Circuit Debugger module available from Microchip or one of the third party development tool companies.

23.9 Single-Supply ICSP™ Programming

The LVP bit in Configuration Register 4L (CONFIG4L<2>) enables Single-Supply ICSP Programming. When LVP is enabled, the microcontroller can be programmed without requiring high voltage being applied to the $\overline{\text{MCLR}}$/VPP pin, but the RB5/PGM pin is then dedicated to controlling Program mode entry and is not available as a general purpose I/O pin.

LVP is enabled in erased devices.

While programming, using Single-Supply Programming, VDD is applied to the $\overline{\text{MCLR}}$/VPP pin as in normal execution mode. To enter Programming mode, VDD is applied to the PGM pin.

Note 1: High-voltage programming is always available, regardless of the state of the LVP bit or the PGM pin, by applying VIHH to the $\overline{\text{MCLR}}$ pin.

2: When Single-Supply Programming is enabled, the RB5 pin can no longer be used as a general purpose I/O pin.

3: When LVP is enabled externally, pull the PGM pin to VSS to allow normal program execution.

If Single-Supply ICSP Programming mode will not be used, the LVP bit can be cleared and RB5/PGM becomes available as the digital I/O pin RB5. The LVP bit may be set or cleared only when using standard high-voltage programming (VIHH applied to the $\overline{\text{MCLR}}$/VPP pin). Once LVP has been disabled, only the standard high-voltage programming is available and must be used to program the device.

Memory that is not code-protected can be erased using either a block erase, or erased row by row, then written at any specified VDD. If code-protected memory is to be erased, a block erase is required. If a block erase is to be performed when using Single-Supply Programming, the device must be supplied with VDD of 4.5V to 5.5V.

TABLE 26-2: LOW-VOLTAGE DETECT CHARACTERISTICS (CONTINUED)

PIC18LF2331/2431/4331/4431 (Industrial)				**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial				
PIC18F2331/2431/4331/4431 (Industrial, Extended)				**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
Param No.	**Symbol**	**Characteristic**		**Min**	**Typ†**	**Max**	**Units**	**Conditions**
D420B	VLVD	LVD Voltage on VDD Transition High-to-Low		Industrial Low Voltage (-40°C to -10°C)				
		PIC18LF2X31/4X31	LVDL<3:0> = 0000	N/A	N/A	N/A	V	Reserved
			LVDL<3:0> = 0001	N/A	N/A	N/A	V	Reserved
			LVDL<3:0> = 0010	1.99	2.26	2.53	V	
			LVDL<3:0> = 0011	2.16	2.45	2.75	V	
			LVDL<3:0> = 0100	2.25	2.55	2.86	V	
			LVDL<3:0> = 0101	2.43	2.77	3.10	V	
			LVDL<3:0> = 0110	2.53	2.87	3.21	V	
			LVDL<3:0> = 0111	2.70	3.07	3.43	V	
			LVDL<3:0> = 1000	2.96	3.36	3.77	V	
			LVDL<3:0> = 1001	3.14	3.57	4.00	V	
			LVDL<3:0> = 1010	3.23	3.67	4.11	V	
			LVDL<3:0> = 1011	3.41	3.87	4.34	V	
			LVDL<3:0> = 1100	3.58	4.07	4.56	V	
			LVDL<3:0> = 1101	3.76	4.28	4.79	V	
			LVDL<3:0> = 1110	4.04	4.60	5.15	V	
D420C	VLVD	LVD Voltage on VDD Transition High-to-Low		Industrial (-10°C to +85°C)				
		PIC18F2X31/4X31	LVDL<3:0> = 1101	3.93	4.28	4.62	V	
			LVDL<3:0> = 1110	4.23	4.60	4.96	V	
D420D	VLVD	LVD Voltage on VDD Transition High-to-Low		Industrial (-40°C to -10°C)				
		PIC18F2X31/4X31	LVDL<3:0> = 1101	3.76	4.28	4.79	V	Reserved
			LVDL<3:0> = 1110	4.04	4.60	5.15	V	
D420E	VLVD	LVD Voltage on VDD Transition High-to-Low		Extended (-10°C to +85°C)				
		PIC18F2X31/4X31	LVDL<3:0> = 1101	3.94	4.28	4.62	V	
			LVDL<3:0> = 1110	4.23	4.60	4.96	V	
D420F	VLVD	LVD Voltage on VDD Transition High-to-Low		Extended (-40°C to -10°C, +85°C to +125°C)				
		PIC18F2X31/4X31	LVDL<3:0> = 1101	3.77	4.28	4.79	V	Reserved
			LVDL<3:0> = 1110	4.05	4.60	5.15	V	

Legend: Shading of rows is to assist in readability of the table.

† Production tested at TAMB = 25°C. Specifications over temperature limits ensured by characterization.

FIGURE 26-10: CAPTURE/COMPARE/PWM TIMINGS (ALL CCP MODULES)

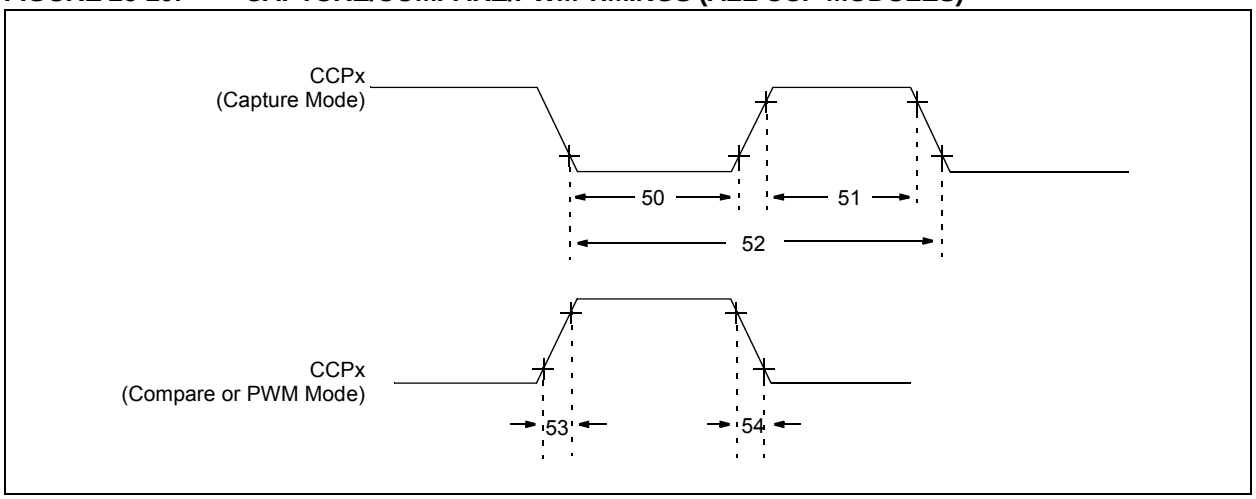


TABLE 26-10: CAPTURE/COMPARE/PWM REQUIREMENTS (ALL CCP MODULES)

Param No.	Symbol	Characteristic			Min	Max	Units	Conditions
50	TccL	CCPx Input Low Time	No prescaler		0.5 TCY + 20	—	ns	
			With prescaler	PIC18FXX31	10	—	ns	
				PIC18LFXX31	20	—	ns	
51	TccH	CCPx Input High Time	No prescaler		0.5 TCY + 20	—	ns	
			With prescaler	PIC18FXX31	10	—	ns	
				PIC18LFXX31	20	—	ns	
52	TccP	CCPx Input Period			$\frac{3\ T_{CY} + 40}{N}$	—	ns	N = prescale value (1, 4 or 16)
53	TccR	CCPx Output Fall Time		PIC18FXX31	—	25	ns	
				PIC18LFXX31	—	45	ns	
54	TccF	CCPx Output Fall Time		PIC18FXX31	—	25	ns	
				PIC18LFXX31	—	45	ns	

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