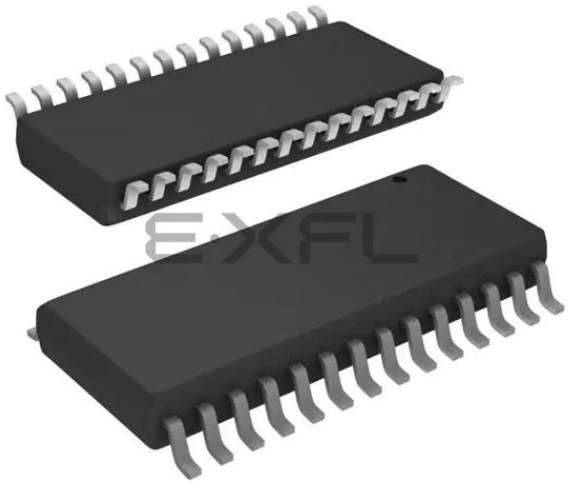

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	PIC
Core Size	8-Bit
Speed	40MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVD, Power Control PWM, QEI, POR, PWM, WDT
Number of I/O	24
Program Memory Size	8KB (4K x 16)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 5x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18lf2331t-i-so

PIC18F2331/2431/4331/4431

28/40/44-Pin Enhanced Flash Microcontrollers with nanoWatt Technology, High-Performance PWM and A/D

14-Bit Power Control PWM Module:

- Up to 4 Channels with Complementary Outputs
- Edge or Center-Aligned Operation
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- Simultaneous Update of Duty Cycle and Period:
  - Flexible Special Event Trigger output

Motion Feedback Module:

- Three Independent Input Capture Channels:
  - Flexible operating modes for period and pulse-width measurement
  - Special Hall sensor interface module
  - Special Event Trigger output to other modules
- Quadrature Encoder Interface:
  - 2-phase inputs and one index input from encoder
  - High and low position tracking with direction status and change of direction interrupt
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High-Speed, 200 ksps 10-Bit A/D Converter:

- Up to 9 Channels
- Simultaneous, Two-Channel Sampling
- Sequential Sampling: 1, 2 or 4 Selected Channels
- Auto-Conversion Capability
- 4-Word FIFO with Selectable Interrupt Frequency
- Selectable External Conversion Triggers
- Programmable Acquisition Time

Flexible Oscillator Structure:

- Four Crystal modes up to 40 MHz
- Two External Clock modes up to 40 MHz
- Internal Oscillator Block:
  - 8 user-selectable frequencies: 31 kHz to 8 MHz
  - OSCTUNE can compensate for frequency drift
- Secondary Oscillator using Timer1 @ 32 kHz
- Fail-Safe Clock Monitor:
  - Allows for safe shutdown of device if clock fails

Power-Managed Modes:

- Run: CPU on, Peripherals on
- Idle: CPU off, Peripherals on
- Sleep: CPU off, Peripherals off
- Ultra Low, 50 nA Input Leakage
- Idle mode Currents Down to 5.8 μA, Typical
- Sleep Current Down to 0.1 μA, Typical
- Timer1 Oscillator, 1.8 μA, Typical, 32 kHz, 2V
- Watchdog Timer (WDT), 2.1 μA, typical
- Oscillator Two-Speed Start-up
  - Fast wake from Sleep and Idle, 1 μs, typical

Peripheral Highlights:

- High-Current Sink/Source 25 mA/25 mA
- Three External Interrupts
- Two Capture/Compare/PWM (CCP) modules
- Enhanced USART module:
  - Supports RS-485, RS-232 and LIN/J2602
  - Auto-wake-up on Start bit
  - Auto-Baud Detect

Special Microcontroller Features:

- 100,000 Erase/Write Cycle Enhanced Flash Program Memory, Typical
- 1,000,000 Erase/Write Cycle Data EEPROM Memory, Typical
- Flash/Data EEPROM Retention: 100 Years
- Self-Programmable under Software Control
- Priority Levels for Interrupts
- 8 x 8 Single-Cycle Hardware Multiplier
- Extended Watchdog Timer (WDT):
  - Programmable period from 41 ms to 131s
- Single-Supply In-Circuit Serial Programming™ (ICSP™) via Two Pins
- In-Circuit Debug (ICD) via Two Pins:
  - Drives PWM outputs safely when debugging

Device	Program Memory		Data Memory		I/O	10-Bit A/D (ch)	CCP	SSP		EUSART	Quadrature Encoder	14-Bit PWM (ch)	Timers 8/16-Bit
	Flash (bytes)	#Single-Word Instructions	SRAM (bytes)	EEPROM (bytes)				SPI	Slave I^2C™				
PIC18F2331	8192	4096	768	256	24	5	2	Y	Y	Y	Y	6	1/3
PIC18F2431	16384	8192	768	256	24	5	2	Y	Y	Y	Y	6	1/3
PIC18F4331	8192	4096	768	256	36	9	2	Y	Y	Y	Y	8	1/3
PIC18F4431	16384	8192	768	256	36	9	2	Y	Y	Y	Y	8	1/3

NOTES:

4.5.4 EXIT WITHOUT AN OSCILLATOR START-UP DELAY

Certain exits from power-managed modes do not invoke the OST at all. There are two cases:

- PRI_IDLE mode, where the primary clock source is not stopped; and
- the primary clock source is not any of the LP, XT, HS or HSPLL modes.

In these instances, the primary clock source either does not require an oscillator start-up delay since it is already running (PRI_IDLE), or normally does not require an oscillator start-up delay (RC, EC and INTIO Oscillator modes). However, a fixed delay of interval, TCSD, following the wake event, is still required when leaving Sleep and Idle modes to allow the CPU to prepare for execution. Instruction execution resumes on the first clock cycle following this delay.

TABLE 4-2: EXIT DELAY ON WAKE-UP BY RESET FROM SLEEP MODE OR ANY IDLE MODE (BY CLOCK SOURCES)

Clock Source Before Wake-up	Clock Source After Wake-up	Exit Delay	Clock Ready Status Bit (OSCCON)
Primary Device Clock (PRI_IDLE mode)	LP, XT, HS	T_{CSD}(1)	OSTS
	HSPLL		
	EC, RC		
	INTOSC(2)		IOFS
T1OSC	LP, XT, HS	T_{OST}(3)	OSTS
	HSPLL	$T_{OST} + t_{rc}$(3)	
	EC, RC	T_{CSD}(1)	
	INTOSC(2)	T_{IOBST}(4)	IOFS
INTOSC(3)	LP, XT, HS	T_{OST}(3)	OSTS
	HSPLL	$T_{OST} + t_{rc}$(3)	
	EC, RC	T_{CSD}(1)	
	INTOSC(2)	None	IOFS
None (Sleep mode)	LP, XT, HS	T_{OST}(3)	OSTS
	HSPLL	$T_{OST} + t_{rc}$(3)	
	EC, RC	T_{CSD}(1)	
	INTOSC(2)	T_{IOBST}(4)	IOFS

Note 1: TCSD (Parameter 38) is a required delay when waking from Sleep and all Idle modes, and runs concurrently with any other required delays (see **Section 4.4 “Idle Modes”**).

2: Includes both the INTOSC 8 MHz source and postscaler derived frequencies.

3: TOST is the Oscillator Start-up Timer (Parameter 32). t_{rc} is the PLL Lock-out Timer (Parameter F12); it is also designated as TPLL.

4: Execution continues during TIOBST (Parameter 39), the INTOSC stabilization period.

5.1 RCON Register

Device Reset events are tracked through the RCON register (Register 5-1). The lower five bits of the register indicate that a specific Reset event has occurred. In most cases, these bits can only be cleared by the event and must be set by the application after the event. The state of these flag bits, taken together, can be read to indicate the type of Reset that just occurred. This is described in more detail in **Section 5.6 "Reset State of Registers"**.

The RCON register also has control bits for setting interrupt priority (IPEN) and software control of the BOR (SBOREN). Interrupt priority is discussed in **Section 10.0 "Interrupts"**. BOR is covered in **Section 5.4 "Brown-out Reset (BOR)"**.

Note 1: If the BOREN Configuration bit is set (Brown-out Reset enabled), the $\overline{BOR}$ bit is '1' on a Power-on Reset. After a Brown-out Reset has occurred, the BOR bit will be cleared and must be set by firmware to indicate the occurrence of the next Brown-out Reset.

2: It is recommended that the $\overline{POR}$ bit be set after a Power-on Reset has been detected, so that subsequent Power-on Resets may be detected.

REGISTER 5-1: RCON: RESET CONTROL REGISTER

R/W-0	U-0	U-0	R/W-1	R-1	R-1	R/W-0	R/W-0
IPEN	—	—	$\overline{RI}$	$\overline{TO}$	$\overline{PD}$	$\overline{POR}$(2)	$\overline{BOR}$(1)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **IPEN:** Interrupt Priority Enable bit
1 = Enable priority levels on interrupts
0 = Disable priority levels on interrupts (PIC16CXXX Compatibility mode)

bit 6-5 **Unimplemented:** Read as '0'

bit 4 **$\overline{RI}$:** RESET Instruction Flag bit
1 = The RESET instruction was not executed (set by firmware only)
0 = The RESET instruction was executed causing a device Reset (must be set in software after a Brown-out Reset occurs)

bit 3 **$\overline{TO}$:** Watchdog Time-out Flag bit
1 = Set by power-up, CLRWDT instruction or SLEEP instruction
0 = A WDT time-out occurred

bit 2 **$\overline{PD}$:** Power-Down Detection Flag bit
1 = Set by power-up or by the CLRWDT instruction
0 = Set by execution of the SLEEP instruction

bit 1 **$\overline{POR}$:** Power-on Reset Status bit(2)
1 = A Power-on Reset has not occurred (set by firmware only)
0 = A Power-on Reset occurred (must be set in software after a Power-on Reset occurs)

bit 0 **$\overline{BOR}$:** Brown-out Reset Status bit(1)
1 = A Brown-out Reset has not occurred (set by firmware only)
0 = A Brown-out Reset occurred (must be set in software after a Brown-out Reset occurs)

Note 1: If SBOREN is enabled, its Reset state is '1'; otherwise, it is '0'.

2: The actual Reset value of $\overline{POR}$ is determined by the type of device Reset. See the notes following this register and **Section 5.6 "Reset State of Registers"** for additional information.

Note 1: It is recommended that the $\overline{POR}$ bit be set after a Power-on Reset has been detected so that subsequent Power-on Resets may be detected.

2: Brown-out Reset is said to have occurred when $\overline{BOR}$ is '0' and $\overline{POR}$ is '1' (assuming that POR was set to '1' by software immediately after a Power-on Reset).

5.6 Reset State of Registers

Most registers are unaffected by a Reset. Their status is unknown on POR and unchanged by all other Resets. The other registers are forced to a “Reset state” depending on the type of Reset that occurred.

Most registers are not affected by a WDT wake-up, since this is viewed as the resumption of normal operation.

Status bits from the RCON register ($\overline{RI}$, $\overline{TO}$, $\overline{PD}$, $\overline{POR}$ and $\overline{BOR}$) are set or cleared differently in different Reset situations, as indicated in Table 5-2. These bits are used in software to determine the nature of the Reset.

Table 5-3 describes the Reset states for all of the Special Function Registers. These are categorized by Power-on and Brown-out Resets, Master Clear and WDT Resets, and WDT wake-ups.

FIGURE 5-3: TIME-OUT SEQUENCE ON POWER-UP ($\overline{MCLR}$ TIED TO V_{DD}, V_{DD} RISE < T_{PWRT})

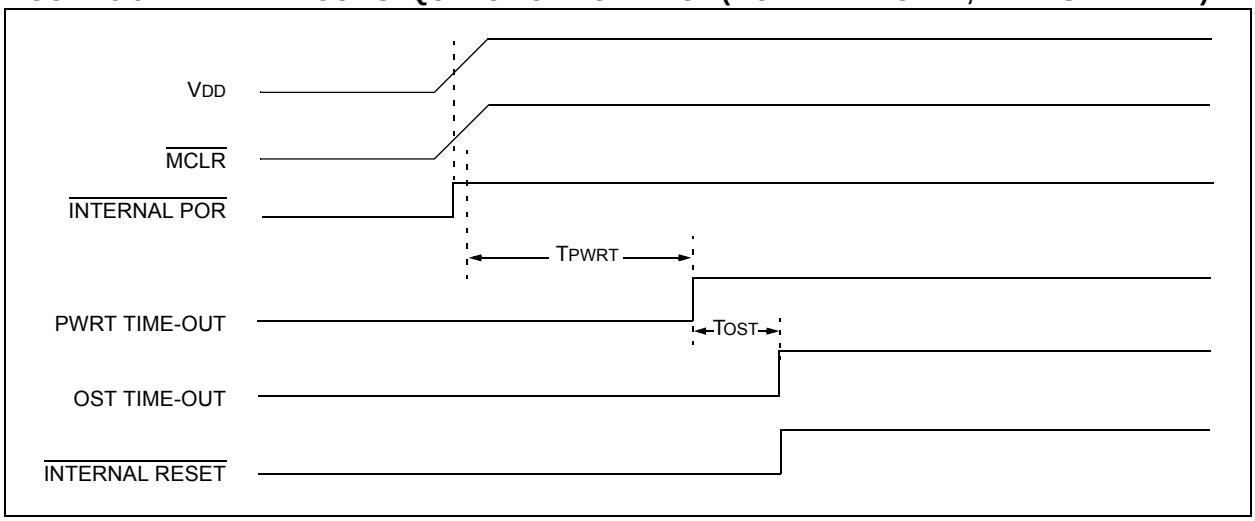


FIGURE 5-4: TIME-OUT SEQUENCE ON POWER-UP ($\overline{MCLR}$ NOT TIED TO V_{DD}): CASE 1

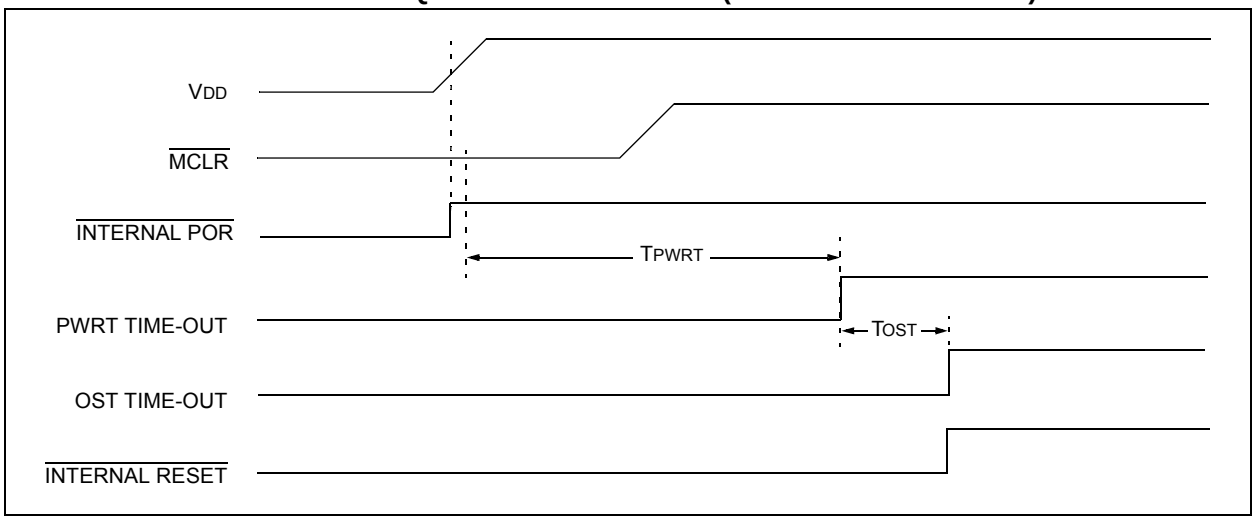
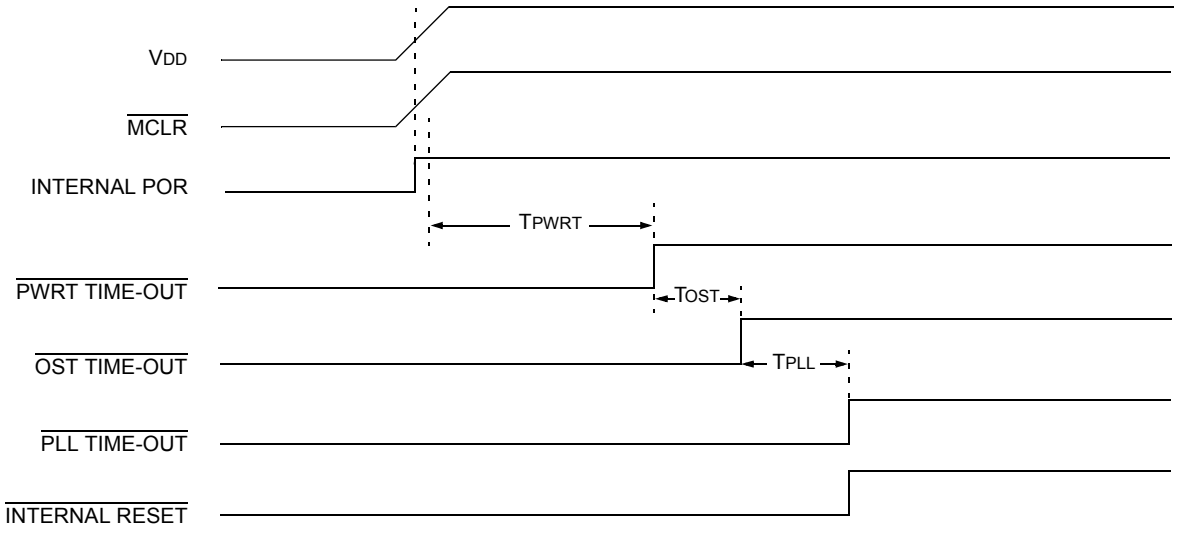


FIGURE 5-7: TIME-OUT SEQUENCE ON POR w/PLL ENABLED (MCLR TIED TO VDD)



Note: TOST = 1024 clock cycles.
TPLL ≈ 2 ms max. First three stages of the PWRT timer.

TABLE 5-2: STATUS BITS, THEIR SIGNIFICANCE AND THE INITIALIZATION CONDITION FOR RCON REGISTER

Condition	Program Counter	RCON Register	RI	TO	PD	POR	BOR	STKFUL	STKUNF
Power-on Reset	0000h	0--1 1100	1	1	1	0	0	0	0
RESET Instruction	0000h	0--0 uuuu	0	u	u	u	u	u	u
Brown-out	0000h	0--1 11u-	1	1	1	u	0	u	u
MCLR Reset during power-managed Run modes	0000h	0--u 1uuu	u	1	u	u	u	u	u
MCLR Reset during power-managed Idle and Sleep modes	0000h	0--u 10uu	u	1	0	u	u	u	u
WDT Time-out during full power or power-managed Run modes	0000h	0--u 0uuu	u	0	u	u	u	u	u
MCLR Reset during full-power execution	0000h	0--u uuuu	u	u	u	u	u	u	u
Stack Full Reset (STVREN = 1)								1	u
Stack Underflow Reset (STVREN = 1)								u	1
Stack Underflow Error (not an actual Reset, STVREN = 0)	0000h	u--u uuuu	u	u	u	u	u	u	1
WDT time-out during power-managed Idle or Sleep modes	PC + 2	u--u 00uu	u	0	0	u	u	u	u
Interrupt exit from power-managed modes	PC + 2(1)	u--u u0uu	u	u	0	u	u	u	u

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as '0'.

Note 1: When the wake-up is due to an interrupt and the GIEH or GIEL bits are set, the PC is loaded with the interrupt vector (0x000008h or 0x000018h).

10.0 INTERRUPTS

The PIC18F2331/2431/4331/4431 devices have multiple interrupt sources and an interrupt priority feature that allows each interrupt source to be assigned a high-priority level or a low-priority level. The high-priority interrupt vector is at 000008h and the low-priority interrupt vector is at 000018h. High-priority interrupt events will interrupt any low-priority interrupts that may be in progress.

There are thirteen registers which are used to control interrupt operation. These registers are:

- RCON
- INTCON
- INTCON2
- INTCON3
- PIR1, PIR2, PIR3
- PIE1, PIE2, PIE3
- IPR1, IPR2, IPR3

It is recommended that the Microchip header files supplied with MPLAB® IDE be used for the symbolic bit names in these registers. This allows the assembler/compiler to automatically take care of the placement of these bits within the specified register.

In general, each interrupt source has three bits to control its operation. The functions of these bits are:

- Flag bit to indicate that an interrupt event occurred
- Enable bit that allows program execution to branch to the interrupt vector address when the flag bit is set
- Priority bit to select high priority or low priority (most interrupt sources have priority bits)

The interrupt priority feature is enabled by setting the IPEN bit (RCON<7>). When interrupt priority is enabled, there are two bits which enable interrupts globally. Setting the GIEH bit (INTCON<7>) enables all interrupts that have the priority bit set (high priority). Setting the GIEL bit (INTCON<6>) enables all interrupts that have the priority bit cleared (low priority). When the interrupt flag, enable bit and appropriate global interrupt enable bit are set, the interrupt will vector immediately to address 000008h or 000018h depending on the priority bit setting. Individual interrupts can be disabled through their corresponding enable bits.

When the IPEN bit is cleared (default state), the interrupt priority feature is disabled and interrupts are compatible with PIC® mid-range devices. In Compatibility mode, the interrupt priority bits for each source have no effect. INTCON<6> is the PEIE bit, which enables/disables all peripheral interrupt sources. INTCON<7> is the GIE bit, which enables/disables all interrupt sources. All interrupts branch to address 000008h in Compatibility mode.

When an interrupt is responded to, the global interrupt enable bit is cleared to disable further interrupts. If the IPEN bit is cleared, this is the GIE bit. If interrupt priority levels are used, this will be either the GIEH or GIEL bit. High-priority interrupt sources can interrupt a low-priority interrupt. Low-priority interrupts are not processed while high-priority interrupts are in progress.

The return address is pushed onto the stack and the PC is loaded with the interrupt vector address (000008h or 000018h). Once in the Interrupt Service Routine, the source(s) of the interrupt can be determined by polling the interrupt flag bits. The interrupt flag bits must be cleared in software before re-enabling interrupts to avoid recursive interrupts.

The “return from interrupt” instruction, `RETFIE`, exits the interrupt routine and sets the GIE bit (GIEH or GIEL if priority levels are used), which re-enables interrupts.

For external interrupt events, such as the INTx pins or the PORTB input change interrupt, the interrupt latency will be three to four instruction cycles. The exact latency is the same for one or two-cycle instructions. Individual interrupt flag bits are set, regardless of the status of their corresponding enable bit or the GIE bit.

Note:	Do not use the `MOVFF` instruction to modify any of the Interrupt Control registers while **any** interrupt is enabled. Doing so may cause erratic microcontroller behavior.

10.5 RCON Register

The RCON register contains bits used to determine the cause of the last Reset or wake-up from a power-managed mode. RCON also contains the bit that enables interrupt priorities (IPEN).

REGISTER 10-13: RCON: RESET CONTROL REGISTER

R/W-0	U-0	U-0	R/W-1	R-1	R-1	R/W-0	R/W-0
IPEN	—	—	$\overline{RI}$	$\overline{TO}$	$\overline{PD}$	$\overline{POR}$	$\overline{BOR}$
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **IPEN:** Interrupt Priority Enable bit
1 = Enable priority levels on interrupts
0 = Disable priority levels on interrupts (PIC16CXXX Compatibility mode)

bit 6-5 **Unimplemented:** Read as ‘0’

bit 4 **$\overline{RI}$:** RESET Instruction Flag bit
For details of bit operation, see Register 5-1.

bit 3 **$\overline{TO}$:** Watchdog Timer Time-out Flag bit
For details of bit operation, see Register 5-1.

bit 2 **$\overline{PD}$:** Power-Down Detection Flag bit
For details of bit operation, see Register 5-1.

bit 1 **$\overline{POR}$:** Power-on Reset Status bit
For details of bit operation, see Register 5-1.

bit 0 **$\overline{BOR}$:** Brown-out Reset Status bit
For details of bit operation, see Register 5-1.

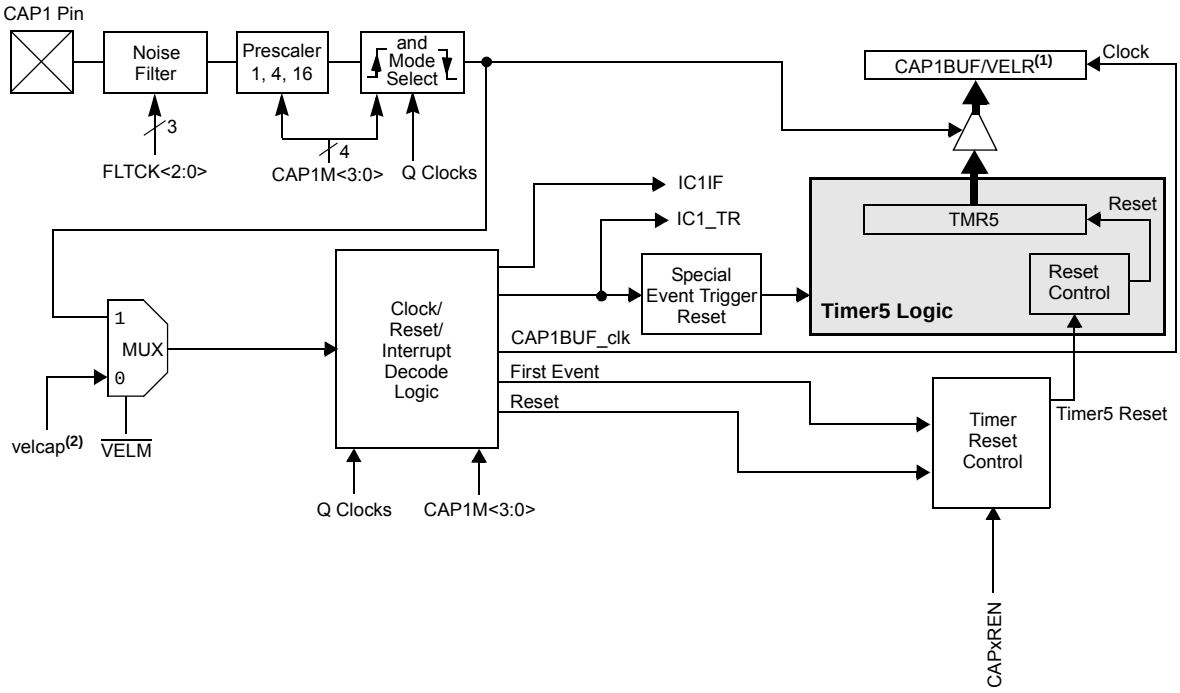
17.1 Input Capture

The Input Capture (IC) submodule implements the following features:

- Three channels of independent input capture (16-bits/channel) on the CAP1, CAP2 and CAP3 pins
- Edge-Trigger, Period or Pulse-Width Measurement Operating modes for each channel
- Programmable prescaler on every input capture channel
- Special Event Trigger output (IC1 only)
- Selectable noise filters on each capture input

Input Channel 1 (IC1) includes a Special Event Trigger that can be configured for use in Velocity Measurement mode. Its block diagram is shown in Figure 17-2. IC2 and IC3 are similar, but lack the Special Event Trigger features or additional velocity measurement logic. A representative block diagram is shown in Figure 17-3. Please note that the time base is Timer5.

FIGURE 17-2: INPUT CAPTURE BLOCK DIAGRAM FOR IC1



Note 1: CAP1BUF register is reconfigured as VELR register when QEI mode is active.

2: QEI generated velocity pulses, vel_out, are downsampled to produce this velocity capture signal.

17.1.5 ENTERING INPUT CAPTURE MODE AND CAPTURE TIMING

The following is a summary of functional operation upon entering any of the Input Capture modes:

1. After the module is configured for one of the Capture modes by setting the Capture Mode Select bits (CAPxM<3:0>), the first detected edge captures the Timer5 value and stores it in the CAPxBUF register. The timer is then reset (depending on the setting of CAPxREN bit) and starts to increment according to its settings (see Figure 17-4, Figure 17-5 and Figure 17-6).
2. On all edges, the capture logic performs the following:
   a) Input Capture mode is decoded and the active edge is identified.
   b) The CAPxREN bit is checked to determine whether Timer5 is reset or not.
   c) On every active edge, the Timer5 value is recorded in the Input Capture Buffer (CAPxBUF).
   d) Reset Timer5 after capturing the value of the timer when the CAPxREN bit is enabled. Timer5 is reset on every active capture edge in this case.
   e) On all continuing capture edge events, repeat steps (a) through (d) until the operational mode is terminated, either by user firmware, POR or BOR.
   f) The timer value is not affected when switching into and out of various Input Capture modes.

17.1.6 TIMER5 RESET

Every input capture trigger can optionally reset (TMR5). The Capture Reset Enable bit, CAPxREN, gates the automatic Reset of the time base of the capture event with this enable Reset signal. All capture events reset the selected timer when CAPxREN is set. Resets are disabled when CAPxREN is cleared (see Figure 17-4, Figure 17-5 and Figure 17-6).

Note:	The CAPxREN bit has no effect in Pulse-Width Measurement mode.

17.1.7 IC INTERRUPTS

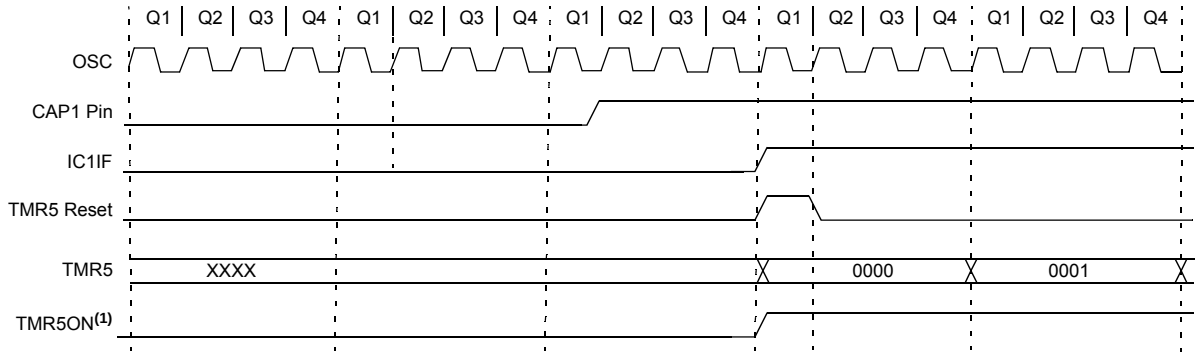
There are four operating modes for which the IC module can generate an interrupt and set one of the Interrupt Capture Flag bits (IC1IF, IC2QEIF or IC3DRIF). The interrupt flag that is set depends on the channel in which the event occurs. The modes are:

- Edge Capture (CAPxM<3:0> = 0001, 0010, 0011 or 0100)
- Period Measurement Event (CAPxM<3:0> = 0101)
- Pulse-Width Measurement Event (CAPxM<3:0> = 0110 or 0111)
- State Change Event (CAPxM<3:0> = 1000)

Note:	The Special Event Trigger is generated only in the Special Event Trigger mode on the CAP1 input (CAP1M<3:0> = 1110 and 1111). IC1IF interrupt is not set in this mode.

The timing of interrupt and Special Event Trigger events is shown in Figure 17-7. Any active edge is detected on the rising edge of Q2 and propagated on the rising edge of Q4 rising edge. If an active edge happens to occur any later than this (on the falling edge of Q2, for example), then it will be recognized on the next Q2 rising edge.

FIGURE 17-7: CAPx INTERRUPTS AND IC1 SPECIAL EVENT TRIGGER



Note 1: Timer5 is only reset and enabled (assuming TMR5ON = 0 and T5MOD = 1) when the Special Event Trigger Reset is enabled for the Timer5 Reset input. The TMR5ON bit is asserted and Timer5 is reset on the Q1 rising edge following the event capture. With the Special Event Trigger Reset disabled, Timer5 cannot be reset by the Special Event Trigger Reset on the CAP1 input. In order for the Special Event Trigger Reset to work as the Reset trigger to Timer5, IC1 must be configured in the Special Event Trigger mode (CAP1M<3:0> = 1110 or 1111).

17.3 Noise Filters

The Motion Feedback Module includes three noise rejection filters on RA2/AN2/VREF-/CAP1/INDX, RA3/AN3/VREF+/CAP2/QEA and RA4/AN4/CAP3/QEB. The filter block also includes a fourth filter for the T5CKI pin. They are intended to help reduce spurious noise spikes which may cause the input signals to become corrupted at the inputs. The filter ensures that the input signals are not permitted to change until a stable value has been registered for three consecutive sampling clock cycles.

The filters are controlled using the Digital Filter Control (DFLTCON) register (see Register 17-3). The filters can be individually enabled or disabled by setting or clearing the corresponding FLTxEN bit in the DFLTCON register. The sampling frequency, which must be the same for all three noise filters, can be programmed by the FLTCK<2:0> Configuration bits. TCY is used as the clock reference to the clock divider block.

The noise filters can either be added or removed from the input capture, or QEI signal path, by setting or clearing the appropriate FLTxEN bit, respectively. Each capture channel provides for individual enable control of the filter output. The FLT4EN bit enables or disables the noise filter available on the T5CKI input in the Timer5 module.

The filter network for all channels is disabled on Power-on and Brown-out Resets, as the DFLTCON register is cleared on Resets. The operation of the filter is shown in the timing diagram in Figure 17-14.

REGISTER 17-3: DFLTCON: DIGITAL FILTER CONTROL REGISTER

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	FLT4EN	FLT3EN(1)	FLT2EN(1)	FLT1EN(1)	FLTCK2	FLTCK1	FLTCK0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **Unimplemented:** Read as ‘0’

bit 6 **FLT4EN:** Noise Filter Output Enable bit (T5CKI input)
1 = Enabled
0 = Disabled

bit 5 **FLT3EN:** Noise Filter Output Enable bit (CAP3/QEB input)(1)
1 = Enabled
0 = Disabled

bit 4 **FLT2EN:** Noise Filter Output Enable bit (CAP2/QEA input)(1)
1 = Enabled
0 = Disabled

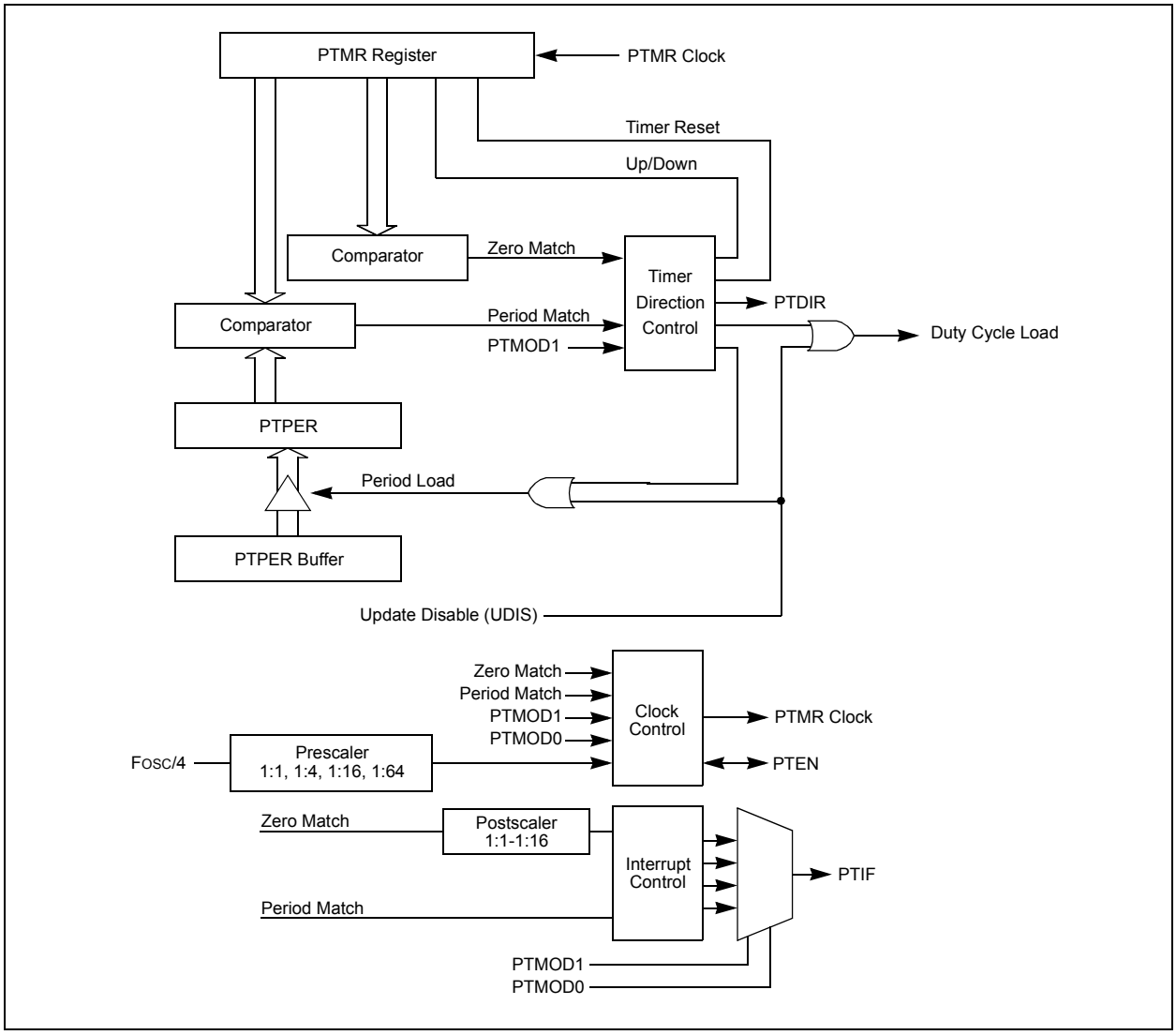
bit 3 **FLT1EN:** Noise Filter Output Enable bit (CAP1/INDX Input)(1)
1 = Enabled
0 = Disabled

bit 2-0 **FLTCK<2:0>:** Noise Filter Clock Divider Ratio bits
111 = Unused
110 = 1:128
101 = 1:64
100 = 1:32
011 = 1:16
010 = 1:4
001 = 1:2
000 = 1:1

Note 1: The noise filter output enables are functional in both QEI and IC Operating modes.

Note: The noise filter is intended for random high-frequency filtering and not continuous high-frequency filtering.

FIGURE 18-4: PWM TIME BASE BLOCK DIAGRAM



The PWM time base can be configured for four different modes of operation:

- Free-Running mode
- Single-Shot mode
- Continuous Up/Down Count mode
- Continuous Up/Down Count mode with interrupts for double updates

These four modes are selected by the PTMOD<1:0> bits in the PTCON0 register. The Free-Running mode produces edge-aligned PWM generation. The Continuous Up/Down Count modes produce center-aligned PWM generation. The Single-Shot mode allows the PWM module to support pulse control of certain Electronically Commutated Motors (ECMs) and produces edge-aligned operation.

REGISTER 19-2: SSPCON: SYNCHRONOUS SERIAL PORT CONTROL REGISTER (CONTINUED)

bit 3-0 **SSPM<3:0>**: Synchronous Serial Port Mode Select bits(3)

0000 = SPI Master mode, Clock = FOSC/4
0001 = SPI Master mode, Clock = FOSC/16
0010 = SPI Master mode, Clock = FOSC/64
0011 = SPI Master mode, Clock = TMR2 output/2
0100 = SPI Slave mode, Clock = SCK pin, $\overline{SS}$ pin control enabled
0101 = SPI Slave mode, Clock = SCK pin, $\overline{SS}$ pin control disabled, $\overline{SS}$ can be used as I/O pin
0110 = I^2C Slave mode, 7-bit address
0111 = I^2C Slave mode, 10-bit address
1011 = I^2C Firmware Controlled Master mode (slave Idle)
1110 = I^2C Slave mode, 7-bit address with Start and Stop bit interrupts enabled
1111 = I^2C Slave mode, 10-bit address with Start and Stop bit interrupts enabled

Note 1: In Master mode, the overflow bit is not set since each new reception (and transmission) is initiated by writing to the SSPBUF register.

2: When enabled, these pins must be properly configured as inputs or outputs.

3: Bit combinations not specifically listed here are either reserved or implemented in I^2C™ mode only.

20.3 EUSART Asynchronous Mode

The Asynchronous mode of operation is selected by clearing the SYNC bit (TXSTA<4>). In this mode, the EUSART uses standard Non-Return-to-Zero (NRZ) format (one Start bit, eight or nine data bits and one Stop bit). The most common data format is 8 bits. An on-chip dedicated 8-bit/16-bit Baud Rate Generator can be used to derive standard baud rate frequencies from the oscillator.

The EUSART transmits and receives the LSb first. The EUSART's transmitter and receiver are functionally independent, but use the same data format and baud rate. The Baud Rate Generator produces a clock, either x16 or x64 of the bit shift rate, depending on the BRGH and BRG16 bits (TXSTA<2> and BAUDCON<3>). Parity is not supported by the hardware but can be implemented in software and stored as the 9th data bit.

Asynchronous mode is available in all Low-Power modes; it is available in Sleep mode only when Auto-Wake-up on Sync Break is enabled. When in PRI_IDLE mode, no changes to the Baud Rate Generator values are required; however, other Low-Power mode clocks may operate at another frequency than the primary clock. Therefore, the Baud Rate Generator values may need to be adjusted.

When operating in Asynchronous mode, the EUSART module consists of the following important elements:

- Baud Rate Generator
- Sampling Circuit
- Asynchronous Transmitter
- Asynchronous Receiver
- Auto-Wake-up on Sync Break Character
- 12-Bit Break Character Transmit
- Auto-Baud Rate Detection

20.3.1 EUSART ASYNCHRONOUS TRANSMITTER

The EUSART transmitter block diagram is shown in Figure 20-2. The heart of the transmitter is the Transmit (Serial) Shift Register (TSR). The Shift register obtains its data from the Read/Write Transmit Buffer register, TXREG. The TXREG register is loaded with data in software. The TSR register is not loaded until the Stop bit has been transmitted from the previous load. As soon as the Stop bit is transmitted, the TSR is loaded with new data from the TXREG register (if available).

Once the TXREG register transfers the data to the TSR register (occurs in one TCY), the TXREG register is empty and flag bit, TXIF (PIR1<4>), is set. This interrupt can be enabled/disabled by setting/clearing enable bit, TXIE (PIE1<4>). Flag bit, TXIF, will be set, regardless of the state of enable bit TXIE and cannot be cleared in software. Flag bit, TXIF, is not cleared immediately upon loading the Transmit Buffer register, TXREG. TXIF becomes valid in the second instruction cycle following the load instruction. Polling TXIF immediately following a load of TXREG will return invalid results.

While flag bit, TXIF, indicates the status of the TXREG register, another bit, TRMT (TXSTA<1>), shows the status of the TSR register. Status bit, TRMT, is a read-only bit, which is set when the TSR register is empty. No interrupt logic is tied to this bit, so the user has to poll this bit in order to determine if the TSR register is empty.

Note 1: The TSR register is not mapped in data memory, so it is not available to the user.

2: Flag bit, TXIF, is set when enable bit, TXEN, is set.

To set up an Asynchronous Transmission:

1. Initialize the SPBRGH:SPBRG registers for the appropriate baud rate. Set or clear the BRGH and BRG16 bits, as required, to achieve the desired baud rate.
2. Enable the asynchronous serial port by clearing bit, SYNC, and setting bit, SPEN.
3. If interrupts are desired, set enable bit, TXIE.
4. If 9-bit transmission is desired, set transmit bit, TX9. Can be used as address/data bit.
5. Enable the transmission by setting bit, TXEN, which will also set bit, TXIF.
6. If 9-bit transmission is selected, the ninth bit should be loaded in bit, TX9D.
7. Load data to the TXREG register (starts transmission).

If using interrupts, ensure that the GIE and PEIE bits in the INTCON register (INTCON<7:6>) are set.

TABLE 21-3: SUMMARY OF A/D REGISTERS

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on Page:
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	54
PIR1	—	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	57
PIE1	—	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	57
IPR1	—	ADIP	RCIP	TXIP	SSPIP	CCP1IP	TMR2IP	TMR1IP	57
PIR2	OSCFIF	—	—	EEIF	—	LVDIF	—	CCP2IF	57
PIE2	OSCFIE	—	—	EEIE	—	LVDIE	—	CCP2IE	57
IPR2	OSCFIP	—	—	EEIP	—	LVDIP	—	CCP2IP	57
ADRESH	A/D Result Register High Byte								56
ADRESL	A/D Result Register Low Byte								56
ADCON0	—	—	ACONV	ACSCH	ACMOD1	ACMOD0	GO/$\overline{\text{DONE}}$	ADON	56
ADCON1	VCFG1	VCFG0	—	FIFOEN	BFEMT	BFOVFL	ADPNT1	ADPNT0	56
ADCON2	ADFM	ACQT3	ACQT2	ACQT1	ACQT0	ADCS2	ADCS1	ADCS0	56
ADCON3	ADRS1	ADRS0	—	SSRC4	SSRC3	SSRC2	SSRC1	SSRC0	56
ADCHS	GDSEL1	GDSEL0	GBSEL1	GBSEL0	GCSEL1	GCSEL0	GASEL1	GASEL0	56
ANSEL0	ANS7(6)	ANS6(6)	ANS5(6)	ANS4	ANS3	ANS2	ANS1	ANS0	56
ANSEL1	—	—	—	—	—	—	—	ANS8(5)	56
PORTA	RA7(4)	RA6(4)	RA5	RA4	RA3	RA2	RA1	RA0	57
TRISA	TRISA7(4)	TRISA6(4)	PORTA Data Direction Register						57
PORTE(2)	—	—	—	—	RE3(1,3)	RA2(3)	RA1(3)	RA0(3)	57
TRISE(3)	—	—	—	—	—	PORTE Data Direction Register			57
LATE(3)	—	—	—	—	—	LATE Data Output Register			57

Legend: — = unimplemented, read as '0'. Shaded cells are not used for A/D conversion.

Note 1: The RE3 port bit is available only as an input pin when the MCLRE bit in the CONFIG3H register is '0'.

2: This register is not implemented on PIC18F2331/2431 devices.

3: These bits are not implemented on PIC18F2331/2431 devices.

4: These pins may be configured as port pins depending on the oscillator mode selected.

5: ANS5 through ANS8 are available only on the PIC18F4331/4431 devices.

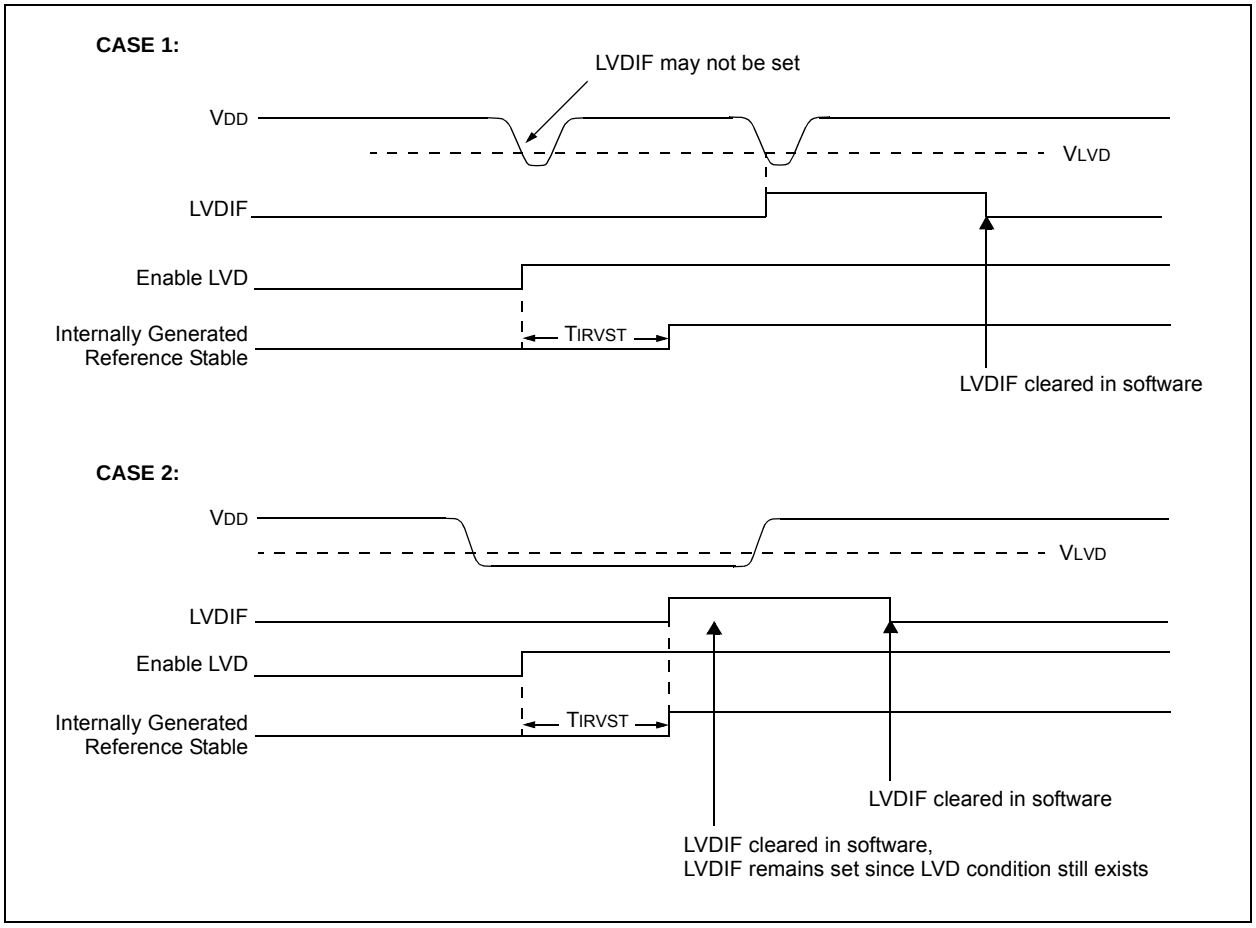
6: Not available on 28-pin devices.

22.4 LVD Start-up Time

The internal reference voltage of the LVD module, specified in electrical specification Parameter D420, may be used by other internal circuitry, such as the Programmable Brown-out Reset. If the LVD, or other circuits using the voltage reference, are disabled to lower the device's current consumption, the reference voltage circuit will require time to become stable before a low-voltage condition can be reliably detected. This start-up time, TIRVST, is an interval that is independent of device clock speed. It is specified in electrical specification Parameter 36.

The LVD interrupt flag is not enabled until TIRVST has expired and a stable reference voltage is reached. For this reason, brief excursions beyond the set point may not be detected during this interval (refer to Figure 22-2).

FIGURE 22-2: LOW-VOLTAGE DETECT WAVEFORMS



CPFSGT **Compare f with W, Skip if f > W**

Syntax: [*label*] CPFSGT f [,a]

Operands: $0 \le f \le 255$
$a \in [0,1]$

Operation: (f) − (W),
skip if (f) > (W)
(unsigned comparison)

Status Affected: None

Encoding:

0110	010a	ffff	ffff

Description: Compares the contents of data memory location, 'f', to the contents of the W by performing an unsigned subtraction. If the contents of 'f' are greater than the contents of WREG, then the fetched instruction is discarded and a NOP is executed instead, making this a two-cycle instruction. If 'a' is '0', the Access Bank will be selected, overriding the BSR value. If 'a' = 1, then the bank will be selected as per the BSR value.

Words: 1

Cycles: 1(2)
Note: 3 cycles if skip and followed by a 2-word instruction.

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	No operation

If skip:

Q1	Q2	Q3	Q4
No operation	No operation	No operation	No operation

If skip and followed by 2-word instruction:

Q1	Q2	Q3	Q4
No operation	No operation	No operation	No operation
No operation	No operation	No operation	No operation

Example:
```
HERE      CPFSGT REG
NGREATER  :
GREATER   :
```
Before Instruction
PC = Address (HERE)
W = ?
After Instruction
If REG > W;
PC = Address (GREATER)
If REG ≤ W;
PC = Address (NGREATER)

CPFSLT **Compare f with W, Skip if f < W**

Syntax: [*label*] CPFSLT f [,a]

Operands: $0 \le f \le 255$
$a \in [0,1]$

Operation: (f) – (W),
skip if (f) < (W)
(unsigned comparison)

Status Affected: None

Encoding:

0110	000a	ffff	ffff

Description: Compares the contents of data memory location, 'f', to the contents of W by performing an unsigned subtraction. If the contents of 'f' are less than the contents of W, then the fetched instruction is discarded and a NOP is executed instead, making this a two-cycle instruction. If 'a' is '0', the Access Bank will be selected. If 'a' is '1', the BSR will not be overridden.

Words: 1

Cycles: 1(2)
Note: 3 cycles if skip and followed by a 2-word instruction.

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	No operation

If skip:

Q1	Q2	Q3	Q4
No operation	No operation	No operation	No operation

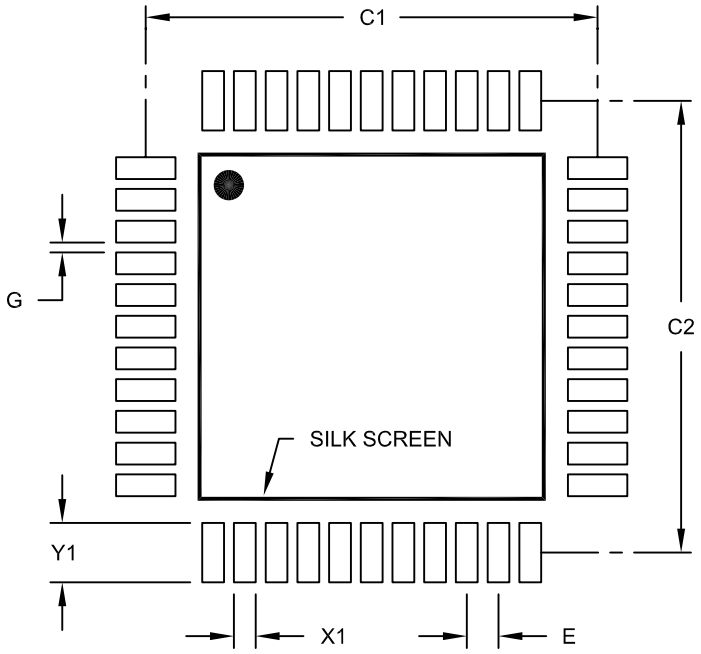
If skip and followed by 2-word instruction:

Q1	Q2	Q3	Q4
No operation	No operation	No operation	No operation
No operation	No operation	No operation	No operation

Example:
```
HERE    CPFSLT REG
NLESS   :
LESS    :
```
Before Instruction
PC = Address (HERE)
W = ?
After Instruction
If REG < W;
PC = Address (LESS)
If REG ≥ W;
PC = Address (NLESS)

44-Lead Plastic Thin Quad Flatpack (PT) – 10x10x1 mm Body, 2.00 mm [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.80 BSC	
Contact Pad Spacing	C1		11.40	
Contact Pad Spacing	C2		11.40	
Contact Pad Width (X44)	X1			0.55
Contact Pad Length (X44)	Y1			1.50
Distance Between Pads	G	0.25		

Notes:

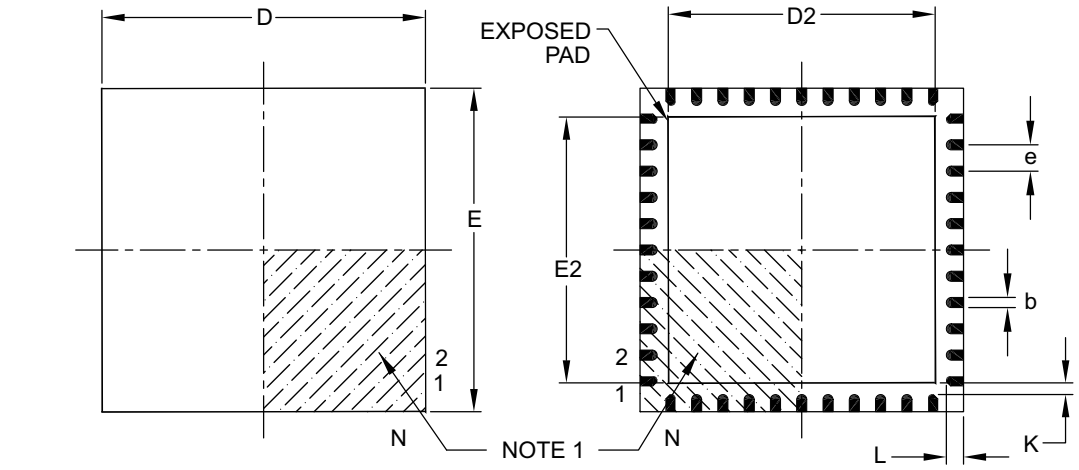
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

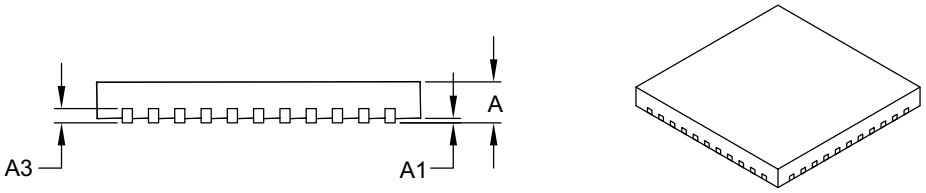
Microchip Technology Drawing No. C04-2076A

44-Lead Plastic Quad Flat, No Lead Package (ML) – 8x8 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW **BOTTOM VIEW**



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		44	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Width	E		8.00 BSC	
Exposed Pad Width	E2	6.30	6.45	6.80
Overall Length	D		8.00 BSC	
Exposed Pad Length	D2	6.30	6.45	6.80
Contact Width	b	0.25	0.30	0.38
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	–	–

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-103B

Q

R