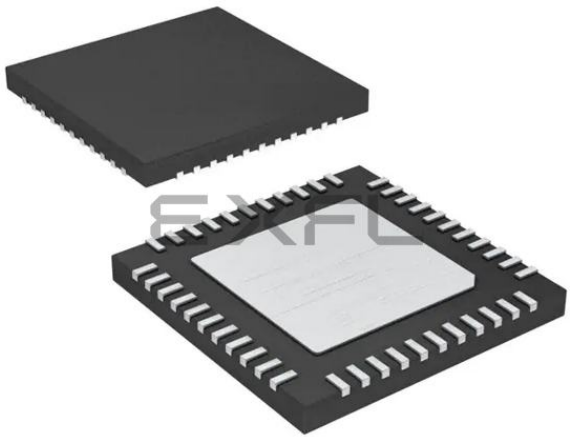

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	40MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVD, Power Control PWM, QEI, POR, PWM, WDT
Number of I/O	36
Program Memory Size	16KB (8K x 16)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 9x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18lf4431-i-ml

1.2 Other Special Features

- **Memory Endurance:** The enhanced Flash cells for both program memory and data EEPROM are rated to last for many thousands of erase/write cycles – up to 100,000 for program memory and 1,000,000 for EEPROM. Data retention without refresh is conservatively estimated to be greater than 100 years.
- **Self-Programmability:** These devices can write to their own program memory spaces under internal software control. By using a bootloader routine located in the protected boot block at the top of program memory, it becomes possible to create an application that can update itself in the field.
- **Power Control PWM Module:** In PWM mode, this module provides 1, 2 or 4 modulated outputs for controlling half-bridge and full-bridge drivers. Other features include auto-shutdown on Fault detection and auto-restart to reactivate outputs once the condition has cleared.
- **Enhanced Addressable USART:** This serial communication module is capable of standard RS-232 operation and provides support for the LIN/J2602 bus protocol. Other enhancements include automatic baud rate detection and a 16-bit Baud Rate Generator for improved resolution. When the microcontroller is using the internal oscillator block, the EUSART provides stable operation for applications that talk to the outside world without using an external crystal (or its accompanying power requirement).
- **Extended Watchdog Timer (WDT):** This enhanced version incorporates a 16-bit prescaler, allowing an extended time-out range that is stable across operating voltage and temperature. See **Section 26.0 “Electrical Characteristics”** for time-out periods.
- **High-Speed 10-Bit A/D Converter:** This module incorporates programmable acquisition time, allowing for a channel to be selected and a conversion to be initiated without waiting for a sampling period and thus, reducing code overhead.
- **Motion Feedback Module** (MFM): This module features a Quadrature Encoder Interface (QEI) and an Input Capture (IC) module. The QEI accepts two phase inputs (QEA, QEB) and one index input (INDX) from an incremental encoder. The QEI supports high and low precision position tracking, direction status and change of direction interrupt and velocity measurement. The input capture features 3 channels of independent input capture with Timer5 as the time base, a Special Event Trigger to other modules and an adjustable noise filter on each IC input.
- **Extended Watchdog Timer (WDT):** This enhanced version incorporates a 16-bit prescaler, allowing a time-out range from 4 ms to over 2 minutes, that is stable across operating voltage and temperature.

TABLE 1-3: PIC18F4331/4431 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	PDIP	TQFP	QFN			
						PORTE is a bidirectional I/O port.
RE0/AN6	8	25	25			
RE0				I/O	ST	Digital I/O.
AN6				I	Analog	Analog Input 6.
RE1/AN7	9	26	26			
RE1				I/O	ST	Digital I/O.
AN7				I	Analog	Analog Input 7.
RE2/AN8	10	27	27			
RE2				I/O	ST	Digital I/O.
AN8				I	Analog	Analog Input 8.
VSS	12, 31	6, 29	6, 30, 31	P	—	Ground reference for logic and I/O pins.
VDD	11, 32	7, 28	7, 8, 28, 29	P	—	Positive supply for logic and I/O pins.
NC	—	12, 13, 33, 34	13	NC	NC	No connect.

Legend: TTL = TTL compatible input; CMOS = CMOS compatible input or output; ST = Schmitt Trigger input with CMOS levels; I = Input; O = Output; P = Power

Note 1: RC3 is the alternate pin for T0CKI/T5CKI; RC4 is the alternate pin for SDI/SDA; RC5 is the alternate pin for SCK/SCL; RC7 is the alternate pin for SDO.

2: RD4 is the alternate pin for $\overline{\text{FLTA}}$.

3: RD5 is the alternate pin for PWM4.

2.5 External Oscillator Pins

Many microcontrollers have options for at least two oscillators: a high-frequency primary oscillator and a low-frequency secondary oscillator (refer to **Section 3.0 "Oscillator Configurations"** for details).

The oscillator circuit should be placed on the same side of the board as the device. Place the oscillator circuit close to the respective oscillator pins with no more than 0.5 inch (12 mm) between the circuit components and the pins. The load capacitors should be placed next to the oscillator itself, on the same side of the board.

Use a grounded copper pour around the oscillator circuit to isolate it from surrounding circuits. The grounded copper pour should be routed directly to the MCU ground. Do not run any signal traces or power traces inside the ground pour. Also, if using a two-sided board, avoid any traces on the other side of the board where the crystal is placed.

Layout suggestions are shown in Figure 2-4. In-line packages may be handled with a single-sided layout that completely encompasses the oscillator pins. With fine-pitch packages, it is not always possible to completely surround the pins and components. A suitable solution is to tie the broken guard sections to a mirrored ground layer. In all cases, the guard trace(s) must be returned to ground.

In planning the application's routing and I/O assignments, ensure that adjacent port pins and other signals in close proximity to the oscillator are benign (i.e., free of high frequencies, short rise and fall times, and other similar noise).

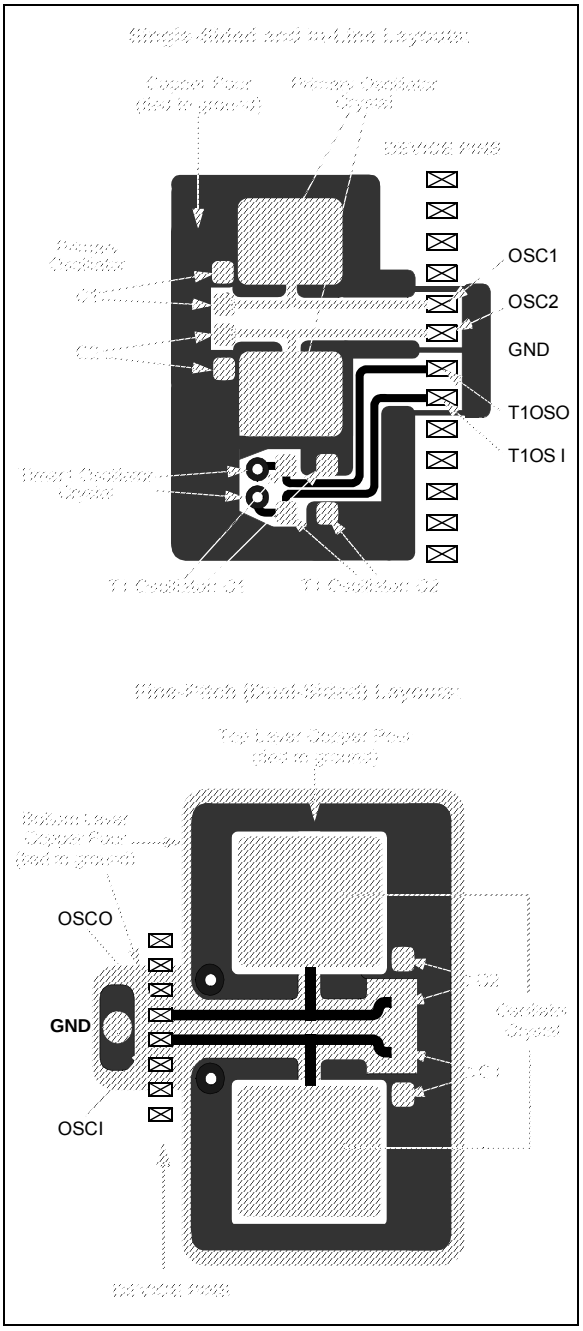
For additional information and design guidance on oscillator circuits, please refer to these Microchip Application Notes, available at the corporate web site (www.microchip.com):

- *AN826, "Crystal Oscillator Basics and Crystal Selection for rfPIC™ and PICmicro® Devices"*
- *AN849, "Basic PICmicro® Oscillator Design"*
- *AN943, "Practical PICmicro® Oscillator Analysis and Design"*
- *AN949, "Making Your Oscillator Work"*

2.6 Unused I/Os

Unused I/O pins should be configured as outputs and driven to a logic low state. Alternatively, connect a 1 kΩ to 10 kΩ resistor to VSS on unused pins and drive the output to logic low.

FIGURE 2-3: SUGGESTED PLACEMENT OF THE OSCILLATOR CIRCUIT



REGISTER 3-1: OSCTUNE: OSCILLATOR TUNING REGISTER

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	TUN5	TUN4	TUN3	TUN2	TUN1	TUN0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **TUN<5:0>:** Frequency Tuning bits

011111 = Maximum frequency
•
•
000001
000000 = Center frequency. Oscillator module is running at the calibrated frequency.
111111
•
•
100000 = Minimum frequency

3.6.4.1 Compensating with the EUSART

An adjustment may be required when the EUSART begins generating framing errors or receives data with errors while in Asynchronous mode. Framing errors frequently indicate that the device clock frequency is too high. To adjust for this, decrement the value in the OSCTUNE register to reduce the clock frequency.

Conversely, errors in data may suggest that the clock speed is too low; to compensate, increment the OSCTUNE register to increase the clock frequency.

3.6.4.2 Compensating with the Timers

This technique compares the device clock speed to that of a reference clock. Two timers may be used: one timer clocked by the peripheral clock and the other by a fixed reference source, such as the Timer1 oscillator.

Both timers are cleared, but the timer clocked by the reference generates interrupts. When an interrupt occurs, the internally clocked timer is read and both timers are cleared. If the internally clocked timer value is greater than expected, the internal oscillator block is running too fast. To adjust for this, decrement the OSCTUNE register.

3.6.4.3 Compensating with the CCP Module in Capture Mode

A CCP module can use free-running Timer1 (or Timer3), clocked by the internal oscillator block and an external event with a known period (such as the AC power frequency). The time of the first event is captured in the CCPRxH:CCPRxL registers and recorded for later use. When the second event causes a capture, the time of the first event is subtracted from the time of the second event. Since the period of the external event is known, the time difference between events can be calculated.

If the measured time is much greater than the calculated time, the internal oscillator block is running too fast. To compensate for this, decrement the OSCTUNE register. If the measured time is much less than the calculated time, the internal oscillator block is running too slow and the OSCTUNE register should be incremented.

5.5 Device Reset Timers

PIC18F2331/2431/4331/4431 devices incorporate three separate on-chip timers that help regulate the Power-on Reset process. Their main function is to ensure that the device clock is stable before code is executed. These timers are:

- Power-up Timer (PWRT)
- Oscillator Start-up Timer (OST)
- PLL Lock Time-out

5.5.1 POWER-UP TIMER (PWRT)

The Power-up Timer (PWRT) of PIC18F2331/2431/4331/4431 devices is an 11-bit counter that uses the INTRC source as the clock input. This yields an approximate time interval of 2,048 x 32 μs = 65.6 ms.

While the PWRT is counting, the device is held in Reset. The power-up time delay depends on the INTRC clock and will vary from chip to chip due to temperature and process variation. See DC Parameter 33 for details.

The PWRT is enabled by clearing the PWRTEN Configuration bit.

5.5.2 OSCILLATOR START-UP TIMER (OST)

The Oscillator Start-up Timer (OST) provides a 1,024 oscillator cycle (from OSC1 input) delay after the PWRT delay is over (Parameter 33). This ensures that the crystal oscillator or resonator has started and stabilized.

The OST time-out is invoked only for XT, LP, HS and HSPLL modes, and on Power-on Reset or on exit from most power-managed modes.

5.5.3 PLL LOCK TIME-OUT

With the PLL enabled in its PLL mode, the time-out sequence following a Power-on Reset is slightly different from other oscillator modes. A separate timer is used to provide a fixed time-out that is sufficient for the PLL to lock to the main oscillator frequency. This PLL Lock Time-out (T_{PLL}) is typically 2 ms and follows the oscillator start-up time-out.

5.5.4 TIME-OUT SEQUENCE

On power-up, the time-out sequence is as follows:

1. After the POR pulse has cleared, the PWRT time-out is invoked (if enabled).
2. Then, the OST is activated.

The total time-out will vary based on oscillator configuration and the status of the PWRT. Figure 5-3 through Figure 5-7 depict time-out sequences on power-up, with the Power-up Timer enabled and the device operating in HS Oscillator mode. Figure 5-3 through Figure 5-6 also apply to devices operating in XT or LP modes.

For devices in RC mode, and with the PWRT disabled, there will be no time-out at all. Since the time-outs occur from the POR pulse, if $\overline{MCLR}$ is kept low long enough, all time-outs will expire. Bringing $\overline{MCLR}$ high will begin execution immediately (Figure 5-5). This is useful for testing purposes or synchronization of more than one PIC18FXXXX device operating in parallel.

TABLE 5-1: TIME-OUT IN VARIOUS SITUATIONS

Oscillator Configuration	Power-up(2) and Brown-out		Exit From Power-Managed Mode
	$\overline{PWRTEN}$ = 0	$\overline{PWRTEN}$ = 1	
HSPLL	66 ms(1) + 1024 TOSC + 2 ms(2)	1024 TOSC + 2 ms(2)	1024 TOSC + 2 ms(2)
HS, XT, LP	66 ms(1) + 1024 TOSC	1024 TOSC	1024 TOSC
EC, ECIO	66 ms(1)	—	—
RC, RCIO	66 ms(1)	—	—
INTIO1, INTIO2	66 ms(1)	—	—

Note 1: 66 ms (65.5 ms) is the nominal Power-up Timer (PWRT) delay.
2: 2 ms is the nominal time required for the 4x PLL to lock.

TABLE 5-3: INITIALIZATION CONDITIONS FOR ALL REGISTERS

Register	Applicable Devices				Power-on Reset, Brown-out Reset	$\overline{\text{MCLR}}$ Resets WDT Reset RESET Instruction Stack Resets	Wake-up via WDT or Interrupt
TOSU	2331	2431	4331	4431	---0 0000	---0 0000	---0 uuuu(3)
TOSH	2331	2431	4331	4431	0000 0000	0000 0000	uuuu uuuu(3)
TOSL	2331	2431	4331	4431	0000 0000	0000 0000	uuuu uuuu(3)
STKPTR	2331	2431	4331	4431	00-0 0000	uu-0 0000	uu-u uuuu(3)
PCLATU	2331	2431	4331	4431	---0 0000	---0 0000	---u uuuu
PCLATH	2331	2431	4331	4431	0000 0000	0000 0000	uuuu uuuu
PCL	2331	2431	4331	4431	0000 0000	0000 0000	PC + 2(2)
TBLPTRU	2331	2431	4331	4431	--00 0000	--00 0000	--uu uuuu
TBLPTRH	2331	2431	4331	4431	0000 0000	0000 0000	uuuu uuuu
TBLPTRL	2331	2431	4331	4431	0000 0000	0000 0000	uuuu uuuu
TABLAT	2331	2431	4331	4431	0000 0000	0000 0000	uuuu uuuu
PRODH	2331	2431	4331	4431	xxxx xxxx	uuuu uuuu	uuuu uuuu
PRODL	2331	2431	4331	4431	xxxx xxxx	uuuu uuuu	uuuu uuuu
INTCON	2331	2431	4331	4431	0000 000x	0000 000u	uuuu uuuu(1)
INTCON2	2331	2431	4331	4431	1111 -1-1	1111 -1-1	uuuu -u-u(1)
INTCON3	2331	2431	4331	4431	11-0 0-00	11-0 0-00	uu-u u-uu(1)
INDF0	2331	2431	4331	4431	N/A	N/A	N/A
POSTINC0	2331	2431	4331	4431	N/A	N/A	N/A
POSTDEC0	2331	2431	4331	4431	N/A	N/A	N/A
PREINC0	2331	2431	4331	4431	N/A	N/A	N/A
PLUSW0	2331	2431	4331	4431	N/A	N/A	N/A
FSR0H	2331	2431	4331	4431	---- xxxx	---- uuuu	---- uuuu
FSR0L	2331	2431	4331	4431	xxxx xxxx	uuuu uuuu	uuuu uuuu
WREG	2331	2431	4331	4431	xxxx xxxx	uuuu uuuu	uuuu uuuu
INDF1	2331	2431	4331	4431	N/A	N/A	N/A
POSTINC1	2331	2431	4331	4431	N/A	N/A	N/A
POSTDEC1	2331	2431	4331	4431	N/A	N/A	N/A
PREINC1	2331	2431	4331	4431	N/A	N/A	N/A
PLUSW1	2331	2431	4331	4431	N/A	N/A	N/A

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as '0', q = value depends on condition. Shaded cells indicate conditions do not apply for the designated device.

Note 1: One or more bits in the INTCONx or PIRx registers will be affected (to cause wake-up).

2: When the wake-up is due to an interrupt and the GIEL or GIEH bit is set, the PC is loaded with the interrupt vector (0008h or 0018h).

3: When the wake-up is due to an interrupt and the GIEL or GIEH bit is set, the TOSU, TOSH and TOSL are updated with the current value of the PC. The STKPTR is modified to point to the next location in the hardware stack.

4: See Table 5-2 for Reset value for specific condition.

5: Bits 6 and 7 of PORTA, LATA and TRISA are enabled depending on the oscillator mode selected. When not enabled as PORTA pins, they are disabled and read '0'.

6: Bit 3 of PORTE and LATE are enabled if $\overline{\text{MCLR}}$ functionality is disabled. When not enabled as the PORTE pin, they are disabled and read as '0'. The 28-pin devices do not have only RE3 implemented.

TABLE 5-3: INITIALIZATION CONDITIONS FOR ALL REGISTERS (CONTINUED)

Register	Applicable Devices				Power-on Reset, Brown-out Reset	MCLR Resets WDT Reset RESET Instruction Stack Resets	Wake-up via WDT or Interrupt
IPR2	2331	2431	4331	4431	1--1 -1-1	1--1 -1-1	u--u -u-u
PIR2	2331	2431	4331	4431	0--0 -0-0	0--0 -0-0	u--u -u-u
PIE2	2331	2431	4331	4431	0--0 -0-0	0--0 -0-0	u--u -u-u
IPR1	2331	2431	4331	4431	-111 1111	-111 1111	-uuu uuuu
PIR1	2331	2431	4331	4431	-000 0000	-000 0000	-uuu uuuu(1)
	2331	2431	4331	4431	-000 0000	-000 0000	-uuu uuuu(1)
PIE1	2331	2431	4331	4431	0000 0000	0000 0000	uuuu uuuu
	2331	2431	4331	4431	-000 0000	-000 0000	-uuu uuuu
OSCTUNE	2331	2431	4331	4431	--00 0000	--00 0000	--uu uuuu
TRISE(6)	2331	2431	4331	4431	---- -111	---- -111	---- -uuu
TRISD	2331	2431	4331	4431	1111 1111	1111 1111	uuuu uuuu
TRISC	2331	2431	4331	4431	1111 1111	1111 1111	uuuu uuuu
TRISB	2331	2431	4331	4431	1111 1111	1111 1111	uuuu uuuu
TRISA(5)	2331	2431	4331	4431	1111 1111(5)	1111 1111(5)	uuuu uuuu(5)
PR5H	2331	2431	4331	4431	1111 1111	1111 1111	uuuu uuuu
PR5L	2331	2431	4331	4431	1111 1111	1111 1111	uuuu uuuu
LATE(6)	2331	2431	4331	4431	---- -xxx	---- -uuu	---- -uuu
LATD	2331	2431	4331	4431	xxxx xxxx	uuuu uuuu	uuuu uuuu
LATC	2331	2431	4331	4431	xxxx xxxx	uuuu uuuu	uuuu uuuu
LATB	2331	2431	4331	4431	xxxx xxxx	uuuu uuuu	uuuu uuuu
LATA(5)	2331	2431	4331	4431	xxxx xxxx(5)	uuuu uuuu(5)	uuuu uuuu(5)
TMR5H	2331	2431	4331	4431	xxxx xxxx	uuuu uuuu	uuuu uuuu
TMR5L	2331	2431	4331	4431	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTE(6)	2331	2431	4331	4431	---- xxxx	---- xxxx	---- uuuu
PORTD	2331	2431	4331	4431	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTC	2331	2431	4331	4431	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTB	2331	2431	4331	4431	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTA(5)	2331	2431	4331	4431	xx0x 0000(5)	uu0u 0000(5)	uuuu uuuu(5)

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as '0', q = value depends on condition. Shaded cells indicate conditions do not apply for the designated device.

Note 1: One or more bits in the INTCONx or PIRx registers will be affected (to cause wake-up).

2: When the wake-up is due to an interrupt and the GIEL or GIEH bit is set, the PC is loaded with the interrupt vector (0008h or 0018h).

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6.0 MEMORY ORGANIZATION

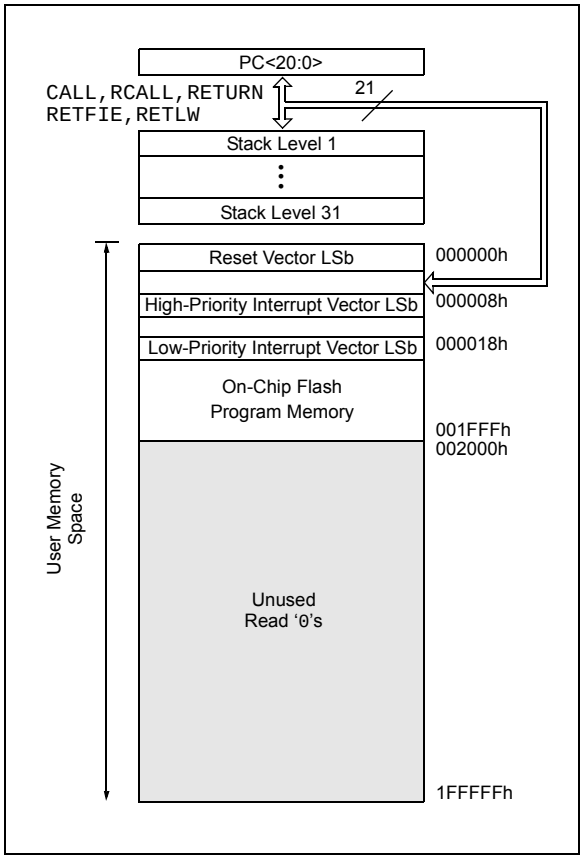
There are three memory types in enhanced MCU devices. These memory types are:

- Program Memory
- Data RAM
- Data EEPROM

As Harvard architecture devices, the data and program memories use separate buses, enabling concurrent access of the two memory spaces. The data EEPROM, for practical purposes, can be regarded as a peripheral device, since it is addressed and accessed through a set of control registers.

Additional detailed information on the operation of the Flash program memory is provided in **Section 8.0 "Flash Program Memory"**. Data EEPROM is discussed separately in **Section 7.0 "Data EEPROM Memory"**.

FIGURE 6-1: PROGRAM MEMORY MAP AND STACK FOR PIC18F2331/4331



6.1 Program Memory Organization

PIC18 microcontrollers implement a 21-bit program counter that can address a 2-Mbyte program memory space. Accessing a location between the upper boundary of the physically implemented memory and the 2-Mbyte address will return all '0's (a NOP instruction).

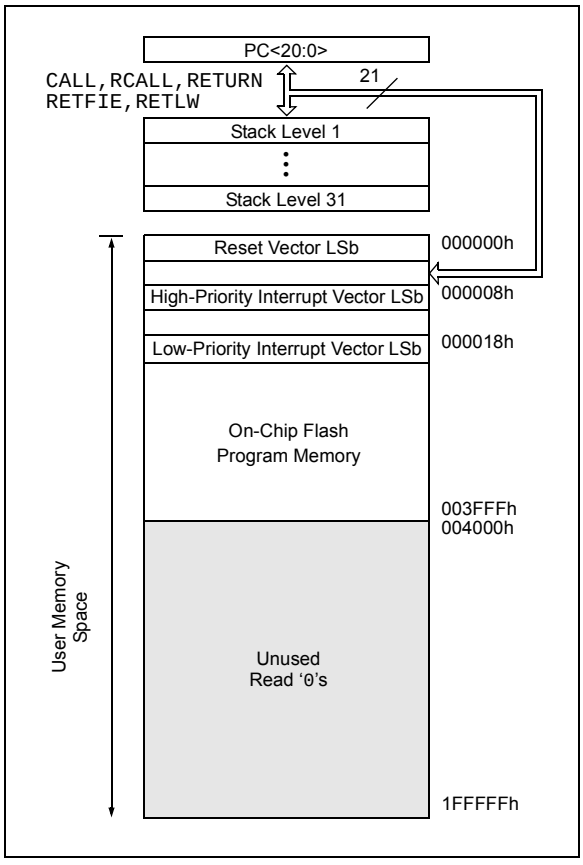
The PIC18F2331/4331 devices each have 8 Kbytes of Flash memory and can store up to 4,096 single-word instructions.

The PIC18F2431/4431 devices each have 16 Kbytes of Flash memory and can store up to 8,192 single-word instructions.

PIC18 devices have two interrupt vectors. The Reset vector address is at 000000h and the interrupt vector addresses are at 000008h and 000018h.

The program memory maps for PIC18F2331/4331 and PIC18F2431/4431 devices are shown in Figure 6-1 and Figure 6-2, respectively.

FIGURE 6-2: PROGRAM MEMORY MAP AND STACK FOR PIC18F2431/4431



8.4 Erasing Flash Program Memory

The minimum erase block is 32 words or 64 bytes. Larger blocks of program memory can be bulk erased only through the use of an external programmer or ICSP control. Word erase in the Flash array is not supported.

When initiating an erase sequence from the microcontroller itself, a block of 64 bytes of program memory is erased. The Most Significant 16 bits of the TBLPTR<21:6> point to the block being erased; TBLPTR<5:0> are ignored.

The EECON1 register commands the erase operation. The EEPGD bit (EECON1<7>) must be set to point to the Flash program memory. The WREN bit (EECON1<2>) must be set to enable write operations. The FREE bit (EECON1<4>) is set to select an erase operation.

For protection, the write initiate sequence using EECON2 must be used.

A long write is necessary for erasing the internal Flash. Instruction execution is halted while in a long write cycle. The long write will be terminated by the internal programming timer.

8.4.1 FLASH PROGRAM MEMORY ERASE SEQUENCE

The sequence of events for erasing a block of internal program memory location is:

1. Load the Table Pointer with the address of the row being erased.
2. Set the EECON1 register for the erase operation:
   - set the EEPGD bit to point to program memory;
   - clear the CFGS bit to access program memory;
   - set the WREN bit to enable writes;
   - set the FREE bit to enable the erase.
3. Disable interrupts.
4. Write 55h to EECON2.
5. Write 0AAh to EECON2.
6. Set the WR bit. This will begin the row erase cycle.
7. The CPU will stall for the duration of the erase (about 2 ms using internal timer).
8. Execute a NOP.
9. Re-enable interrupts.

EXAMPLE 8-2: ERASING A FLASH PROGRAM MEMORY ROW

```
                MOVLW   CODE_ADDR_UPPER    ; load TBLPTR with the base
                MOVWF   TBLPTRU            ; address of the memory block
                MOVLW   CODE_ADDR_HIGH
                MOVWF   TBLPTRH
                MOVLW   CODE_ADDR_LOW
                MOVWF   TBLPTRL
      ERASE_ROW
                BSF     EECON1, EEPGD      ; point to Flash program memory
                BCF     EECON1, CFGS       ; access Flash program memory
                BSF     EECON1, WREN       ; enable write to memory
                BSF     EECON1, FREE       ; enable Row Erase operation
                BCF     INTCON, GIE        ; disable interrupts
                MOVLW   55h
                MOVWF   EECON2             ; write 55H
  Required      MOVLW   0AAh
  Sequence      MOVWF   EECON2             ; write 0AAH
                BSF     EECON2, WR         ; start erase (CPU stall)
                NOP
                BSF     INTCON, GIE        ; re-enable interrupts
```

8.5.1 FLASH PROGRAM MEMORY WRITE SEQUENCE

The sequence of events for programming an internal program memory location should be:

1. Read 64 bytes into RAM.
2. Update data values in RAM as necessary.
3. Load Table Pointer with address being erased.
4. Do the row erase procedure (see **Section 8.4.1 "Flash Program Memory Erase Sequence"**).
5. Load Table Pointer with the address of the first byte being written.
6. Write the first 8 bytes into the holding registers with auto-increment.
7. Set the EECON1 register for the write operation by doing the following:
   - Set the EEPGD bit to point to program memory
   - Clear the CFGS bit to access program memory
   - Set the WREN bit to enable byte writes
8. Disable interrupts.
9. Write 55h to EECON2.
10. Write 0AAh to EECON2.
11. Set the WR bit. This will begin the write cycle.
12. The CPU will stall for the duration of the write (about 2 ms using internal timer).
13. Execute a NOP.
14. Re-enable interrupts.
15. Repeat Steps 6-14 seven times to write 64 bytes.
16. Verify the memory (table read).

This procedure will require about 18 ms to update one row of 64 bytes of memory. An example of the required code is given in Example 8-3.

10.0 INTERRUPTS

The PIC18F2331/2431/4331/4431 devices have multiple interrupt sources and an interrupt priority feature that allows each interrupt source to be assigned a high-priority level or a low-priority level. The high-priority interrupt vector is at 000008h and the low-priority interrupt vector is at 000018h. High-priority interrupt events will interrupt any low-priority interrupts that may be in progress.

There are thirteen registers which are used to control interrupt operation. These registers are:

- RCON
- INTCON
- INTCON2
- INTCON3
- PIR1, PIR2, PIR3
- PIE1, PIE2, PIE3
- IPR1, IPR2, IPR3

It is recommended that the Microchip header files supplied with MPLAB® IDE be used for the symbolic bit names in these registers. This allows the assembler/compiler to automatically take care of the placement of these bits within the specified register.

In general, each interrupt source has three bits to control its operation. The functions of these bits are:

- Flag bit to indicate that an interrupt event occurred
- Enable bit that allows program execution to branch to the interrupt vector address when the flag bit is set
- Priority bit to select high priority or low priority (most interrupt sources have priority bits)

The interrupt priority feature is enabled by setting the IPEN bit (RCON<7>). When interrupt priority is enabled, there are two bits which enable interrupts globally. Setting the GIEH bit (INTCON<7>) enables all interrupts that have the priority bit set (high priority). Setting the GIEL bit (INTCON<6>) enables all interrupts that have the priority bit cleared (low priority). When the interrupt flag, enable bit and appropriate global interrupt enable bit are set, the interrupt will vector immediately to address 000008h or 000018h depending on the priority bit setting. Individual interrupts can be disabled through their corresponding enable bits.

When the IPEN bit is cleared (default state), the interrupt priority feature is disabled and interrupts are compatible with PIC® mid-range devices. In Compatibility mode, the interrupt priority bits for each source have no effect. INTCON<6> is the PEIE bit, which enables/disables all peripheral interrupt sources. INTCON<7> is the GIE bit, which enables/disables all interrupt sources. All interrupts branch to address 000008h in Compatibility mode.

When an interrupt is responded to, the global interrupt enable bit is cleared to disable further interrupts. If the IPEN bit is cleared, this is the GIE bit. If interrupt priority levels are used, this will be either the GIEH or GIEL bit. High-priority interrupt sources can interrupt a low-priority interrupt. Low-priority interrupts are not processed while high-priority interrupts are in progress.

The return address is pushed onto the stack and the PC is loaded with the interrupt vector address (000008h or 000018h). Once in the Interrupt Service Routine, the source(s) of the interrupt can be determined by polling the interrupt flag bits. The interrupt flag bits must be cleared in software before re-enabling interrupts to avoid recursive interrupts.

The “return from interrupt” instruction, `RETFIE`, exits the interrupt routine and sets the GIE bit (GIEH or GIEL if priority levels are used), which re-enables interrupts.

For external interrupt events, such as the INTx pins or the PORTB input change interrupt, the interrupt latency will be three to four instruction cycles. The exact latency is the same for one or two-cycle instructions. Individual interrupt flag bits are set, regardless of the status of their corresponding enable bit or the GIE bit.

Note:	Do not use the `MOVFF` instruction to modify any of the Interrupt Control registers while **any** interrupt is enabled. Doing so may cause erratic microcontroller behavior.

REGISTER 10-5: PIR2: PERIPHERAL INTERRUPT REQUEST (FLAG) REGISTER 2

R/W-0	U-0	U-0	R/W-0	U-0	R/W-0	U-0	R/W-0
OSCFIF	—	—	EEIF	—	LVDIF	—	CCP2IF
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **OSCFIF:** Oscillator Fail Interrupt Flag bit
1 = Device oscillator failed, clock input has changed to INTOSC (must be cleared in software)
0 = Device clock operating

bit 6-5 **Unimplemented:** Read as '0'

bit 4 **EEIF:** EEPROM or Flash Write Operation Interrupt Flag bit
1 = The write operation is complete (must be cleared in software)
0 = The write operation is not complete or has not been started

bit 3 **Unimplemented:** Read as '0'

bit 2 **LVDIF:** Low-Voltage Detect Interrupt Flag bit
1 = The supply voltage has fallen below the specified LVD voltage (must be cleared in software)
0 = The supply voltage is greater than the specified LVD voltage

bit 1 **Unimplemented:** Read as '0'

bit 0 **CCP2IF:** CCP2 Interrupt Flag bit
Capture mode:
1 = A TMR1 register capture occurred (must be cleared in software)
0 = No TMR1 register capture occurred
Compare mode:
1 = A TMR1 register compare match occurred (must be cleared in software)
0 = No TMR1 register compare match occurred
PWM mode:
Not used in this mode.

NOTES:

17.1.3.1 Pulse-Width Measurement Timing

Pulse-width measurement accuracy can only be ensured when the pulse-width high and low present on the CAPx input exceeds one TCY clock cycle. The limitations depend on the mode selected:

- When CAPxM<3:0> = 0110 (rising to falling edge delay), the CAPx input high pulse width (TCCH) must exceed TCY + 10 ns.
- When CAPxM<3:0> = 0111 (falling to rising edge delay), the CAPx input low pulse width (TCCL) must exceed TCY + 10 ns.

Note 1: The Period Measurement mode will produce valid results upon sampling of the second rising edge of the input capture. CAPxBUF values latched during the first active edge after initialization are invalid.

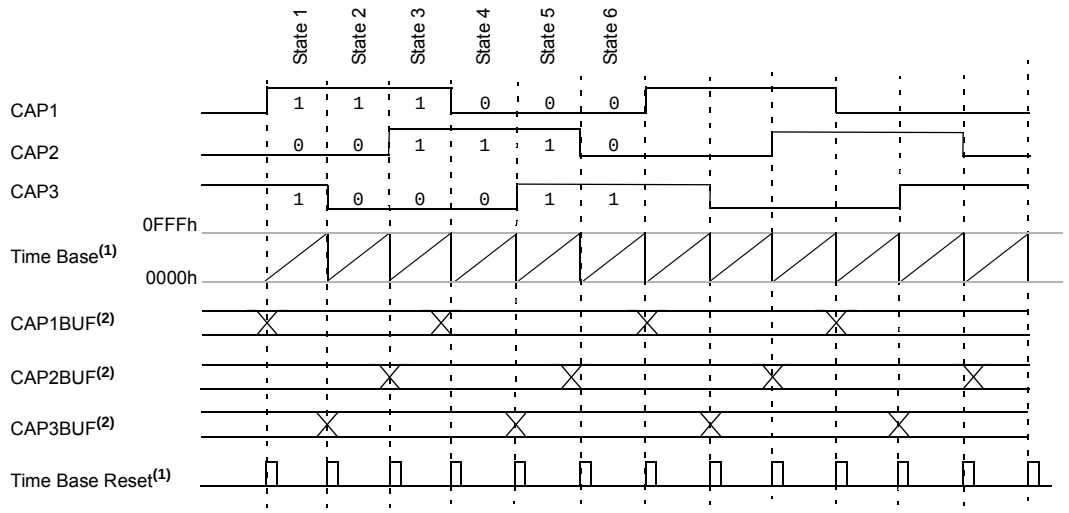
2: The Pulse-Width Measurement mode will latch the value of the timer upon sampling of the first input signal edge by the input capture.

17.1.4 INPUT CAPTURE ON STATE CHANGE

When CAPxM<3:0> = 1000, the value is captured on every signal change on the CAPx input. If all three capture channels are configured in this mode, the three input captures can be used as the Hall effect sensor state transition detector. The value of Timer5 can be captured, Timer5 reset and the interrupt generated. Any change on CAP1, CAP2 or CAP3 is detected and the associated time base count is captured.

For position and velocity measurement in this mode, the timer can be optionally reset (see **Section 17.1.6 "Timer5 Reset"** for Reset options).

FIGURE 17-6: INPUT CAPTURE ON STATE CHANGE (HALL EFFECT SENSOR MODE)



Note 1: TMR5 can be selected as the time base for input capture. The time base can be optionally reset when the Capture Reset Enable bit is set (CAPxREN = 1).

2: Detailed CAPxBUF event timing (all modes reflect the same capture and Reset timing) is shown in Figure 17-4. There are six commutation BLDC Hall effect sensor states shown. The other two remaining states (i.e., 000h and 111h) are invalid in the normal operation. They remain to be decoded by the CPU firmware in BLDC motor application.

Table 18-1 shows the minimum PWM frequencies that can be generated with the PWM time base and the prescaler. An operating frequency of 40 MHz (F_{CYC} = 10 MHz) and PTPER = 0xFFF is assumed in the table. The PWM module must be capable of generating PWM signals at the line frequency (50 Hz or 60 Hz) for certain power control applications.

TABLE 18-1: MINIMUM PWM FREQUENCY

Minimum PWM Frequencies vs. Prescaler Value for F_{CYC} = 10 MIPS (PTPER = 0FFFh)		
Prescale	**PWM Frequency Edge-Aligned**	**PWM Frequency Center-Aligned**
1:1	2441 Hz	1221 Hz
1:4	610 Hz	305 Hz
1:16	153 Hz	76 Hz
1:64	38 Hz	19 Hz

18.3.5 PWM TIME BASE POSTSCALER

The match output of PTMR can optionally be postscaled through a 4-bit postscaler (which gives a 1:1 to 1:16 scaling inclusive) to generate an interrupt. The postscaler counter is cleared when any of the following occurs:

- Write to the PTMR register
- Write to the PTCON register
- Any device Reset

The PTMR register is not cleared when PTCON is written.

18.4 PWM Time Base Interrupts

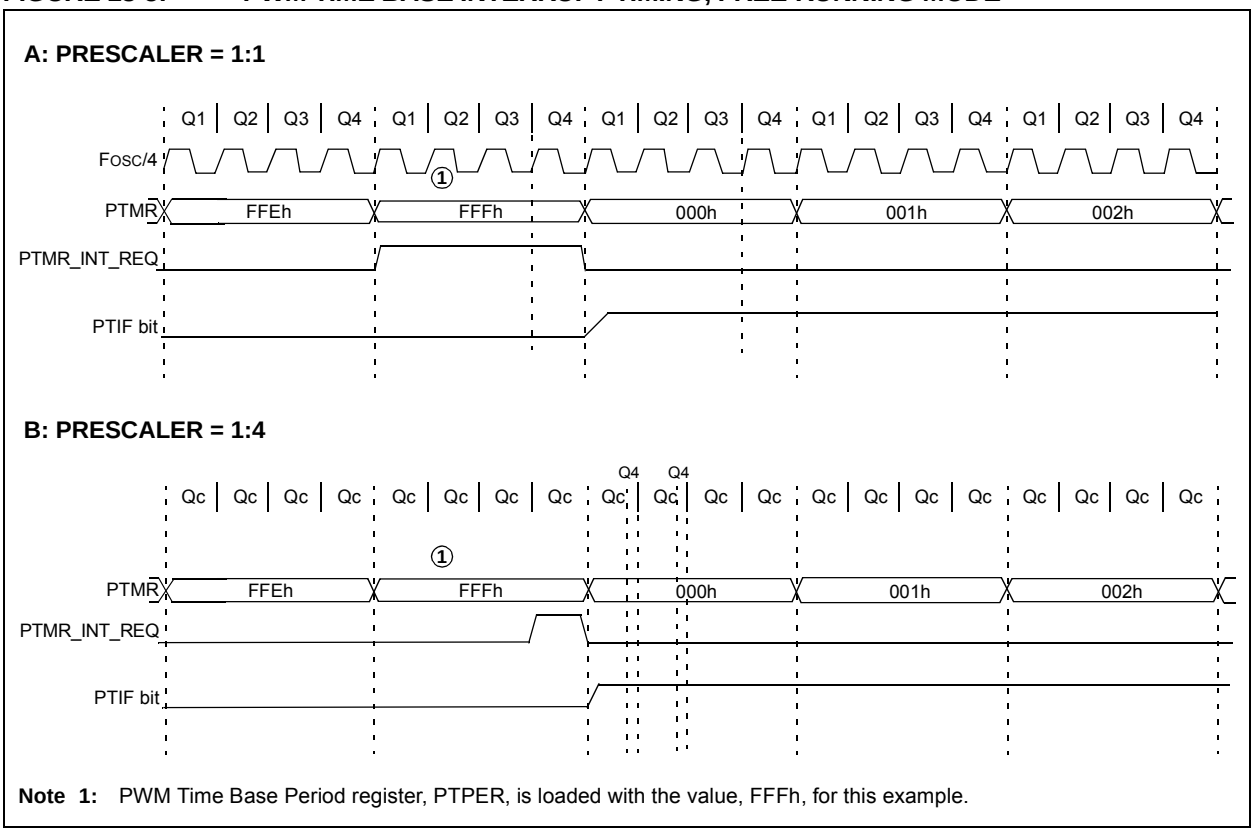
The PWM timer can generate interrupts based on the modes of operation selected by the PTMOD<1:0> bits and the postscaler bits (PTOPS<3:0>).

18.4.1 INTERRUPTS IN FREE-RUNNING MODE

When the PWM time base is in the Free-Running mode (PTMOD<1:0> = 00), an interrupt event is generated each time a match with the PTPER register occurs. The PTMR register is reset to zero in the following clock edge.

Using a postscaler selection other than 1:1 will reduce the frequency of interrupt events.

FIGURE 18-5: PWM TIME BASE INTERRUPT TIMING, FREE-RUNNING MODE



Note 1: PWM Time Base Period register, PTPER, is loaded with the value, FFFh, for this example.

21.0 10-BIT HIGH-SPEED ANALOG-TO-DIGITAL CONVERTER (A/D) MODULE

The high-speed Analog-to-Digital (A/D) Converter module allows conversion of an analog signal to a corresponding 10-bit digital number.

The A/D module supports up to 5 input channels on PIC18F2331/2431 devices, and up to 9 channels on the PIC18F4331/4431 devices.

This high-speed 10-bit A/D module offers the following features:

- Up to 200K samples per second
- Two sample and hold inputs for dual-channel simultaneous sampling
- Selectable Simultaneous or Sequential Sampling modes
- 4-word data buffer for A/D results
- Selectable data acquisition timing
- Selectable A/D event trigger
- Operation in Sleep using internal oscillator

These features lend themselves to many applications including motor control, sensor interfacing, data acquisition and process control. In many cases, these features will reduce the software overhead associated with standard A/D modules.

The module has 9 registers:

- A/D Result High Register (ADRESH)
- A/D Result Low Register (ADRESL)
- A/D Control Register 0 (ADCON0)
- A/D Control Register 1 (ADCON1)
- A/D Control Register 2 (ADCON2)
- A/D Control Register 3 (ADCON3)
- A/D Channel Select Register (ADCHS)
- Analog I/O Select Register 0 (ANSEL0)
- Analog I/O Select Register 1 (ANSEL1)

21.2 A/D Result Buffer

The A/D module has a 4-level result buffer with an address range of 0 to 3, enabled by setting the FIFOEN bit in the ADCON1 register. This buffer is implemented in a circular fashion, where the A/D result is stored in one location and the address is incremented. If the address is greater than 3, the pointer is wrapped back around to 0. The result buffer has a Buffer Empty Flag, BFEMT, indicating when any data is in the buffer. It also has a Buffer Overflow Flag, BFOVFL, which indicates when a new sample has overwritten a location that was not previously read.

Associated with the buffer is a pointer to the address for the next read operation. The ADPNT<1:0> bits configure the address for the next read operation. These bits are read-only.

The Result Buffer also has a configurable interrupt trigger level that is configured by the ADRS<1:0> bits. The user has three selections: interrupt flag set on every write to the buffer, interrupt on every second write to the buffer, or interrupt on every fourth write to the buffer. ADPNT<1:0> are reset to '00' every time a conversion sequence is started (either by setting the GO/DONE bit or on a trigger).

Note:	When right justified, reading ADRESL increments the ADPNT<1:0> bits. When left justified, reading ADRESH increments the ADPNT<1:0> bits.

21.3 A/D Acquisition Requirements

For the A/D Converter to meet its specified accuracy, the charge holding capacitor (CHOLD) must be allowed to fully charge to the input channel voltage level. The analog input model is shown in Figure 21-2. The source impedance (RS) and the internal sampling switch (RSS) impedance directly affect the time required to charge the capacitor CHOLD. The sampling switch (RSS) impedance varies over the device voltage (VDD). The source impedance affects the offset voltage at the analog input (due to pin leakage current). **The maximum recommended impedance for analog sources is 2.5 kΩ.** After the analog input channel is selected (changed), the channel must be sampled for at least the minimum acquisition time before starting a conversion.

Note:	When the conversion is started, the holding capacitor is disconnected from the input pin.

To calculate the minimum acquisition time, Equation 21-1 may be used. This equation assumes that 1/2 LSb error is used (1024 steps for the A/D). The 1/2 LSb error is the maximum error allowed for the A/D to meet its specified resolution.

Example 21-1 shows the calculation of the minimum required acquisition time TACQ. In this case, the converter module is fully powered up at the outset and therefore, the amplifier settling time, TAMP, is negligible. This calculation is based on the following application system assumptions:

CHOLD	=	9 pF
Rs	=	100Ω
Conversion Error	≤	1/2 LSb
VDD	=	5V → Rss = 6 kΩ
Temperature	=	50°C (system max.)
VHOLD	=	0V @ time = 0

EQUATION 21-1: ACQUISITION TIME

$$T_{ACQ} = \text{Amplifier Settling Time} + \text{Holding Capacitor Charging Time} + \text{Temperature Coefficient}$$
$$= T_{AMP} + T_C + T_{COFF}$$

EQUATION 21-2: MINIMUM A/D HOLDING CAPACITOR CHARGING TIME

$$V_{HOLD} = (V_{REF} - (V_{REF}/2048)) \bullet (1 - e^{(-T_C/C_{HOLD}(R_{IC} + R_{SS} + R_S))})$$
or
$$T_C = -(C_{HOLD})(R_{IC} + R_{SS} + R_S) \ln(1/2048)$$

26.1 DC Characteristics: Supply Voltage PIC18F2331/2431/4331/4431 (Industrial, Extended) PIC18LF2331/2431/4331/4431 (Industrial)

PIC18LF2331/2431/4331/4431 (Industrial)			**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial				
PIC18F2331/2431/4331/4431 (Industrial, Extended)			**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
D001	VDD	**Supply Voltage**					
		PIC18LF2X31/4X31	2.0	—	5.5	V	
		PIC18F2X31/4X31	4.2	—	5.5	V	
D001C	AVDD	**Analog Supply Voltage**	VDD – 0.3	—	VDD + 0.3	V	
D001D	AVSS	**Analog Ground Voltage**	VSS – 0.3	—	VSS + 0.3	V	
D002	VDR	**RAM Data Retention Voltage(1)**	1.5	—	—	V	
D003	VPOR	**VDD Start Voltage** to Ensure Internal Power-on Reset Signal	—	—	0.7	V	See section on Power-on Reset for details
D004	SVDD	**VDD Rise Rate** to Ensure Internal Power-on Reset Signal	0.05	—	—	V/ms	See section on Power-on Reset for details
D005A	VBOR	**Brown-out Reset Voltage**					
		PIC18LF2X31/4X31	Industrial Low Voltage (-10°C to +85°C)				
		BORV<1:0> = 11	N/A	N/A	N/A	V	Reserved
		BORV<1:0> = 10	2.50	2.72	2.94	V	
		BORV<1:0> = 01	3.88	4.22	4.56	V	
		BORV<1:0> = 00	4.18	4.54	4.90	V	
D005B		PIC18LF2X31/4X31	Industrial Low Voltage (-40°C to -10°C)				
		BORV<1:0> = 11	N/A	N/A	N/A	V	Reserved
		BORV<1:0>= 10	2.34	2.72	3.10	V	
		BORV<1:0> = 01	3.63	4.22	4.81	V	
		BORV<1:0> = 00	3.90	4.54	5.18	V	
D005C		PIC18F2X31/4X31	Industrial (-10°C to +85°C)				
		BORV<1:0>= 1x	N/A	N/A	N/A	V	Reserved
		BORV<1:0> = 01	3.88	4.22	4.56	V	**(Note 2)**
		BORV<1:0> = 00	4.18	4.54	4.90	V	**(Note 2)**
D005D		PIC18F2X31/4X31	Industrial (-40°C to -10°C)				
		BORV<1:0>= 1x	N/A	N/A	N/A	V	Reserved
		BORV<1:0> = 01	N/A	N/A	N/A	V	Reserved
		BORV<1:0> = 00	3.90	4.54	5.18	V	**(Note 2)**
D005E		PIC18F2X31/4X31	Extended (-10°C to +85°C)				
		BORV<1:0> = 1x	N/A	N/A	N/A	V	Reserved
		BORV<1:0> = 01	3.88	4.22	4.56	V	**(Note 2)**
		BORV<1:0> = 00	4.18	4.54	4.90	V	**(Note 2)**
D005F		PIC18F2X31/4X31	Extended (-40°C to -10°C, +85°C to +125°C)				
		BORV<1:0> = 1x	N/A	N/A	N/A	V	Reserved
		BORV<1:0> = 01	N/A	N/A	N/A	V	Reserved
		BORV<1:0> = 00	3.90	4.54	5.18	V	**(Note 2)**

Legend: Shading of rows is to assist in readability of the table.

Note 1: This is the limit to which VDD can be lowered in Sleep mode, or during a device Reset, without losing RAM data.

2: When BOR is on and BORV<1:0> = 0x, the device will operate correctly at 40 MHz for any VDD at which the BOR allows execution.

FIGURE 26-3: LOW-VOLTAGE DETECT CHARACTERISTICS

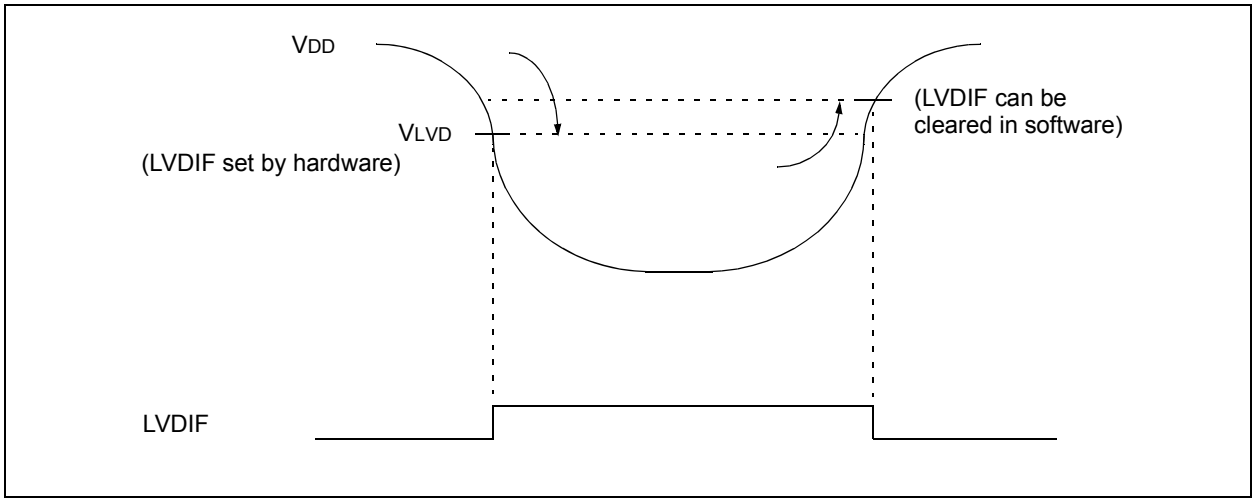


TABLE 26-2: LOW-VOLTAGE DETECT CHARACTERISTICS

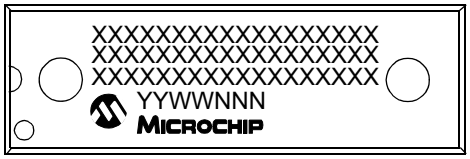
PIC18LF2331/2431/4331/4431 (Industrial)				**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial				
PIC18F2331/2431/4331/4431 (Industrial, Extended)				**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
Param No.	**Symbol**	**Characteristic**		**Min**	**Typ†**	**Max**	**Units**	**Conditions**
D420A	VLVD	LVD Voltage on VDD Transition High-to-Low		Industrial Low Voltage (-10°C to +85°C)				
		PIC18LF2X31/4X31	LVDL<3:0> = 0000	N/A	N/A	N/A	V	Reserved
			LVDL<3:0> = 0001	N/A	N/A	N/A	V	Reserved
			LVDL<3:0> = 0010	2.08	2.26	2.44	V	
			LVDL<3:0> = 0011	2.26	2.45	2.65	V	
			LVDL<3:0> = 0100	2.35	2.55	2.76	V	
			LVDL<3:0> = 0101	2.55	2.77	2.99	V	
			LVDL<3:0> = 0110	2.64	2.87	3.10	V	
			LVDL<3:0> = 0111	2.82	3.07	3.31	V	
			LVDL<3:0> = 1000	3.09	3.36	3.63	V	
			LVDL<3:0> = 1001	3.29	3.57	3.86	V	
			LVDL<3:0> = 1010	3.38	3.67	3.96	V	
			LVDL<3:0> = 1011	3.56	3.87	4.18	V	
			LVDL<3:0> = 1100	3.75	4.07	4.40	V	
			LVDL<3:0> = 1101	3.93	4.28	4.62	V	
			LVDL<3:0> = 1110	4.23	4.60	4.96	V	

Legend: Shading of rows is to assist in readability of the table.

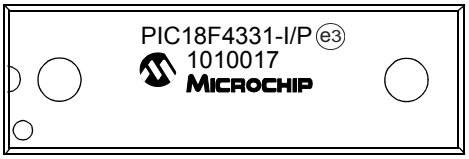
† Production tested at TAMB = 25°C. Specifications over temperature limits ensured by characterization.

27.1 Package Marking Information (Continued)

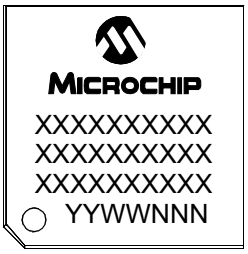
40-Lead PDIP



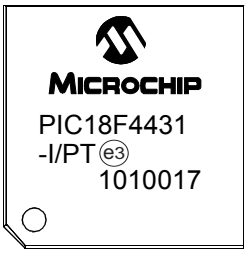
Example



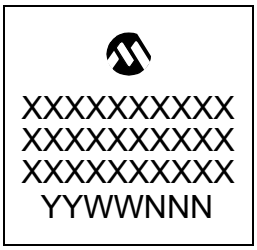
44-Lead TQFP



Example



44-Lead QFN



Example