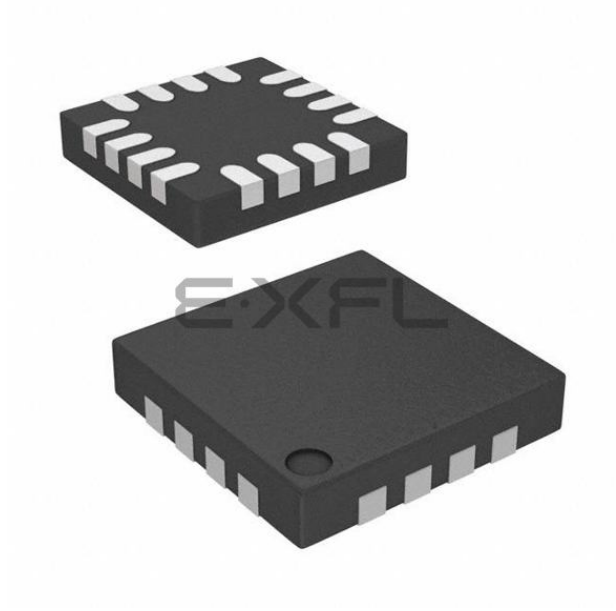


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	M8C
Core Size	8-Bit
Speed	12MHz
Connectivity	I²C, SPI
Peripherals	LVD, POR, WDT
Number of I/O	13
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.25V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	16-UFQFN
Supplier Device Package	16-QFN (3x3)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c20234-12lkxit

More Information

Cypress provides a wealth of data at www.cypress.com to help you to select the right PSoC device for your design, and to help you to quickly and effectively integrate the device into your design. For a comprehensive list of resources, see the knowledge base article KBA92181, Resources Available for CapSense® Controllers. Following is an abbreviated list for CapSense devices:

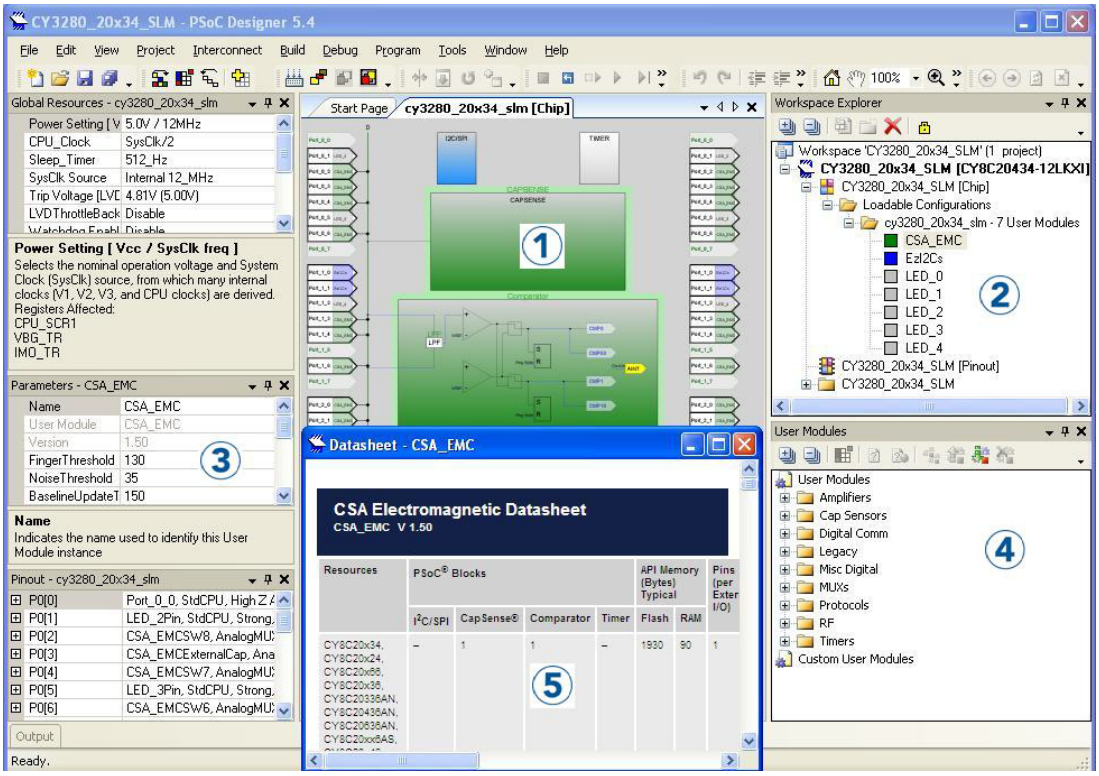
- Overview: CapSense Portfolio, CapSense Roadmap
- Product Selectors: CapSense, CapSense Plus, CapSense Express, PSoC3 with CapSense, PSoC5 with CapSense, PSoC4. In addition, PSoC Designer offers a device selection tool at the time of creating a new project.
- Application Notes: Cypress offers CapSense application notes covering a broad range of topics, from basic to advanced level. Recommended application notes for getting started with CapSense are:
  - AN64846 – Getting Started With CapSense
  - CY8C20x34 CapSense® Design Guide
  - AN2397 – CapSense® Data Viewing Tools
- Technical Reference Manual (TRM):
  - PSoC® CY8C20x24, CY8C20x34 Family Technical Reference Manual
- Development Kits:
  - CY3280-20x34 Universal CapSense Controller Kit features a predefined control circuitry and plug-in hardware to make prototyping and debugging easy. Programming and I2C-to-USB Bridge hardware are included for tuning and data acquisition.
  - CY3280-SLM Linear Slider Module Kit consists of five CapSense buttons, one linear slider (with ten sensors) and five LEDs. This module connects to any CY3280 Universal CapSense Controller Board, including CY3280-20x34 kit.
  - CY3280-BBM Universal CapSense Prototyping Module Kit provides access to every signal routed to the 44-pin connector on the attached controller board including CY3280-20x34 kit.
- Programming
  - PSoC supports a number of different programming modes and tools. For more information see the General Programming page.

PSoC Designer

PSoC Designer is a free Windows-based Integrated Design Environment (IDE). It enables concurrent hardware and firmware design of systems based on CapSense (see Figure 1). With PSoC Designer, you can:

1. Drag and drop User Modules to build your hardware system design in the main design workspace
2. Codesign your application firmware with the PSoC hardware, using the PSoC Designer IDE C compiler
3. Configure User Module
4. Explore the library of user modules
5. Review user module datasheets

Figure 1. PSoC Designer Features



Getting Started

For in-depth information, along with detailed programming details, see the *PSoC® Technical Reference Manual*.

For up-to-date ordering, packaging, and electrical specification information, see the latest PSoC device datasheets on the web.

Application Notes

Cypress application notes are an excellent introduction to the wide variety of possible PSoC designs.

Development Kits

PSoC Development Kits are available online from and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark.

Training

Free PSoC technical training (on demand, webinars, and workshops), which is available online via www.cypress.com, covers a wide variety of topics and skill levels to assist you in your designs.

CYPros Consultants

Certified PSoC consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC consultant go to the CYPros Consultants web site.

Solutions Library

Visit our growing library of solution focused designs. Here you can find various application designs that include firmware and hardware design files that enable you to complete your designs quickly.

Technical Support

Technical support – including a searchable Knowledge Base articles and technical forums – is also available online. If you cannot find an answer to your question, call our Technical Support hotline at 1-800-541-4736.

Designing with PSoC Designer

The development process for the PSoC device differs from that of a traditional fixed function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and by lowering inventory costs. These configurable resources, called PSoC Blocks, have the ability to implement a wide variety of user-selectable functions. The PSoC development process is summarized in four steps:

1. Select User Modules.
2. Configure User Modules.
3. Organize and Connect.
4. Generate, Verify, and Debug.

Select User Modules

PSoC Designer provides a library of prebuilt, pretested hardware peripheral components called “user modules.” User modules make selecting and implementing peripheral devices, both analog and digital, simple.

Configure User Modules

Each user module that you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. For example, a PWM User Module configures one or more digital PSoC blocks, one for each 8 bits of resolution. The user module parameters permit you to establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus. All the user modules are documented in datasheets that may be viewed directly in PSoC Designer or on the Cypress website. These user module datasheets explain the internal operation of the user module and provide performance specifications. Each datasheet describes the use of each user module parameter, and other information you may need to successfully implement your design.

Organize and Connect

You build signal chains at the chip level by interconnecting user modules to each other and the I/O pins. You perform the selection, configuration, and routing so that you have complete control over all on-chip resources.

Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, you perform the “Generate Configuration Files” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system. The generated code provides application programming interfaces (APIs) with high-level functions to control and respond to hardware events at run-time and interrupt service routines that you can adapt as needed.

A complete code development environment allows you to develop and customize your applications in either C, assembly language, or both.

The last step in the development process takes place inside PSoC Designer’s debugger (access by clicking the Connect icon). PSoC Designer downloads the HEX image to the ICE where it runs at full speed. PSoC Designer debugging capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint, and watch-variable features, the debug interface provides a large trace buffer and allows you to define complex breakpoint events. These include monitoring address and data bus values, memory locations, and external signals.

16-Pin SOIC Pinout

Figure 4. CY8C20234-12SXI 16-Pin SOIC Pinout

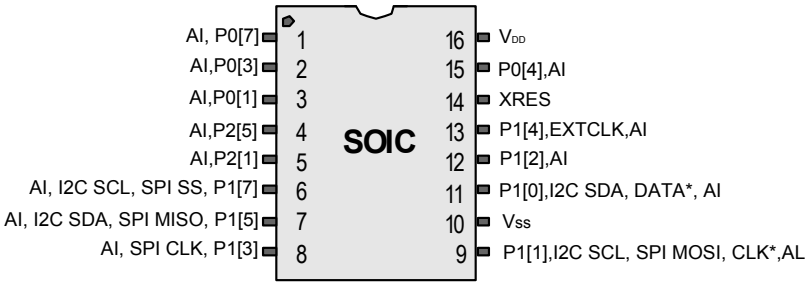


Table 3. Pin Definitions – CY8C20234 16-Pin (SOIC)

Pin No.	Digital	Analog	Name	Description
1	I/O	I	P0[7]	Analog column mux input
2	I/O	I	P0[3]	Analog column mux input and column input, integrating input
3	I/O	I	P0[1]	Analog column mux input, integrating input
4	I/O	I	P2[5]	Analog column mux input
5	I/O	I	P2[1]	Analog column mux input
6	I/O	I	P1[7]	I2C serial clock (SCL), SPI SS
7	I/O	I	P1[5]	I2C serial data (SDA),SPI MISO
8	I/O	I	P1[3]	Analog column mux input, SPI CLK
9	I/O	I	P1[1]	I2C serial clock (SCL), ISSP-SCLK,SPI MOSI
10	Power		V_{SS}	Ground connection
11	I/O	I	P1[0]	I2C serial data (SDA), ISSP-SDATA
12	I/O	I	P1[2]	Analog column mux input
13	I/O	I	P1[4]	Analog column mux input, optional external clock input (EXTCLK)
14	I/O	I	XRES	XRES
15	I/O	I	P0[4]	Analog column mux input
16	Power		V_{DD}	Supply voltage

A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive.

48-Pin OCD Part Pinout

The 48-Pin QFN part table and pin diagram is for the CY8C20000 On-Chip Debug (OCD) PSoC device. This part is only used for in-circuit debugging. It is NOT available for production.

Figure 5. CY8C20000 48-Pin OCD PSoC Device

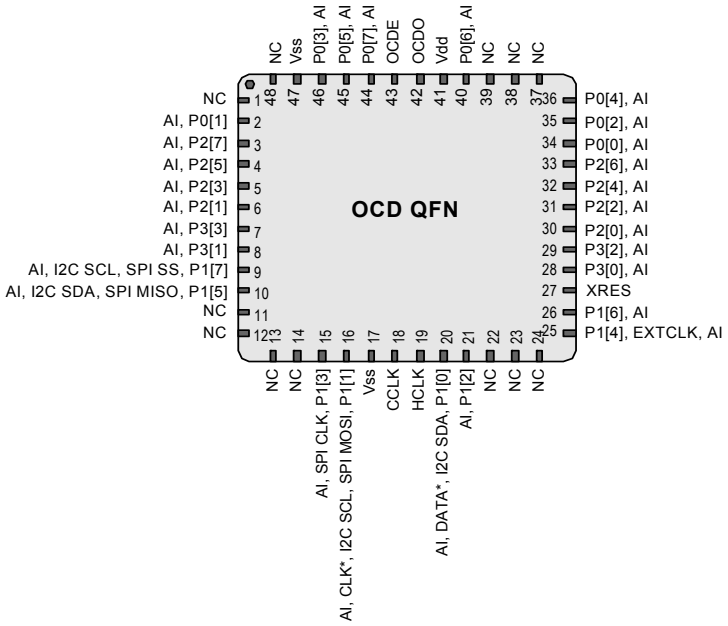


Table 4. Pin Definitions – CY8C20000 48-Pin OCD (QFN) [3]

Pin No.	Digital	Analog	Name	Description
1			NC	No connection
2	I/O	I	P0[1]	
3	I/O	I	P2[7]	
4	I/O	I	P2[5]	
5	I/O	I	P2[3]	
6	I/O	I	P2[1]	
7	I/O	I	P3[3]	
8	I/O	I	P3[1]	
9	I_{OH}	I	P1[7]	I^2C SCL, SPI SS
10	I_{OH}	I	P1[5]	I^2C SDA, SPI MISO
11	I/O	I	P0[1]	
12			NC	No connection
13			NC	No Connection
14			NC	No Connection
15			NC	SPI CLK
16	I_{OH}	I	P1[3]	CLK[4], I^2C SCL, SPI MOSI
17	I_{OH}	I	P1[1]	Ground connection

Notes
3. The center pad on the QFN package is connected to ground (V_{SS}) for best mechanical, thermal, and electrical performance. If not connected to ground, it is electrically floated and not connected to any other signal.
4. These are the ISSP pins, that are not High Z at POR (Power-on-Reset). See the *PSoC Technical Reference Manual* for details.

24-Pin Part Pinout

Figure 7. CY8C20334 24-Pin PSoC Device

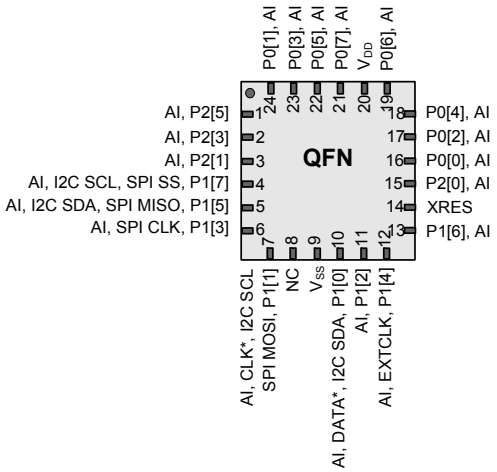


Table 6. Pin Definitions – CY8C20334 24-Pin (QFN) [7]

Pin No.	Type		Name	Description
	Digital	Analog		
1	I/O	I	P2[5]	
2	I/O	I	P2[3]	
3	I/O	I	P2[1]	
4	I_{OH}	I	P1[7]	I^2C SCL, SPI SS
5	I_{OH}	I	P1[5]	I^2C SDA, SPI MISO
6	I_{OH}	I	P1[3]	SPI CLK
7	I_{OH}	I	P1[1]	CLK[8], I^2C SCL, SPI MOSI
8			NC	No Connection
9	Power		V_{SS}	Ground Connection
10	I_{OH}	I	P1[0]	DATA[8], I^2C SDA
11	I_{OH}	I	P1[2]	
12	I_{OH}	I	P1[4]	Optional external clock input (EXTCLK)
13	I_{OH}	I	P1[6]	
14	Input		XRES	Active high external reset with internal pull-down
15	I/O	I	P2[0]	
16	I/O	I	P0[0]	
17	I/O	I	P0[2]	
18	I/O	I	P0[4]	
19	I/O	I	P0[6]	Analog bypass
20	Power		V_{DD}	Supply voltage
21	I/O	I	P0[7]	
22	I/O	I	P0[5]	
23	I/O	I	P0[3]	Integrating input
24	I/O	I	P0[1]	
CP	Power		V_{SS}	Center pad is connected to ground

A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive

Notes
7. The center pad on the QFN package is connected to ground (V_{SS}) for best mechanical, thermal, and electrical performance. If not connected to ground, it is electrically floated and not connected to any other signal.
8. These are the ISSP pins, that are not High Z at POR (Power-on-Reset). See the *PSoC Technical Reference Manual* for details.

Table 7. Pin Definitions – CY8C20434 32-Pin (QFN) [9]

Pin No.	Type		Name	Description
	Digital	Analog		
18	I/O	I	P3[0]	
19	I/O	I	P3[2]	
20	I/O	I	P2[0]	
21	I/O	I	P2[2]	
22	I/O	I	P2[4]	
23	I/O	I	P2[6]	
24	I/O	I	P0[0]	
25	I/O	I	P0[2]	
26	I/O	I	P0[4]	
27	I/O	I	P0[6]	Analog bypass
28	Power		V_{DD}	Supply voltage
29	I/O	I	P0[7]	
30	I/O	I	P0[5]	
31	I/O	I	P0[3]	Integrating input
32	Power		V_{SS}	Ground connection[12]
CP	Power		V_{SS}	Center pad is connected to ground

A = Analog, I = Input, O = Output, OH = 5 mA high output drive.

Note
12. All V_{SS} pins should be brought out to one common GND plane.

28-Pin Part Pinout

Figure 9. CY8C20534 28-Pin PSoC Device

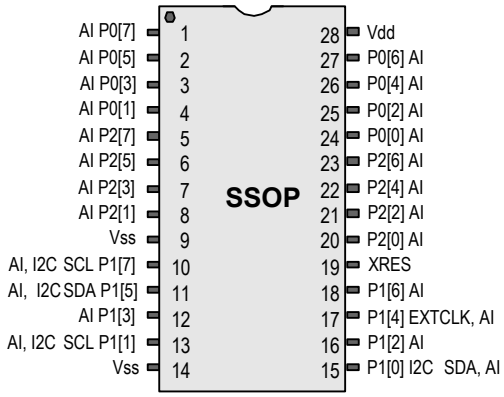


Table 8. Pin Definitions – CY8C20534 28-Pin (SSOP)

Pin No.	Type		Name	Description
	Digital	Analog		
1	I/O	I	P0[7]	Analog column mux input
2	I/O	I	P0[5]	Analog column mux input and column output
3	I/O	I	P0[3]	Analog column mux input and column output, integrating input
4	I/O	I	P0[1]	Analog column mux input, integrating input
5	I/O	I	P2[7]	
6	I/O	I	P2[5]	
7	I/O	I	P2[3]	Direct switched capacitor block input
8	I/O	I	P2[1]	Direct switched capacitor block input
9	Power		V_{SS}	Ground connection[13]
10	I/O	I	P1[7]	I2C serial clock (SCL)
11	I/O	I	P1[5]	I2C serial data (SDA)
12	I/O	I	P1[3]	
13	I/O	I	P1[1]	I2C serial clock (SCL), ISSP-SCLK[14]
14	Power		V_{SS}	Ground connection
15	I/O	I	P1[0]	I2C serial data (SDA), ISSP-SDATA[14]
16	I/O	I	P1[2]	
17	I/O	I	P1[4]	Optional external clock input (EXTCLK)
18	I/O	I	P1[6]	
19	Input		XRES	Active high external reset with internal pull-down
20	I/O	I	P2[0]	Direct switched capacitor block input
21	I/O	I	P2[2]	Direct switched capacitor block input
22	I/O	I	P2[4]	
23	I/O	I	P2[6]	
24	I/O	I	P0[0]	Analog column mux input
25	I/O	I	P0[2]	Analog column mux input
26	I/O	I	P0[4]	Analog column mux input
27	I/O	I	P0[6]	Analog column mux input
28	Power		V_{DD}	Supply voltage

A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive.

Notes
13. All V_{SS} pins should be brought out to one common GND plane.
14. These are the ISSP pins, that are not High Z at POR (Power-on-Reset). See the *PSoC Technical Reference Manual* for details.

30-Ball Part Pinout

Figure 10. CY8C20634 30-Ball PSoC Device

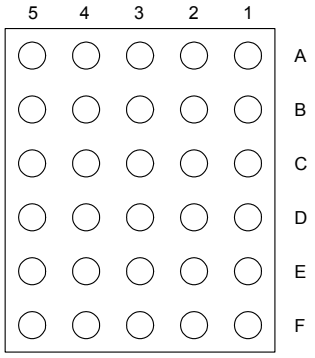


Table 9. 30-Ball Part Pinout (WLCSP)

Pin No.	Type		Name	Description
	Digital	Analog		
A1	Power		V_{DD}	Supply voltage
A2	I/O	I	P0[6]	Analog bypass
A3	I/O	I	P0[4]	
A4	I/O	I	P0[3]	Integrating input
A5	I/O	I	P2[7]	
B1	I/O	I	P0[2]	
B2	I/O	I	P0[0]	
B3	I/O	I	P2[6]	
B4	I/O	I	P0[5]	
B5	I/O	I	P0[1]	
C1	I/O	I	P2[4]	
C2	I/O	I	P2[2]	
C3	I/O	I	P3[1]	
C4	I/O	I	P0[7]	
C5	I/O	I	P2[1]	
D1	I/O	I	P2[0]	
D2	I/O	I	P3[0]	
D3	I/O	I	P3[2]	
D4	I_{OH}	I	P1[1]	CLK[15], I^2C SCL, SPI MOSI
D5	I/O	I	P2[3]	
E1	Input		XRES	Active high external reset with internal pull-down
E2	I_{OH}	I	P1[6]	
E3	I_{OH}	I	P1[4]	Optional external clock input (EXTCLK)
E4	I_{OH}	I	P1[5]	I^2C SDA, SPI MISO
E5	I/O	I	P2[5]	
F1	Power		V_{SS}	Ground connection[16]
F2	I_{OH}	I	P1[2]	
F3	I_{OH}	I	P1[0]	DATA[15], I^2C SDA
F4	I_{OH}	I	P1[3]	SPI CLK
F5	I_{OH}	I	P1[7]	I^2C SCL, SPI SS

A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive.

Notes
15. These are the ISSP pins, that are not High Z at POR (Power-on-Reset). See the *PSoC Technical Reference Manual* for details.
16. All V_{SS} pins should be brought out to one common GND plane.

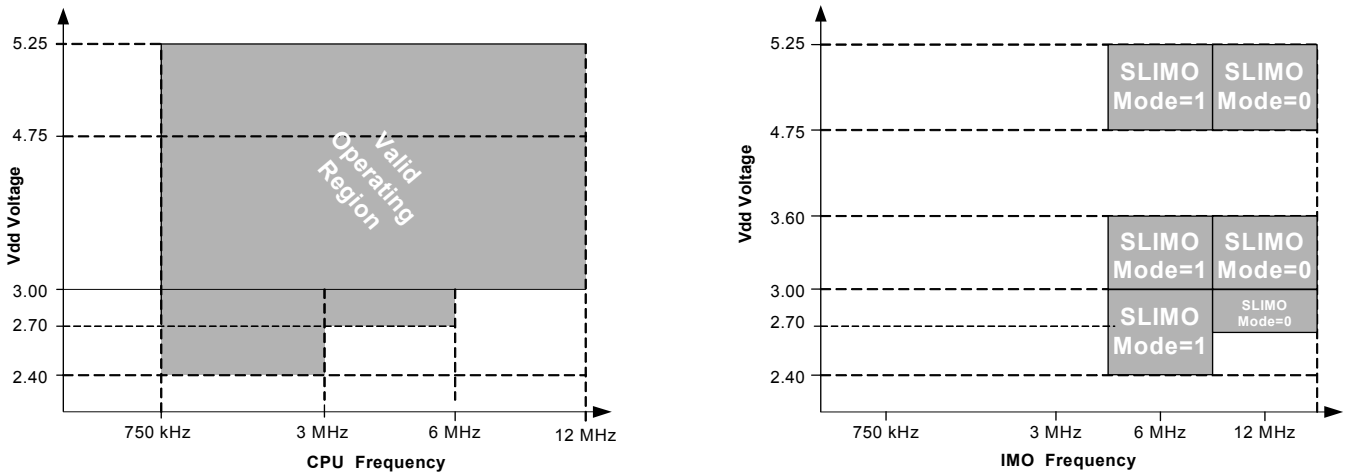
Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8C20234, CY8C20334, CY8C20434, CY8C20534, and CY8C20634 PSoC devices. For the latest electrical specifications, check the most recent datasheet by visiting the web at http://www.cypress.com.

Specifications are valid for –40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C as specified, except where mentioned.

Refer to Table 19 on page 25 for the electrical specifications on the internal main oscillator (IMO) using SLIMO mode.

Figure 11. Voltage versus CPU Frequency and IMO Frequency Trim Options



Absolute Maximum Ratings

Table 10. Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Units	Notes
T_{STG}	Storage Temperature	–55	25	+100	°C	Higher storage temperatures reduces data retention time. Recommended storage temperature is +25 °C ± 25 °C. Extended duration storage temperatures above 65 °C degrades reliability.
$T_{BAKETEMP}$	Bake temperature	–	125	See package label	°C	
$t_{BAKETIME}$	Bake time	See package label	–	72	Hours	
T_A	Ambient temperature with power applied	–40	–	+85	°C	
V_{DD}	Supply voltage on V_{DD} relative to V_{SS}	–0.5	–	+6.0	V	
V_{IO}	DC input voltage	V_{SS} – 0.5	–	V_{DD} + 0.5	V	
V_{IOZ}	DC voltage applied to tri-state	V_{SS} – 0.5	–	V_{DD} + 0.5	V	
I_{MIO}	Maximum current into any port pin	–25	–	+50	mA	
ESD	Electro static discharge voltage	2000	–	–	V	Human body model ESD.
LU	Latch-up current	–	–	200	mA	

Operating Temperature

Table 11. Operating Temperature

Symbol	Description	Min	Typ	Max	Units	Notes
T_A	Ambient temperature	–40	–	+85	°C	
T_J	Junction temperature	–40	–	+100	°C	The temperature rise from ambient to junction is package specific. See Table 16 on page 23. The user must limit the power consumption to comply with this requirement.

DC Electrical Characteristics

DC Chip Level Specifications

Table 12 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0V to 3.6V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C. These are for design guidance only.

Table 12. DC Chip Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{DD}	Supply voltage	2.40	–	5.25	V	See Table 16 on page 23.
I_{DD12}	Supply current, IMO = 12 MHz	–	1.5	2.5	mA	Conditions are V_{DD} = 3.0 V, T_A = 25 °C, CPU = 12 MHz.
I_{DD6}	Supply current, IMO = 6 MHz	–	1	1.5	mA	Conditions are V_{DD} = 3.0 V, T_A = 25 °C, CPU = 6 MHz
I_{SB27}	Sleep (mode) current with POR, LVD, Sleep timer, WDT, and internal slow oscillator active. Mid temperature range.	–	2.6	4	µA	V_{DD} = 2.55 V, 0 °C ≤ T_A ≤ 40 °C
I_{SB}	Sleep (mode) current with POR, LVD, Sleep timer, WDT, and internal slow oscillator active.	–	2.8	5	µA	V_{DD} = 3.3 V, –40 °C ≤ T_A ≤ 85 °C

DC GPIO Specifications

Unless otherwise noted, Table 13 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or Table 14 for 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V, 3.3 V, and 2.7 V at 25 °C. These are for design guidance only.

Table 13. 5-V and 3.3-V DC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{PU}	Pull-up resistor	4	5.6	8	kΩ	
V_{OH1}	High output voltage Port 0, 2, or 3 pins	V_{DD} – 0.2	–	–	V	I_{OH} ≤ 10 µA, V_{DD} ≥ 3.0 V, maximum of 20 mA source current in all I/Os.
V_{OH2}	High output voltage Port 0, 2, or 3 pins	V_{DD} – 0.9	–	–	V	I_{OH} = 1 mA, V_{DD} ≥ 3.0 V, maximum of 20 mA source current in all I/Os.
V_{OH3}	High output voltage Port 1 pins with LDO regulator disabled	V_{DD} – 0.2	–	–	V	I_{OH} < 10 µA, V_{DD} ≥ 3.0 V, maximum of 10 mA source current in all I/Os.
V_{OH4}	High output voltage Port 1 pins with LDO regulator disabled	V_{DD} – 0.9	–	–	V	I_{OH} = 5 mA, V_{DD} ≥ 3.0 V, maximum of 20 mA source current in all I/Os.
V_{OH5}	High output voltage Port 1 pins with 3.0 V LDO regulator enabled	2.7	3.0	3.3	V	I_{OH} < 10 µA, V_{DD} ≥ 3.1 V, maximum of 4 I/Os all sourcing 5 mA.
V_{OH6}	High output voltage Port 1 pins with 3.0 V LDO regulator enabled	2.2	–	–	V	I_{OH} = 5 mA, V_{DD} ≥ 3.1 V, maximum of 20 mA source current in all I/Os.

DC POR and LVD Specifications

Table 16 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively.
Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C. These are for design guidance only.

Table 16. DC POR and LVD Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
	V_{DD} value for PPOR trip					V_{DD} is greater than or equal to 2.5 V during startup, reset from the XRES pin, or reset from watchdog.
V_{PPOR0}	PORLEV[1:0] = 00b	–	2.36	2.40	V	
V_{PPOR1}	PORLEV[1:0] = 01b	–	2.60	2.65	V	
V_{PPOR2}	PORLEV[1:0] = 10b	–	2.82	2.95	V	
	V_{DD} value for LVD trip					
V_{LVD0}	VM[2:0] = 000b	2.39	2.45	2.51[17]	V	
V_{LVD1}	VM[2:0] = 001b	2.54	2.71	2.78[18]	V	
V_{LVD2}	VM[2:0] = 010b	2.75	2.92	2.99[19]	V	
V_{LVD3}	VM[2:0] = 011b	2.85	3.02	3.09	V	
V_{LVD4}	VM[2:0] = 100b	2.96	3.13	3.20	V	
V_{LVD5}	VM[2:0] = 101b	–	–	–	V	
V_{LVD6}	VM[2:0] = 110b	–	–	–	V	
V_{LVD7}	VM[2:0] = 111b	4.52	4.73	4.83	V	

Notes
17. Always greater than 50 mV above V_{PPOR} (PORLEV = 00) for falling supply.
18. Always greater than 50 mV above V_{PPOR} (PORLEV = 01) for falling supply.
19. Always greater than 50 mV above V_{PPOR} (PORLEV = 10) for falling supply.

DC I²C Specifications

Table 18 lists the guaranteed minimum and maximum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C. These are for design guidance only. Flash endurance and retention specifications with the use of the EEPROM user module are valid only within the range: 25 °C +/–20C during the Flash Write operation. Reference the EEPROM User Module datasheet instructions for EEPROM flash Write requirements outside of the 25 °C +/–20 °C temperature window.

Table 18. DC I²C Specifications[22]

Symbol	Description	Min	Typ	Max	Units	Notes
V_{ILI2C}	Input low level	–	–	0.3 × V_{DD}	V	2.4 V ≤ V_{DD} ≤ 3.6 V
		–	–	0.25 × V_{DD}	V	4.75 V ≤ V_{DD} ≤ 5.25 V
V_{IHI2C}	Input high level	0.7 × V_{DD}	–	–	V	2.4 V ≤ V_{DD} ≤ 5.25 V

AC Electrical Characteristics

AC Chip Level Specifications

Table 19, Table 20, and Table 21 list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C. These are for design guidance only.

Table 19. 5-V and 3.3-V AC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{CPU1}	CPU frequency (3.3 V nominal)	0.75	–	12.6	MHz	12 MHz only for SLIMO Mode = 0.
F_{32K1}	Internal low speed oscillator frequency	15	32	64	kHz	
F_{32K_U}	Internal low speed oscillator (ILO) untrimmed frequency	5	–	100	kHz	After a reset and before the M8C starts to run, the ILO is not trimmed. See the System Resets section of the PSoC Technical Reference Manual for details on this timing.
F_{IMO12}	Internal main oscillator stability for 12 MHz (commercial temperature)[23]	11.4	12	12.6	MHz	Trimmed for 3.3 V operation using factory trim values. See Figure 11 on page 19, SLIMO mode = 0.
F_{IMO6}	Internal main oscillator stability for 6 MHz (commercial temperature)	5.5	6.0	6.5	MHz	Trimmed for 3.3 V operation using factory trim values. See Figure 11 on page 19, SLIMO mode = 1.
DC_{IMO}	Duty cycle of IMO	40	50	60	%	
DC_{ILO}	Internal low speed oscillator duty cycle	20	50	80	%	
t_{XRST}	External reset pulse width	10	–	–	µs	
$t_{POWERUP}$	Time from end of POR to CPU executing code	–	16	100	ms	Power-up from 0 V. See the System Resets section of the PSoC Technical Reference Manual.
SR_{POWER_UP}	Power supply slew rate	–	–	250	V/ms	
t_{jit_IMO} [24]	12 MHz IMO cycle-to-cycle jitter (RMS)	–	200	1600	ps	
	12 MHz IMO long term N cycle-to-cycle jitter (RMS)	–	600	1400	ps	N = 32
	12 MHz IMO period jitter (RMS)	–	100	900	ps	

Notes
22. All GPIO meet the DC GPIO V_{IL} and V_{IH} specifications found in the DC GPIO Specifications sections. The I²C GPIO pins also meet the above specs.
23. 0 to 70 °C ambient, V_{DD} = 3.3 V.
24. Refer to Cypress Jitter Specifications Application Note – AN5054 at http://www.cypress.com for more information.

Table 20. 2.7-V AC Chip Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{CPU1}	CPU Frequency (2.7 V nominal)	0.75	–	3.25	MHz	SLIMO mode = 0
F_{32K1}	Internal low speed oscillator frequency	8	32	96	kHz	
F_{32K_U}	Internal low speed oscillator (ILO) untrimmed frequency	5	–	100	kHz	After a reset and before the M8C starts to run, the ILO is not trimmed. See the System Resets section of the PSoC Technical Reference Manual for details on this timing.
F_{IMO12}	IMO stability for 12 MHz (commercial temperature)[25]	11.0	12	12.9	MHz	Trimmed for 2.7 V operation using factory trim values. See Figure 11 on page 19, SLIMO mode = 0.
F_{IMO6}	IMO stability for 6 MHz (commercial temperature)	5.5	6.0	6.5	MHz	Trimmed for 2.7 V operation using factory trim values. See Figure 11 on page 19, SLIMO mode = 1.
DC_{IMO}	Duty cycle of IMO	40	50	60	%	
DC_{ILO}	Internal low speed oscillator duty cycle	20	50	80	%	
t_{XRST}	External reset pulse width	10	–	–	µs	
$t_{POWERUP}$	Time from end of POR to CPU executing code	–	16	100	ms	Power-up from 0 V. See the System Resets section of the PSoC Technical Reference Manual
SR_{POWER_UP}	Power supply slew rate	–	–	250	V/ms	
t_{JIT_IMO} [26]	12 MHz IMO cycle-to-cycle jitter (RMS)	–	500	900	ps	
	12 MHz IMO long term N cycle-to-cycle jitter (RMS)	–	800	1400	ps	N = 32
	12 MHz IMO period jitter (RMS)	–	300	500	ps	

Notes
25. 0 °C to 70 °C ambient, V_{DD} = 3.3 V.
26. Refer to Cypress Jitter Specifications Application Note – AN5054 at http://www.cypress.com for more information.

AC External Clock Specifications

Table 24, Table 25, Table 26, and Table 27 list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C. These are for design guidance only.

Table 24. 5-V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{OSCEXT}	Frequency	0.750	–	12.6	MHz	
–	High period	38	–	5300	ns	
–	Low period	38	–	–	ns	
–	Power-up IMO to switch	150	–	–	µs	

Table 25. 3.3-V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{OSCEXT}	Frequency with CPU clock divide by 1	0.750	–	12.6	MHz	Maximum CPU frequency is 12 MHz at 3.3 V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements.
–	High period with CPU clock divide by 1	41.7	–	5300	ns	
–	Low period with CPU clock divide by 1	41.7	–	–	ns	
–	Power-up IMO to switch	150	–	–	µs	

Table 26. 2.7-V (Nominal) AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{OSCEXT}	Frequency with CPU clock divide by 1	0.750	–	3.08	MHz	Maximum CPU frequency is 3 MHz at 2.7 V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements.
F_{OSCEXT}	Frequency with CPU clock divide by 2 or greater	0.15	–	6.35	MHz	If the frequency of the external clock is greater than 3 MHz, the CPU clock divider is set to 2 or greater. In this case, the CPU clock divider ensures that the fifty percent duty cycle requirement is met.
–	High period with CPU clock divide by 1	160	–	5300	ns	
–	Low period with CPU clock divide by 1	160	–	–	ns	
–	Power-up IMO to switch	150	–	–	µs	

Table 27. 2.7-V (Minimum) AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{OSCEXT}	Frequency with CPU clock divide by 1	0.750	–	6.3	MHz	Maximum CPU frequency is 6 MHz at 2.7 V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements.
F_{OSCEXT}	Frequency with CPU clock divide by 2 or greater	0.15	–	12.6	MHz	If the frequency of the external clock is greater than 6 MHz, the CPU clock divider is set to 2 or greater. In this case, the CPU clock divider ensures that the fifty percent duty cycle requirement is met.
–	High period with CPU clock divide by 1	160	–	5300	ns	
–	Low period with CPU clock divide by 1	160	–	–	ns	
–	Power-up IMO to switch	150	–	–	µs	

AC SPI Specifications

Table 31 and Table 32 list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C. These are for design guidance only.

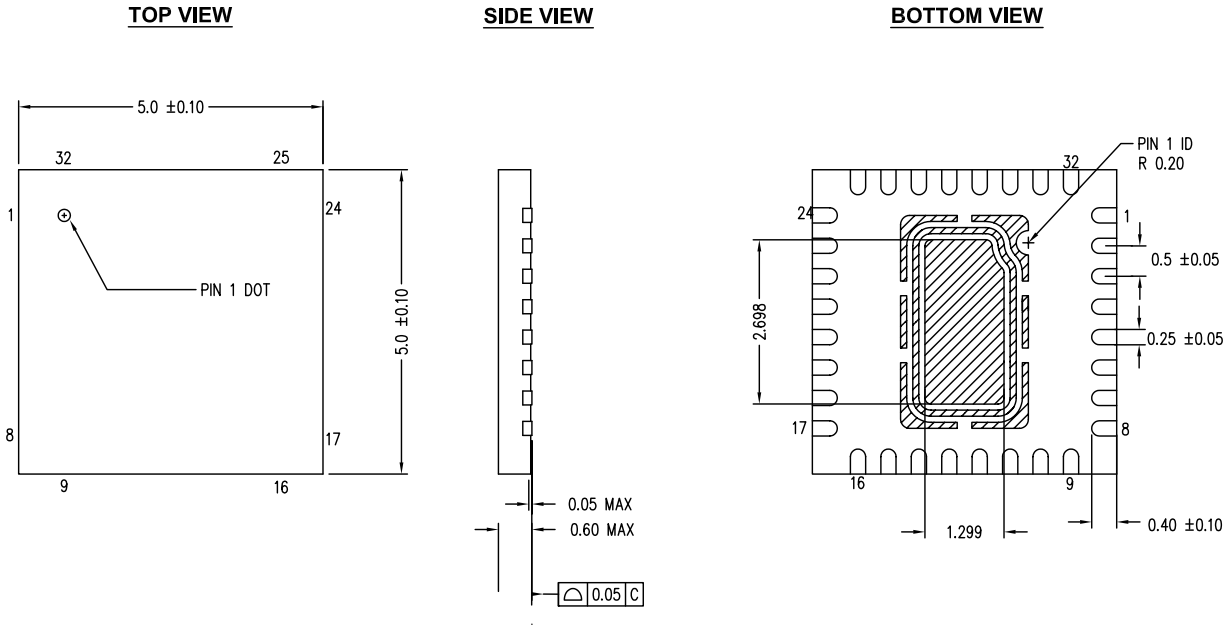
Table 31. SPI Master AC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
F_{SCLK}	SCLK clock frequency	–	–	–	12	MHz
DC_{SCLK}	SCLK duty cycle	–	–	50	–	%
t_{SETUP}	MISO to SCLK setup time	–	40	–	–	ns
t_{HOLD}	SCLK to MISO hold time	–	40	–	–	ns
t_{OUT_VAL}	SCLK to MOSI valid time	–	–	–	40	ns
t_{OUT_H}	MOSI high time	–	40	–	–	ns

Table 32. SPI Slave AC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
F_{SCLK}	SCLK clock frequency	–	–	–	4	MHz
t_{LOW}	SCLK low time	–	41.67	–	–	ns
t_{HIGH}	SCLK high time	–	41.67	–	–	ns
t_{SETUP}	MOSI to SCLK setup time	–	30	–	–	ns
t_{HOLD}	SCLK to MOSI hold time	–	50	–	–	ns
t_{SS_MISO}	SS low to MISO valid	–	–	–	153	ns
t_{SCLK_MISO}	SCLK to MISO valid	–	–	–	125	ns
t_{SS_HIGH}	SS high time	–	50	–	–	ns
t_{SS_SCLK}	Time from SS low to first SCLK	–	$2/F_{SCLK}$	–	–	ns
t_{SCLK_SS}	Time from last SCLK to SS high	–	$2/F_{SCLK}$	–	–	ns

Figure 19. 32-Pin QFN 5 × 5 × 0.55 mm (Sawn)

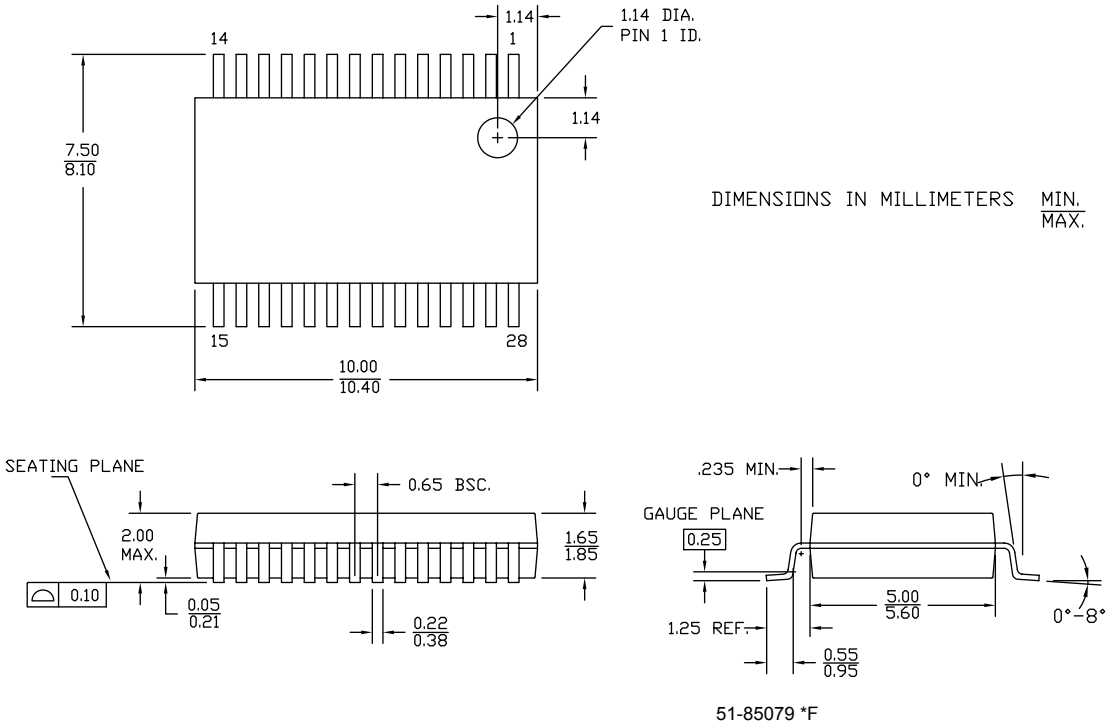


NOTES:

1. HATCH AREA IS SOLDERABLE EXPOSED PAD
2. BASED ON REF JEDEC # MO-248
3. PACKAGE WEIGHT: 38mg ± 4 mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-48913 *D

Figure 20. 28-pin SSOP (210 Mils)



51-85079 *F

Device Programmers

All device programmers are purchased from the Cypress Online Store.

CY3216 Modular Programmer

The CY3216 Modular Programmer kit features a modular programmer and the MiniProg1 programming unit. The modular programmer includes three programming module cards and supports multiple Cypress products. The kit includes:

- Modular Programmer Base
- 3 Programming Module Cards
- MiniProg Programming Unit
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

CY3207ISSP In-System Serial Programmer (ISSP)

The CY3207ISSP is a production programmer. It includes protection circuitry and an industrial case that is more robust than the MiniProg in a production programming environment. Note that CY3207ISSP needs special software and is not compatible with PSoC Programmer. The kit includes:

- CY3207 Programmer Unit
- PSoC ISSP Software CD
- 110 ~ 240V Power Supply, Euro-Plug Adapter
- USB 2.0 Cable

Accessories (Emulation and Programming)

Table 35. Emulation and Programming Accessories

Part Number	Pin Package	Flex-Pod Kit [31]	Foot Kit [32]	Prototyping Module	Adapter [33]
CY8C20234-12LKXI	16 QFN	Not Available	CY3250-16QFN-FK	CY3210-20X34	Not Available
CY8C20334-12LQXI	24 QFN	CY3250-20334QFN	CY3250-24QFN-FK	CY3210-20X34	AS-24-28-01ML-6
CY8C20634-12FDXI	30 WLCSP	Not available		CY3210-20X34	Not Available

Notes
31. Dual function Digital I/O Pins also connect to the common analog mux.
32. This part may be used for in-circuit debugging. It is NOT available for production.
33. Programming adapter converts non-DIP package to DIP footprint. Specific details and ordering information for each of the adapters is available at http://www.emulation.com.

Document History Page

Document Title: CY8C20134/CY8C20234/CY8C20334/CY8C20434/CY8C20534/CY8C20634, PSoC® Programmable System-on-Chip™ Document Number: 001-05356				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*I	2717566	DRSW / AESA	06/11/2009	Updated AC Chip-Level, and AC Programming Specifications as follows: Modified F_{IMO6} (page 20), T_{WRITE} specifications (page 23) Added I_{OH}, I_{OL} (page 17), Flash endurance note (page 19), DCILO (page 20), F32K_U (page 20), $T_{POWERUP}$ (page 20), $T_{ERASEALL}$ (page 23), $T_{PROGRAM\_HOT}$ (page 24), and $T_{PROGRAM\_COLD}$ (page 24) specifications Added AC SPI Master and Slave Specifications Added 30-Ball WLCSP Package
*J	2825336	ISW	12/10/2009	Updated pin description table for 48-pin OCD. Updated Ordering information table to include CY8C20534-12PVXA parts. Updated package diagrams for 48-pin QFN, 16-pin QFN (sawn), 24-pin QFN (sawn), and 30-ball WLCSP specs.
*K	2892629	NJF	03/15/2010	Updated Programmable pin configuration details in Features. Updated Analog Multiplexer System. Updated Cypress website links. Updated PSoC Designer Software Subsystems. Added $T_{BAKETEMP}$ and $T_{BAKETIME}$ parameters in Absolute Maximum Ratings. Removed the following sections: DC Low Power Comparator Specifications, AC Analog Mux Bus Specifications, AC Low Power Comparator Specifications, Third Party Tools, and Build a PSoC Emulator into your Board. Modified Notes in Packaging Dimensions. Updated Ordering Code Definitions. Removed inactive parts from Ordering Information. Updated links in Sales, Solutions, and Legal Information.
*L	2872902	VMAD	04/06/2010	Added part number CY8C20134 to the title. Added 8-pin and 16-pin SOIC pin and package details. Updated content to match current style guide and datasheet template. Moved acronyms and units of measure tables to page 35.
*M	3043170	NJF	09/30/2010	Added PSoC Device Characteristics table . Added DC I^2C Specifications table. Added F_{32K_U} max limit. Added Tjit_IMO specification, removed existing jitter specifications. Updated Units of Measure, Acronyms, Glossary, and References sections. Updated solder reflow specifications. No specific changed were made to I^2C Timing Diagram. Updated for clearer understanding. Template and styles update.
*N	3173718	NJF	02/16/2011	CY8C20134-12SX1I and CY8C20234-12SX2I typo error fixed in the ordering information table and changed in to CY8C20134-12SXI and CY8C20234-12SXI. Updated document version and date. Updated package diagram to 001-12919 *C.
*O	3248613	TOF	06/10/2011	Under Table 13, the text "Table 13 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V, 3.3 V, and 2.7 V at 25 °C. These are for design guidance only." changed to "Table 13 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or Table 14 for 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V, 3.3 V, and 2.7 V at 25 °C. These are for design guidance only". Updated Table 34 on page 37 table. Updated sections, "Getting Started", "Development Tools", and "Designing with PSoC Designer" to remove references to the system level designs. Updated package diagram 51-85066 to *E revision.
*P	3394775	KPOL	10/04/2011	Updated 16-pin SOIC and 16-pin QFN package drawings.

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