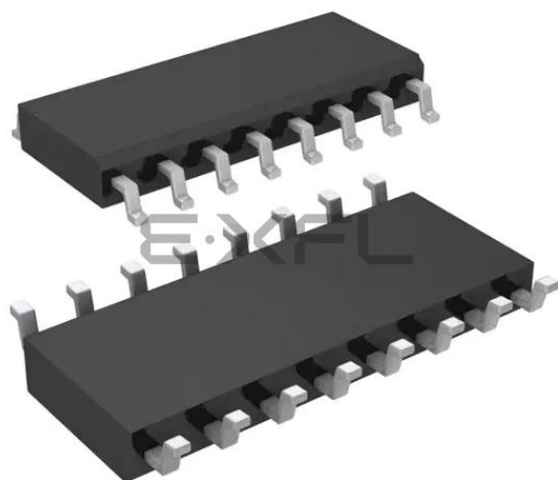




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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

|                            |                                                                                                                                                                     |
|----------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Product Status             | Active                                                                                                                                                              |
| Core Processor             | M8C                                                                                                                                                                 |
| Core Size                  | 8-Bit                                                                                                                                                               |
| Speed                      | 12MHz                                                                                                                                                               |
| Connectivity               | I <sup>2</sup> C, SPI                                                                                                                                               |
| Peripherals                | LVD, POR, WDT                                                                                                                                                       |
| Number of I/O              | 13                                                                                                                                                                  |
| Program Memory Size        | 8KB (8K x 8)                                                                                                                                                        |
| Program Memory Type        | FLASH                                                                                                                                                               |
| EEPROM Size                | -                                                                                                                                                                   |
| RAM Size                   | 512 x 8                                                                                                                                                             |
| Voltage - Supply (Vcc/Vdd) | 2.4V ~ 5.25V                                                                                                                                                        |
| Data Converters            | -                                                                                                                                                                   |
| Oscillator Type            | Internal                                                                                                                                                            |
| Operating Temperature      | -40°C ~ 85°C (TA)                                                                                                                                                   |
| Mounting Type              | Surface Mount                                                                                                                                                       |
| Package / Case             | 16-SOIC (0.154", 3.90mm Width)                                                                                                                                      |
| Supplier Device Package    | 16-SOIC                                                                                                                                                             |
| Purchase URL               | <a href="https://www.e-xfl.com/product-detail/infineon-technologies/cy8c20234-12sxi">https://www.e-xfl.com/product-detail/infineon-technologies/cy8c20234-12sxi</a> |

## Additional System Resources

System Resources provide additional capability useful to complete systems. Additional resources include low voltage detection and power on reset. Brief statements describing the merits of each system resource follow:

- The I<sup>2</sup>C slave or SPI master-slave module provides 50/100/400 kHz communication over two wires. SPI communication over three or four wires run at speeds of 46.9 kHz to 3 MHz (lower for a slower system clock).

- Low voltage detection (LVD) interrupts signal the application of falling voltage levels, while the advanced POR (Power On Reset) circuit eliminates the need for a system supervisor.
- An internal 1.8 V reference provides an absolute reference for capacitive sensing.
- The 5 V maximum input, 3 V fixed output, low dropout regulator (LDO) provides regulation for I/Os. A register controlled bypass mode enables the user to disable the LDO.

## PSoC Device Characteristics

Depending on your PSoC device characteristics, the digital and analog systems can have 16, 8, or 4 digital blocks, and 12, 6, or 4 analog blocks. [Table 1](#) lists the resources available for specific PSoC device groups. The PSoC device covered by this datasheet is highlighted.

**Table 1. PSoC Device Characteristics**

| PSoC Part Number | Digital I/O | Digital Rows | Digital Blocks | Analog Inputs | Analog Outputs | Analog Columns | Analog Blocks               | SRAM Size | Flash Size |
|------------------|-------------|--------------|----------------|---------------|----------------|----------------|-----------------------------|-----------|------------|
| CY8C29x66        | up to 64    | 4            | 16             | up to 12      | 4              | 4              | 12                          | 2 K       | 32 K       |
| CY8C28xxx        | up to 44    | up to 3      | up to 12       | up to 44      | up to 4        | up to 6        | up to 12 + 4 <sup>[1]</sup> | 1 K       | 16 K       |
| CY8C27x43        | up to 44    | 2            | 8              | up to 12      | 4              | 4              | 12                          | 256       | 16 K       |
| CY8C24x94        | up to 56    | 1            | 4              | up to 48      | 2              | 2              | 6                           | 1 K       | 16 K       |
| CY8C24x23A       | up to 24    | 1            | 4              | up to 12      | 2              | 2              | 6                           | 256       | 4 K        |
| CY8C23x33        | up to 26    | 1            | 4              | up to 12      | 2              | 2              | 4                           | 256       | 8 K        |
| CY8C22x45        | up to 38    | 2            | 8              | up to 38      | 0              | 4              | 6 <sup>[1]</sup>            | 1 K       | 16 K       |
| CY8C21x45        | up to 24    | 1            | 4              | up to 24      | 0              | 4              | 6 <sup>[1]</sup>            | 512       | 8 K        |
| CY8C21x34        | up to 28    | 1            | 4              | up to 28      | 0              | 2              | 4 <sup>[1]</sup>            | 512       | 8 K        |
| CY8C21x23        | up to 16    | 1            | 4              | up to 8       | 0              | 2              | 4 <sup>[1]</sup>            | 256       | 4 K        |
| CY8C20x34        | up to 28    | 0            | 0              | up to 28      | 0              | 0              | 3 <sup>[1,2]</sup>          | 512       | 8 K        |
| CY8C20xx6        | up to 36    | 0            | 0              | up to 36      | 0              | 0              | 3 <sup>[1,2]</sup>          | up to 2 K | up to 32 K |

### Notes

1. Limited analog functionality
2. Two analog blocks and one CapSense®.

## Getting Started

For in-depth information, along with detailed programming details, see the PSoC® [Technical Reference Manual](#).

For up-to-date ordering, packaging, and electrical specification information, see the latest [PSoC device datasheets](#) on the web.

### Application Notes

[Cypress application notes](#) are an excellent introduction to the wide variety of possible PSoC designs.

### Development Kits

[PSoC Development Kits](#) are available online from and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark.

### Training

[Free PSoC technical training](#) (on demand, webinars, and workshops), which is available online via [www.cypress.com](http://www.cypress.com),

covers a wide variety of topics and skill levels to assist you in your designs.

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[Technical support](#) – including a searchable Knowledge Base articles and technical forums – is also available online. If you cannot find an answer to your question, call our Technical Support hotline at 1-800-541-4736.

## 16-Pin SOIC Pinout

Figure 4. CY8C20234-12SXI 16-Pin SOIC Pinout

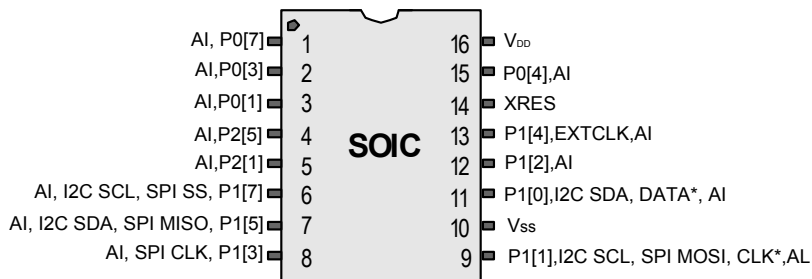


Table 3. Pin Definitions – CY8C20234 16-Pin (SOIC)

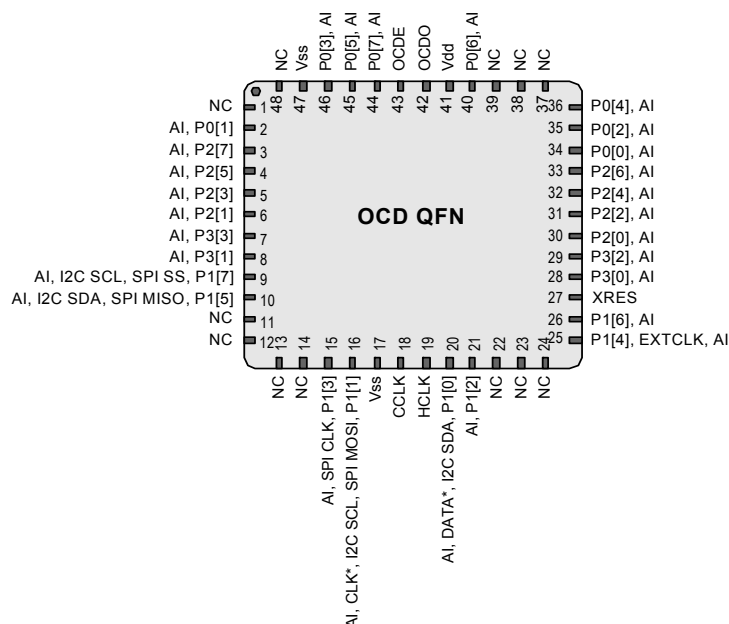
| Pin No. | Digital | Analog | Name            | Description                                                     |
|---------|---------|--------|-----------------|-----------------------------------------------------------------|
| 1       | I/O     | I      | P0[7]           | Analog column mux input                                         |
| 2       | I/O     | I      | P0[3]           | Analog column mux input and column input, integrating input     |
| 3       | I/O     | I      | P0[1]           | Analog column mux input, integrating input                      |
| 4       | I/O     | I      | P2[5]           | Analog column mux input                                         |
| 5       | I/O     | I      | P2[1]           | Analog column mux input                                         |
| 6       | I/O     | I      | P1[7]           | I2C serial clock (SCL), SPI SS                                  |
| 7       | I/O     | I      | P1[5]           | I2C serial data (SDA), SPI MISO                                 |
| 8       | I/O     | I      | P1[3]           | Analog column mux input, SPI CLK                                |
| 9       | I/O     | I      | P1[1]           | I2C serial clock (SCL), ISSP-SCLK, SPI MOSI                     |
| 10      | Power   |        | V <sub>SS</sub> | Ground connection                                               |
| 11      | I/O     | I      | P1[0]           | I2C serial data (SDA), ISSP-SDATA                               |
| 12      | I/O     | I      | P1[2]           | Analog column mux input                                         |
| 13      | I/O     | I      | P1[4]           | Analog column mux input, optional external clock input (EXTCLK) |
| 14      | I/O     | I      | XRES            | XRES                                                            |
| 15      | I/O     | I      | P0[4]           | Analog column mux input                                         |
| 16      | Power   |        | V <sub>DD</sub> | Supply voltage                                                  |

A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive.

## 48-Pin OCD Part Pinout

The 48-Pin QFN part table and pin diagram is for the CY8C20000 On-Chip Debug (OCD) PSoC device. This part is only used for in-circuit debugging. It is NOT available for production.

**Figure 5. CY8C20000 48-Pin OCD PSoC Device**



**Table 4. Pin Definitions – CY8C20000 48-Pin OCD (QFN)** [3]

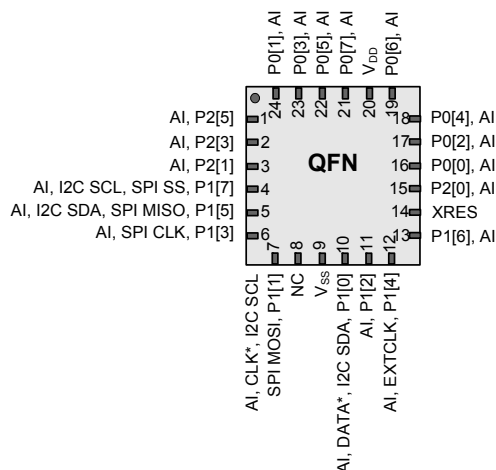
| Pin No. | Digital         | Analog | Name  | Description                                         |
|---------|-----------------|--------|-------|-----------------------------------------------------|
| 1       |                 |        | NC    | No connection                                       |
| 2       | I/O             | I      | P0[1] |                                                     |
| 3       | I/O             | I      | P2[7] |                                                     |
| 4       | I/O             | I      | P2[5] |                                                     |
| 5       | I/O             | I      | P2[3] |                                                     |
| 6       | I/O             | I      | P2[1] |                                                     |
| 7       | I/O             | I      | P3[3] |                                                     |
| 8       | I/O             | I      | P3[1] |                                                     |
| 9       | I <sub>OH</sub> | I      | P1[7] | I <sup>2</sup> C SCL, SPI SS                        |
| 10      | I <sub>OH</sub> | I      | P1[5] | I <sup>2</sup> C SDA, SPI MISO                      |
| 11      | I/O             | I      | P0[1] |                                                     |
| 12      |                 |        | NC    | No connection                                       |
| 13      |                 |        | NC    | No Connection                                       |
| 14      |                 |        | NC    | No Connection                                       |
| 15      |                 |        | NC    | SPI CLK                                             |
| 16      | I <sub>OH</sub> | I      | P1[3] | CLK <sup>[4]</sup> , I <sup>2</sup> C SCL, SPI MOSI |
| 17      | I <sub>OH</sub> | I      | P1[1] | Ground connection                                   |

### Notes

- The center pad on the QFN package is connected to ground (V<sub>SS</sub>) for best mechanical, thermal, and electrical performance. If not connected to ground, it is electrically floated and not connected to any other signal.
- These are the ISSP pins, that are not High Z at POR (Power-on-Reset). See the [PSoC Technical Reference Manual](#) for details.

## 24-Pin Part Pinout

**Figure 7. CY8C20334 24-Pin PSoC Device**



**Table 6. Pin Definitions – CY8C20334 24-Pin (QFN) [7]**

| Pin No. | Type            |        | Name            | Description                                         |
|---------|-----------------|--------|-----------------|-----------------------------------------------------|
|         | Digital         | Analog |                 |                                                     |
| 1       | I/O             | I      | P2[5]           |                                                     |
| 2       | I/O             | I      | P2[3]           |                                                     |
| 3       | I/O             | I      | P2[1]           |                                                     |
| 4       | I <sub>OH</sub> | I      | P1[7]           | I <sup>2</sup> C SCL, SPI SS                        |
| 5       | I <sub>OH</sub> | I      | P1[5]           | I <sup>2</sup> C SDA, SPI MISO                      |
| 6       | I <sub>OH</sub> | I      | P1[3]           | SPI CLK                                             |
| 7       | I <sub>OH</sub> | I      | P1[1]           | CLK <sup>[8]</sup> , I <sup>2</sup> C SCL, SPI MOSI |
| 8       |                 |        | NC              | No Connection                                       |
| 9       | Power           |        | V <sub>SS</sub> | Ground Connection                                   |
| 10      | I <sub>OH</sub> | I      | P1[0]           | DATA <sup>[8]</sup> , I <sup>2</sup> C SDA          |
| 11      | I <sub>OH</sub> | I      | P1[2]           |                                                     |
| 12      | I <sub>OH</sub> | I      | P1[4]           | Optional external clock input (EXTCLK)              |
| 13      | I <sub>OH</sub> | I      | P1[6]           |                                                     |
| 14      | Input           |        | XRES            | Active high external reset with internal pull-down  |
| 15      | I/O             | I      | P2[0]           |                                                     |
| 16      | I/O             | I      | P0[0]           |                                                     |
| 17      | I/O             | I      | P0[2]           |                                                     |
| 18      | I/O             | I      | P0[4]           |                                                     |
| 19      | I/O             | I      | P0[6]           | Analog bypass                                       |
| 20      | Power           |        | V <sub>DD</sub> | Supply voltage                                      |
| 21      | I/O             | I      | P0[7]           |                                                     |
| 22      | I/O             | I      | P0[5]           |                                                     |
| 23      | I/O             | I      | P0[3]           | Integrating input                                   |
| 24      | I/O             | I      | P0[1]           |                                                     |
| CP      | Power           |        | V <sub>SS</sub> | Center pad is connected to ground                   |

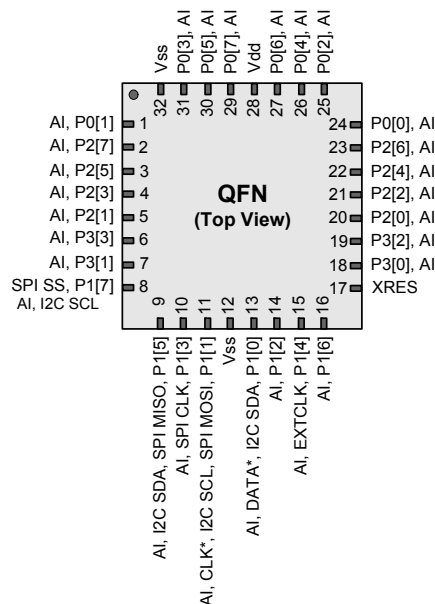
A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive

### Notes

- The center pad on the QFN package is connected to ground (V<sub>SS</sub>) for best mechanical, thermal, and electrical performance. If not connected to ground, it is electrically floated and not connected to any other signal.
- These are the ISSP pins, that are not High Z at POR (Power-on-Reset). See the [PSoC Technical Reference Manual](#) for details.

## 32-Pin Part Pinout

**Figure 8. CY8C20434 32-Pin PSoC Device**



**Table 7. Pin Definitions – CY8C20434 32-Pin (QFN) <sup>[9]</sup>**

| Pin No. | Type            |        | Name            | Description                                          |
|---------|-----------------|--------|-----------------|------------------------------------------------------|
|         | Digital         | Analog |                 |                                                      |
| 1       | I/O             | I      | P0[1]           |                                                      |
| 2       | I/O             | I      | P2[7]           |                                                      |
| 3       | I/O             | I      | P2[5]           |                                                      |
| 4       | I/O             | I      | P2[3]           |                                                      |
| 5       | I/O             | I      | P2[1]           |                                                      |
| 6       | I/O             | I      | P3[3]           |                                                      |
| 7       | I/O             | I      | P3[1]           |                                                      |
| 8       | I <sub>OH</sub> | I      | P1[7]           | I <sup>2</sup> C SCL, SPI SS                         |
| 9       | I <sub>OH</sub> | I      | P1[5]           | I <sup>2</sup> C SDA, SPI MISO                       |
| 10      | I <sub>OH</sub> | I      | P1[3]           | SPI CLK                                              |
| 11      | I <sub>OH</sub> | I      | P1[1]           | CLK <sup>[10]</sup> , I <sup>2</sup> C SCL, SPI MOSI |
| 12      | Power           |        | V <sub>SS</sub> | Ground Connection <sup>[11]</sup>                    |
| 13      | I <sub>OH</sub> | I      | P1[0]           | DATA <sup>[10]</sup> , I <sup>2</sup> C SDA          |
| 14      | I <sub>OH</sub> | I      | P1[2]           |                                                      |
| 15      | I <sub>OH</sub> | I      | P1[4]           | Optional external clock input (EXTCLK)               |
| 16      | I <sub>OH</sub> | I      | P1[6]           |                                                      |
| 17      | Input           |        | XRES            | Active high external reset with internal pull-down   |

### Notes

9. The center pad on the QFN package is connected to ground (V<sub>SS</sub>) for best mechanical, thermal, and electrical performance. If not connected to ground, it is electrically floated and not connected to any other signal.

10. These are the ISSP pins, that are not High Z at POR (Power-on-Reset). See the *PSoC Technical Reference Manual* for details.

11. All V<sub>SS</sub> pins should be brought out to one common GND plane.

**Table 7. Pin Definitions – CY8C20434 32-Pin (QFN) <sup>[9]</sup>**

| Pin No. | Type    |        | Name            | Description                       |
|---------|---------|--------|-----------------|-----------------------------------|
|         | Digital | Analog |                 |                                   |
| 18      | I/O     | I      | P3[0]           |                                   |
| 19      | I/O     | I      | P3[2]           |                                   |
| 20      | I/O     | I      | P2[0]           |                                   |
| 21      | I/O     | I      | P2[2]           |                                   |
| 22      | I/O     | I      | P2[4]           |                                   |
| 23      | I/O     | I      | P2[6]           |                                   |
| 24      | I/O     | I      | P0[0]           |                                   |
| 25      | I/O     | I      | P0[2]           |                                   |
| 26      | I/O     | I      | P0[4]           |                                   |
| 27      | I/O     | I      | P0[6]           | Analog bypass                     |
| 28      | Power   |        | V <sub>DD</sub> | Supply voltage                    |
| 29      | I/O     | I      | P0[7]           |                                   |
| 30      | I/O     | I      | P0[5]           |                                   |
| 31      | I/O     | I      | P0[3]           | Integrating input                 |
| 32      | Power   |        | V <sub>SS</sub> | Ground connection <sup>[12]</sup> |
| CP      | Power   |        | V <sub>SS</sub> | Center pad is connected to ground |

A = Analog, I = Input, O = Output, OH = 5 mA high output drive.

**Note**

12. All V<sub>SS</sub> pins should be brought out to one common GND plane.

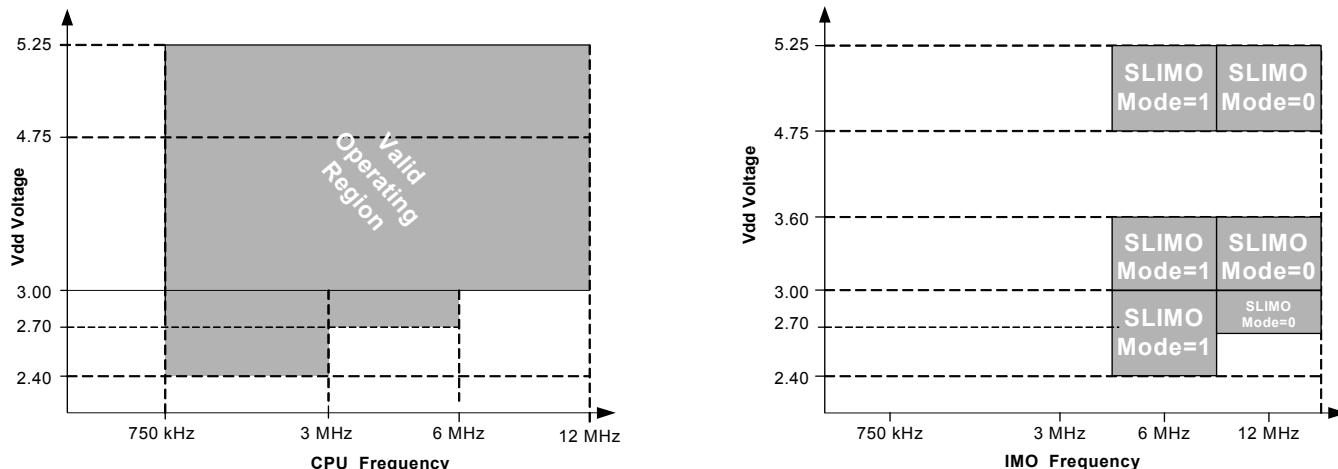
## Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8C20234, CY8C20334, CY8C20434, CY8C20534, and CY8C20634 PSoC devices. For the latest electrical specifications, check the most recent datasheet by visiting the web at <http://www.cypress.com>.

Specifications are valid for  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$  and  $T_J \leq 100^{\circ}\text{C}$  as specified, except where mentioned.

Refer to [Table 19 on page 25](#) for the electrical specifications on the internal main oscillator (IMO) using SLIMO mode.

**Figure 11. Voltage versus CPU Frequency and IMO Frequency Trim Options**



## Absolute Maximum Ratings

**Table 10. Absolute Maximum Ratings**

| Symbol         | Description                                     | Min               | Typ | Max               | Units              | Notes                                                                                                                                                                                                                              |
|----------------|-------------------------------------------------|-------------------|-----|-------------------|--------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| $T_{STG}$      | Storage Temperature                             | -55               | 25  | +100              | $^{\circ}\text{C}$ | Higher storage temperatures reduces data retention time. Recommended storage temperature is $+25^{\circ}\text{C} \pm 25^{\circ}\text{C}$ . Extended duration storage temperatures above $65^{\circ}\text{C}$ degrades reliability. |
| $T_{BAKETEMP}$ | Bake temperature                                | –                 | 125 | See package label | $^{\circ}\text{C}$ |                                                                                                                                                                                                                                    |
| $t_{BAKETIME}$ | Bake time                                       | See package label | –   | 72                | Hours              |                                                                                                                                                                                                                                    |
| $T_A$          | Ambient temperature with power applied          | -40               | –   | +85               | $^{\circ}\text{C}$ |                                                                                                                                                                                                                                    |
| $V_{DD}$       | Supply voltage on $V_{DD}$ relative to $V_{SS}$ | -0.5              | –   | +6.0              | V                  |                                                                                                                                                                                                                                    |
| $V_{IO}$       | DC input voltage                                | $V_{SS} - 0.5$    | –   | $V_{DD} + 0.5$    | V                  |                                                                                                                                                                                                                                    |
| $V_{IOZ}$      | DC voltage applied to tri-state                 | $V_{SS} - 0.5$    | –   | $V_{DD} + 0.5$    | V                  |                                                                                                                                                                                                                                    |
| $I_{MIO}$      | Maximum current into any port pin               | -25               | –   | +50               | mA                 |                                                                                                                                                                                                                                    |
| ESD            | Electro static discharge voltage                | 2000              | –   | –                 | V                  | Human body model ESD.                                                                                                                                                                                                              |
| LU             | Latch-up current                                | –                 | –   | 200               | mA                 |                                                                                                                                                                                                                                    |

**Table 14. 2.7-V DC GPIO Specifications**

| Symbol            | Description                                                       | Min                   | Typ | Max  | Units | Notes                                                                                                                                                                                                               |
|-------------------|-------------------------------------------------------------------|-----------------------|-----|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| R <sub>PU</sub>   | Pull-up resistor                                                  | 4                     | 5.6 | 8    | kΩ    |                                                                                                                                                                                                                     |
| V <sub>OH1</sub>  | High output voltage<br>Port 1 pins with LDO regulator disabled    | V <sub>DD</sub> – 0.2 | –   | –    | V     | I <sub>OH</sub> < 10 μA, maximum of 10 mA source current in all I/Os.                                                                                                                                               |
| V <sub>OH2</sub>  | High output voltage<br>Port 1 pins with LDO regulator disabled    | V <sub>DD</sub> – 0.5 | –   | –    | V     | I <sub>OH</sub> = 2 mA, maximum of 10 mA source current in all I/Os.                                                                                                                                                |
| V <sub>OL</sub>   | Low output voltage                                                | –                     | –   | 0.75 | V     | I <sub>OL</sub> = 10 mA, maximum of 30 mA sink current on even port pins (for example, P0[2] and P1[4]) and 30 mA sink current on odd port pins (for example, P0[3] and P1[5]).                                     |
| I <sub>OH2</sub>  | High level source current port 1 Pins with LDO regulator disabled | 2                     | –   | –    | mA    | V <sub>OH</sub> = V <sub>DD</sub> – 0.5, for the limitations of the total current and I <sub>OH</sub> at other V <sub>OH</sub> levels see the notes for V <sub>OH</sub> .                                           |
| I <sub>OL</sub>   | Low level sink current                                            | 10                    | –   | –    | mA    | V <sub>OH</sub> = .75 V, see the limitations of the total current in the note for V <sub>OL</sub> .                                                                                                                 |
| V <sub>OLP1</sub> | Low output voltage port 1 pins                                    | –                     | –   | 0.4  | V     | I <sub>OL</sub> = 5 mA<br>Maximum of 50 mA sink current on even port pins (for example, P0[2] and P3[4]) and 50 mA sink current on odd port pins (for example, P0[3] and P2[5]).<br>2.4 V ≤ V <sub>DD</sub> < 3.6 V |
| V <sub>IL</sub>   | Input low voltage                                                 | –                     | –   | 0.75 | V     | 2.4 V ≤ V <sub>DD</sub> < 3.6 V                                                                                                                                                                                     |
| V <sub>IH1</sub>  | Input high voltage                                                | 1.4                   | –   | –    | V     | 2.4 V ≤ V <sub>DD</sub> < 2.7 V                                                                                                                                                                                     |
| V <sub>IH2</sub>  | Input high voltage                                                | 1.6                   | –   | –    | V     | 2.7 V ≤ V <sub>DD</sub> < 3.6 V                                                                                                                                                                                     |
| V <sub>H</sub>    | Input hysteresis voltage                                          | –                     | 60  | –    | mV    |                                                                                                                                                                                                                     |
| I <sub>IL</sub>   | Input leakage (absolute value)                                    | –                     | 1   | –    | nA    | Gross tested to 1 μA                                                                                                                                                                                                |
| C <sub>IN</sub>   | Capacitive load on pins as input                                  | 0.5                   | 1.7 | 5    | pF    | Package and pin dependent<br>Temperature = 25 °C                                                                                                                                                                    |
| C <sub>OUT</sub>  | Capacitive load on pins as output                                 | 0.5                   | 1.7 | 5    | pF    | Package and pin dependent<br>Temperature = 25 °C                                                                                                                                                                    |

#### DC Analog Mux Bus Specifications

Table 15 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T<sub>A</sub> ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T<sub>A</sub> ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T<sub>A</sub> ≤ 85 °C, respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C. These are for design guidance only.

**Table 15. DC Analog Mux Bus Specifications**

| Symbol          | Description                            | Min | Typ | Max        | Units  | Notes                                                      |
|-----------------|----------------------------------------|-----|-----|------------|--------|------------------------------------------------------------|
| R <sub>SW</sub> | Switch resistance to common analog bus | –   | –   | 400<br>800 | Ω<br>Ω | V <sub>DD</sub> ≥ 2.7 V<br>2.4 V ≤ V <sub>DD</sub> ≤ 2.7 V |

### DC I<sup>2</sup>C Specifications

Table 18 lists the guaranteed minimum and maximum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , 3.0 V to 3.6 V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , or 2.4 V to 3.0 V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C. These are for design guidance only. Flash endurance and retention specifications with the use of the EEPROM user module are valid only within the range: 25 °C  $\pm$  20°C during the Flash Write operation. Reference the EEPROM User Module datasheet instructions for EEPROM flash Write requirements outside of the 25 °C  $\pm$  20 °C temperature window.

**Table 18. DC I<sup>2</sup>C Specifications**<sup>[22]</sup>

| Symbol             | Description      | Min                 | Typ | Max                  | Units | Notes                                            |
|--------------------|------------------|---------------------|-----|----------------------|-------|--------------------------------------------------|
| V <sub>ILI2C</sub> | Input low level  | –                   | –   | $0.3 \times V_{DD}$  | V     | $2.4 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$   |
|                    |                  | –                   | –   | $0.25 \times V_{DD}$ | V     | $4.75 \text{ V} \leq V_{DD} \leq 5.25 \text{ V}$ |
| V <sub>IHI2C</sub> | Input high level | $0.7 \times V_{DD}$ | –   | –                    | V     | $2.4 \text{ V} \leq V_{DD} \leq 5.25 \text{ V}$  |

### AC Electrical Characteristics

#### AC Chip Level Specifications

Table 19, Table 20, and Table 21 list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , 3.0 V to 3.6 V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , or 2.4 V to 3.0 V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$  respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C. These are for design guidance only.

**Table 19. 5-V and 3.3-V AC Chip-Level Specifications**

| Symbol                                             | Description                                                                            | Min  | Typ | Max  | Units | Notes                                                                                                                                                                                    |
|----------------------------------------------------|----------------------------------------------------------------------------------------|------|-----|------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| F <sub>CPU1</sub>                                  | CPU frequency (3.3 V nominal)                                                          | 0.75 | –   | 12.6 | MHz   | 12 MHz only for SLIMO Mode = 0.                                                                                                                                                          |
| F <sub>32K1</sub>                                  | Internal low speed oscillator frequency                                                | 15   | 32  | 64   | kHz   |                                                                                                                                                                                          |
| F <sub>32K_U</sub>                                 | Internal low speed oscillator (ILO) untrimmed frequency                                | 5    | –   | 100  | kHz   | After a reset and before the M8C starts to run, the ILO is not trimmed. See the System Resets section of the <a href="#">PSoC Technical Reference Manual</a> for details on this timing. |
| F <sub>IMO12</sub>                                 | Internal main oscillator stability for 12 MHz (commercial temperature) <sup>[23]</sup> | 11.4 | 12  | 12.6 | MHz   | Trimmed for 3.3 V operation using factory trim values. See <a href="#">Figure 11 on page 19</a> , SLIMO mode = 0.                                                                        |
| F <sub>IMO6</sub>                                  | Internal main oscillator stability for 6 MHz (commercial temperature)                  | 5.5  | 6.0 | 6.5  | MHz   | Trimmed for 3.3 V operation using factory trim values. See <a href="#">Figure 11 on page 19</a> , SLIMO mode = 1.                                                                        |
| DC <sub>IMO</sub>                                  | Duty cycle of IMO                                                                      | 40   | 50  | 60   | %     |                                                                                                                                                                                          |
| DC <sub>ILO</sub>                                  | Internal low speed oscillator duty cycle                                               | 20   | 50  | 80   | %     |                                                                                                                                                                                          |
| t <sub>XRST</sub>                                  | External reset pulse width                                                             | 10   | –   | –    | μs    |                                                                                                                                                                                          |
| t <sub>POWERUP</sub>                               | Time from end of POR to CPU executing code                                             | –    | 16  | 100  | ms    | Power-up from 0 V. See the System Resets section of the <a href="#">PSoC Technical Reference Manual</a> .                                                                                |
| SR <sub>POWER UP</sub>                             | Power supply slew rate                                                                 | –    | –   | 250  | V/ms  |                                                                                                                                                                                          |
| t <sub>jitter</sub> <sub>IMO</sub> <sup>[24]</sup> | 12 MHz IMO cycle-to-cycle jitter (RMS)                                                 | –    | 200 | 1600 | ps    |                                                                                                                                                                                          |
|                                                    | 12 MHz IMO long term N cycle-to-cycle jitter (RMS)                                     | –    | 600 | 1400 | ps    | N = 32                                                                                                                                                                                   |
|                                                    | 12 MHz IMO period jitter (RMS)                                                         | –    | 100 | 900  | ps    |                                                                                                                                                                                          |

#### Notes

22. All GPIO meet the DC GPIO V<sub>IL</sub> and V<sub>IH</sub> specifications found in the DC GPIO Specifications sections. The I<sup>2</sup>C GPIO pins also meet the above specs.

23. 0 to 70 °C ambient, V<sub>DD</sub> = 3.3 V.

24. Refer to [Cypress Jitter Specifications Application Note – AN5054](#) at <http://www.cypress.com> for more information.

#### AC SPI Specifications

Table 31 and Table 32 list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , 3.0 V to 3.6 V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , or 2.4 V to 3.0 V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$  respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C. These are for design guidance only.

**Table 31. SPI Master AC Specifications**

| Symbol                | Parameter               | Conditions | Min | Typ | Max | Units |
|-----------------------|-------------------------|------------|-----|-----|-----|-------|
| $F_{\text{SCLK}}$     | SCLK clock frequency    | —          | —   | —   | 12  | MHz   |
| $DC_{\text{SCLK}}$    | SCLK duty cycle         | —          | —   | 50  | —   | %     |
| $t_{\text{SETUP}}$    | MISO to SCLK setup time | —          | 40  | —   | —   | ns    |
| $t_{\text{HOLD}}$     | SCLK to MISO hold time  | —          | 40  | —   | —   | ns    |
| $t_{\text{OUT\_VAL}}$ | SCLK to MOSI valid time | —          | —   | —   | 40  | ns    |
| $t_{\text{OUT\_H}}$   | MOSI high time          | —          | 40  | —   | —   | ns    |

**Table 32. SPI Slave AC Specifications**

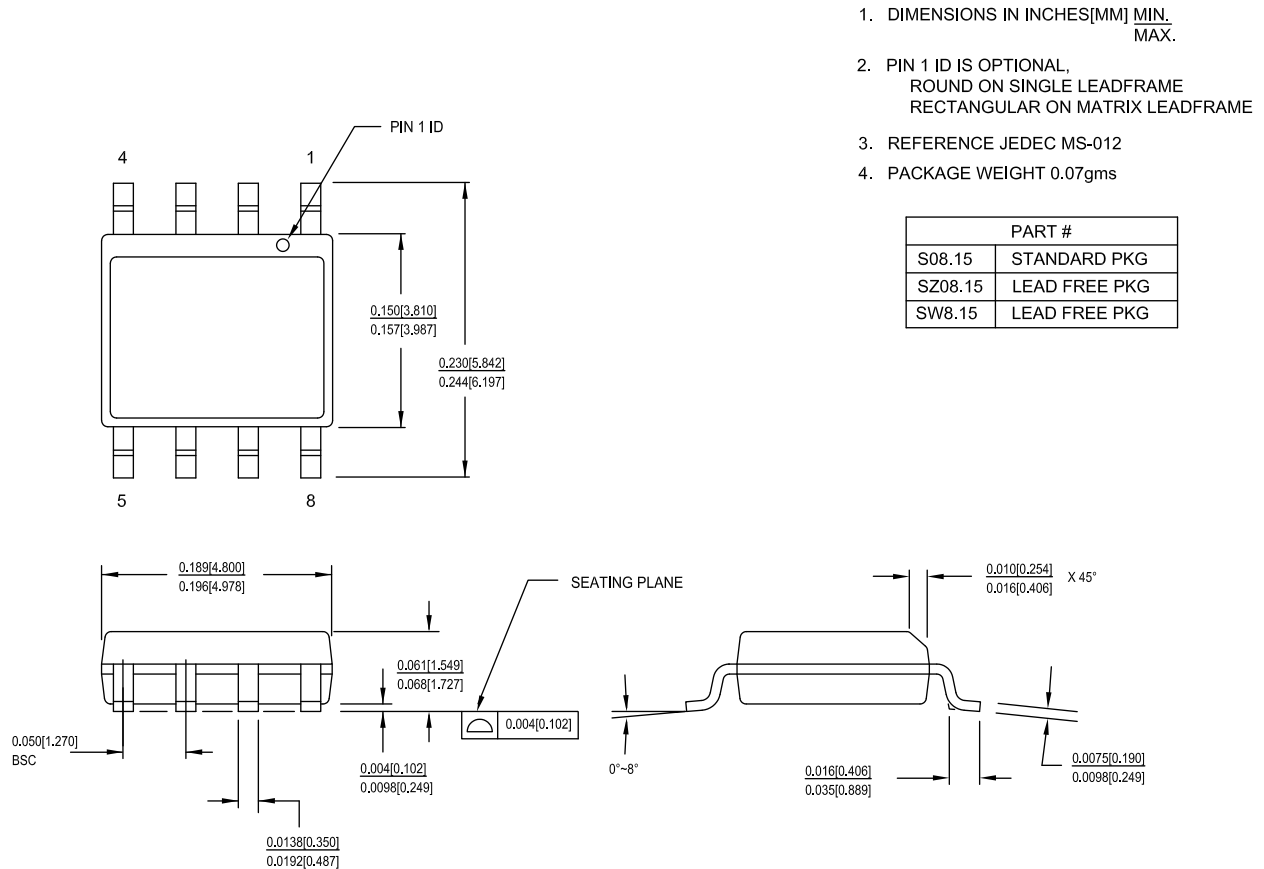
| Symbol                  | Parameter                      | Conditions | Min                 | Typ | Max | Units |
|-------------------------|--------------------------------|------------|---------------------|-----|-----|-------|
| $F_{\text{SCLK}}$       | SCLK clock frequency           | —          | —                   | —   | 4   | MHz   |
| $t_{\text{LOW}}$        | SCLK low time                  | —          | 41.67               | —   | —   | ns    |
| $t_{\text{HIGH}}$       | SCLK high time                 | —          | 41.67               | —   | —   | ns    |
| $t_{\text{SETUP}}$      | MOSI to SCLK setup time        | —          | 30                  | —   | —   | ns    |
| $t_{\text{HOLD}}$       | SCLK to MOSI hold time         | —          | 50                  | —   | —   | ns    |
| $t_{\text{SS\_MISO}}$   | SS low to MISO valid           | —          | —                   | —   | 153 | ns    |
| $t_{\text{SCLK\_MISO}}$ | SCLK to MISO valid             | —          | —                   | —   | 125 | ns    |
| $t_{\text{SS\_HIGH}}$   | SS high time                   | —          | 50                  | —   | —   | ns    |
| $t_{\text{SS\_SCLK}}$   | Time from SS low to first SCLK | —          | $2/F_{\text{SCLK}}$ | —   | —   | ns    |
| $t_{\text{SCLK\_SS}}$   | Time from last SCLK to SS high | —          | $2/F_{\text{SCLK}}$ | —   | —   | ns    |

## Packaging Dimensions

This section illustrates the packaging specifications for the CY8C20234, CY8C20334, CY8C20434, CY8C20534, and CY8C20634 PSoC devices along with the thermal impedances for each package.

**Important Note** Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulation tools' dimensions, refer to the emulator pod drawings at <http://www.cypress.com>.

**Figure 14. 8-pin SOIC (150 Mils)**



51-85066 \*G

Pin one mark

1 2 3 4 5

A B C D E F

2.309±0.025

1.849 ±0.025

0.40 MAX

0.080

0.022±0.003

0.279±0.013

0.030

Note: 1. RDL bump pad size 270um  
2.. UBM pad diameter size 250um  
Ø0.250±0.03

5 4 3 2 1

A B C D E F

1.900

0.760

0.380

0.2045±0.015

0.370

0.740

1.480

1.849

0.1845±0.015

001-44613 \*C

**Important Note** For information on the preferred dimensions for mounting the QFN packages, see the application note *Design Guidelines for Cypress Quad Flat No Extended Lead (QFN) Packaged Devices – AN72845* available at <http://www.cypress.com>. It is important to note that pinned vias for thermal conduction are not required for the low power 24, 32, and 48-pin QFN PSoC devices.

## Thermal Impedances

Table 33 illustrates the minimum solder reflow peak temperature to achieve good solderability.

**Table 33. Thermal Impedances Per Package**

| Package                | Typical $\theta_{JA}$ <sup>[28]</sup> |
|------------------------|---------------------------------------|
| 8 SOIC                 | 127 °C/W                              |
| 16 SOIC                | 80 °C/W                               |
| 16 QFN                 | 46 °C/W                               |
| 24 QFN <sup>[29]</sup> | 25 °C/W                               |
| 28 SSOP                | 96 °C/W                               |
| 30 WLCSP               | 54 °C/W                               |
| 32 QFN <sup>[29]</sup> | 27 °C/W                               |
| 48 QFN <sup>[29]</sup> | 28 °C/W                               |

## Solder Reflow Specifications

Table 34 shows the solder reflow temperature limits that must not be exceeded.

**Table 34. Solder Reflow Specifications**

| Package      | Maximum Peak Temperature ( $T_C$ ) | Maximum Time above $T_C - 5$ °C |
|--------------|------------------------------------|---------------------------------|
| 8-Pin SOIC   | 260 °C                             | 30 seconds                      |
| 16-Pin SOIC  | 260 °C                             | 30 seconds                      |
| 16-Pin QFN   | 260 °C                             | 30 seconds                      |
| 24-Pin QFN   | 260 °C                             | 30 seconds                      |
| 28-Pin SSOP  | 260 °C                             | 30 seconds                      |
| 30-Pin WLCSP | 260 °C                             | 30 seconds                      |
| 32-Pin QFN   | 260 °C                             | 30 seconds                      |
| 48-Pin QFN   | 260 °C                             | 30 seconds                      |

### Notes

28.  $T_J = T_A + \text{Power} \times \theta_{JA}$ .

29. To achieve the thermal impedance specified for the QFN package, refer to application note *Design Guidelines for Cypress Quad Flat No Extended Lead (QFN) Packaged Devices – AN72845* available at <http://www.cypress.com>.

30. Higher temperatures is required based on the solder melting point. Typical temperatures for solder are  $220 \pm 5$  °C with Sn-Pb or  $245 \pm 5$  °C with Sn-Ag-Cu paste. Refer to the solder manufacturer specifications.

## Development Tool Selection

### Software

#### *PSoC Designer™*

At the core of the PSoC development software suite is PSoC Designer, used to generate PSoC firmware applications. PSoC Designer is available free of charge at <http://www.cypress.com> and includes a free C compiler.

#### *PSoC Programmer*

PSoC Programmer is flexible enough and is used on the bench in development and also suitable for factory programming. PSoC Programmer works either as a standalone programming application or operates directly from PSoC Designer. PSoC Programmer software is compatible with both PSoC ICE Cube In-Circuit Emulator and PSoC MiniProg. PSoC programmer is available free of charge at <http://www.cypress.com>.

### Development Kits

All development kits are sold at the Cypress Online Store.

#### *CY3215-DK Basic Development Kit*

The CY3215-DK is for prototyping and development with PSoC Designer. This kit supports in-circuit emulation and the software interface enables users to run, halt, and single step the processor and view the content of specific memory locations. PSoC Designer supports the advance emulation features also. The kit includes:

- PSoC Designer Software CD
- ICE-Cube In-Circuit Emulator
- ICE Flex-Pod for CY8C29x66 Family
- Cat-5 Adapter
- Mini-Eval Programming Board
- 110 ~ 240V Power Supply, Euro-Plug Adapter
- iMAGEcraft C Compiler (Registration Required)
- ISSP Cable
- USB 2.0 Cable and Blue Cat-5 Cable
- 2 CY8C29466-24PXI 28-PDIP Chip Samples

## Evaluation Tools

All evaluation tools are sold at the Cypress Online Store.

#### *CY3210-MiniProg1*

The CY3210-MiniProg1 kit enables the user to program PSoC devices via the MiniProg1 programming unit. The MiniProg is a small, compact prototyping programmer that connects to the PC via a provided USB 2.0 cable. The kit includes:

- MiniProg Programming Unit
- MiniEval Socket Programming and Evaluation Board
- 28-Pin CY8C29466-24PXI PDIP PSoC Device Sample
- 28-Pin CY8C27443-24PXI PDIP PSoC Device Sample
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

#### *CY3210-PSoCEval1*

The CY3210-PSoCEval1 kit features an evaluation board and the MiniProg1 programming unit. The evaluation board includes an LCD module, potentiometer, LEDs, and plenty of bread-boarding space to meet all of your evaluation needs. The kit includes:

- Evaluation Board with LCD Module
- MiniProg Programming Unit
- 28-Pin CY8C29466-24PXI PDIP PSoC Device Sample (2)
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

#### *CY3214-PSoCEvalUSB*

The CY3214-PSoCEvalUSB evaluation kit features a development board for the CY8C24794-24LFXI PSoC device. Special features of the board include both USB and capacitive sensing development and debugging support. This evaluation board also includes an LCD module, potentiometer, LEDs, an enunciator and plenty of bread boarding space to meet all of your evaluation needs. The kit includes:

- PSoCEvalUSB Board
- LCD Module
- MiniProg Programming Unit
- Mini USB Cable
- PSoC Designer and Example Projects CD
- Getting Started Guide
- Wire Pack

## Acronyms

### Acronyms Used

Table 37 lists the acronyms that are used in this document.

**Table 37. Acronyms Used in this Datasheet**

| Acronym | Description                                         | Acronym | Description                     |
|---------|-----------------------------------------------------|---------|---------------------------------|
| AC      | alternating current                                 | MIPS    | million instructions per second |
| ADC     | analog-to-digital converter                         | OCD     | on-chip debug                   |
| API     | application programming interface                   | PCB     | printed circuit board           |
| CMOS    | complementary metal oxide semiconductor             | PGA     | programmable gain amplifier     |
| CPU     | central processing unit                             | POR     | power on reset                  |
| EEPROM  | electrically erasable programmable read-only memory | PPOR    | precision power on reset        |
| GPIO    | general purpose I/O                                 | PSoC®   | Programmable System-on-Chip     |
| ICE     | in-circuit emulator                                 | PWM     | pulse width modulator           |
| IDAC    | current DAC                                         | QFN     | quad flat no leads              |
| IDE     | integrated development environment                  | SLIMO   | slow IMO                        |
| ILO     | internal low speed oscillator                       | SPI™    | serial peripheral interface     |
| IMO     | internal main oscillator                            | SRAM    | static random access memory     |
| I/O     | input/output                                        | SROM    | supervisory read only memory    |
| ISSP    | in-system serial programming                        | SSOP    | shrink small-outline package    |
| LCD     | liquid crystal display                              | USB     | universal serial bus            |
| LDO     |                                                     | WDT     | watchdog timer                  |
| LED     | light-emitting diode                                | WLCSP   | wafer level chip scale package  |
| LVD     | low voltage detect                                  | XRES    | external reset                  |
| MCU     | microcontroller unit                                |         |                                 |

## Reference Documents

PSoC® CY8C20x34 and PSoC® CY8C20x24 Technical Reference Manual (TRM) – 001-13033

Design Aids – Reading and Writing PSoC® Flash - AN2015 (001-40459)

Design Guidelines for Cypress Quad Flat No Extended Lead (QFN) Packaged Devices – AN72845 available at <http://www.cypress.com>.

## Document Conventions

### Units of Measure

Table 38 lists the unit sof measures.

**Table 38. Units of Measure**

| Symbol | Unit of Measure | Symbol | Unit of Measure |
|--------|-----------------|--------|-----------------|
| °C     | degree Celsius  | ms     | millisecond     |
| pF     | picofarad       | ns     | nanosecond      |
| kHz    | kilohertz       | ps     | picosecond      |
| MHz    | megahertz       | μV     | microvolts      |
| kΩ     | kilohm          | mV     | millivolts      |
| Ω      | ohm             | V      | volts           |
| μA     | microampere     | W      | watt            |
| mA     | milliampere     | mm     | millimeter      |
| nA     | nanoampere      | %      | percent         |
| μs     | microsecond     |        |                 |

### Numeric Conventions

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase 'h' (for example, '14h' or '3Ah'). Hexadecimal numbers may also be represented by a '0x' prefix, the C coding convention. Binary numbers have an appended lowercase 'b' (for example, '01010100b' or '01000011b'). Numbers not indicated by an 'h' or 'b' are decimals.

## Glossary

|                                         |                                                                                                                                                                                                                                                                                                                                                                  |
|-----------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| active high                             | <ol style="list-style-type: none"> <li>1. A logic signal having its asserted state as the logic 1 state.</li> <li>2. A logic signal having the logic 1 state as the higher voltage of the two states.</li> </ol>                                                                                                                                                 |
| analog blocks                           | The basic programmable opamp circuits. These are SC (switched capacitor) and CT (continuous time) blocks. These blocks can be interconnected to provide ADCs, DACs, multi-pole filters, gain stages, and much more.                                                                                                                                              |
| analog-to-digital (ADC)                 | A device that changes an analog signal to a digital signal of corresponding magnitude. Typically, an ADC converts a voltage to a digital number. The digital-to-analog (DAC) converter performs the reverse operation.                                                                                                                                           |
| Application programming interface (API) | A series of software routines that comprise an interface between a computer application and lower level services and functions (for example, user modules and libraries). APIs serve as building blocks for programmers that create software applications.                                                                                                       |
| asynchronous                            | A signal whose data is acknowledged or acted upon immediately, irrespective of any clock signal.                                                                                                                                                                                                                                                                 |
| Bandgap reference                       | A stable voltage reference design that matches the positive temperature coefficient of $V_T$ with the negative temperature coefficient of $V_{BE}$ , to produce a zero temperature coefficient (ideally) reference.                                                                                                                                              |
| bandwidth                               | <ol style="list-style-type: none"> <li>1. The frequency range of a message or information processing system measured in hertz.</li> <li>2. The width of the spectral region over which an amplifier (or absorber) has substantial gain (or loss); it is sometimes represented more specifically as, for example, full width at half maximum.</li> </ol>          |
| bias                                    | <ol style="list-style-type: none"> <li>1. A systematic deviation of a value from a reference value.</li> <li>2. The amount by which the average of a set of values departs from a reference value.</li> <li>3. The electrical, mechanical, magnetic, or other force (field) applied to a device to establish a reference level to operate the device.</li> </ol> |

## Glossary

|                 |                                                                                                                                                                                                                                                                                                       |
|-----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| SRAM            | An acronym for static random access memory. A memory device where you can store and retrieve data at a high rate of speed. The term static is used because, after a value is loaded into an SRAM cell, it remains unchanged until it is explicitly altered or until power is removed from the device. |
| SROM            | An acronym for supervisory read only memory. The SROM holds code that is used to boot the device, calibrate circuitry, and perform Flash operations. The functions of the SROM may be accessed in normal user code, operating from Flash.                                                             |
| stop bit        | A signal following a character or block that prepares the receiving device to receive the next character or block.                                                                                                                                                                                    |
| synchronous     | <ol style="list-style-type: none"><li>1. A signal whose data is not acknowledged or acted upon until the next active edge of a clock signal.</li><li>2. A system whose operation is synchronized by a clock signal.</li></ol>                                                                         |
| tri-state       | A function whose output can adopt three states: 0, 1, and Z (high-impedance). The function does not drive any value in the Z state and, in many respects, may be considered to be disconnected from the rest of the circuit, allowing another output to drive the same net.                           |
| UART            | A UART or universal asynchronous receiver-transmitter translates between parallel bits of data and serial bits.                                                                                                                                                                                       |
| user modules    | Pre-build, pre-tested hardware/firmware peripheral functions that take care of managing and configuring the lower level Analog and Digital PSoC Blocks. User Modules also provide high level <b>API (Application Programming Interface)</b> for the peripheral function.                              |
| user space      | The bank 0 space of the register map. The registers in this bank are more likely to be modified during normal program execution and not just during initialization. Registers in bank 1 are most likely to be modified only during the initialization phase of the program.                           |
| V <sub>DD</sub> | A name for a power net meaning "voltage drain." The most positive power supply signal. Usually 5 V or 3.3 V.                                                                                                                                                                                          |
| V <sub>SS</sub> | A name for a power net meaning "voltage source." The most negative power supply signal.                                                                                                                                                                                                               |
| watchdog timer  | A timer that must be serviced periodically. If it is not serviced, the CPU resets after a specified period of time.                                                                                                                                                                                   |

## Document History Page

| Document Title: CY8C20134/CY8C20234/CY8C20334/CY8C20434/CY8C20534/CY8C20634,<br>PSoC® Programmable System-on-Chip™<br>Document Number: 001-05356 |         |                 |                 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|--------------------------------------------------------------------------------------------------------------------------------------------------|---------|-----------------|-----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Revision                                                                                                                                         | ECN     | Orig. of Change | Submission Date | Description of Change                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| *I                                                                                                                                               | 2717566 | DRSW / AESA     | 06/11/2009      | Updated AC Chip-Level, and AC Programming Specifications as follows:<br>Modified $F_{IMO6}$ (page 20), $T_{WRITE}$ specifications (page 23) Added $I_{OH}$ , $I_{OL}$ (page 17), Flash endurance note (page 19), DCILO (page 20), $F_{32K\_U}$ (page 20), $T_{POWERUP}$ (page 20), $T_{ERASEALL}$ (page 23), $T_{PROGRAM\_HOT}$ (page 24), and $T_{PROGRAM\_COLD}$ (page 24) specifications<br>Added AC SPI Master and Slave Specifications<br>Added 30-Ball WLCSP Package                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| *J                                                                                                                                               | 2825336 | ISW             | 12/10/2009      | Updated pin description table for 48-pin QFN. Updated Ordering information table to include CY8C20534-12PVXA parts. Updated package diagrams for 48-pin QFN, 16-pin QFN (sawn), 24-pin QFN (sawn), and 30-ball WLCSP specs.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| *K                                                                                                                                               | 2892629 | NJF             | 03/15/2010      | Updated Programmable pin configuration details in Features.<br>Updated <a href="#">Analog Multiplexer System</a> .<br>Updated Cypress website links.<br>Updated <a href="#">PSoC Designer Software Subsystems</a> .<br>Added $T_{BAKETEMP}$ and $T_{BAKETIME}$ parameters in <a href="#">Absolute Maximum Ratings</a> .<br>Removed the following sections:<br>DC Low Power Comparator Specifications, AC Analog Mux Bus Specifications, AC Low Power Comparator Specifications, Third Party Tools, and Build a PSoC Emulator into your Board.<br>Modified Notes in <a href="#">Packaging Dimensions</a> .<br>Updated <a href="#">Ordering Code Definitions</a> .<br>Removed inactive parts from <a href="#">Ordering Information</a> .<br>Updated links in <a href="#">Sales, Solutions, and Legal Information</a> .                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| *L                                                                                                                                               | 2872902 | VMAD            | 04/06/2010      | Added part number CY8C20134 to the title.<br>Added 8-pin and 16-pin SOIC pin and package details.<br>Updated content to match current style guide and datasheet template.<br>Moved acronyms and units of measure tables to page 35.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| *M                                                                                                                                               | 3043170 | NJF             | 09/30/2010      | Added PSoC Device Characteristics table .<br>Added DC $I^2C$ Specifications table.<br>Added $F_{32K\_U}$ max limit.<br>Added $T_{jit\_IMO}$ specification, removed existing jitter specifications.<br>Updated Units of Measure, Acronyms, Glossary, and References sections.<br>Updated solder reflow specifications.<br>No specific changes were made to $I^2C$ Timing Diagram. Updated for clearer understanding.<br>Template and styles update.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| *N                                                                                                                                               | 3173718 | NJF             | 02/16/2011      | CY8C20134-12SX1I and CY8C20234-12SX2I typo error fixed in the ordering information table and changed in to CY8C20134-12SXI and CY8C20234-12SXI. Updated document version and date.<br>Updated package diagram to 001-12919 *C.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| *O                                                                                                                                               | 3248613 | TOF             | 06/10/2011      | Under <a href="#">Table 13</a> , the text “ <a href="#">Table 13</a> lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40^{\circ}C \leq T_A \leq 85^{\circ}C$ , 3.0 V to 3.6 V and $-40^{\circ}C \leq T_A \leq 85^{\circ}C$ , or 2.4 V to 3.0 V and $-40^{\circ}C \leq T_A \leq 85^{\circ}C$ , respectively. Typical parameters apply to 5 V, 3.3 V, and 2.7 V at $25^{\circ}C$ . These are for design guidance only.” changed to “ <a href="#">Table 13</a> lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40^{\circ}C \leq T_A \leq 85^{\circ}C$ , 3.0 V to 3.6 V and $-40^{\circ}C \leq T_A \leq 85^{\circ}C$ , or <a href="#">Table 14</a> for 2.4 V to 3.0 V and $-40^{\circ}C \leq T_A \leq 85^{\circ}C$ , respectively. Typical parameters apply to 5 V, 3.3 V, and 2.7 V at $25^{\circ}C$ . These are for design guidance only”.<br>Updated <a href="#">Table 34 on page 37</a> table.<br>Updated sections, “ <a href="#">Getting Started</a> ”, “ <a href="#">Development Tools</a> ”, and “ <a href="#">Designing with PSoC Designer</a> ” to remove references to the system level designs.<br>Updated package diagram 51-85066 to *E revision. |
| *P                                                                                                                                               | 3394775 | KPOL            | 10/04/2011      | Updated 16-pin SOIC and 16-pin QFN package drawings.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |

## Document History Page

| Document Title: CY8C20134/CY8C20234/CY8C20334/CY8C20434/CY8C20534/CY8C20634,<br>PSoC® Programmable System-on-Chip™<br>Document Number: 001-05356 |         |                 |                 |                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|--------------------------------------------------------------------------------------------------------------------------------------------------|---------|-----------------|-----------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Revision                                                                                                                                         | ECN     | Orig. of Change | Submission Date | Description of Change                                                                                                                                                                                                                                                                                                                                                                                                                              |
| *Q                                                                                                                                               | 3638597 | BVI             | 06/06/2012      | Updated F <sub>SCLK</sub> parameter in the <a href="#">Table 32, "SPI Slave AC Specifications,"</a> on page 31.<br>Changed t <sub>OUT_HIGH</sub> to t <sub>OUT_H</sub> in <a href="#">Table 31, "SPI Master AC Specifications,"</a> on page 31<br>Updated package diagrams:<br>001-13937 to *D<br>001-44613 to *B<br>Removed obsolete specs 001-17397 and 001-14503 referenced in page 40                                                          |
| *R                                                                                                                                               | 4306760 | PRKU            | 03/26/2014      | Added note to connect all V <sub>SS</sub> pins to one common GND plane.<br>Updated 16-pin COL (Sawn) package drawing.                                                                                                                                                                                                                                                                                                                              |
| *S                                                                                                                                               | 4455557 | DIMA            | 08/13/2014      | Replaced references of "Application Notes for Surface Mount Assembly of Amkor's MicroLeadFrame (MLF) Packages" with "Design Guidelines for Cypress Quad Flat No Extended Lead (QFN) Packaged Devices – AN72845" in all instances across the document.<br><br>Added CapSense Design Resources.<br><br>Updated <a href="#">Ordering Information</a> :<br>Updated <a href="#">Table 36</a> :<br>Added CY8C20234-12SXIT and its corresponding details. |
| *T                                                                                                                                               | 4748586 | DIMA            | 05/14/2015      | Removed "CapSense Design Resources".<br>Added <a href="#">More Information</a> .<br>Updated <a href="#">Packaging Dimensions</a> :<br>spec 51-85066 – Changed revision from *F to *G.<br>spec 001-13937 – Changed revision from *E to *F.<br>spec 51-85079 – Changed revision from *E to *F.<br>Updated to new template.<br>Completing Sunset Review.                                                                                              |