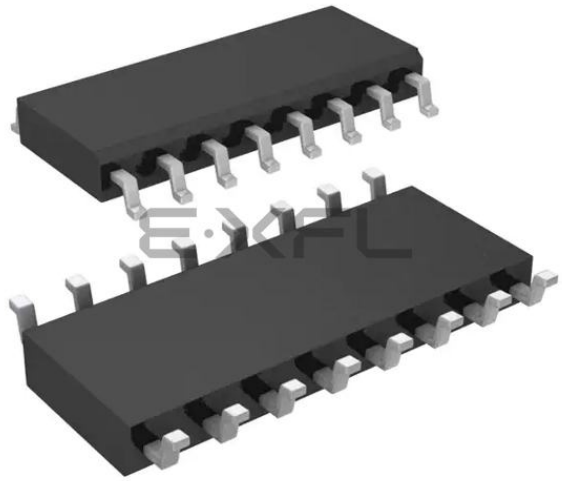


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	M8C
Core Size	8-Bit
Speed	12MHz
Connectivity	I²C, SPI
Peripherals	LVD, POR, WDT
Number of I/O	13
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.25V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	16-SOIC (0.154", 3.90mm Width)
Supplier Device Package	16-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c20234-12sxit

More Information

Cypress provides a wealth of data at www.cypress.com to help you to select the right PSoC device for your design, and to help you to quickly and effectively integrate the device into your design. For a comprehensive list of resources, see the knowledge base article KBA92181, Resources Available for CapSense® Controllers. Following is an abbreviated list for CapSense devices:

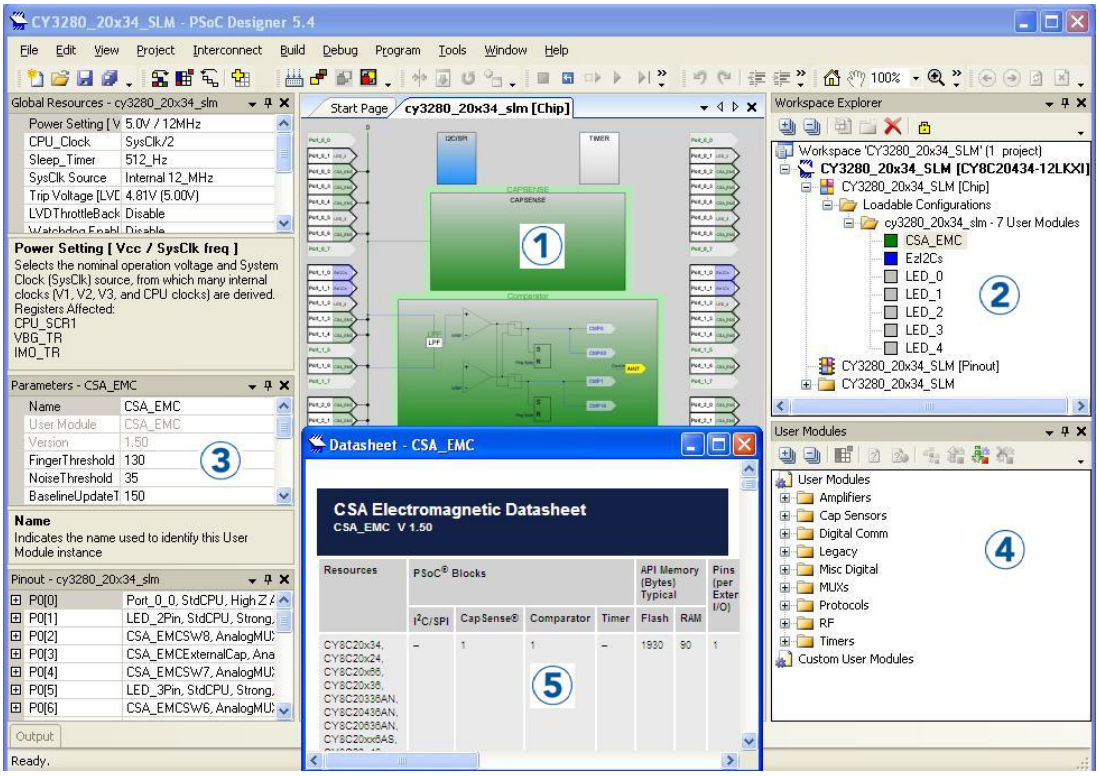
- Overview: CapSense Portfolio, CapSense Roadmap
- Product Selectors: CapSense, CapSense Plus, CapSense Express, PSoC3 with CapSense, PSoC5 with CapSense, PSoC4. In addition, PSoC Designer offers a device selection tool at the time of creating a new project.
- Application Notes: Cypress offers CapSense application notes covering a broad range of topics, from basic to advanced level. Recommended application notes for getting started with CapSense are:
  - AN64846 – Getting Started With CapSense
  - CY8C20x34 CapSense® Design Guide
  - AN2397 – CapSense® Data Viewing Tools
- Technical Reference Manual (TRM):
  - PSoC® CY8C20x24, CY8C20x34 Family Technical Reference Manual
- Development Kits:
  - CY3280-20x34 Universal CapSense Controller Kit features a predefined control circuitry and plug-in hardware to make prototyping and debugging easy. Programming and I2C-to-USB Bridge hardware are included for tuning and data acquisition.
  - CY3280-SLM Linear Slider Module Kit consists of five CapSense buttons, one linear slider (with ten sensors) and five LEDs. This module connects to any CY3280 Universal CapSense Controller Board, including CY3280-20x34 kit.
  - CY3280-BBM Universal CapSense Prototyping Module Kit provides access to every signal routed to the 44-pin connector on the attached controller board including CY3280-20x34 kit.
- Programming
  - PSoC supports a number of different programming modes and tools. For more information see the General Programming page.

PSoC Designer

PSoC Designer is a free Windows-based Integrated Design Environment (IDE). It enables concurrent hardware and firmware design of systems based on CapSense (see Figure 1). With PSoC Designer, you can:

1. Drag and drop User Modules to build your hardware system design in the main design workspace
2. Codesign your application firmware with the PSoC hardware, using the PSoC Designer IDE C compiler
3. Configure User Module
4. Explore the library of user modules
5. Review user module datasheets

Figure 1. PSoC Designer Features



Contents

Additional System Resources

System Resources provide additional capability useful to complete systems. Additional resources include low voltage detection and power on reset. Brief statements describing the merits of each system resource follow:

- The I^2C slave or SPI master-slave module provides 50/100/400 kHz communication over two wires. SPI communication over three or four wires run at speeds of 46.9 kHz to 3 MHz (lower for a slower system clock).
- Low voltage detection (LVD) interrupts signal the application of falling voltage levels, while the advanced POR (Power On Reset) circuit eliminates the need for a system supervisor.
- An internal 1.8 V reference provides an absolute reference for capacitive sensing.
- The 5 V maximum input, 3 V fixed output, low dropout regulator (LDO) provides regulation for I/Os. A register controlled bypass mode enables the user to disable the LDO.

PSoC Device Characteristics

Depending on your PSoC device characteristics, the digital and analog systems can have 16, 8, or 4 digital blocks, and 12, 6, or 4 analog blocks. Table 1 lists the resources available for specific PSoC device groups. The PSoC device covered by this datasheet is highlighted.

Table 1. PSoC Device Characteristics

PSoC Part Number	Digital I/O	Digital Rows	Digital Blocks	Analog Inputs	Analog Outputs	Analog Columns	Analog Blocks	SRAM Size	Flash Size
CY8C29x66	up to 64	4	16	up to 12	4	4	12	2 K	32 K
CY8C28xxx	up to 44	up to 3	up to 12	up to 44	up to 4	up to 6	up to 12 + 4[1]	1 K	16 K
CY8C27x43	up to 44	2	8	up to 12	4	4	12	256	16 K
CY8C24x94	up to 56	1	4	up to 48	2	2	6	1 K	16 K
CY8C24x23A	up to 24	1	4	up to 12	2	2	6	256	4 K
CY8C23x33	up to 26	1	4	up to 12	2	2	4	256	8 K
CY8C22x45	up to 38	2	8	up to 38	0	4	6[1]	1 K	16 K
CY8C21x45	up to 24	1	4	up to 24	0	4	6[1]	512	8 K
CY8C21x34	up to 28	1	4	up to 28	0	2	4[1]	512	8 K
CY8C21x23	up to 16	1	4	up to 8	0	2	4[1]	256	4 K
CY8C20x34	up to 28	0	0	up to 28	0	0	3[1,2]	512	8 K
CY8C20xx6	up to 36	0	0	up to 36	0	0	3[1,2]	up to 2 K	up to 32 K

Notes
1. Limited analog functionality
2. Two analog blocks and one CapSense®.

Development Tools

PSoC Designer™ is the revolutionary integrated design environment (IDE) that you can use to customize PSoC to meet your specific application requirements. PSoC Designer software accelerates system design and time to market. Develop your applications using a library of precharacterized analog and digital peripherals (called user modules) in a drag-and-drop design environment. Then, customize your design by leveraging the dynamically generated application programming interface (API) libraries of code. Finally, debug and test your designs with the integrated debug environment, including in-circuit emulation and standard software debug features. PSoC Designer includes:

- Application editor graphical user interface (GUI) for device and user module configuration and dynamic reconfiguration
- Extensive user module catalog
- Integrated source-code editor (C and assembly)
- Free C compiler with no size restrictions or time limits
- Built-in debugger
- In-circuit emulation
- Built-in support for communication interfaces:
  - Hardware and software I^2C slaves and masters
  - Full-speed USB 2.0
  - Up to four full-duplex universal asynchronous receiver/transmitters (UARTs), SPI master and slave, and wireless

PSoC Designer supports the entire library of PSoC 1 devices and runs on Windows XP, Windows Vista, and Windows 7.

PSoC Designer Software Subsystems

Design Entry

In the chip-level view, choose a base device to work with. Then select different onboard analog and digital components that use the PSoC blocks, which are called user modules. Examples of user modules are ADCs, DACs, amplifiers, and filters. Configure the user modules for your chosen application and connect them to each other and to the proper pins. Then generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The tool also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic reconfiguration makes it possible to change configurations at run time. In essence, this allows you to use more than 100 percent of PSoC's resources for an application.

Code Generation Tools

The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. You can develop your design in C, assembly, or a combination of the two.

Assemblers. The assemblers allow you to merge assembly code seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and are linked with other software modules to get absolute addressing.

C Language Compilers. C language compilers are available that support the PSoC family of devices. The products allow you to create complete C programs for the PSoC family devices. The optimizing C compilers provide all of the features of C, tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

Debugger

PSoC Designer has a debug environment that provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow you to read and program and read and write data memory, and read and write I/O registers. You can read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also allows you to create a trace buffer of registers and memory locations of interest.

Online Help System

The online help system displays online, context-sensitive help. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an online support Forum to aid the designer.

In-Circuit Emulator

A low-cost, high-functionality in-circuit emulator (ICE) is available for development support. This hardware can program single devices.

The emulator consists of a base unit that connects to the PC using a USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full-speed (24 MHz) operation.

Designing with PSoC Designer

The development process for the PSoC device differs from that of a traditional fixed function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and by lowering inventory costs. These configurable resources, called PSoC Blocks, have the ability to implement a wide variety of user-selectable functions. The PSoC development process is summarized in four steps:

1. Select User Modules.
2. Configure User Modules.
3. Organize and Connect.
4. Generate, Verify, and Debug.

Select User Modules

PSoC Designer provides a library of prebuilt, pretested hardware peripheral components called “user modules.” User modules make selecting and implementing peripheral devices, both analog and digital, simple.

Configure User Modules

Each user module that you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. For example, a PWM User Module configures one or more digital PSoC blocks, one for each 8 bits of resolution. The user module parameters permit you to establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus. All the user modules are documented in datasheets that may be viewed directly in PSoC Designer or on the Cypress website. These user module datasheets explain the internal operation of the user module and provide performance specifications. Each datasheet describes the use of each user module parameter, and other information you may need to successfully implement your design.

Organize and Connect

You build signal chains at the chip level by interconnecting user modules to each other and the I/O pins. You perform the selection, configuration, and routing so that you have complete control over all on-chip resources.

Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, you perform the “Generate Configuration Files” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system. The generated code provides application programming interfaces (APIs) with high-level functions to control and respond to hardware events at run-time and interrupt service routines that you can adapt as needed.

A complete code development environment allows you to develop and customize your applications in either C, assembly language, or both.

The last step in the development process takes place inside PSoC Designer’s debugger (access by clicking the Connect icon). PSoC Designer downloads the HEX image to the ICE where it runs at full speed. PSoC Designer debugging capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint, and watch-variable features, the debug interface provides a large trace buffer and allows you to define complex breakpoint events. These include monitoring address and data bus values, memory locations, and external signals.

Pin Information

This section describes, lists, and illustrates the CY8C20234, CY8C20334, CY8C20434, CY8C20534, and CY8C20634 PSoC device pins and pinout configurations.

The CY8C20x34 PSoC device is available in a variety of packages that are listed and shown in the following tables. Every port pin (labeled with a “P”) is capable of Digital I/O and connection to the common analog bus. However, V_{SS}, V_{DD}, and XRES are not capable of Digital I/O.

8-Pin SOIC Pinout

Figure 3. CY8C20134-12SXI 8-Pin SOIC Pinout

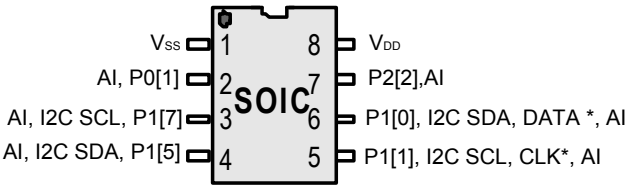


Table 2. Pin Definitions – CY8C20134 8-Pin (SOIC)

Pin No.	Digital	Analog	Name	Description
1	Power		V_{SS}	Ground connection
2	I/O	I	P0[1]	Analog column mux input, integrating input
3	I/O	I	P1[7]	I2C serial clock (SCL)
4	I/O	I	P1[5]	I2C serial data (SDA)
5	I/O	I	P1[1]	I2C serial clock (SCL), ISSP-SCLK
6	I/O	I	P1[0]	I2C serial data (SDA), ISSP-SDATA
7	I/O	I	P2[2]	Analog column mux input
8	Power		V_{DD}	Supply voltage

A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive.

16-Pin SOIC Pinout

Figure 4. CY8C20234-12SXI 16-Pin SOIC Pinout

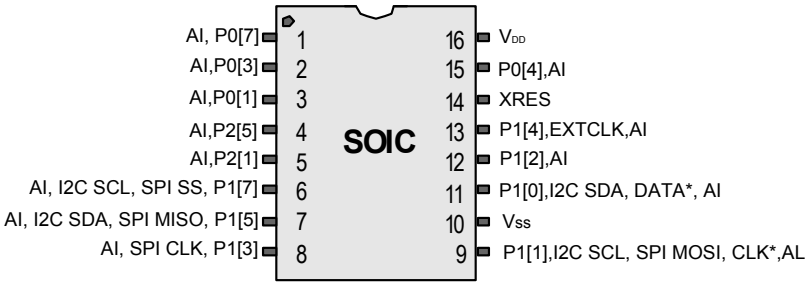


Table 3. Pin Definitions – CY8C20234 16-Pin (SOIC)

Pin No.	Digital	Analog	Name	Description
1	I/O	I	P0[7]	Analog column mux input
2	I/O	I	P0[3]	Analog column mux input and column input, integrating input
3	I/O	I	P0[1]	Analog column mux input, integrating input
4	I/O	I	P2[5]	Analog column mux input
5	I/O	I	P2[1]	Analog column mux input
6	I/O	I	P1[7]	I2C serial clock (SCL), SPI SS
7	I/O	I	P1[5]	I2C serial data (SDA),SPI MISO
8	I/O	I	P1[3]	Analog column mux input, SPI CLK
9	I/O	I	P1[1]	I2C serial clock (SCL), ISSP-SCLK,SPI MOSI
10	Power		V_{SS}	Ground connection
11	I/O	I	P1[0]	I2C serial data (SDA), ISSP-SDATA
12	I/O	I	P1[2]	Analog column mux input
13	I/O	I	P1[4]	Analog column mux input, optional external clock input (EXTCLK)
14	I/O	I	XRES	XRES
15	I/O	I	P0[4]	Analog column mux input
16	Power		V_{DD}	Supply voltage

A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive.

Table 7. Pin Definitions – CY8C20434 32-Pin (QFN) [9]

Pin No.	Type		Name	Description
	Digital	Analog		
18	I/O	I	P3[0]	
19	I/O	I	P3[2]	
20	I/O	I	P2[0]	
21	I/O	I	P2[2]	
22	I/O	I	P2[4]	
23	I/O	I	P2[6]	
24	I/O	I	P0[0]	
25	I/O	I	P0[2]	
26	I/O	I	P0[4]	
27	I/O	I	P0[6]	Analog bypass
28	Power		V_{DD}	Supply voltage
29	I/O	I	P0[7]	
30	I/O	I	P0[5]	
31	I/O	I	P0[3]	Integrating input
32	Power		V_{SS}	Ground connection[12]
CP	Power		V_{SS}	Center pad is connected to ground

A = Analog, I = Input, O = Output, OH = 5 mA high output drive.

Note
12. All V_{SS} pins should be brought out to one common GND plane.

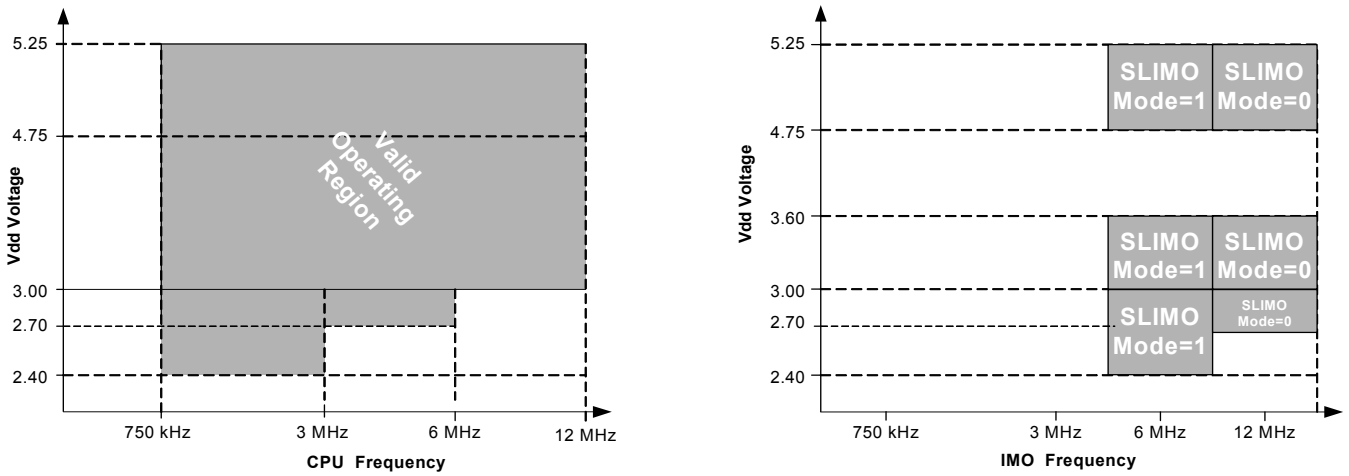
Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8C20234, CY8C20334, CY8C20434, CY8C20534, and CY8C20634 PSoC devices. For the latest electrical specifications, check the most recent datasheet by visiting the web at http://www.cypress.com.

Specifications are valid for –40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C as specified, except where mentioned.

Refer to Table 19 on page 25 for the electrical specifications on the internal main oscillator (IMO) using SLIMO mode.

Figure 11. Voltage versus CPU Frequency and IMO Frequency Trim Options



Absolute Maximum Ratings

Table 10. Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Units	Notes
T_{STG}	Storage Temperature	–55	25	+100	°C	Higher storage temperatures reduces data retention time. Recommended storage temperature is +25 °C ± 25 °C. Extended duration storage temperatures above 65 °C degrades reliability.
$T_{BAKETEMP}$	Bake temperature	–	125	See package label	°C	
$t_{BAKETIME}$	Bake time	See package label	–	72	Hours	
T_A	Ambient temperature with power applied	–40	–	+85	°C	
V_{DD}	Supply voltage on V_{DD} relative to V_{SS}	–0.5	–	+6.0	V	
V_{IO}	DC input voltage	V_{SS} – 0.5	–	V_{DD} + 0.5	V	
V_{IOZ}	DC voltage applied to tri-state	V_{SS} – 0.5	–	V_{DD} + 0.5	V	
I_{MIO}	Maximum current into any port pin	–25	–	+50	mA	
ESD	Electro static discharge voltage	2000	–	–	V	Human body model ESD.
LU	Latch-up current	–	–	200	mA	

Table 14. 2.7-V DC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{PU}	Pull-up resistor	4	5.6	8	kΩ	
V_{OH1}	High output voltage Port 1 pins with LDO regulator disabled	V_{DD} – 0.2	–	–	V	I_{OH} < 10 µA, maximum of 10 mA source current in all I/Os.
V_{OH2}	High output voltage Port 1 pins with LDO regulator disabled	V_{DD} – 0.5	–	–	V	I_{OH} = 2 mA, maximum of 10 mA source current in all I/Os.
V_{OL}	Low output voltage	–	–	0.75	V	I_{OL} = 10 mA, maximum of 30 mA sink current on even port pins (for example, P0[2] and P1[4]) and 30 mA sink current on odd port pins (for example, P0[3] and P1[5]).
I_{OH2}	High level source current port 1 Pins with LDO regulator disabled	2	–	–	mA	V_{OH} = V_{DD} – 0.5, for the limitations of the total current and I_{OH} at other V_{OH} levels see the notes for V_{OH}.
I_{OL}	Low level sink current	10	–	–	mA	V_{OH} = .75 V, see the limitations of the total current in the note for V_{OL}
V_{OLP1}	Low output voltage port 1 pins	–	–	0.4	V	I_{OL} = 5 mA Maximum of 50 mA sink current on even port pins (for example, P0[2] and P3[4]) and 50 mA sink current on odd port pins (for example, P0[3] and P2[5]). 2.4 V ≤ V_{DD} < 3.6 V
V_{IL}	Input low voltage	–	–	0.75	V	2.4 V ≤ V_{DD} < 3.6 V
V_{IH1}	Input high voltage	1.4	–	–	V	2.4 V ≤ V_{DD} < 2.7 V
V_{IH2}	Input high voltage	1.6	–	–	V	2.7 V ≤ V_{DD} < 3.6 V
V_H	Input hysteresis voltage	–	60	–	mV	
I_{IL}	Input leakage (absolute value)	–	1	–	nA	Gross tested to 1 µA
C_{IN}	Capacitive load on pins as input	0.5	1.7	5	pF	Package and pin dependent Temperature = 25 °C
C_{OUT}	Capacitive load on pins as output	0.5	1.7	5	pF	Package and pin dependent Temperature = 25 °C

DC Analog Mux Bus Specifications

Table 15 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C. These are for design guidance only.

Table 15. DC Analog Mux Bus Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{SW}	Switch resistance to common analog bus	–	–	400 800	Ω Ω	V_{DD} ≥ 2.7 V 2.4 V ≤ V_{DD} ≤ 2.7 V

DC POR and LVD Specifications

Table 16 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively.
Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C. These are for design guidance only.

Table 16. DC POR and LVD Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
	V_{DD} value for PPOR trip					V_{DD} is greater than or equal to 2.5 V during startup, reset from the XRES pin, or reset from watchdog.
V_{PPOR0}	PORLEV[1:0] = 00b	–	2.36	2.40	V	
V_{PPOR1}	PORLEV[1:0] = 01b	–	2.60	2.65	V	
V_{PPOR2}	PORLEV[1:0] = 10b	–	2.82	2.95	V	
	V_{DD} value for LVD trip					
V_{LVD0}	VM[2:0] = 000b	2.39	2.45	2.51[17]	V	
V_{LVD1}	VM[2:0] = 001b	2.54	2.71	2.78[18]	V	
V_{LVD2}	VM[2:0] = 010b	2.75	2.92	2.99[19]	V	
V_{LVD3}	VM[2:0] = 011b	2.85	3.02	3.09	V	
V_{LVD4}	VM[2:0] = 100b	2.96	3.13	3.20	V	
V_{LVD5}	VM[2:0] = 101b	–	–	–	V	
V_{LVD6}	VM[2:0] = 110b	–	–	–	V	
V_{LVD7}	VM[2:0] = 111b	4.52	4.73	4.83	V	

Notes
17. Always greater than 50 mV above V_{PPOR} (PORLEV = 00) for falling supply.
18. Always greater than 50 mV above V_{PPOR} (PORLEV = 01) for falling supply.
19. Always greater than 50 mV above V_{PPOR} (PORLEV = 10) for falling supply.

DC Programming Specifications

Table 17 lists the guaranteed minimum and maximum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C. These are for design guidance only. Flash endurance and retention specifications with the use of the EEPROM User Module are valid only within the range: 25 °C +/–20C during the Flash Write operation. Reference the EEPROM User Module datasheet instructions for EEPROM flash write requirements outside of the 25 °C +/–20 °C temperature window.

Table 17. DC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{DDP}	V_{DD} for programming and erase	4.5	5	5.5	V	This specification applies to the functional requirements of external programmer tools
V_{DDLV}	Low V_{DD} for verify	2.4	2.5	2.6	V	This specification applies to the functional requirements of external programmer tools
V_{DDHV}	High V_{DD} for verify	5.1	5.2	5.3	V	This specification applies to the functional requirements of external programmer tools
$V_{DDIWRITE}$	Supply voltage for flash write operation	2.7	–	5.25	V	This specification applies to this device when it is executing internal flash writes
I_{DDP}	Supply current during programming or verify	–	5	25	mA	
V_{ILP}	Input low voltage during programming or verify	–	–	0.8	V	
V_{IHP}	Input high voltage during programming or verify	2.2	–	–	V	
I_{ILP}	Input current when applying V_{ILP} to P1[0] or P1[1] during programming or verify	–	–	0.2	mA	Driving internal pull-down resistor.
I_{IHP}	Input current when applying V_{IHP} to P1[0] or P1[1] during programming or verify	–	–	1.5	mA	Driving internal pull-down resistor.
V_{OLV}	Output low voltage during programming or verify	–	–	V_{SS} + 0.75	V	
V_{OHV}	Output high voltage during programming or verify	V_{DD} – 1.0	–	V_{DD}	V	
$Flash_{ENPB}$	Flash endurance (per block)	50,000[21]	–	–	–	Erase/write cycles per block.
$Flash_{ENT}$	Flash endurance (total)[20]	1,800,000	–	–	–	Erase/write cycles.
$Flash_{DR}$	Flash data retention	10	–	–	Years	

Notes
20. A maximum of 36 × 50,000 block endurance cycles is allowed. This is balanced between operations on 36 × 1 blocks of 50,000 maximum cycles each, 36 × 2 blocks of 25,000 maximum cycles each, or 36 × 4 blocks of 12,500 maximum cycles each (to limit the total number of cycles to 36 × 50,000 and that no single block ever sees more than 50,000 cycles).
21. The 50,000 cycle flash endurance per block is only guaranteed if the flash is operating within one voltage range. Voltage ranges are 2.4 V to 3.0 V, 3.0 V to 3.6 V and 4.75 V to 5.25 V.

AC SPI Specifications

Table 31 and Table 32 list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C. These are for design guidance only.

Table 31. SPI Master AC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
F_{SCLK}	SCLK clock frequency	–	–	–	12	MHz
DC_{SCLK}	SCLK duty cycle	–	–	50	–	%
t_{SETUP}	MISO to SCLK setup time	–	40	–	–	ns
t_{HOLD}	SCLK to MISO hold time	–	40	–	–	ns
t_{OUT_VAL}	SCLK to MOSI valid time	–	–	–	40	ns
t_{OUT_H}	MOSI high time	–	40	–	–	ns

Table 32. SPI Slave AC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
F_{SCLK}	SCLK clock frequency	–	–	–	4	MHz
t_{LOW}	SCLK low time	–	41.67	–	–	ns
t_{HIGH}	SCLK high time	–	41.67	–	–	ns
t_{SETUP}	MOSI to SCLK setup time	–	30	–	–	ns
t_{HOLD}	SCLK to MOSI hold time	–	50	–	–	ns
t_{SS_MISO}	SS low to MISO valid	–	–	–	153	ns
t_{SCLK_MISO}	SCLK to MISO valid	–	–	–	125	ns
t_{SS_HIGH}	SS high time	–	50	–	–	ns
t_{SS_SCLK}	Time from SS low to first SCLK	–	$2/F_{SCLK}$	–	–	ns
t_{SCLK_SS}	Time from last SCLK to SS high	–	$2/F_{SCLK}$	–	–	ns

Packaging Dimensions

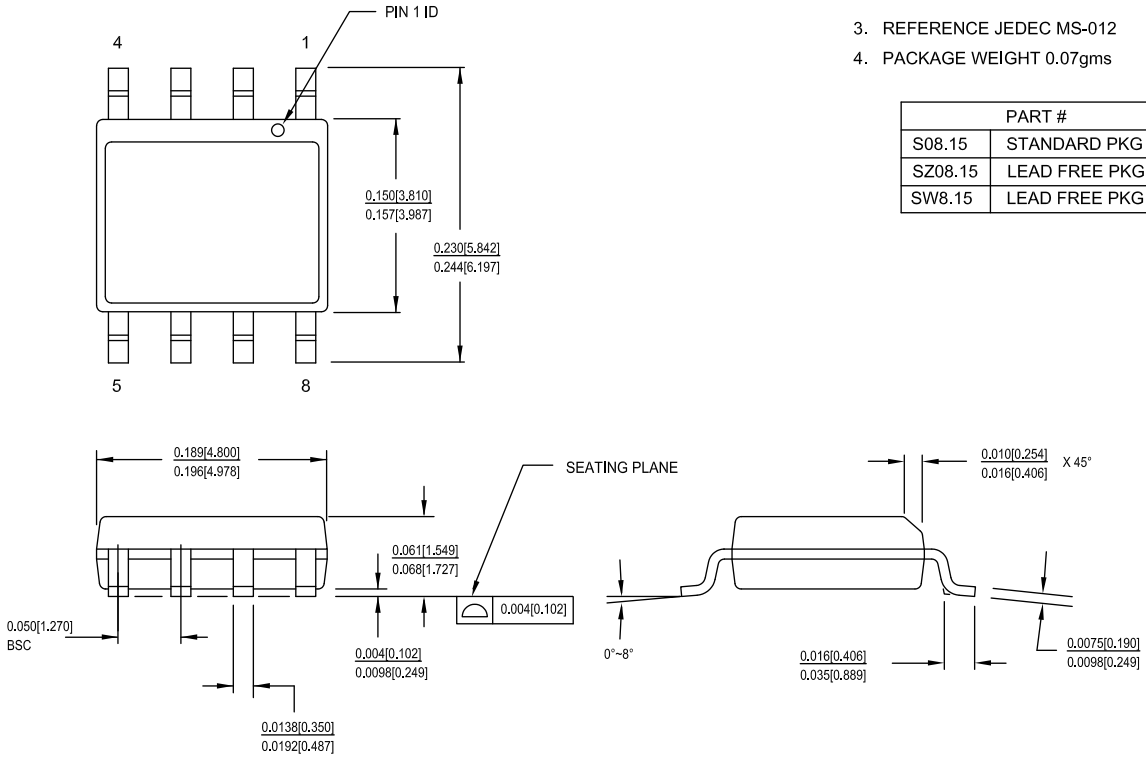
This section illustrates the packaging specifications for the CY8C20234, CY8C20334, CY8C20434, CY8C20534, and CY8C20634 PSoC devices along with the thermal impedances for each package.

Important Note Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulation tools' dimensions, refer to the emulator pod drawings at http://www.cypress.com.

Figure 14. 8-pin SOIC (150 Mils)

1. DIMENSIONS IN INCHES[MM] MIN.
   MAX.
2. PIN 1 ID IS OPTIONAL,
   ROUND ON SINGLE LEADFRAME
   RECTANGULAR ON MATRIX LEADFRAME
3. REFERENCE JEDEC MS-012
4. PACKAGE WEIGHT 0.07gms

PART #	
S08.15	STANDARD PKG
SZ08.15	LEAD FREE PKG
SW8.15	LEAD FREE PKG



51-85066 *G

Development Tool Selection

Software

PSoC Designer™

At the core of the PSoC development software suite is PSoC Designer, used to generate PSoC firmware applications. PSoC Designer is available free of charge at http://www.cypress.com and includes a free C compiler.

PSoC Programmer

PSoC Programmer is flexible enough and is used on the bench in development and also suitable for factory programming. PSoC Programmer works either as a standalone programming application or operates directly from PSoC Designer. PSoC Programmer software is compatible with both PSoC ICE Cube In-Circuit Emulator and PSoC MiniProg. PSoC programmer is available free of charge at http://www.cypress.com.

Development Kits

All development kits are sold at the Cypress Online Store.

CY3215-DK Basic Development Kit

The CY3215-DK is for prototyping and development with PSoC Designer. This kit supports in-circuit emulation and the software interface enables users to run, halt, and single step the processor and view the content of specific memory locations. PSoC Designer supports the advance emulation features also. The kit includes:

- PSoC Designer Software CD
- ICE-Cube In-Circuit Emulator
- ICE Flex-Pod for CY8C29x66 Family
- Cat-5 Adapter
- Mini-Eval Programming Board
- 110 ~ 240V Power Supply, Euro-Plug Adapter
- iMAGEcraft C Compiler (Registration Required)
- ISSP Cable
- USB 2.0 Cable and Blue Cat-5 Cable
- 2 CY8C29466-24PXI 28-PDIP Chip Samples

Evaluation Tools

All evaluation tools are sold at the Cypress Online Store.

CY3210-MiniProg1

The CY3210-MiniProg1 kit enables the user to program PSoC devices via the MiniProg1 programming unit. The MiniProg is a small, compact prototyping programmer that connects to the PC via a provided USB 2.0 cable. The kit includes:

- MiniProg Programming Unit
- MiniEval Socket Programming and Evaluation Board
- 28-Pin CY8C29466-24PXI PDIP PSoC Device Sample
- 28-Pin CY8C27443-24PXI PDIP PSoC Device Sample
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

CY3210-PSoCEval1

The CY3210-PSoCEval1 kit features an evaluation board and the MiniProg1 programming unit. The evaluation board includes an LCD module, potentiometer, LEDs, and plenty of bread-boarding space to meet all of your evaluation needs. The kit includes:

- Evaluation Board with LCD Module
- MiniProg Programming Unit
- 28-Pin CY8C29466-24PXI PDIP PSoC Device Sample (2)
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

CY3214-PSoCEvalUSB

The CY3214-PSoCEvalUSB evaluation kit features a development board for the CY8C24794-24LFXI PSoC device. Special features of the board include both USB and capacitive sensing development and debugging support. This evaluation board also includes an LCD module, potentiometer, LEDs, an enunciator and plenty of bread boarding space to meet all of your evaluation needs. The kit includes:

- PSoCEvalUSB Board
- LCD Module
- MIniProg Programming Unit
- Mini USB Cable
- PSoC Designer and Example Projects CD
- Getting Started Guide
- Wire Pack

Device Programmers

All device programmers are purchased from the Cypress Online Store.

CY3216 Modular Programmer

The CY3216 Modular Programmer kit features a modular programmer and the MiniProg1 programming unit. The modular programmer includes three programming module cards and supports multiple Cypress products. The kit includes:

- Modular Programmer Base
- 3 Programming Module Cards
- MiniProg Programming Unit
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

CY3207ISSP In-System Serial Programmer (ISSP)

The CY3207ISSP is a production programmer. It includes protection circuitry and an industrial case that is more robust than the MiniProg in a production programming environment. Note that CY3207ISSP needs special software and is not compatible with PSoC Programmer. The kit includes:

- CY3207 Programmer Unit
- PSoC ISSP Software CD
- 110 ~ 240V Power Supply, Euro-Plug Adapter
- USB 2.0 Cable

Accessories (Emulation and Programming)

Table 35. Emulation and Programming Accessories

Part Number	Pin Package	Flex-Pod Kit [31]	Foot Kit [32]	Prototyping Module	Adapter [33]
CY8C20234-12LKXI	16 QFN	Not Available	CY3250-16QFN-FK	CY3210-20X34	Not Available
CY8C20334-12LQXI	24 QFN	CY3250-20334QFN	CY3250-24QFN-FK	CY3210-20X34	AS-24-28-01ML-6
CY8C20634-12FDXI	30 WLCSP	Not available		CY3210-20X34	Not Available

Notes
31. Dual function Digital I/O Pins also connect to the common analog mux.
32. This part may be used for in-circuit debugging. It is NOT available for production.
33. Programming adapter converts non-DIP package to DIP footprint. Specific details and ordering information for each of the adapters is available at http://www.emulation.com.

Ordering Information

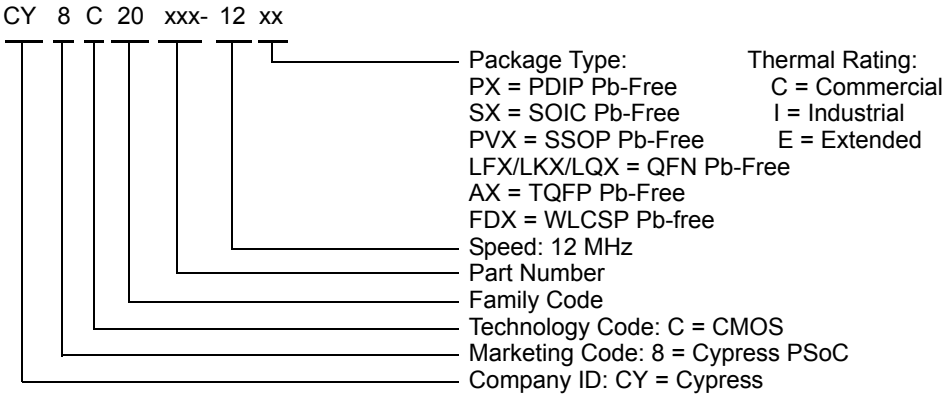
Table 36 lists the CY8C20234, CY8C20334, CY8C20434, CY8C20534, and CY8C20634 PSoC device's key package features and ordering codes.

Table 36. PSoC Device Key Features and Ordering Information

Ordering Code	Package	Flash (Bytes)	SRAM (Bytes)	Digital Blocks	CapSense-Blocks	Digital I/O Pins	Analog Inputs	Analog Outputs	XRES Pin
CY8C20134-12SXI	8-Pin SOIC	8 K	512	0	1	6	6	0	No
CY8C20234-12SXI	16-Pin SOIC	8 K	512	0	1	13	13	0	Yes
CY8C20234-12SXIT	16-pin SOIC	8 K	512	0	1	13	13	0	Yes
CY8C20534-12PVXI	28-Pin SSOP	8 K	512	0	1	24	24[31]	0	Yes
CY8C20534-12PVXIT	28-Pin SSOP	8 K	512	0	1	24	24[31]	0	Yes
CY8C20000-12LFXI	48-Pin OCD QFN[16]	8 K	512	0	1	28	28[31]	0	Yes
CY8C20234-12LKXI	16-Pin (3 × 3 mm 0.60 Max) Sawn QFN	8 K	512	0	1	13	13[31]	0	Yes
CY8C20234-12LKXIT	16-Pin (3 × 3 mm 0.60 Max) Sawn QFN (Tape and Reel)	8 K	512	0	1	13	13[31]	0	Yes
CY8C20334-12LQXI	24-Pin (4 × 4 mm 0.60 Max) Sawn QFN	8 K	512	0	1	20	20[31]	0	Yes
CY8C20334-12LQXIT	24-Pin (4 × 4 mm 0.60 Max) Sawn QFN (Tape and Reel)	8 K	512	0	1	20	20[31]	0	Yes
CY8C20434-12LQXI	32-Pin (5 × 5 mm 0.60 Max) Thin Sawn QFN	8 K	512	0	1	28	28	0	Yes
CY8C20434-12LQXIT	32-Pin (5 × 5 mm 0.60 Max) Thin Sawn QFN (Tape and Reel)	8 K	512	0	1	28	28	0	Yes
CY8C20634-12FDXI	30-Ball WLCSP	8 K	512	0	1	27	27	0	Yes
CY8C20634-12FDXIT	30-Ball WLCSP (Tape and Reel)	8 K	512	0	1	27	27	0	Yes

Note For Die sales information, contact a local Cypress sales office or Field Applications Engineer (FAE).

Ordering Code Definitions



Document Conventions

Units of Measure

Table 38 lists the unit sof measures.

Table 38. Units of Measure

Symbol	Unit of Measure	Symbol	Unit of Measure
°C	degree Celsius	ms	millisecond
pF	picofarad	ns	nanosecond
kHz	kilohertz	ps	picosecond
MHz	megahertz	µV	microvolts
kΩ	kilohm	mV	millivolts
Ω	ohm	V	volts
µA	microampere	W	watt
mA	milliampere	mm	millimeter
nA	nanoampere	%	percent
µs	microsecond		

Numeric Conventions

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase ‘h’ (for example, ‘14h’ or ‘3Ah’). Hexadecimal numbers may also be represented by a ‘0x’ prefix, the C coding convention. Binary numbers have an appended lowercase ‘b’ (for example, 01010100b’ or ‘01000011b’). Numbers not indicated by an ‘h’ or ‘b’ are decimals.

Glossary

active high	1. A logic signal having its asserted state as the logic 1 state. 2. A logic signal having the logic 1 state as the higher voltage of the two states.
analog blocks	The basic programmable opamp circuits. These are SC (switched capacitor) and CT (continuous time) blocks. These blocks can be interconnected to provide ADCs, DACs, multi-pole filters, gain stages, and much more.
analog-to-digital (ADC)	A device that changes an analog signal to a digital signal of corresponding magnitude. Typically, an ADC converts a voltage to a digital number. The digital-to-analog (DAC) converter performs the reverse operation.
Application programming interface (API)	A series of software routines that comprise an interface between a computer application and lower level services and functions (for example, user modules and libraries). APIs serve as building blocks for programmers that create software applications.
asynchronous	A signal whose data is acknowledged or acted upon immediately, irrespective of any clock signal.
Bandgap reference	A stable voltage reference design that matches the positive temperature coefficient of VT with the negative temperature coefficient of VBE, to produce a zero temperature coefficient (ideally) reference.
bandwidth	1. The frequency range of a message or information processing system measured in hertz. 2. The width of the spectral region over which an amplifier (or absorber) has substantial gain (or loss); it is sometimes represented more specifically as, for example, full width at half maximum.
bias	1. A systematic deviation of a value from a reference value. 2. The amount by which the average of a set of values departs from a reference value. 3. The electrical, mechanical, magnetic, or other force (field) applied to a device to establish a reference level to operate the device.

Glossary

External Reset (XRES)	An active high signal that is driven into the PSoC device. It causes all operation of the CPU and blocks to stop and return to a pre-defined state.
Flash	An electrically programmable and erasable, non-volatile technology that provides you the programmability and data storage of EPROMs, plus in-system erasability. Non-volatile means that the data is retained when power is OFF.
Flash block	The smallest amount of Flash ROM space that may be programmed at one time and the smallest amount of Flash space that may be protected. A Flash block holds 64 bytes.
frequency	The number of cycles or events per unit of time, for a periodic function.
gain	The ratio of output current, voltage, or power to input current, voltage, or power, respectively. Gain is usually expressed in dB.
I^2C	A two-wire serial computer bus by Philips Semiconductors (now NXP Semiconductors). I2C is an Inter-Integrated Circuit. It is used to connect low-speed peripherals in an embedded system. The original system was created in the early 1980s as a battery control interface, but it was later used as a simple internal bus system for building control electronics. I2C uses only two bi-directional pins, clock and data, both running at +5V and pulled high with resistors. The bus operates at 100 kbits/second in standard mode and 400 kbits/second in fast mode.
ICE	The in-circuit emulator that allows you to test the project in a hardware environment, while viewing the debugging device activity in a software environment (PSoC Designer).
input/output (I/O)	A device that introduces data into or extracts data from a system.
interrupt	A suspension of a process, such as the execution of a computer program, caused by an event external to that process, and performed in such a way that the process can be resumed.
interrupt service routine (ISR)	A block of code that normal code execution is diverted to when the M8C receives a hardware interrupt. Many interrupt sources may each exist with its own priority and individual ISR code block. Each ISR code block ends with the RETI instruction, returning the device to the point in the program where it left normal program execution.
jitter	1. A misplacement of the timing of a transition from its ideal position. A typical form of corruption that occurs on serial data streams. 2. The abrupt and unwanted variations of one or more signal characteristics, such as the interval between successive pulses, the amplitude of successive cycles, or the frequency or phase of successive cycles.
low-voltage detect (LVD)	A circuit that senses V_{DD} and provides an interrupt to the system when V_{DD} falls lower than a selected threshold.
M8C	An 8-bit Harvard-architecture microprocessor. The microprocessor coordinates all activity inside a PSoC by interfacing to the Flash, SRAM, and register space.
master device	A device that controls the timing for data exchanges between two devices. Or when devices are cascaded in width, the master device is the one that controls the timing for data exchanges between the cascaded devices and an external interface. The controlled device is called the ***slave device.***
microcontroller	An integrated circuit chip that is designed primarily for control systems and products. In addition to a CPU, a microcontroller typically includes memory, timing circuits, and IO circuitry. The reason for this is to permit the realization of a controller with a minimal quantity of chips, thus achieving maximal possible miniaturization. This in turn, reduces the volume and the cost of the controller. The microcontroller is normally not used for general-purpose computation as is a microprocessor.
mixed-signal	The reference to a circuit containing both analog and digital techniques and components.

Document History Page

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Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*Q	3638597	BVI	06/06/2012	Updated F_{SCLK} parameter in the Table 32, “SPI Slave AC Specifications,” on page 31. Changed t_{OUT_HIGH} to t_{OUT_H} in Table 31, “SPI Master AC Specifications,” on page 31 Updated package diagrams: 001-13937 to *D 001-44613 to *B Removed obsolete specs 001-17397 and 001-14503 referenced in page 40
*R	4306760	PRKU	03/26/2014	Added note to connect all V_{SS} pins to one common GND plane. Updated 16-pin COL (Sawn) package drawing.
*S	4455557	DIMA	08/13/2014	Replaced references of “Application Notes for Surface Mount Assembly of Amkor’s MicroLeadFrame (MLF) Packages” with “Design Guidelines for Cypress Quad Flat No Extended Lead (QFN) Packaged Devices – AN72845” in all instances across the document. Added CapSense Design Resources. Updated Ordering Information: Updated Table 36: Added CY8C20234-12SXIT and its corresponding details.
*T	4748586	DIMA	05/14/2015	Removed “CapSense Design Resources”. Added More Information. Updated Packaging Dimensions: spec 51-85066 – Changed revision from *F to *G. spec 001-13937 – Changed revision from *E to *F. spec 51-85079 – Changed revision from *E to *F. Updated to new template. Completing Sunset Review.