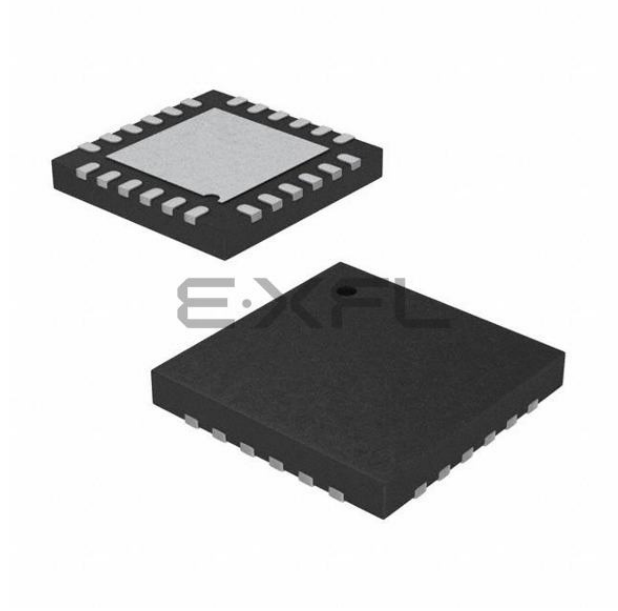


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	M8C
Core Size	8-Bit
Speed	12MHz
Connectivity	I²C, SPI
Peripherals	LVD, POR, WDT
Number of I/O	20
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.25V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	24-UFQFN Exposed Pad
Supplier Device Package	24-QFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c20334-12lqxi

More Information

Cypress provides a wealth of data at www.cypress.com to help you to select the right PSoC device for your design, and to help you to quickly and effectively integrate the device into your design. For a comprehensive list of resources, see the knowledge base article KBA92181, Resources Available for CapSense® Controllers. Following is an abbreviated list for CapSense devices:

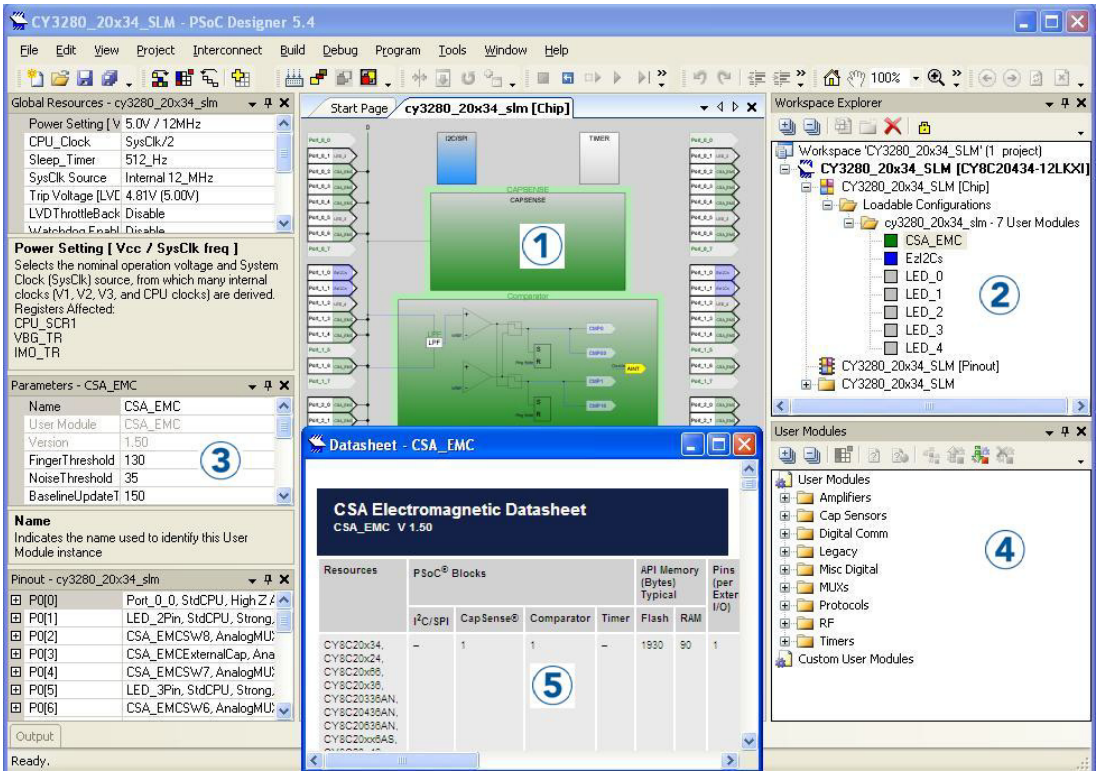
- Overview: CapSense Portfolio, CapSense Roadmap
- Product Selectors: CapSense, CapSense Plus, CapSense Express, PSoC3 with CapSense, PSoC5 with CapSense, PSoC4. In addition, PSoC Designer offers a device selection tool at the time of creating a new project.
- Application Notes: Cypress offers CapSense application notes covering a broad range of topics, from basic to advanced level. Recommended application notes for getting started with CapSense are:
  - AN64846 – Getting Started With CapSense
  - CY8C20x34 CapSense® Design Guide
  - AN2397 – CapSense® Data Viewing Tools
- Technical Reference Manual (TRM):
  - PSoC® CY8C20x24, CY8C20x34 Family Technical Reference Manual
- Development Kits:
  - CY3280-20x34 Universal CapSense Controller Kit features a predefined control circuitry and plug-in hardware to make prototyping and debugging easy. Programming and I2C-to-USB Bridge hardware are included for tuning and data acquisition.
  - CY3280-SLM Linear Slider Module Kit consists of five CapSense buttons, one linear slider (with ten sensors) and five LEDs. This module connects to any CY3280 Universal CapSense Controller Board, including CY3280-20x34 kit.
  - CY3280-BBM Universal CapSense Prototyping Module Kit provides access to every signal routed to the 44-pin connector on the attached controller board including CY3280-20x34 kit.
- Programming
  - PSoC supports a number of different programming modes and tools. For more information see the General Programming page.

PSoC Designer

PSoC Designer is a free Windows-based Integrated Design Environment (IDE). It enables concurrent hardware and firmware design of systems based on CapSense (see Figure 1). With PSoC Designer, you can:

1. Drag and drop User Modules to build your hardware system design in the main design workspace
2. Codesign your application firmware with the PSoC hardware, using the PSoC Designer IDE C compiler
3. Configure User Module
4. Explore the library of user modules
5. Review user module datasheets

Figure 1. PSoC Designer Features



Additional System Resources

System Resources provide additional capability useful to complete systems. Additional resources include low voltage detection and power on reset. Brief statements describing the merits of each system resource follow:

- The I^2C slave or SPI master-slave module provides 50/100/400 kHz communication over two wires. SPI communication over three or four wires run at speeds of 46.9 kHz to 3 MHz (lower for a slower system clock).
- Low voltage detection (LVD) interrupts signal the application of falling voltage levels, while the advanced POR (Power On Reset) circuit eliminates the need for a system supervisor.
- An internal 1.8 V reference provides an absolute reference for capacitive sensing.
- The 5 V maximum input, 3 V fixed output, low dropout regulator (LDO) provides regulation for I/Os. A register controlled bypass mode enables the user to disable the LDO.

PSoC Device Characteristics

Depending on your PSoC device characteristics, the digital and analog systems can have 16, 8, or 4 digital blocks, and 12, 6, or 4 analog blocks. Table 1 lists the resources available for specific PSoC device groups. The PSoC device covered by this datasheet is highlighted.

Table 1. PSoC Device Characteristics

PSoC Part Number	Digital I/O	Digital Rows	Digital Blocks	Analog Inputs	Analog Outputs	Analog Columns	Analog Blocks	SRAM Size	Flash Size
CY8C29x66	up to 64	4	16	up to 12	4	4	12	2 K	32 K
CY8C28xxx	up to 44	up to 3	up to 12	up to 44	up to 4	up to 6	up to 12 + 4[1]	1 K	16 K
CY8C27x43	up to 44	2	8	up to 12	4	4	12	256	16 K
CY8C24x94	up to 56	1	4	up to 48	2	2	6	1 K	16 K
CY8C24x23A	up to 24	1	4	up to 12	2	2	6	256	4 K
CY8C23x33	up to 26	1	4	up to 12	2	2	4	256	8 K
CY8C22x45	up to 38	2	8	up to 38	0	4	6[1]	1 K	16 K
CY8C21x45	up to 24	1	4	up to 24	0	4	6[1]	512	8 K
CY8C21x34	up to 28	1	4	up to 28	0	2	4[1]	512	8 K
CY8C21x23	up to 16	1	4	up to 8	0	2	4[1]	256	4 K
CY8C20x34	up to 28	0	0	up to 28	0	0	3[1,2]	512	8 K
CY8C20xx6	up to 36	0	0	up to 36	0	0	3[1,2]	up to 2 K	up to 32 K

Notes
1. Limited analog functionality
2. Two analog blocks and one CapSense®.

Pin Information

This section describes, lists, and illustrates the CY8C20234, CY8C20334, CY8C20434, CY8C20534, and CY8C20634 PSoC device pins and pinout configurations.

The CY8C20x34 PSoC device is available in a variety of packages that are listed and shown in the following tables. Every port pin (labeled with a “P”) is capable of Digital I/O and connection to the common analog bus. However, V_{SS}, V_{DD}, and XRES are not capable of Digital I/O.

8-Pin SOIC Pinout

Figure 3. CY8C20134-12SXI 8-Pin SOIC Pinout

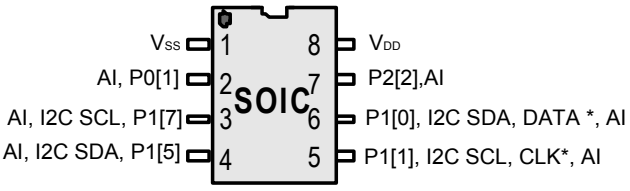


Table 2. Pin Definitions – CY8C20134 8-Pin (SOIC)

Pin No.	Digital	Analog	Name	Description
1	Power		V_{SS}	Ground connection
2	I/O	I	P0[1]	Analog column mux input, integrating input
3	I/O	I	P1[7]	I2C serial clock (SCL)
4	I/O	I	P1[5]	I2C serial data (SDA)
5	I/O	I	P1[1]	I2C serial clock (SCL), ISSP-SCLK
6	I/O	I	P1[0]	I2C serial data (SDA), ISSP-SDATA
7	I/O	I	P2[2]	Analog column mux input
8	Power		V_{DD}	Supply voltage

A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive.

16-Pin Part Pinout

Figure 6. CY8C20234 16-Pin PSoC Device

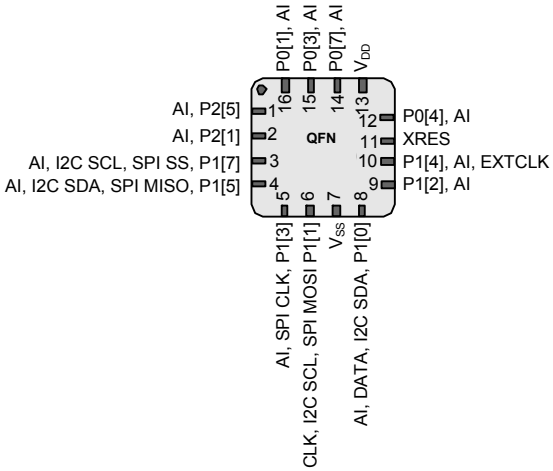


Table 5. Pin Definitions – CY8C20234 16-Pin (QFN no e-pad)

Pin No.	Type		Name	Description
	Digital	Analog		
1	I/O	I	P2[5]	
2	I/O	I	P2[1]	
3	I_{OH}	I	P1[7]	I^2C SCL, SPI SS
4	I_{OH}	I	P1[5]	I^2C SDA, SPI MISO
5	I_{OH}	I	P1[3]	SPI CLK
6	I_{OH}	I	P1[1]	CLK[6], I^2C SCL, SPI MOSI
7	Power		V_{SS}	Ground connection
8	I_{OH}	I	P1[0]	DATA[6], I^2C SDA
9	I_{OH}	I	P1[2]	
10	I_{OH}	I	P1[4]	Optional external clock input (EXTCLK)
11	Input		XRES	Active high external reset with internal pull-down
12	I/O	I	P0[4]	
13	Power		V_{DD}	Supply voltage
14	I/O	I	P0[7]	
15	I/O	I	P0[3]	Integrating Input
16	I/O	I	P0[1]	

A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive

Note
6. These are the ISSP pins, that are not High Z at POR (Power-on-Reset). See the *PSoC Technical Reference Manual* for details.

30-Ball Part Pinout

Figure 10. CY8C20634 30-Ball PSoC Device

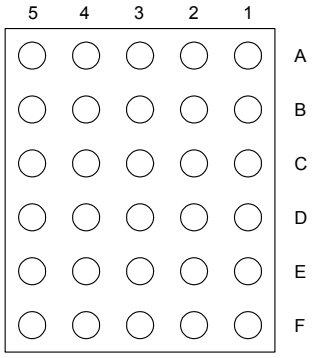


Table 9. 30-Ball Part Pinout (WLCSP)

Pin No.	Type		Name	Description
	Digital	Analog		
A1	Power		V_{DD}	Supply voltage
A2	I/O	I	P0[6]	Analog bypass
A3	I/O	I	P0[4]	
A4	I/O	I	P0[3]	Integrating input
A5	I/O	I	P2[7]	
B1	I/O	I	P0[2]	
B2	I/O	I	P0[0]	
B3	I/O	I	P2[6]	
B4	I/O	I	P0[5]	
B5	I/O	I	P0[1]	
C1	I/O	I	P2[4]	
C2	I/O	I	P2[2]	
C3	I/O	I	P3[1]	
C4	I/O	I	P0[7]	
C5	I/O	I	P2[1]	
D1	I/O	I	P2[0]	
D2	I/O	I	P3[0]	
D3	I/O	I	P3[2]	
D4	I_{OH}	I	P1[1]	CLK[15], I^2C SCL, SPI MOSI
D5	I/O	I	P2[3]	
E1	Input		XRES	Active high external reset with internal pull-down
E2	I_{OH}	I	P1[6]	
E3	I_{OH}	I	P1[4]	Optional external clock input (EXTCLK)
E4	I_{OH}	I	P1[5]	I^2C SDA, SPI MISO
E5	I/O	I	P2[5]	
F1	Power		V_{SS}	Ground connection[16]
F2	I_{OH}	I	P1[2]	
F3	I_{OH}	I	P1[0]	DATA[15], I^2C SDA
F4	I_{OH}	I	P1[3]	SPI CLK
F5	I_{OH}	I	P1[7]	I^2C SCL, SPI SS

A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive.

Notes
15. These are the ISSP pins, that are not High Z at POR (Power-on-Reset). See the *PSoC Technical Reference Manual* for details.
16. All V_{SS} pins should be brought out to one common GND plane.

Operating Temperature

Table 11. Operating Temperature

Symbol	Description	Min	Typ	Max	Units	Notes
T_A	Ambient temperature	–40	–	+85	°C	
T_J	Junction temperature	–40	–	+100	°C	The temperature rise from ambient to junction is package specific. See Table 16 on page 23. The user must limit the power consumption to comply with this requirement.

DC Electrical Characteristics

DC Chip Level Specifications

Table 12 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0V to 3.6V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C. These are for design guidance only.

Table 12. DC Chip Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{DD}	Supply voltage	2.40	–	5.25	V	See Table 16 on page 23.
I_{DD12}	Supply current, IMO = 12 MHz	–	1.5	2.5	mA	Conditions are V_{DD} = 3.0 V, T_A = 25 °C, CPU = 12 MHz.
I_{DD6}	Supply current, IMO = 6 MHz	–	1	1.5	mA	Conditions are V_{DD} = 3.0 V, T_A = 25 °C, CPU = 6 MHz
I_{SB27}	Sleep (mode) current with POR, LVD, Sleep timer, WDT, and internal slow oscillator active. Mid temperature range.	–	2.6	4	µA	V_{DD} = 2.55 V, 0 °C ≤ T_A ≤ 40 °C
I_{SB}	Sleep (mode) current with POR, LVD, Sleep timer, WDT, and internal slow oscillator active.	–	2.8	5	µA	V_{DD} = 3.3 V, –40 °C ≤ T_A ≤ 85 °C

DC GPIO Specifications

Unless otherwise noted, Table 13 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or Table 14 for 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V, 3.3 V, and 2.7 V at 25 °C. These are for design guidance only.

Table 13. 5-V and 3.3-V DC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{PU}	Pull-up resistor	4	5.6	8	kΩ	
V_{OH1}	High output voltage Port 0, 2, or 3 pins	V_{DD} – 0.2	–	–	V	I_{OH} ≤ 10 µA, V_{DD} ≥ 3.0 V, maximum of 20 mA source current in all I/Os.
V_{OH2}	High output voltage Port 0, 2, or 3 pins	V_{DD} – 0.9	–	–	V	I_{OH} = 1 mA, V_{DD} ≥ 3.0 V, maximum of 20 mA source current in all I/Os.
V_{OH3}	High output voltage Port 1 pins with LDO regulator disabled	V_{DD} – 0.2	–	–	V	I_{OH} < 10 µA, V_{DD} ≥ 3.0 V, maximum of 10 mA source current in all I/Os.
V_{OH4}	High output voltage Port 1 pins with LDO regulator disabled	V_{DD} – 0.9	–	–	V	I_{OH} = 5 mA, V_{DD} ≥ 3.0 V, maximum of 20 mA source current in all I/Os.
V_{OH5}	High output voltage Port 1 pins with 3.0 V LDO regulator enabled	2.7	3.0	3.3	V	I_{OH} < 10 µA, V_{DD} ≥ 3.1 V, maximum of 4 I/Os all sourcing 5 mA.
V_{OH6}	High output voltage Port 1 pins with 3.0 V LDO regulator enabled	2.2	–	–	V	I_{OH} = 5 mA, V_{DD} ≥ 3.1 V, maximum of 20 mA source current in all I/Os.

Table 14. 2.7-V DC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{PU}	Pull-up resistor	4	5.6	8	kΩ	
V_{OH1}	High output voltage Port 1 pins with LDO regulator disabled	V_{DD} – 0.2	–	–	V	I_{OH} < 10 µA, maximum of 10 mA source current in all I/Os.
V_{OH2}	High output voltage Port 1 pins with LDO regulator disabled	V_{DD} – 0.5	–	–	V	I_{OH} = 2 mA, maximum of 10 mA source current in all I/Os.
V_{OL}	Low output voltage	–	–	0.75	V	I_{OL} = 10 mA, maximum of 30 mA sink current on even port pins (for example, P0[2] and P1[4]) and 30 mA sink current on odd port pins (for example, P0[3] and P1[5]).
I_{OH2}	High level source current port 1 Pins with LDO regulator disabled	2	–	–	mA	V_{OH} = V_{DD} – 0.5, for the limitations of the total current and I_{OH} at other V_{OH} levels see the notes for V_{OH}.
I_{OL}	Low level sink current	10	–	–	mA	V_{OH} = .75 V, see the limitations of the total current in the note for V_{OL}
V_{OLP1}	Low output voltage port 1 pins	–	–	0.4	V	I_{OL} = 5 mA Maximum of 50 mA sink current on even port pins (for example, P0[2] and P3[4]) and 50 mA sink current on odd port pins (for example, P0[3] and P2[5]). 2.4 V ≤ V_{DD} < 3.6 V
V_{IL}	Input low voltage	–	–	0.75	V	2.4 V ≤ V_{DD} < 3.6 V
V_{IH1}	Input high voltage	1.4	–	–	V	2.4 V ≤ V_{DD} < 2.7 V
V_{IH2}	Input high voltage	1.6	–	–	V	2.7 V ≤ V_{DD} < 3.6 V
V_H	Input hysteresis voltage	–	60	–	mV	
I_{IL}	Input leakage (absolute value)	–	1	–	nA	Gross tested to 1 µA
C_{IN}	Capacitive load on pins as input	0.5	1.7	5	pF	Package and pin dependent Temperature = 25 °C
C_{OUT}	Capacitive load on pins as output	0.5	1.7	5	pF	Package and pin dependent Temperature = 25 °C

DC Analog Mux Bus Specifications

Table 15 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C. These are for design guidance only.

Table 15. DC Analog Mux Bus Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{SW}	Switch resistance to common analog bus	–	–	400 800	Ω Ω	V_{DD} ≥ 2.7 V 2.4 V ≤ V_{DD} ≤ 2.7 V

DC POR and LVD Specifications

Table 16 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively.
Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C. These are for design guidance only.

Table 16. DC POR and LVD Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
	V_{DD} value for PPOR trip					V_{DD} is greater than or equal to 2.5 V during startup, reset from the XRES pin, or reset from watchdog.
V_{PPOR0}	PORLEV[1:0] = 00b	–	2.36	2.40	V	
V_{PPOR1}	PORLEV[1:0] = 01b	–	2.60	2.65	V	
V_{PPOR2}	PORLEV[1:0] = 10b	–	2.82	2.95	V	
	V_{DD} value for LVD trip					
V_{LVD0}	VM[2:0] = 000b	2.39	2.45	2.51[17]	V	
V_{LVD1}	VM[2:0] = 001b	2.54	2.71	2.78[18]	V	
V_{LVD2}	VM[2:0] = 010b	2.75	2.92	2.99[19]	V	
V_{LVD3}	VM[2:0] = 011b	2.85	3.02	3.09	V	
V_{LVD4}	VM[2:0] = 100b	2.96	3.13	3.20	V	
V_{LVD5}	VM[2:0] = 101b	–	–	–	V	
V_{LVD6}	VM[2:0] = 110b	–	–	–	V	
V_{LVD7}	VM[2:0] = 111b	4.52	4.73	4.83	V	

Notes
17. Always greater than 50 mV above V_{PPOR} (PORLEV = 00) for falling supply.
18. Always greater than 50 mV above V_{PPOR} (PORLEV = 01) for falling supply.
19. Always greater than 50 mV above V_{PPOR} (PORLEV = 10) for falling supply.

Table 20. 2.7-V AC Chip Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{CPU1}	CPU Frequency (2.7 V nominal)	0.75	–	3.25	MHz	SLIMO mode = 0
F_{32K1}	Internal low speed oscillator frequency	8	32	96	kHz	
F_{32K_U}	Internal low speed oscillator (ILO) untrimmed frequency	5	–	100	kHz	After a reset and before the M8C starts to run, the ILO is not trimmed. See the System Resets section of the PSoC Technical Reference Manual for details on this timing.
F_{IMO12}	IMO stability for 12 MHz (commercial temperature)[25]	11.0	12	12.9	MHz	Trimmed for 2.7 V operation using factory trim values. See Figure 11 on page 19, SLIMO mode = 0.
F_{IMO6}	IMO stability for 6 MHz (commercial temperature)	5.5	6.0	6.5	MHz	Trimmed for 2.7 V operation using factory trim values. See Figure 11 on page 19, SLIMO mode = 1.
DC_{IMO}	Duty cycle of IMO	40	50	60	%	
DC_{ILO}	Internal low speed oscillator duty cycle	20	50	80	%	
t_{XRST}	External reset pulse width	10	–	–	µs	
$t_{POWERUP}$	Time from end of POR to CPU executing code	–	16	100	ms	Power-up from 0 V. See the System Resets section of the PSoC Technical Reference Manual
SR_{POWER_UP}	Power supply slew rate	–	–	250	V/ms	
t_{JIT_IMO} [26]	12 MHz IMO cycle-to-cycle jitter (RMS)	–	500	900	ps	
	12 MHz IMO long term N cycle-to-cycle jitter (RMS)	–	800	1400	ps	N = 32
	12 MHz IMO period jitter (RMS)	–	300	500	ps	

Notes
25. 0 °C to 70 °C ambient, V_{DD} = 3.3 V.
26. Refer to Cypress Jitter Specifications Application Note – AN5054 at http://www.cypress.com for more information.

AC External Clock Specifications

Table 24, Table 25, Table 26, and Table 27 list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C. These are for design guidance only.

Table 24. 5-V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{OSCEXT}	Frequency	0.750	–	12.6	MHz	
–	High period	38	–	5300	ns	
–	Low period	38	–	–	ns	
–	Power-up IMO to switch	150	–	–	µs	

Table 25. 3.3-V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{OSCEXT}	Frequency with CPU clock divide by 1	0.750	–	12.6	MHz	Maximum CPU frequency is 12 MHz at 3.3 V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements.
–	High period with CPU clock divide by 1	41.7	–	5300	ns	
–	Low period with CPU clock divide by 1	41.7	–	–	ns	
–	Power-up IMO to switch	150	–	–	µs	

Table 26. 2.7-V (Nominal) AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{OSCEXT}	Frequency with CPU clock divide by 1	0.750	–	3.08	MHz	Maximum CPU frequency is 3 MHz at 2.7 V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements.
F_{OSCEXT}	Frequency with CPU clock divide by 2 or greater	0.15	–	6.35	MHz	If the frequency of the external clock is greater than 3 MHz, the CPU clock divider is set to 2 or greater. In this case, the CPU clock divider ensures that the fifty percent duty cycle requirement is met.
–	High period with CPU clock divide by 1	160	–	5300	ns	
–	Low period with CPU clock divide by 1	160	–	–	ns	
–	Power-up IMO to switch	150	–	–	µs	

Table 27. 2.7-V (Minimum) AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{OSCEXT}	Frequency with CPU clock divide by 1	0.750	–	6.3	MHz	Maximum CPU frequency is 6 MHz at 2.7 V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements.
F_{OSCEXT}	Frequency with CPU clock divide by 2 or greater	0.15	–	12.6	MHz	If the frequency of the external clock is greater than 6 MHz, the CPU clock divider is set to 2 or greater. In this case, the CPU clock divider ensures that the fifty percent duty cycle requirement is met.
–	High period with CPU clock divide by 1	160	–	5300	ns	
–	Low period with CPU clock divide by 1	160	–	–	ns	
–	Power-up IMO to switch	150	–	–	µs	

Figure 15. 16-Pin SOIC (150 Mils)

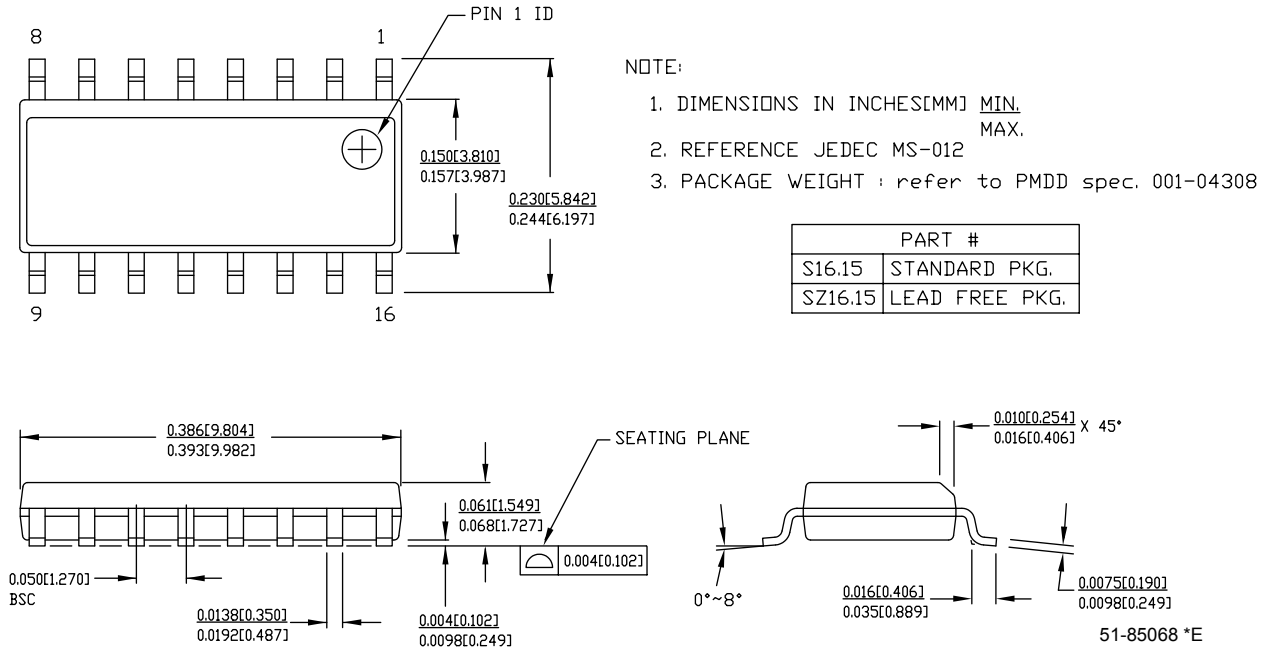


Figure 16. 48-Pin (7 × 7 × 1.0 mm) QFN

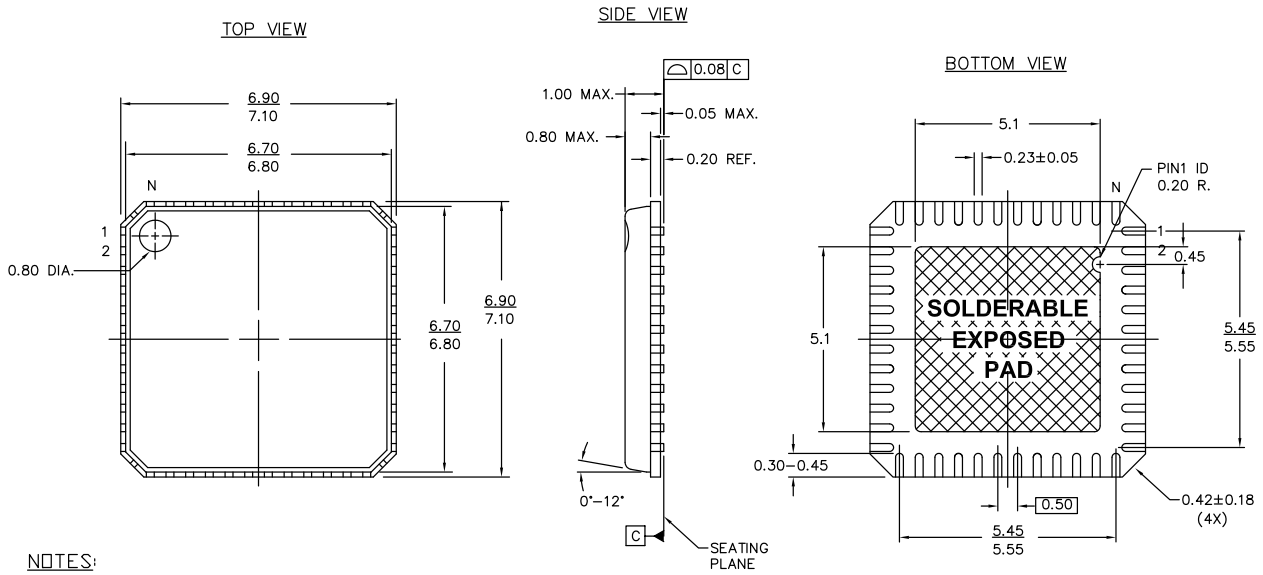
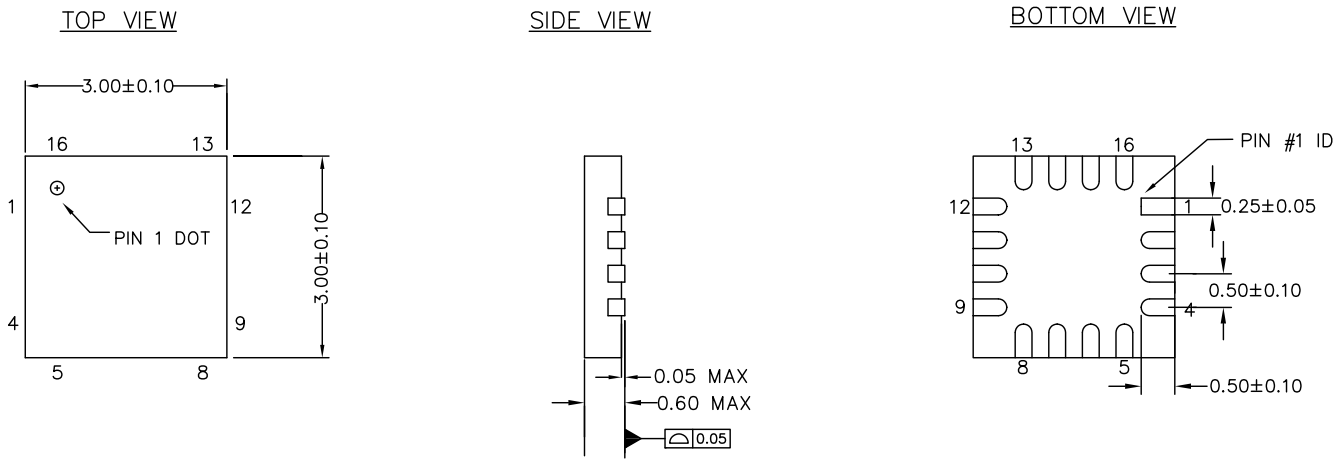


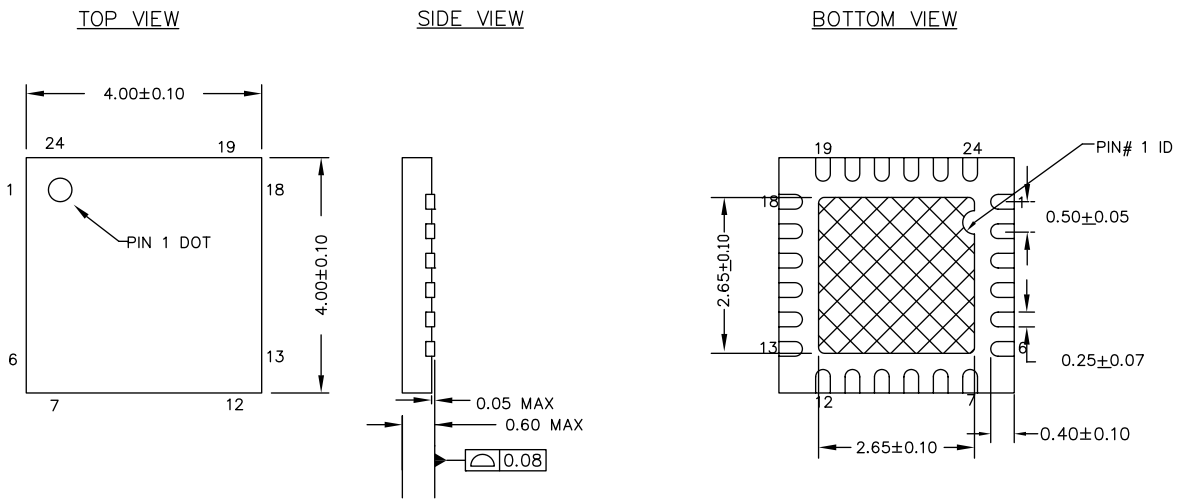
Figure 17. 16-pin (3 × 3 mm × 0.6 Max) COL (Sawn)



NOTES
1. REFERENCE JEDEC # MO−220
2. ALL DIMENSIONS ARE IN MILLIMETERS

001-09116 *J

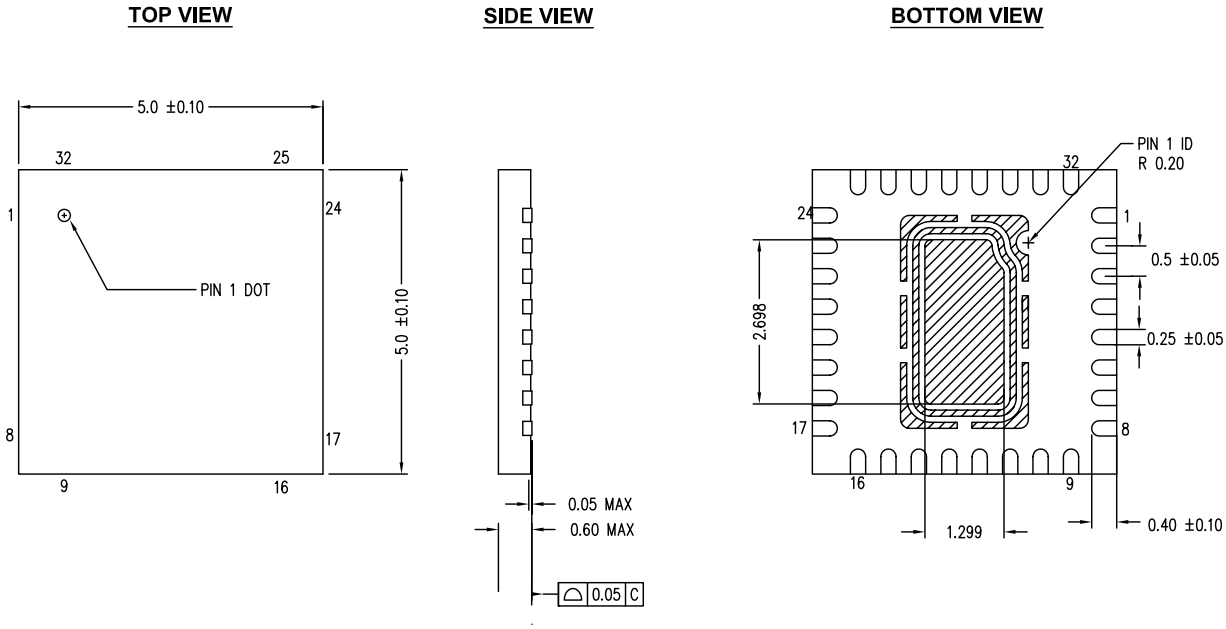
Figure 18. 24-pin QFN (4 × 4 × 0.55 mm) Sawn



NOTES :
1. HATCH IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC # MO−248
3. PACKAGE WEIGHT : 29 ± 3 mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-13937 *F

Figure 19. 32-Pin QFN 5 × 5 × 0.55 mm (Sawn)

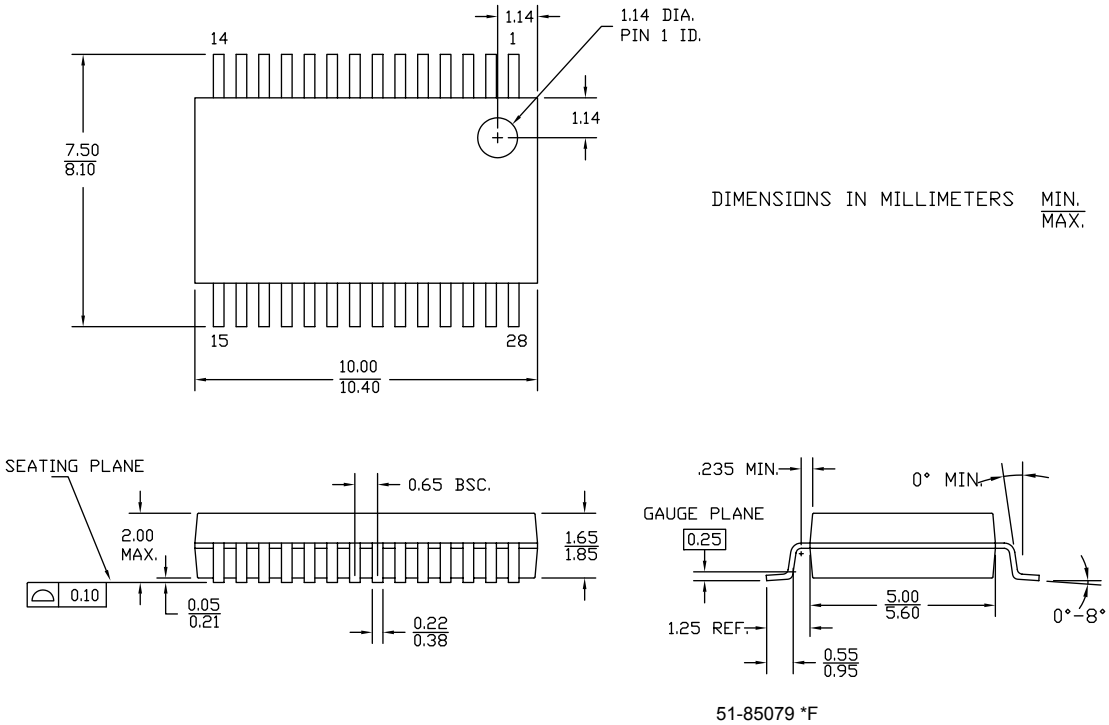


NOTES:

1. HATCH AREA IS SOLDERABLE EXPOSED PAD
2. BASED ON REF JEDEC # MO-248
3. PACKAGE WEIGHT: 38mg ± 4 mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

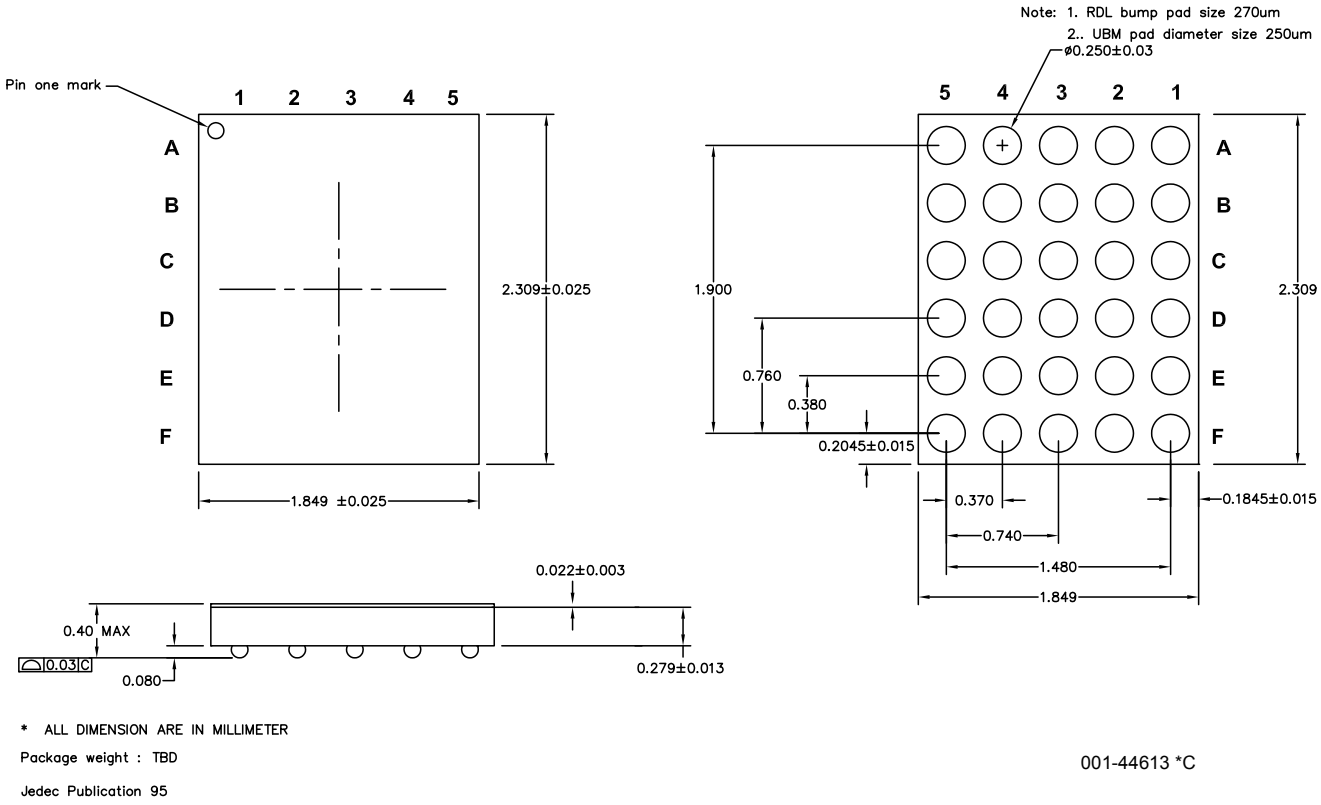
001-48913 *D

Figure 20. 28-pin SSOP (210 Mils)



51-85079 *F

Figure 21. 30-Ball (1.85 × 2.31 × 0.40 mm) WLCSP



Important Note For information on the preferred dimensions for mounting the QFN packages, see the application note *Design Guidelines for Cypress Quad Flat No Extended Lead (QFN) Packaged Devices – AN72845* available at http://www.cypress.com.

It is important to note that pinned vias for thermal conduction are not required for the low power 24, 32, and 48-pin QFN PSoC devices.

Ordering Information

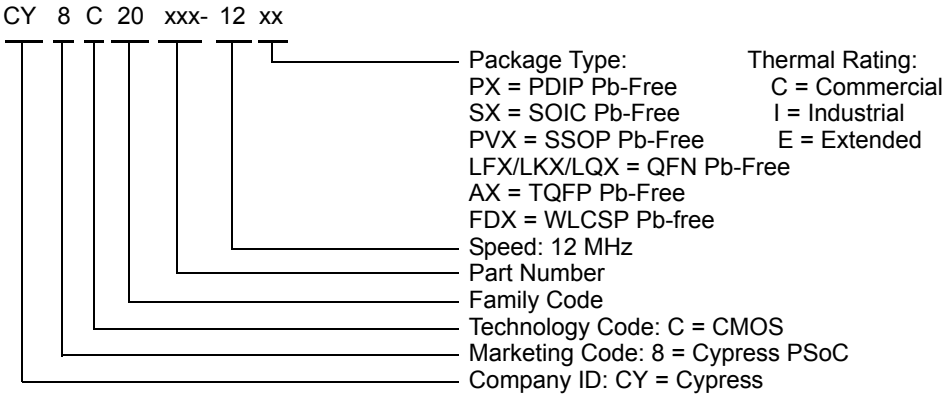
Table 36 lists the CY8C20234, CY8C20334, CY8C20434, CY8C20534, and CY8C20634 PSoC device's key package features and ordering codes.

Table 36. PSoC Device Key Features and Ordering Information

Ordering Code	Package	Flash (Bytes)	SRAM (Bytes)	Digital Blocks	CapSense-Blocks	Digital I/O Pins	Analog Inputs	Analog Outputs	XRES Pin
CY8C20134-12SXI	8-Pin SOIC	8 K	512	0	1	6	6	0	No
CY8C20234-12SXI	16-Pin SOIC	8 K	512	0	1	13	13	0	Yes
CY8C20234-12SXIT	16-pin SOIC	8 K	512	0	1	13	13	0	Yes
CY8C20534-12PVXI	28-Pin SSOP	8 K	512	0	1	24	24[31]	0	Yes
CY8C20534-12PVXIT	28-Pin SSOP	8 K	512	0	1	24	24[31]	0	Yes
CY8C20000-12LFXI	48-Pin OCD QFN[16]	8 K	512	0	1	28	28[31]	0	Yes
CY8C20234-12LKXI	16-Pin (3 × 3 mm 0.60 Max) Sawn QFN	8 K	512	0	1	13	13[31]	0	Yes
CY8C20234-12LKXIT	16-Pin (3 × 3 mm 0.60 Max) Sawn QFN (Tape and Reel)	8 K	512	0	1	13	13[31]	0	Yes
CY8C20334-12LQXI	24-Pin (4 × 4 mm 0.60 Max) Sawn QFN	8 K	512	0	1	20	20[31]	0	Yes
CY8C20334-12LQXIT	24-Pin (4 × 4 mm 0.60 Max) Sawn QFN (Tape and Reel)	8 K	512	0	1	20	20[31]	0	Yes
CY8C20434-12LQXI	32-Pin (5 × 5 mm 0.60 Max) Thin Sawn QFN	8 K	512	0	1	28	28	0	Yes
CY8C20434-12LQXIT	32-Pin (5 × 5 mm 0.60 Max) Thin Sawn QFN (Tape and Reel)	8 K	512	0	1	28	28	0	Yes
CY8C20634-12FDXI	30-Ball WLCSP	8 K	512	0	1	27	27	0	Yes
CY8C20634-12FDXIT	30-Ball WLCSP (Tape and Reel)	8 K	512	0	1	27	27	0	Yes

Note For Die sales information, contact a local Cypress sales office or Field Applications Engineer (FAE).

Ordering Code Definitions



Acronyms

Acronyms Used

Table 37 lists the acronyms that are used in this document.

Table 37. Acronyms Used in this Datasheet

Acronym	Description	Acronym	Description
AC	alternating current	MIPS	million instructions per second
ADC	analog-to-digital converter	OCD	on-chip debug
API	application programming interface	PCB	printed circuit board
CMOS	complementary metal oxide semiconductor	PGA	programmable gain amplifier
CPU	central processing unit	POR	power on reset
EEPROM	electrically erasable programmable read-only memory	PPOR	precision power on reset
GPIO	general purpose I/O	PSoC®	Programmable System-on-Chip
ICE	in-circuit emulator	PWM	pulse width modulator
IDAC	current DAC	QFN	quad flat no leads
IDE	integrated development environment	SLIMO	slow IMO
ILO	internal low speed oscillator	SPI™	serial peripheral interface
IMO	internal main oscillator	SRAM	static random access memory
I/O	input/output	SROM	supervisory read only memory
ISSP	in-system serial programming	SSOP	shrink small-outline package
LCD	liquid crystal display	USB	universal serial bus
LDO		WDT	watchdog timer
LED	light-emitting diode	WLCSP	wafer level chip scale package
LVD	low voltage detect	XRES	external reset
MCU	microcontroller unit		

Reference Documents

PSoC® CY8C20x34 and PSoC® CY8C20x24 Technical Reference Manual (TRM) – 001-13033

Design Aids – Reading and Writing PSoC® Flash - AN2015 (001-40459)

Design Guidelines for Cypress Quad Flat No Extended Lead (QFN) Packaged Devices – AN72845 available at http://www.cypress.com.

Glossary

block	1. A functional unit that performs a single function, such as an oscillator. 2. A functional unit that may be configured to perform one of several functions, such as a digital PSoC block or an analog PSoC block.
buffer	1. A storage area for data that is used to compensate for a speed difference, when transferring data from one device to another. Usually refers to an area reserved for IO operations, into which data is read, or from which data is written. 2. A portion of memory set aside to store data, often before it is sent to an external device or as it is received from an external device. 3. An amplifier used to lower the output impedance of a system.
bus	1. A named connection of nets. Bundling nets together in a bus makes it easier to route nets with similar routing patterns. 2. A set of signals performing a common function and carrying similar data. Typically represented using vector notation; for example, address[7:0]. 3. One or more conductors that serve as a common connection for a group of related devices.
clock	The device that generates a periodic signal with a fixed frequency and duty cycle. A clock is sometimes used to synchronize different logic blocks.
comparator	An electronic circuit that produces an output voltage or current whenever two input levels simultaneously satisfy predetermined amplitude requirements.
compiler	A program that translates a high level language, such as C, into machine language.
configuration space	In PSoC devices, the register space accessed when the XIO bit, in the CPU_F register, is set to ‘1’.
crystal oscillator	An oscillator in which the frequency is controlled by a piezoelectric crystal. Typically a piezoelectric crystal is less sensitive to ambient temperature than other circuit components.
cyclic redundancy check (CRC)	A calculation used to detect errors in data communications, typically performed using a linear feedback shift register. Similar calculations may be used for a variety of other purposes such as data compression.
data bus	A bi-directional set of signals used by a computer to convey information from a memory location to the central processing unit and vice versa. More generally, a set of signals used to convey data between digital functions.
debugger	A hardware and software system that allows you to analyze the operation of the system under development. A debugger usually allows the developer to step through the firmware one step at a time, set break points, and analyze memory.
dead band	A period of time when neither of two or more signals are in their active state or in transition.
digital blocks	The 8-bit logic blocks that can act as a counter, timer, serial receiver, serial transmitter, CRC generator, pseudo-random number generator, or SPI.
digital-to-analog (DAC)	A device that changes a digital signal to an analog signal of corresponding magnitude. The analog-to-digital (ADC) converter performs the reverse operation.
duty cycle	The relationship of a clock period high time to its low time, expressed as a percent.
emulator	Duplicates (provides an emulation of) the functions of one system with a different system, so that the second system appears to behave like the first system.

Document History Page

Document Title: CY8C20134/CY8C20234/CY8C20334/CY8C20434/CY8C20534/CY8C20634, PSoC® Programmable System-on-Chip™ Document Number: 001-05356				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	404571	HMT	See ECN	New silicon and document (Revision **).
*A	418513	HMT	See ECN	Updated Electrical Specifications, including Storage Temperature and Maximum Input Clock Frequency. Updated Features and Analog System Overview. Modified 32-pin QFN E-PAD dimensions. Added new 32-pin QFN. Add High Output Drive indicator to all P1[x] pinouts. Updated trademarks.
*B	490071	HMT	See ECN	Made datasheet “Final”. Added new Development Tool section. Added OCD pinout and package diagram. Added 16-pin QFN. Updated 24-pin and 32-pin QFN package diagrams to 0.60 max thickness. Changed from commercial to industrial temperature range. Updated Storage Temperature specification and notes. Updated thermal resistance data. Added development tool kit part numbers. Finetuned features and electrical specifications.
*C	788177	HMT	See ECN	Added CapSense SNR requirement reference. Added Low Power Comparator (LPC) AC/DC electrical specifications tables. Added 2.7V minimum specifications. Updated figure standards. Updated Technical Training paragraph. Added QFN package clarifications and dimensions. Updated ECN-ed Amkor dimensioned QFN package diagram revisions.
*D	1356805	HMT / SFVTMP3 / HCL / SFV	See ECN	Updated 24-pin QFN Theta JA. Added External Reset Pulse Width, TXRST, specification. Fixed 48-pin QFN.vsd. Updated the table introduction and high output voltage description in section two. The sentence: "Exceeding maximum ratings may shorten the battery life of the device.” does not apply to all datasheets. Therefore, the word "battery" is changed to "useful.” Took out tabs after table and figure numbers in titles and added two hard spaces. Updated the section, DC GPIO Specifications on page 20 with new text. Updated VOH5 and VOH6 to say, ”High Output Voltage, Port 1 Pins with 3.0V LDO Regulator Enabled.” Updated VOH7 and VOH8 with the text, “maximum of 20 mA source current in all I/Os.”Added 28-pin SSOP part, pinout, package. Updated specs. Modified dev. tool part numbers.
*E	2197347	UVS / AESA	See ECN	Added 32-pin Sawn QFN Pin diagram Removed package diagram: 32-Pin (5 × 5 mm) SAWN QFN(001-42168 *A) Updated Ordering Information table with CY8C20434-12LQXI and CY8C20434-12LQXIT ordering details. Corrected Table 16. DC Programming Specifications - Included above the table "Flash Endurance and Retention specifications with the use of the EEPROM User Module are valid only within the range: 25 °C +/-20C during the Flash Write operation. Refer the EEPROM User Module datasheet instructions for EEPROM Flash Write requirements outside of the 25 °C +/-20 °C temperature window."
*F	2542938	RLRM / AESA	07/30/2008	Corrected Ordering Information format. Updated package diagrams 001-13937 and 001-30999. Updated datasheet template. Corrected Figure 6 (28-pin diagram).
*G	2610469	SNV / PYRS	11/20/08	Updated V_{OH5}, V_{OH7}, and V_{OH9} specifications
*H	2693024	DPT / PYRS	04/16/2009	Changed title from PSoC® Mixed Signal Array to PSoC® Programmable System-on-Chip™ Replaced package outline drawing for 32-Pin Sawn QFN Updated “Development Tool Selection” on page 38 Updated “Development Tools” on page 7 and “Designing with PSoC Designer” on page 8 Updated “Getting Started” on page 6

Document History Page

Document Title: CY8C20134/CY8C20234/CY8C20334/CY8C20434/CY8C20534/CY8C20634, PSoC® Programmable System-on-Chip™ Document Number: 001-05356				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*Q	3638597	BVI	06/06/2012	Updated F_{SCLK} parameter in the Table 32, “SPI Slave AC Specifications,” on page 31. Changed t_{OUT_HIGH} to t_{OUT_H} in Table 31, “SPI Master AC Specifications,” on page 31 Updated package diagrams: 001-13937 to *D 001-44613 to *B Removed obsolete specs 001-17397 and 001-14503 referenced in page 40
*R	4306760	PRKU	03/26/2014	Added note to connect all V_{SS} pins to one common GND plane. Updated 16-pin COL (Sawn) package drawing.
*S	4455557	DIMA	08/13/2014	Replaced references of “Application Notes for Surface Mount Assembly of Amkor’s MicroLeadFrame (MLF) Packages” with “Design Guidelines for Cypress Quad Flat No Extended Lead (QFN) Packaged Devices – AN72845” in all instances across the document. Added CapSense Design Resources. Updated Ordering Information: Updated Table 36: Added CY8C20234-12SXIT and its corresponding details.
*T	4748586	DIMA	05/14/2015	Removed “CapSense Design Resources”. Added More Information. Updated Packaging Dimensions: spec 51-85066 – Changed revision from *F to *G. spec 001-13937 – Changed revision from *E to *F. spec 51-85079 – Changed revision from *E to *F. Updated to new template. Completing Sunset Review.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

Products

Automotive	cypress.com/go/automotive
Clocks & Buffers	cypress.com/go/clocks
Interface	cypress.com/go/interface
Lighting & Power Control	cypress.com/go/powerpsoc
Memory	cypress.com/go/memory
PSoC	cypress.com/go/psoc
Touch Sensing	cypress.com/go/touch
USB Controllers	cypress.com/go/USB
Wireless/RF	cypress.com/go/wireless

PSoC® Solutions

psoc.cypress.com/solutions

PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP

Cypress Developer Community

Community | Forums | Blogs | Video | Training

Technical Support

cypress.com/go/support