



Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	M8C
Core Size	8-Bit
Speed	12MHz
Connectivity	I ² C, SPI
Peripherals	LVD, POR, WDT
Number of I/O	28
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.25V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-UFQFN Exposed Pad
Supplier Device Package	32-QFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c20434-12lqxit

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



PSoC Functional Overview

The PSoC family consists of many *Programmable System-on-Chips with On-Chip Controller* devices. These devices are designed to replace multiple traditional MCU based system components with one low cost single chip programmable component. A PSoC device includes configurable analog and digital blocks and programmable interconnect. This architecture enables the user to create customized peripheral configurations to match the requirements of each individual application. Additionally, a fast CPU, flash program memory, SRAM data memory, and configurable I/O are included in a range of convenient pinouts.

The PSoC architecture for this device family, as shown in Figure 2, consists of three main areas: the Core, the System Resources, and the CapSense Analog System. A common versatile bus enables connection between I/O and the analog system. Each CY8C20x34 PSoC device includes a dedicated CapSense block that provides sensing and scanning control circuitry for capacitive sensing applications. Depending on the PSoC package, up to 28 general purpose I/O (GPIO) are also included. The GPIO provide access to the MCU and analog mux.

PSoC Core

The PSoC Core is a powerful engine that supports a rich instruction set. It encompasses SRAM for data storage, an interrupt controller, sleep and watchdog timers, IMO, and ILO. The CPU core, called the M8C, is a powerful processor with speeds up to 12 MHz. The M8C is a two MIPS, 8-bit Harvard-architecture microprocessor.

System Resources provide additional capability such as a configurable I²C slave or SPI master-slave communication interface and various system resets supported by the M8C.

The Analog System consists of the CapSense PSoC block and an internal 1.8 V analog reference. Together they support capacitive sensing of up to 28 inputs.

CapSense Analog System

The Analog System contains the capacitive sensing hardware. Several hardware algorithms are supported. This hardware performs capacitive sensing and scanning without requiring external components. Capacitive sensing is configurable on each GPIO pin. Scanning of enabled CapSense pins is completed quickly and easily across multiple ports.

Figure 2. Analog System Block Diagram



Analog Multiplexer System

The Analog Mux Bus connects to every GPIO pin. Pins are connected to the bus individually or in any combination. The bus also connects to the analog system for analysis with the CapSense block comparator.

Switch control logic enables selected pins to precharge continuously under hardware control. This enables capacitive measurement for applications such as touch sensing. Other multiplexer applications include:

- Complex capacitive sensing interfaces such as sliders and touch pads
- Chip-wide mux that enables analog input from any I/O pin
- Crosspoint connection between any I/O pin combinations



Additional System Resources

System Resources provide additional capability useful to complete systems. Additional resources include low voltage detection and power on reset. Brief statements describing the merits of each system resource follow:

- The I²C slave or SPI master-slave module provides 50/100/400 kHz communication over two wires. SPI communication over three or four wires run at speeds of 46.9 kHz to 3 MHz (lower for a slower system clock).
- Low voltage detection (LVD) interrupts signal the application of falling voltage levels, while the advanced POR (Power On Reset) circuit eliminates the need for a system supervisor.
- An internal 1.8 V reference provides an absolute reference for capacitive sensing.
- The 5 V maximum input, 3 V fixed output, low dropout regulator (LDO) provides regulation for I/Os. A register controlled bypass mode enables the user to disable the LDO.

PSoC Device Characteristics

Depending on your PSoC device characteristics, the digital and analog systems can have 16, 8, or 4 digital blocks, and 12, 6, or 4 analog blocks. Table 1 lists the resources available for specific PSoC device groups. The PSoC device covered by this datasheet is highlighted.

PSoC Part Number	Digital I/O	Digital Rows	Digital Blocks	Analog Inputs	Analog Outputs	Analog Columns	Analog Blocks	SRAM Size	Flash Size
CY8C29x66	up to 64	4	16	up to 12	4	4	12	2 K	32 K
CY8C28xxx	up to 44	up to 3	up to 12	up to 44	up to 4	up to 6	up to 12 + 4 ^[1]	1 K	16 K
CY8C27x43	up to 44	2	8	up to 12	4	4	12	256	16 K
CY8C24x94	up to 56	1	4	up to 48	2	2	6	1 K	16 K
CY8C24x23A	up to 24	1	4	up to 12	2	2	6	256	4 K
CY8C23x33	up to 26	1	4	up to 12	2	2	4	256	8 K
CY8C22x45	up to 38	2	8	up to 38	0	4	6 ^[1]	1 K	16 K
CY8C21x45	up to 24	1	4	up to 24	0	4	6 ^[1]	512	8 K
CY8C21x34	up to 28	1	4	up to 28	0	2	4 ^[1]	512	8 K
CY8C21x23	up to 16	1	4	up to 8	0	2	4 ^[1]	256	4 K
CY8C20x34	up to 28	0	0	up to 28	0	0	3 ^[1,2]	512	8 K
CY8C20xx6	up to 36	0	0	up to 36	0	0	3 ^[1,2]	up to 2 K	up to 32 K

Table 1. PSoC Device Characteristics

Notes

1. Limited analog functionality

2. Two analog blocks and one $CapSense^{\ensuremath{\mathfrak{R}}\xspace}$.



Development Tools

PSoC Designer[™] is the revolutionary integrated design environment (IDE) that you can use to customize PSoC to meet your specific application requirements. PSoC Designer software accelerates system design and time to market. Develop your applications using a library of precharacterized analog and digital peripherals (called user modules) in a drag-and-drop design environment. Then, customize your design by leveraging the dynamically generated application programming interface (API) libraries of code. Finally, debug and test your designs with the integrated debug environment, including in-circuit emulation and standard software debug features. PSoC Designer includes:

- Application editor graphical user interface (GUI) for device and user module configuration and dynamic reconfiguration
- Extensive user module catalog
- Integrated source-code editor (C and assembly)
- Free C compiler with no size restrictions or time limits
- Built-in debugger
- In-circuit emulation
- Built-in support for communication interfaces:
- □ Hardware and software I²C slaves and masters
- □ Full-speed USB 2.0
- Up to four full-duplex universal asynchronous receiver/transmitters (UARTs), SPI master and slave, and wireless

PSoC Designer supports the entire library of PSoC 1 devices and runs on Windows XP, Windows Vista, and Windows 7.

PSoC Designer Software Subsystems

Design Entry

In the chip-level view, choose a base device to work with. Then select different onboard analog and digital components that use the PSoC blocks, which are called user modules. Examples of user modules are ADCs, DACs, amplifiers, and filters. Configure the user modules for your chosen application and connect them to each other and to the proper pins. Then generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The tool also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic reconfiguration makes it possible to change configurations at run time. In essence, this allows you to use more than 100 percent of PSoC's resources for an application.

Code Generation Tools

The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. You can develop your design in C, assembly, or a combination of the two.

Assemblers. The assemblers allow you to merge assembly code seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and are linked with other software modules to get absolute addressing.

C Language Compilers. C language compilers are available that support the PSoC family of devices. The products allow you to create complete C programs for the PSoC family devices. The optimizing C compilers provide all of the features of C, tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

Debugger

PSoC Designer has a debug environment that provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow you to read and program and read and write data memory, and read and write I/O registers. You can read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also allows you to create a trace buffer of registers and memory locations of interest.

Online Help System

The online help system displays online, context-sensitive help. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an online support Forum to aid the designer.

In-Circuit Emulator

A low-cost, high-functionality in-circuit emulator (ICE) is available for development support. This hardware can program single devices.

The emulator consists of a base unit that connects to the PC using a USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full-speed (24 MHz) operation.



Designing with PSoC Designer

The development process for the PSoC device differs from that of a traditional fixed function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and by lowering inventory costs. These configurable resources, called PSoC Blocks, have the ability to implement a wide variety of user-selectable functions. The PSoC development process is summarized in four steps:

- 1. Select User Modules.
- 2. Configure User Modules.
- 3. Organize and Connect.
- 4. Generate, Verify, and Debug.

Select User Modules

PSoC Designer provides a library of prebuilt, pretested hardware peripheral components called "user modules." User modules make selecting and implementing peripheral devices, both analog and digital, simple.

Configure User Modules

Each user module that you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. For example, a PWM User Module configures one or more digital PSoC blocks, one for each 8 bits of resolution. The user module parameters permit you to establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus. All the user modules are documented in datasheets that may be viewed directly in PSoC Designer or on the Cypress website. These user module datasheets explain the internal operation of the user module and provide performance specifications. Each datasheet describes the use of each user module parameter, and other information you may need to successfully implement your design.

Organize and Connect

You build signal chains at the chip level by interconnecting user modules to each other and the I/O pins. You perform the selection, configuration, and routing so that you have complete control over all on-chip resources.

Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, you perform the "Generate Configuration Files" step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system. The generated code provides application programming interfaces (APIs) with high-level functions to control and respond to hardware events at run-time and interrupt service routines that you can adapt as needed.

A complete code development environment allows you to develop and customize your applications in either C, assembly language, or both.

The last step in the development process takes place inside PSoC Designer's debugger (access by clicking the Connect icon). PSoC Designer downloads the HEX image to the ICE where it runs at full speed. PSoC Designer debugging capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint, and watch-variable features, the debug interface provides a large trace buffer and allows you to define complex breakpoint events. These include monitoring address and data bus values, memory locations, and external signals.



16-Pin SOIC Pinout

Figure 4. CY8C20234-12SXI 16-Pin SOIC Pinout



Table 3. Pin Definitions – CY8C20234 16-Pin (SOIC)

Pin No.	Digital	Analog	Name	Description
1	I/O	1	P0[7]	Analog column mux input
2	I/O	I	P0[3]	Analog column mux input and column input, integrating input
3	I/O	I	P0[1]	Analog column mux input, integrating input
4	I/O	I	P2[5]	Analog column mux input
5	I/O	I	P2[1]	Analog column mux input
6	I/O	I	P1[7]	I2C serial clock (SCL), SPI SS
7	I/O	I	P1[5]	I2C serial data (SDA),SPI MISO
8	I/O	I	P1[3]	Analog column mux input, SPI CLK
9	I/O	I	P1[1]	I2C serial clock (SCL), ISSP-SCLK,SPI MOSI
10	Power		V _{SS}	Ground connection
11	I/O	I	P1[0]	I2C serial data (SDA), ISSP-SDATA
12	I/O	I	P1[2]	Analog column mux input
13	I/O	I	P1[4]	Analog column mux input, optional external clock input (EXTCLK)
14	I/O	I	XRES	XRES
15	I/O	I	P0[4]	Analog column mux input
16	Power	•	V _{DD}	Supply voltage

A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive.



48-Pin OCD Part Pinout

The 48-Pin QFN part table and pin diagram is for the CY8C20000 On-Chip Debug (OCD) PSoC device. This part is only used for in-circuit debugging. It is NOT available for production.



Figure 5. CY8C20000 48-Pin OCD PSoC Device

Table 4. Pin Definitions – CY8C20000 48-Pin OCD (QFN) ^[3]

Pin No.	Digital	Analog	Name	Description
1			NC	No connection
2	I/O	I	P0[1]	
3	I/O	I	P2[7]	
4	I/O	I	P2[5]	
5	I/O	I	P2[3]	
6	I/O	I	P2[1]	
7	I/O	I	P3[3]	
8	I/O	I	P3[1]	
9	I _{OH}	I	P1[7]	I ² C SCL, SPI SS
10	I _{ОН}	I	P1[5]	I ² C SDA, SPI MISO
11	I/O	I	P0[1]	
12			NC	No connection
13			NC	No Connection
14			NC	No Connection
15			NC	SPI CLK
16	I _{OH}	I	P1[3]	CLK ^[4] , I ² C SCL, SPI MOSI
17	I _{OH}	I	P1[1]	Ground connection

Notes

3. The center pad on the QFN package is connected to ground (V_{SS}) for best mechanical, thermal, and electrical performance. If not connected to ground, it is electrically

floated and not connected to any other signal.
4. These are the ISSP pins, that are not High Z at POR (Power-on-Reset). See the *PSoC Technical Reference Manual* for details.



16-Pin Part Pinout



Table 5. Pin Definitions – CY8C20234 16-Pin (QFN no e-pad)

Din No	Туре		Namo	Description				
FIII NO.	Digital	Analog	Name	Description				
1	I/O	I	P2[5]					
2	I/O	I	P2[1]					
3	I _{OH}	I	P1[7]	I ² C SCL, SPI SS				
4	I _{OH}	I	P1[5]	I ² C SDA, SPI MISO				
5	I _{OH}	I	P1[3]	SPI CLK				
6	I _{OH}	I	P1[1]	CLK ^[6] , I ² C SCL, SPI MOSI				
7	Power V _S		V _{SS}	Ground connection				
8	I _{OH}	I	P1[0]	DATA ^[6] , I ² C SDA				
9	I _{OH}	I	P1[2]					
10	I _{OH}	I	P1[4]	Optional external clock input (EXTCLK)				
11	Input		XRES	Active high external reset with internal pull-down				
12	I/O	I	P0[4]					
13	Power		V _{DD}	Supply voltage				
14	I/O	I	P0[7]					
15	I/O	I	P0[3]	Integrating Input				
16	I/O	1	P0[1]					

A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive

Note

6. These are the ISSP pins, that are not High Z at POR (Power-on-Reset). See the PSoC Technical Reference Manual for details.



Pin No. Type		/pe	Namo	Description
FIII NO.	Digital Analog		Name	Description
18	I/O	1	P3[0]	
19	I/O	1	P3[2]	
20	I/O	1	P2[0]	
21	I/O	1	P2[2]	
22	I/O	1	P2[4]	
23	I/O	1	P2[6]	
24	I/O	1	P0[0]	
25	I/O	1	P0[2]	
26	I/O	1	P0[4]	
27	I/O	1	P0[6]	Analog bypass
28	Power		V _{DD}	Supply voltage
29	I/O	I	P0[7]	
30	I/O	1	P0[5]	
31	I/O	1	P0[3]	Integrating input
32	Power		V _{SS}	Ground connection ^[12]
CP	Power		V _{SS}	Center pad is connected to ground

Table 7. Pin Definitions – CY8C20434 32-Pin (QFN) [9]

A = Analog, I = Input, O = Output, OH = 5 mA high output drive.



DC POR and LVD Specifications

Table 16 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and $-40 \text{ °C} \le T_A \le 85 \text{ °C}, 3.0 \text{ V to } 3.6 \text{ V and } -40 \text{ °C} \le T_A \le 85 \text{ °C}, \text{ or } 2.4 \text{ V to } 3.0 \text{ V and } -40 \text{ °C} \le T_A \le 85 \text{ °C}, \text{ respectively.}$ Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C. These are for design guidance only.

Table 16. DC POR and LVD Specifications

Symbol	Description	Min	Тур	Мах	Units	Notes
V _{PPOR0} V _{PPOR1} V _{PPOR2}	V _{DD} value for PPOR trip PORLEV[1:0] = 00b PORLEV[1:0] = 01b PORLEV[1:0] = 10b		2.36 2.60 2.82	2.40 2.65 2.95	V V V	V_{DD} is greater than or equal to 2.5 V during startup, reset from the XRES pin, or reset from watchdog.
VLVD0 VLVD1 VLVD2 VLVD3 VLVD4 VLVD5 VLVD6 VLVD7	$\begin{array}{l} V_{DD} \mbox{ value for LVD trip} \\ VM[2:0] = 000b \\ VM[2:0] = 001b \\ VM[2:0] = 010b \\ VM[2:0] = 011b \\ VM[2:0] = 100b \\ VM[2:0] = 101b \\ VM[2:0] = 110b \\ VM[2:0] = 111b \\ VM[2:0] = 111b \end{array}$	2.39 2.54 2.75 2.85 2.96 - - 4.52	2.45 2.71 2.92 3.02 3.13 - 4.73	2.51 ^[17] 2.78 ^[18] 2.99 ^[19] 3.09 3.20 - 4.83	<pre></pre>	

Notes 17. Always greater than 50 mV above V_{PPOR} (PORLEV = 00) for falling supply. 18. Always greater than 50 mV above V_{PPOR} (PORLEV = 01) for falling supply. 19. Always greater than 50 mV above V_{PPOR} (PORLEV = 10) for falling supply.



DC Programming Specifications

Table 17 lists the guaranteed minimum and maximum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and -40 °C \leq T_A \leq 85 °C, 3.0 V to 3.6 V and -40 °C \leq T_A \leq 85 °C, or 2.4 V to 3.0 V and -40 °C \leq T_A \leq 85 °C, respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C. These are for design guidance only. Flash endurance and retention specifications with the use of the EEPROM User Module are valid only within the range: 25 °C +/-20C during the Flash Write operation. Reference the EEPROM User Module datasheet instructions for EEPROM flash write requirements outside of the 25 °C +/-20 °C temperature window.

Table 17.	DC Programming	Specifications
-----------	----------------	----------------

Symbol	Description	Min	Тур	Max	Units	Notes
V _{DDP}	V _{DD} for programming and erase	4.5	5	5.5	V	This specification applies to the functional requirements of external programmer tools
V _{DDLV}	Low V _{DD} for verify	2.4	2.5	2.6	V	This specification applies to the functional requirements of external programmer tools
V _{DDHV}	High V _{DD} for verify	5.1	5.2	5.3	V	This specification applies to the functional requirements of external programmer tools
V _{DDIWRITE}	Supply voltage for flash write operation	2.7	_	5.25	V	This specification applies to this device when it is executing internal flash writes
I _{DDP}	Supply current during programming or verify	-	5	25	mA	
V _{ILP}	Input low voltage during programming or verify	-	-	0.8	V	
V _{IHP}	Input high voltage during programming or verify	2.2	-	-	V	
I _{ILP}	Input current when applying V _{ILP} to P1[0] or P1[1] during programming or verify	-	-	0.2	mA	Driving internal pull-down resistor.
I _{IHP}	Input current when applying V _{IHP} to P1[0] or P1[1] during programming or verify	-	-	1.5	mA	Driving internal pull-down resistor.
V _{OLV}	Output low voltage during programming or verify	-	-	V _{SS} + 0.75	V	
V _{OHV}	Output high voltage during programming or verify	V _{DD} – 1.0	-	V _{DD}	V	
Flash _{ENPB}	Flash endurance (per block)	50,000 ^[21]	_	-	-	Erase/write cycles per block.
Flash _{ENT}	Flash endurance (total) ^[20]	1,800,000	-	-	-	Erase/write cycles.
Flash _{DR}	Flash data retention	10	-	-	Years	

Notes

^{20.} A maximum of 36 × 50,000 block endurance cycles is allowed. This is balanced between operations on 36 × 1 blocks of 50,000 maximum cycles each, 36 × 2 blocks of 25,000 maximum cycles each, or 36 × 4 blocks of 12,500 maximum cycles each (to limit the total number of cycles to 36 × 50,000 and that no single block ever sees more than 50,000 cycles).

^{21.} The 50,000 cycle flash endurance per block is only guaranteed if the flash is operating within one voltage range. Voltage ranges are 2.4 V to 3.0 V, 3.0 V to 3.6 V and 4.75 V to 5.25 V.



DC I²C Specifications

Table 18 lists the guaranteed minimum and maximum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and -40 °C \leq T_A \leq 85 °C, 3.0V to 3.6 V and -40 °C \leq T_A \leq 85 °C, or 2.4 V to 3.0 V and -40 °C \leq T_A \leq 85 °C, respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C. These are for design guidance only. Flash endurance and retention specifications with the use of the EEPROM user module are valid only within the range: 25 °C + -20C during the Flash Write operation. Reference the EEPROM User Module datasheet instructions for EEPROM flash Write requirements outside of the 25 °C +/-20 °C temperature window.

Table 18. DC I²C Specifications^[22]

Symbol	Description	Min	Тур	Max	Units	Notes
V _{ILI2C}	Input low level	-	I	$0.3 \times V_{DD}$	V	$2.4~V \leq V_{DD} \leq 3.6~V$
		-	-	$0.25 \times V_{DD}$	V	$4.75~V \leq V_{DD} \leq 5.25~V$
V _{IHI2C}	Input high level	$0.7 \times V_{DD}$	-	-	V	$2.4~V \leq V_{DD} \leq 5.25~V$

AC Electrical Characteristics

AC Chip Level Specifications

Table 19, Table 20, and Table 21 list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and -40 °C \leq T_A \leq 85 °C, 3.0 V to 3.6 V and -40 °C \leq T_A \leq 85 °C, or 2.4 V to 3.0 V and -40 °C \leq T_A \leq 85 °C respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C. These are for design guidance only.

Table 19. 5-V and 3.3-V AC Chip-Level Specifications

Symbol	Description	Min	Тур	Max	Units	Notes
F _{CPU1}	CPU frequency (3.3 V nominal)	0.75	-	12.6	MHz	12 MHz only for SLIMO Mode = 0.
F _{32K1}	Internal low speed oscillator frequency	15	32	64	kHz	
F _{32K_U}	Internal low speed oscillator (ILO) untrimmed frequency	5	_	100	kHz	After a reset and before the M8C starts to run, the ILO is not trimmed. See the System Resets section of the PSoC Technical Reference Manual for details on this timing.
F _{IMO12}	Internal main oscillator stability for 12 MHz (commercial temperature) ^[23]	11.4	12	12.6	MHz	Trimmed for 3.3 V operation using factory trim values. See Figure 11 on page 19, SLIMO mode = 0.
F _{IMO6}	Internal main oscillator stability for 6 MHz (commercial temperature)	5.5	6.0	6.5	MHz	Trimmed for 3.3 V operation using factory trim values. See Figure 11 on page 19, SLIMO mode = 1.
DC _{IMO}	Duty cycle of IMO	40	50	60	%	
DC _{ILO}	Internal low speed oscillator duty cycle	20	50	80	%	
t _{XRST}	External reset pulse width	10	-	Ι	μS	
t _{POWERUP}	Time from end of POR to CPU executing code	Ι	16	100	ms	Power-up from 0 V. See the System Resets section of the PSoC Technical Reference Manual.
SR _{POWER_UP}	Power supply slew rate	-	-	250	V/ms	
t _{jit_IMO} ^[24]	12 MHz IMO cycle-to-cycle jitter (RMS)	_	200	1600	ps	
	12 MHz IMO long term N cycle-to-cycle jitter (RMS)	1	600	1400	ps	N = 32
	12 MHz IMO period jitter (RMS)	_	100	900	ps	

Notes

- 22. All GPIO meet the DC GPIO V_{IL} and V_{IH} specifications found in the DC GPIO Specifications sections. The I²C GPIO pins also meet the above specs.
 23. 0 to 70 °C ambient, V_{DD} = 3.3 V.
 24. Refer to Cypress Jitter Specifications Application Note AN5054 at http://www.cypress.com for more information.



AC External Clock Specifications

Table 24, Table 25, Table 26, and Table 27 list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and -40 °C \leq T_A \leq 85 °C, 3.0 V to 3.6 V and -40 °C \leq T_A \leq 85 °C, or 2.4 V to 3.0 V and -40 °C \leq T_A \leq 85 °C, respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C. These are for design guidance only.

Table 24. 5-V AC External Clock Specifications

Symbol	Description	Min	Тур	Мах	Units	Notes
F _{OSCEXT}	Frequency	0.750	-	12.6	MHz	
_	High period	38	-	5300	ns	
_	Low period	38	-	-	ns	
-	Power-up IMO to switch	150	-	-	μs	

Table 25. 3.3-V AC External Clock Specifications

Symbol	Description	Min	Тур	Max	Units	Notes
F _{OSCEXT}	Frequency with CPU clock divide by 1	0.750	_	12.6	MHz	Maximum CPU frequency is 12 MHz at 3.3 V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements.
_	High period with CPU clock divide by 1	41.7	-	5300	ns	
-	Low period with CPU clock divide by 1	41.7	-	-	ns	
-	Power-up IMO to switch	150	_	_	μs	

Table 26. 2.7-V (Nominal) AC External Clock Specifications

Symbol	Description	Min	Тур	Max	Units	Notes
F _{OSCEXT}	Frequency with CPU clock divide by 1	0.750	_	3.08	MHz	Maximum CPU frequency is 3 MHz at 2.7 V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements.
F _{OSCEXT}	Frequency with CPU clock divide by 2 or greater	0.15	_	6.35	MHz	If the frequency of the external clock is greater than 3 MHz, the CPU clock divider is set to 2 or greater. In this case, the CPU clock divider ensures that the fifty percent duty cycle requirement is met.
-	High period with CPU clock divide by 1	160	-	5300	ns	
-	Low period with CPU clock divide by 1	160	_	_	ns	
-	Power-up IMO to switch	150	-	-	μs	

Table 27. 2.7-V (Minimum) AC External Clock Specifications

Symbol	Description	Min	Тур	Max	Units	Notes
Foscext	Frequency with CPU clock divide by 1	0.750	_	6.3	MHz	Maximum CPU frequency is 6 MHz at 2.7 V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements.
F _{OSCEXT}	Frequency with CPU clock divide by 2 or greater	0.15	_	12.6	MHz	If the frequency of the external clock is greater than 6 MHz, the CPU clock divider is set to 2 or greater. In this case, the CPU clock divider ensures that the fifty percent duty cycle requirement is met.
-	High period with CPU clock divide by 1	160	-	5300	ns	
-	Low period with CPU clock divide by 1	160	-	-	ns	
-	Power-up IMO to switch	150	_	_	μs	



Packaging Dimensions

This section illustrates the packaging specifications for the CY8C20234, CY8C20334, CY8C20434, CY8C20534, and CY8C20634 PSoC devices along with the thermal impedances for each package.

Important Note Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulation tools' dimensions, refer to the emulator pod drawings at http://www.cypress.com.

Figure 14. 8-pin SOIC (150 Mils)

- 1. DIMENSIONS IN INCHES[MM] MIN. MAX.
- 2. PIN 1 ID IS OPTIONAL, ROUND ON SINGLE LEADFRAME RECTANGULAR ON MATRIX LEADFRAME
- 3. REFERENCE JEDEC MS-012
- 4. PACKAGE WEIGHT 0.07gms

PART #				
S08.15	STANDARD PKG			
SZ08.15	LEAD FREE PKG			
SW8.15	LEAD FREE PKG			





51-85066 *G



Figure 15. 16-Pin SOIC (150 Mils)





Figure 17. 16-pin (3 × 3 mm × 0.6 Max) COL (Sawn)





19 24 PIN# 1 ID 0.50±0.05 0.50±0.05 0.25±0.07 2 -2.65±0.10 -0.40±0.10

<u>NOTES</u> :

- 1. 🕅 HATCH IS SOLDERABLE EXPOSED METAL.
- 2. REFERENCE JEDEC # MO-248
- 3. PACKAGE WEIGHT : 29 ± 3 mg
- 4. ALL DIMENSIONS ARE IN MILLIMETERS

001-13937 *F





Figure 21. 30-Ball (1.85 × 2.31 × 0.40 mm) WLCSP

Important Note For information on the preferred dimensions for mounting the QFN packages, see the application note *Design Guidelines for Cypress Quad Flat No Extended Lead (QFN) Packaged Devices – AN72845* available at http://www.cypress.com. It is important to note that pinned vias for thermal conduction are not required for the low power 24, 32, and 48-pin QFN PSoC devices.



Development Tool Selection

Software

PSoC Designer™

At the core of the PSoC development software suite is PSoC Designer, used to generate PSoC firmware applications. PSoC Designer is available free of charge at http://www.cypress.com and includes a free C compiler.

PSoC Programmer

PSoC Programmer is flexible enough and is used on the bench in development and also suitable for factory programming. PSoC Programmer works either as a standalone programming application or operates directly from PSoC Designer. PSoC Programmer software is compatible with both PSoC ICE Cube In-Circuit Emulator and PSoC MiniProg. PSoC programmer is available free of charge at http://www.cypress.com.

Development Kits

All development kits are sold at the Cypress Online Store.

CY3215-DK Basic Development Kit

The CY3215-DK is for prototyping and development with PSoC Designer. This kit supports in-circuit emulation and the software interface enables users to run, halt, and single step the processor and view the content of specific memory locations. PSoC Designer supports the advance emulation features also. The kit includes:

- PSoC Designer Software CD
- ICE-Cube In-Circuit Emulator
- ICE Flex-Pod for CY8C29x66 Family
- Cat-5 Adapter
- Mini-Eval Programming Board
- 110 ~ 240V Power Supply, Euro-Plug Adapter
- iMAGEcraft C Compiler (Registration Required)
- ISSP Cable
- USB 2.0 Cable and Blue Cat-5 Cable
- 2 CY8C29466-24PXI 28-PDIP Chip Samples

Evaluation Tools

All evaluation tools are sold at the Cypress Online Store.

CY3210-MiniProg1

The CY3210-MiniProg1 kit enables the user to program PSoC devices via the MiniProg1 programming unit. The MiniProg is a small, compact prototyping programmer that connects to the PC via a provided USB 2.0 cable. The kit includes:

- MiniProg Programming Unit
- MiniEval Socket Programming and Evaluation Board
- 28-Pin CY8C29466-24PXI PDIP PSoC Device Sample
- 28-Pin CY8C27443-24PXI PDIP PSoC Device Sample
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

CY3210-PSoCEval1

The CY3210-PSoCEval1 kit features an evaluation board and the MiniProg1 programming unit. The evaluation board includes an LCD module, potentiometer, LEDs, and plenty of breadboarding space to meet all of your evaluation needs. The kit includes:

- Evaluation Board with LCD Module
- MiniProg Programming Unit
- 28-Pin CY8C29466-24PXI PDIP PSoC Device Sample (2)
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

CY3214-PSoCEvalUSB

The CY3214-PSoCEvalUSB evaluation kit features a development board for the CY8C24794-24LFXI PSoC device. Special features of the board include both USB and capacitive sensing development and debugging support. This evaluation board also includes an LCD module, potentiometer, LEDs, an enunciator and plenty of bread boarding space to meet all of your evaluation needs. The kit includes:

- PSoCEvalUSB Board
- LCD Module
- MIniProg Programming Unit
- Mini USB Cable
- PSoC Designer and Example Projects CD
- Getting Started Guide
- Wire Pack



Glossary

block	1. A functional unit that performs a single function, such as an oscillator.
	 A functional unit that may be configured to perform one of several functions, such as a digital PSoC block or an analog PSoC block.
buffer	 A storage area for data that is used to compensate for a speed difference, when transferring data from one device to another. Usually refers to an area reserved for IO operations, into which data is read, or from which data is written.
	2. A portion of memory set aside to store data, often before it is sent to an external device or as it is received from an external device.
	3. An amplifier used to lower the output impedance of a system.
bus	 A named connection of nets. Bundling nets together in a bus makes it easier to route nets with similar routing patterns.
	2. A set of signals performing a common function and carrying similar data. Typically represented using vector notation; for example, address[7:0].
	3. One or more conductors that serve as a common connection for a group of related devices.
clock	The device that generates a periodic signal with a fixed frequency and duty cycle. A clock is sometimes used to synchronize different logic blocks.
comparator	An electronic circuit that produces an output voltage or current whenever two input levels simultaneously satisfy predetermined amplitude requirements.
compiler	A program that translates a high level language, such as C, into machine language.
configuration space	In PSoC devices, the register space accessed when the XIO bit, in the CPU_F register, is set to '1'.
crystal oscillator	An oscillator in which the frequency is controlled by a piezoelectric crystal. Typically a piezoelectric crystal is less sensitive to ambient temperature than other circuit components.
cyclic redundancy check (CRC)	A calculation used to detect errors in data communications, typically performed using a linear feedback shift register. Similar calculations may be used for a variety of other purposes such as data compression.
data bus	A bi-directional set of signals used by a computer to convey information from a memory location to the central processing unit and vice versa. More generally, a set of signals used to convey data between digital functions.
debugger	A hardware and software system that allows you to analyze the operation of the system under development. A debugger usually allows the developer to step through the firmware one step at a time, set break points, and analyze memory.
dead band	A period of time when neither of two or more signals are in their active state or in transition.
digital blocks	The 8-bit logic blocks that can act as a counter, timer, serial receiver, serial transmitter, CRC generator, pseudo-random number generator, or SPI.
digital-to-analog (DAC)	A device that changes a digital signal to an analog signal of corresponding magnitude. The analog-to-digital (ADC) converter performs the reverse operation.
duty cycle	The relationship of a clock period high time to its low time, expressed as a percent.
emulator	Duplicates (provides an emulation of) the functions of one system with a different system, so that the second system appears to behave like the first system.



Glossary

External Reset (XRES)	An active high signal that is driven into the PSoC device. It causes all operation of the CPU and blocks to stop and return to a pre-defined state.
Flash	An electrically programmable and erasable, non-volatile technology that provides you the programmability and data storage of EPROMs, plus in-system erasability. Non-volatile means that the data is retained when power is OFF.
Flash block	The smallest amount of Flash ROM space that may be programmed at one time and the smallest amount of Flash space that may be protected. A Flash block holds 64 bytes.
frequency	The number of cycles or events per unit of time, for a periodic function.
gain	The ratio of output current, voltage, or power to input current, voltage, or power, respectively. Gain is usually expressed in dB.
I ² C	A two-wire serial computer bus by Philips Semiconductors (now NXP Semiconductors). I2C is an Inter-Integrated Circuit. It is used to connect low-speed peripherals in an embedded system. The original system was created in the early 1980s as a battery control interface, but it was later used as a simple internal bus system for building control electronics. I2C uses only two bi-directional pins, clock and data, both running at +5V and pulled high with resistors. The bus operates at 100 kbits/second in standard mode and 400 kbits/second in fast mode.
ICE	The in-circuit emulator that allows you to test the project in a hardware environment, while viewing the debugging device activity in a software environment (PSoC Designer).
input/output (I/O)	A device that introduces data into or extracts data from a system.
interrupt	A suspension of a process, such as the execution of a computer program, caused by an event external to that process, and performed in such a way that the process can be resumed.
interrupt service routine (ISR)	A block of code that normal code execution is diverted to when the M8C receives a hardware interrupt. Many interrupt sources may each exist with its own priority and individual ISR code block. Each ISR code block ends with the RETI instruction, returning the device to the point in the program where it left normal program execution.
jitter	1. A misplacement of the timing of a transition from its ideal position. A typical form of corruption that occurs on serial data streams.
	The abrupt and unwanted variations of one or more signal characteristics, such as the interval between successive pulses, the amplitude of successive cycles, or the frequency or phase of successive cycles.
low-voltage detect (LVD)	A circuit that senses V_{DD} and provides an interrupt to the system when V_{DD} falls lower than a selected threshold.
M8C	An 8-bit Harvard-architecture microprocessor. The microprocessor coordinates all activity inside a PSoC by interfacing to the Flash, SRAM, and register space.
master device	A device that controls the timing for data exchanges between two devices. Or when devices are cascaded in width, the master device is the one that controls the timing for data exchanges between the cascaded devices and an external interface. The controlled device is called the <i>slave device</i> .
microcontroller	An integrated circuit chip that is designed primarily for control systems and products. In addition to a CPU, a microcontroller typically includes memory, timing circuits, and IO circuitry. The reason for this is to permit the realization of a controller with a minimal quantity of chips, thus achieving maximal possible miniaturization. This in turn, reduces the volume and the cost of the controller. The microcontroller is normally not used for general-purpose computation as is a microprocessor.
mixed-signal	The reference to a circuit containing both analog and digital techniques and components.



Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

Products

Automotive	cypress.com/go/automotive
Clocks & Buffers	cypress.com/go/clocks
Interface	cypress.com/go/interface
Lighting & Power Control	cypress.com/go/powerpsoc
Memory	cypress.com/go/memory
PSoC	cypress.com/go/psoc
Touch Sensing	cypress.com/go/touch
USB Controllers	cypress.com/go/USB
Wireless/RF	cypress.com/go/wireless

PSoC[®] Solutions

psoc.cypress.com/solutions PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP

Cypress Developer Community Community | Forums | Blogs | Video | Training

Technical Support cypress.com/go/support

© Cypress Semiconductor Corporation, 2005-2015. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.

Document Number: 001-05356 Rev. *T

Revised May 14, 2015

Page 50 of 50

PSoC Designer[™] and Programmable System-on-Chip[™] are trademarks and PSoC® and CapSense® are registered trademarks of Cypress Semiconductor Corporation. Purchase of I²C components from Cypress or one of its sublicensed Associated Companies conveys a license under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips. As from October 1st, 2006 Philips Semiconductors has a new trade name - NXP Semiconductors. All products and company names mentioned in this document may be the trademarks of their respective holders.