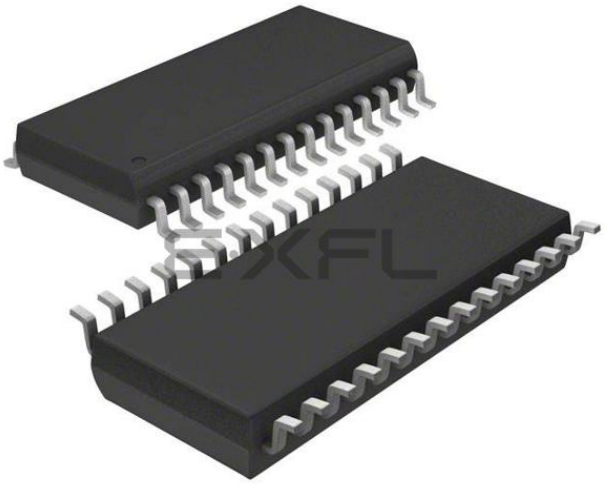

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Details	
Product Status	Active
Core Processor	M8C
Core Size	8-Bit
Speed	12MHz
Connectivity	I²C, SPI
Peripherals	LVD, POR, WDT
Number of I/O	24
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.25V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c20534-12pvxit

Contents

48-Pin OCD Part Pinout

The 48-Pin QFN part table and pin diagram is for the CY8C20000 On-Chip Debug (OCD) PSoC device. This part is only used for in-circuit debugging. It is NOT available for production.

Figure 5. CY8C20000 48-Pin OCD PSoC Device

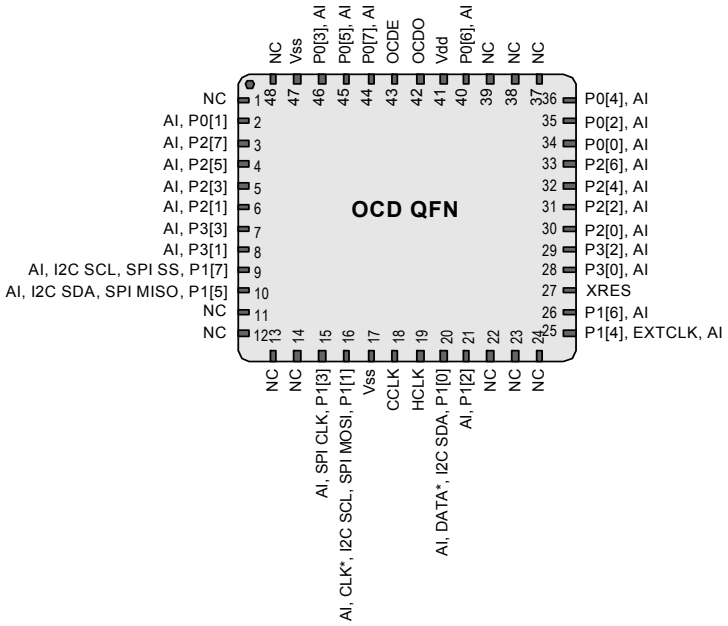


Table 4. Pin Definitions – CY8C20000 48-Pin OCD (QFN) [3]

Pin No.	Digital	Analog	Name	Description
1			NC	No connection
2	I/O	I	P0[1]	
3	I/O	I	P2[7]	
4	I/O	I	P2[5]	
5	I/O	I	P2[3]	
6	I/O	I	P2[1]	
7	I/O	I	P3[3]	
8	I/O	I	P3[1]	
9	I_{OH}	I	P1[7]	I^2C SCL, SPI SS
10	I_{OH}	I	P1[5]	I^2C SDA, SPI MISO
11	I/O	I	P0[1]	
12			NC	No connection
13			NC	No Connection
14			NC	No Connection
15			NC	SPI CLK
16	I_{OH}	I	P1[3]	CLK[4], I^2C SCL, SPI MOSI
17	I_{OH}	I	P1[1]	Ground connection

Notes
3. The center pad on the QFN package is connected to ground (V_{SS}) for best mechanical, thermal, and electrical performance. If not connected to ground, it is electrically floated and not connected to any other signal.
4. These are the ISSP pins, that are not High Z at POR (Power-on-Reset). See the *PSoC Technical Reference Manual* for details.

32-Pin Part Pinout

Figure 8. CY8C20434 32-Pin PSoC Device

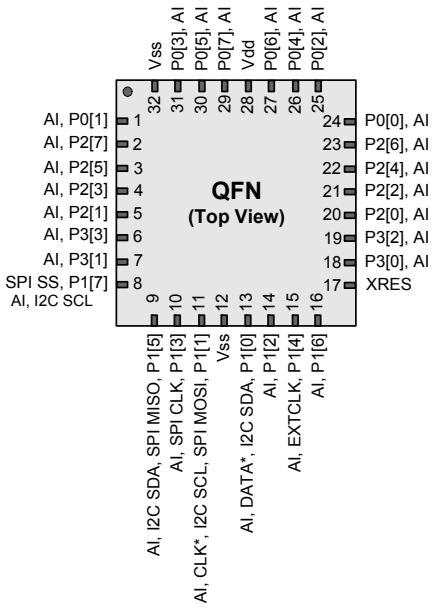


Table 7. Pin Definitions – CY8C20434 32-Pin (QFN) [9]

Pin No.	Type		Name	Description
	Digital	Analog		
1	I/O	I	P0[1]	
2	I/O	I	P2[7]	
3	I/O	I	P2[5]	
4	I/O	I	P2[3]	
5	I/O	I	P2[1]	
6	I/O	I	P3[3]	
7	I/O	I	P3[1]	
8	I_{OH}	I	P1[7]	I^2C SCL, SPI SS
9	I_{OH}	I	P1[5]	I^2C SDA, SPI MISO
10	I_{OH}	I	P1[3]	SPI CLK
11	I_{OH}	I	P1[1]	CLK[10], I^2C SCL, SPI MOSI
12	Power		V_{SS}	Ground Connection[11]
13	I_{OH}	I	P1[0]	DATA[10], I^2C SDA
14	I_{OH}	I	P1[2]	
15	I_{OH}	I	P1[4]	Optional external clock input (EXTCLK)
16	I_{OH}	I	P1[6]	
17	Input		XRES	Active high external reset with internal pull-down

Notes
9. The center pad on the QFN package is connected to ground (V_{SS}) for best mechanical, thermal, and electrical performance. If not connected to ground, it is electrically floated and not connected to any other signal.
10. These are the ISSP pins, that are not High Z at POR (Power-on-Reset). See the *PSoC Technical Reference Manual* for details.
11. All V_{SS} pins should be brought out to one common GND plane.

Table 7. Pin Definitions – CY8C20434 32-Pin (QFN) [9]

Pin No.	Type		Name	Description
	Digital	Analog		
18	I/O	I	P3[0]	
19	I/O	I	P3[2]	
20	I/O	I	P2[0]	
21	I/O	I	P2[2]	
22	I/O	I	P2[4]	
23	I/O	I	P2[6]	
24	I/O	I	P0[0]	
25	I/O	I	P0[2]	
26	I/O	I	P0[4]	
27	I/O	I	P0[6]	Analog bypass
28	Power		V_{DD}	Supply voltage
29	I/O	I	P0[7]	
30	I/O	I	P0[5]	
31	I/O	I	P0[3]	Integrating input
32	Power		V_{SS}	Ground connection[12]
CP	Power		V_{SS}	Center pad is connected to ground

A = Analog, I = Input, O = Output, OH = 5 mA high output drive.

Note
12. All V_{SS} pins should be brought out to one common GND plane.

30-Ball Part Pinout

Figure 10. CY8C20634 30-Ball PSoC Device

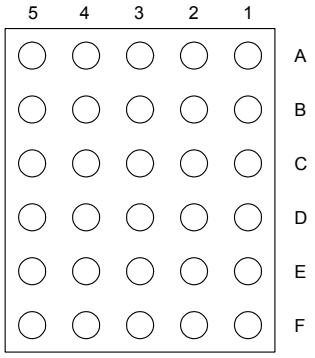


Table 9. 30-Ball Part Pinout (WLCSP)

Pin No.	Type		Name	Description
	Digital	Analog		
A1	Power		V_{DD}	Supply voltage
A2	I/O	I	P0[6]	Analog bypass
A3	I/O	I	P0[4]	
A4	I/O	I	P0[3]	Integrating input
A5	I/O	I	P2[7]	
B1	I/O	I	P0[2]	
B2	I/O	I	P0[0]	
B3	I/O	I	P2[6]	
B4	I/O	I	P0[5]	
B5	I/O	I	P0[1]	
C1	I/O	I	P2[4]	
C2	I/O	I	P2[2]	
C3	I/O	I	P3[1]	
C4	I/O	I	P0[7]	
C5	I/O	I	P2[1]	
D1	I/O	I	P2[0]	
D2	I/O	I	P3[0]	
D3	I/O	I	P3[2]	
D4	I_{OH}	I	P1[1]	CLK[15], I^2C SCL, SPI MOSI
D5	I/O	I	P2[3]	
E1	Input		XRES	Active high external reset with internal pull-down
E2	I_{OH}	I	P1[6]	
E3	I_{OH}	I	P1[4]	Optional external clock input (EXTCLK)
E4	I_{OH}	I	P1[5]	I^2C SDA, SPI MISO
E5	I/O	I	P2[5]	
F1	Power		V_{SS}	Ground connection[16]
F2	I_{OH}	I	P1[2]	
F3	I_{OH}	I	P1[0]	DATA[15], I^2C SDA
F4	I_{OH}	I	P1[3]	SPI CLK
F5	I_{OH}	I	P1[7]	I^2C SCL, SPI SS

A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive.

Notes
15. These are the ISSP pins, that are not High Z at POR (Power-on-Reset). See the *PSoC Technical Reference Manual* for details.
16. All V_{SS} pins should be brought out to one common GND plane.

Table 13. 5-V and 3.3-V DC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OH7}	High output voltage Port 1 pins with 2.4 V LDO regulator enabled	2.1	2.4	2.7	V	I_{OH} < 10 µA, $V_{DD} \geq$ 3.0 V , maximum of 20 mA source current in all I/Os.
V_{OH8}	High output voltage Port 1 pins with 2.4 V LDO regulator enabled	2.0	–	–	V	I_{OH} < 200 µA, $V_{DD} \geq$ 3.0 V, maximum of 20 mA source current in all I/Os.
V_{OH9}	High output voltage Port 1 pins with 1.8 V LDO regulator enabled	1.6	1.8	2.0	V	I_{OH} < 10 µA 3.0V ≤ V_{DD} ≤ 3.6 V 0 °C ≤ T_A ≤ 85 °C Maximum of 20 mA source current in all I/Os.
V_{OH10}	High output voltage Port 1 pins with 1.8 V LDO regulator enabled	1.5	–	–	V	I_{OH} < 100 µA. 3.0V ≤ V_{DD} ≤ 3.6 V. 0 °C ≤ T_A ≤ 85 °C. Maximum of 20 mA source current in all I/Os.
V_{OL}	Low output voltage	–	–	0.75	V	I_{OL} = 20 mA, V_{DD} > 3.0 V, maximum of 60 mA sink current on even port pins (for example, P0[2] and P1[4]) and 60 mA sink current on odd port pins (for example, P0[3] and P1[5]).
I_{OH}	High level source current	–	–	20	mA	V_{OH} = V_{DD} – 0.9. See the limitations of the total current in the Notes for V_{OH}.
I_{OH2}	High level source current port 0, 2, or 3 pins	1	–	–	mA	V_{OH} = V_{DD} – 0.9, for the limitations of the total current and I_{OH} at other V_{OH} levels, see the Notes for V_{OH}.
I_{OH4}	High level source current port 1 Pins with LDO regulator disabled	5	–	–	mA	V_{OH} = V_{DD} – 0.9, for the limitations of the total current and I_{OH} at other V_{OH} levels, see the Notes for V_{OH}.
I_{OL}	Low level sink current	20	–	–	mA	V_{OL} = 0.75 V, see the limitations of the total current in the Notes for V_{OL}
V_{IL}	Input low voltage	–	–	0.8	V	3.6 V ≤ V_{DD} ≤ 5.25 V
V_{IH}	Input high voltage	2.0	–	–	V	3.6 V ≤ V_{DD} ≤ 5.25 V
V_H	Input hysteresis voltage	–	140	–	mV	
I_{IL}	Input leakage (absolute value)	–	1	–	nA	Gross tested to 1 µA
C_{IN}	Capacitive load on pins as input	0.5	1.7	5	pF	Package and pin dependent Temperature = 25 °C
C_{OUT}	Capacitive load on pins as output	0.5	1.7	5	pF	Package and pin dependent Temperature = 25 °C

DC Programming Specifications

Table 17 lists the guaranteed minimum and maximum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C. These are for design guidance only. Flash endurance and retention specifications with the use of the EEPROM User Module are valid only within the range: 25 °C +/–20C during the Flash Write operation. Reference the EEPROM User Module datasheet instructions for EEPROM flash write requirements outside of the 25 °C +/–20 °C temperature window.

Table 17. DC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{DDP}	V_{DD} for programming and erase	4.5	5	5.5	V	This specification applies to the functional requirements of external programmer tools
V_{DDLV}	Low V_{DD} for verify	2.4	2.5	2.6	V	This specification applies to the functional requirements of external programmer tools
V_{DDHV}	High V_{DD} for verify	5.1	5.2	5.3	V	This specification applies to the functional requirements of external programmer tools
$V_{DDIWRITE}$	Supply voltage for flash write operation	2.7	–	5.25	V	This specification applies to this device when it is executing internal flash writes
I_{DDP}	Supply current during programming or verify	–	5	25	mA	
V_{ILP}	Input low voltage during programming or verify	–	–	0.8	V	
V_{IHP}	Input high voltage during programming or verify	2.2	–	–	V	
I_{ILP}	Input current when applying V_{ILP} to P1[0] or P1[1] during programming or verify	–	–	0.2	mA	Driving internal pull-down resistor.
I_{IHP}	Input current when applying V_{IHP} to P1[0] or P1[1] during programming or verify	–	–	1.5	mA	Driving internal pull-down resistor.
V_{OLV}	Output low voltage during programming or verify	–	–	V_{SS} + 0.75	V	
V_{OHV}	Output high voltage during programming or verify	V_{DD} – 1.0	–	V_{DD}	V	
$Flash_{ENPB}$	Flash endurance (per block)	50,000[21]	–	–	–	Erase/write cycles per block.
$Flash_{ENT}$	Flash endurance (total)[20]	1,800,000	–	–	–	Erase/write cycles.
$Flash_{DR}$	Flash data retention	10	–	–	Years	

Notes
20. A maximum of 36 × 50,000 block endurance cycles is allowed. This is balanced between operations on 36 × 1 blocks of 50,000 maximum cycles each, 36 × 2 blocks of 25,000 maximum cycles each, or 36 × 4 blocks of 12,500 maximum cycles each (to limit the total number of cycles to 36 × 50,000 and that no single block ever sees more than 50,000 cycles).
21. The 50,000 cycle flash endurance per block is only guaranteed if the flash is operating within one voltage range. Voltage ranges are 2.4 V to 3.0 V, 3.0 V to 3.6 V and 4.75 V to 5.25 V.

AC External Clock Specifications

Table 24, Table 25, Table 26, and Table 27 list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C. These are for design guidance only.

Table 24. 5-V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{OSCEXT}	Frequency	0.750	–	12.6	MHz	
–	High period	38	–	5300	ns	
–	Low period	38	–	–	ns	
–	Power-up IMO to switch	150	–	–	µs	

Table 25. 3.3-V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{OSCEXT}	Frequency with CPU clock divide by 1	0.750	–	12.6	MHz	Maximum CPU frequency is 12 MHz at 3.3 V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements.
–	High period with CPU clock divide by 1	41.7	–	5300	ns	
–	Low period with CPU clock divide by 1	41.7	–	–	ns	
–	Power-up IMO to switch	150	–	–	µs	

Table 26. 2.7-V (Nominal) AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{OSCEXT}	Frequency with CPU clock divide by 1	0.750	–	3.08	MHz	Maximum CPU frequency is 3 MHz at 2.7 V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements.
F_{OSCEXT}	Frequency with CPU clock divide by 2 or greater	0.15	–	6.35	MHz	If the frequency of the external clock is greater than 3 MHz, the CPU clock divider is set to 2 or greater. In this case, the CPU clock divider ensures that the fifty percent duty cycle requirement is met.
–	High period with CPU clock divide by 1	160	–	5300	ns	
–	Low period with CPU clock divide by 1	160	–	–	ns	
–	Power-up IMO to switch	150	–	–	µs	

Table 27. 2.7-V (Minimum) AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{OSCEXT}	Frequency with CPU clock divide by 1	0.750	–	6.3	MHz	Maximum CPU frequency is 6 MHz at 2.7 V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements.
F_{OSCEXT}	Frequency with CPU clock divide by 2 or greater	0.15	–	12.6	MHz	If the frequency of the external clock is greater than 6 MHz, the CPU clock divider is set to 2 or greater. In this case, the CPU clock divider ensures that the fifty percent duty cycle requirement is met.
–	High period with CPU clock divide by 1	160	–	5300	ns	
–	Low period with CPU clock divide by 1	160	–	–	ns	
–	Power-up IMO to switch	150	–	–	µs	

AC SPI Specifications

Table 31 and Table 32 list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C. These are for design guidance only.

Table 31. SPI Master AC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
F_{SCLK}	SCLK clock frequency	–	–	–	12	MHz
DC_{SCLK}	SCLK duty cycle	–	–	50	–	%
t_{SETUP}	MISO to SCLK setup time	–	40	–	–	ns
t_{HOLD}	SCLK to MISO hold time	–	40	–	–	ns
t_{OUT_VAL}	SCLK to MOSI valid time	–	–	–	40	ns
t_{OUT_H}	MOSI high time	–	40	–	–	ns

Table 32. SPI Slave AC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
F_{SCLK}	SCLK clock frequency	–	–	–	4	MHz
t_{LOW}	SCLK low time	–	41.67	–	–	ns
t_{HIGH}	SCLK high time	–	41.67	–	–	ns
t_{SETUP}	MOSI to SCLK setup time	–	30	–	–	ns
t_{HOLD}	SCLK to MOSI hold time	–	50	–	–	ns
t_{SS_MISO}	SS low to MISO valid	–	–	–	153	ns
t_{SCLK_MISO}	SCLK to MISO valid	–	–	–	125	ns
t_{SS_HIGH}	SS high time	–	50	–	–	ns
t_{SS_SCLK}	Time from SS low to first SCLK	–	$2/F_{SCLK}$	–	–	ns
t_{SCLK_SS}	Time from last SCLK to SS high	–	$2/F_{SCLK}$	–	–	ns

Figure 15. 16-Pin SOIC (150 Mils)

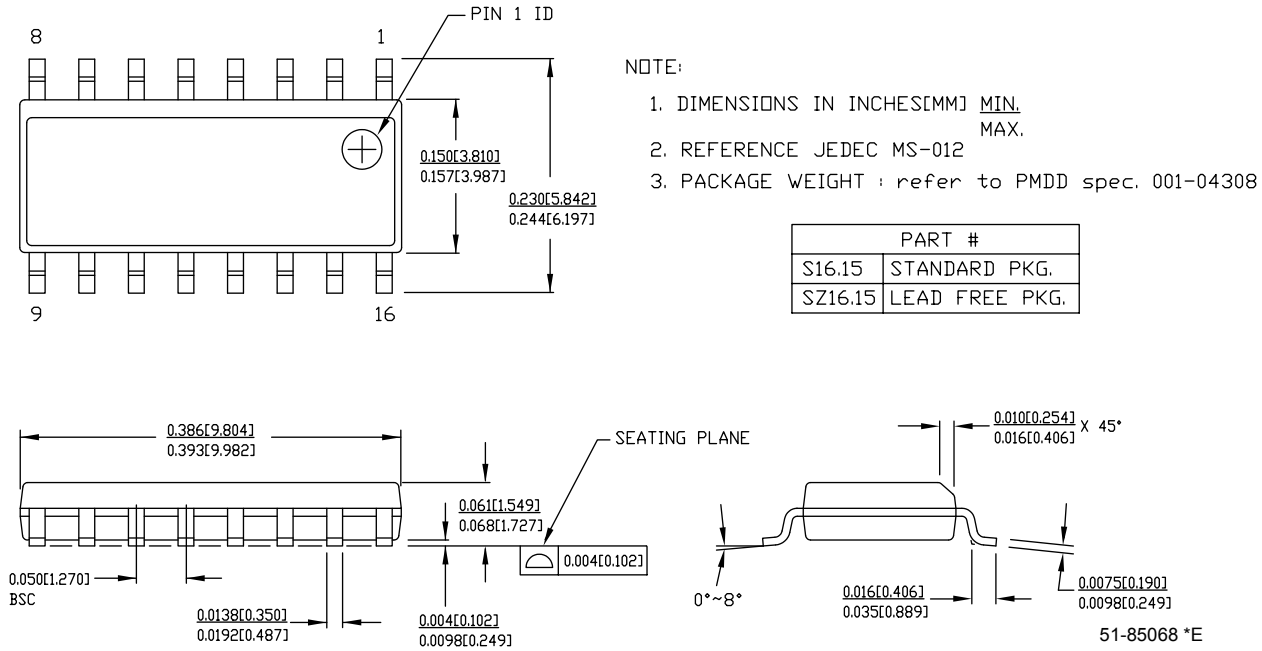


Figure 16. 48-Pin (7 × 7 × 1.0 mm) QFN

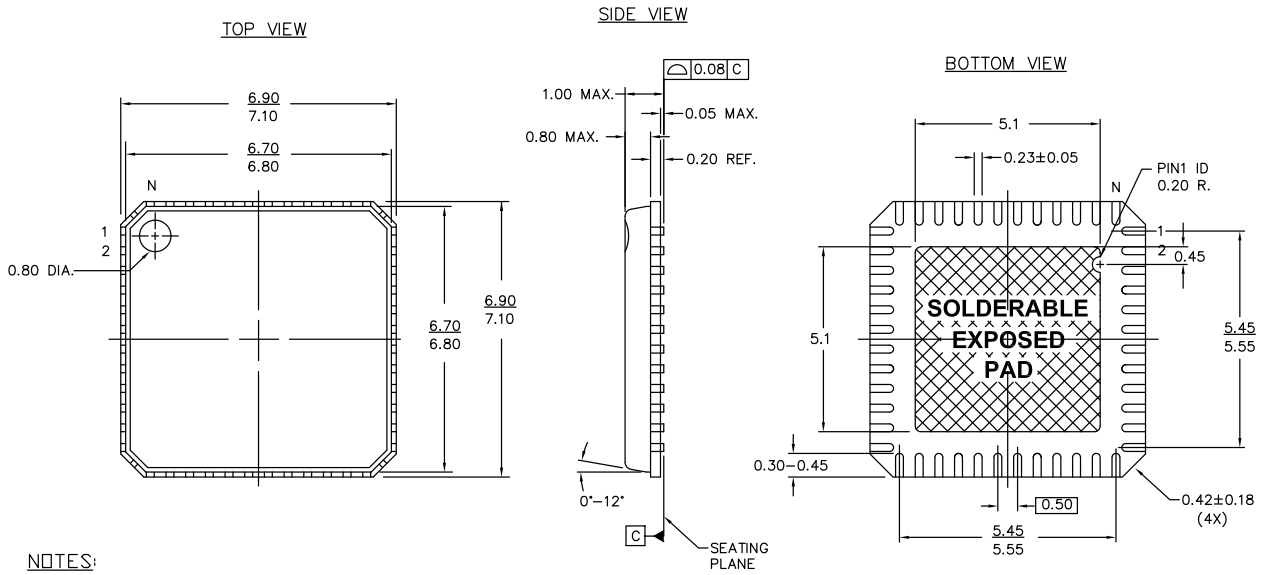
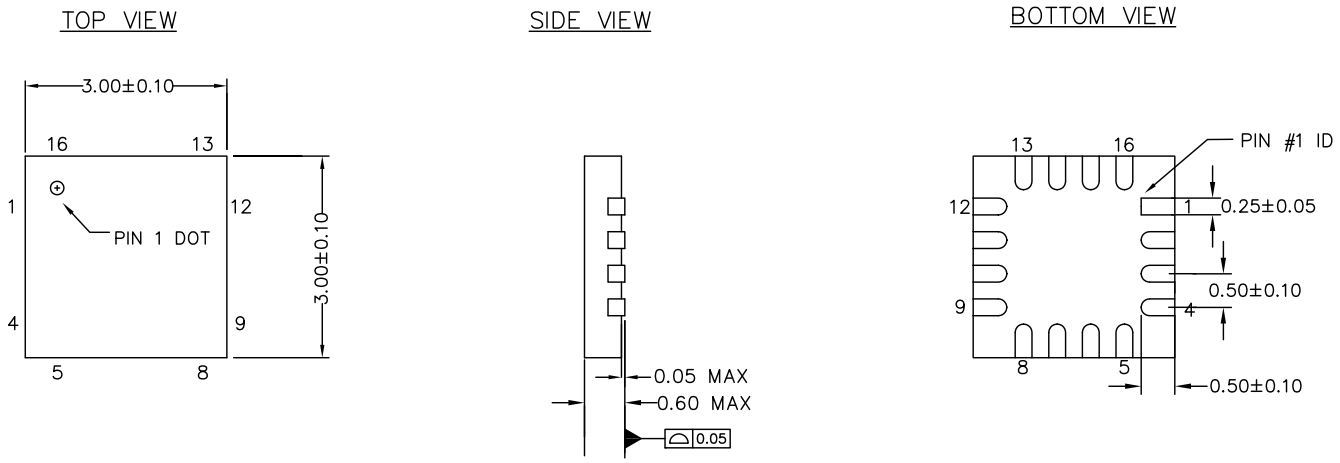


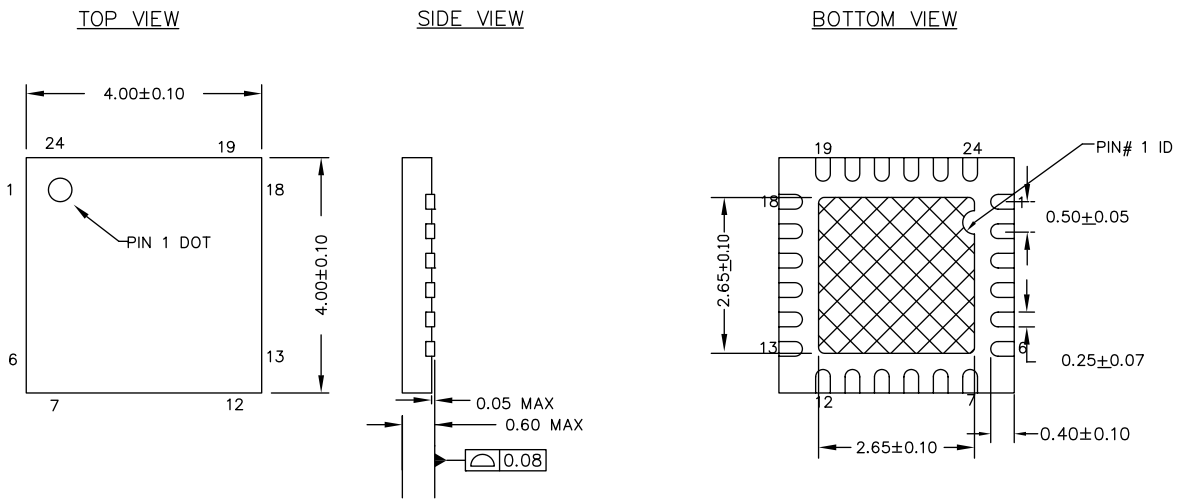
Figure 17. 16-pin (3 × 3 mm × 0.6 Max) COL (Sawn)



NOTES
1. REFERENCE JEDEC # MO−220
2. ALL DIMENSIONS ARE IN MILLIMETERS

001-09116 *J

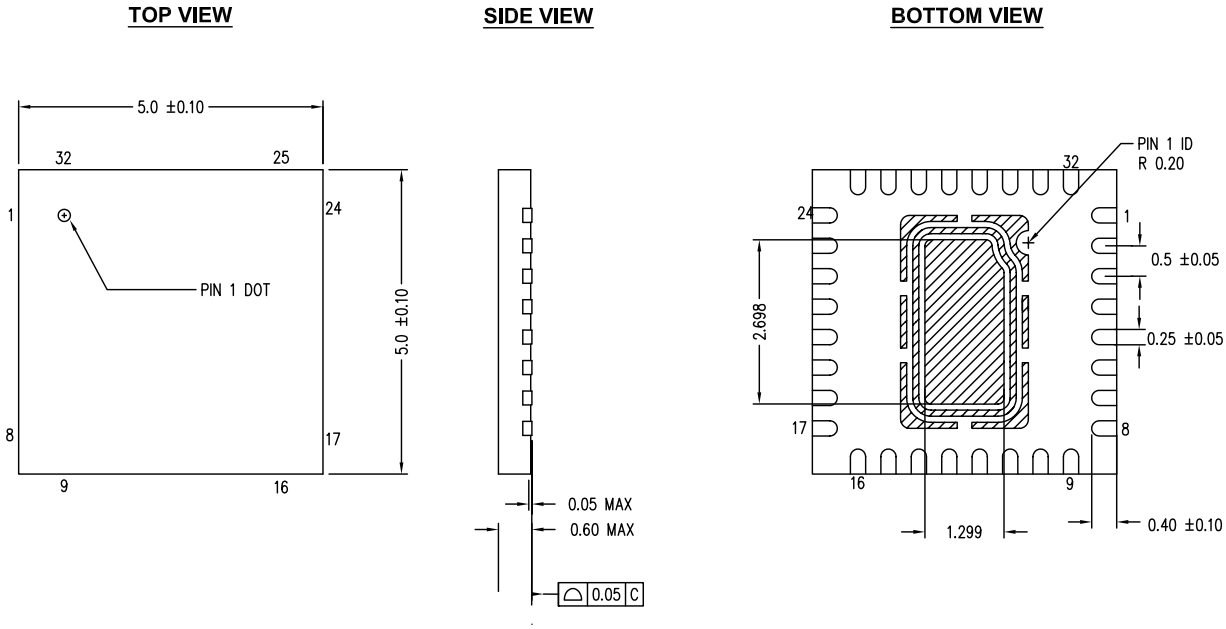
Figure 18. 24-pin QFN (4 × 4 × 0.55 mm) Sawn



NOTES :
1. HATCH IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC # MO−248
3. PACKAGE WEIGHT : 29 ± 3 mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-13937 *F

Figure 19. 32-Pin QFN 5 × 5 × 0.55 mm (Sawn)

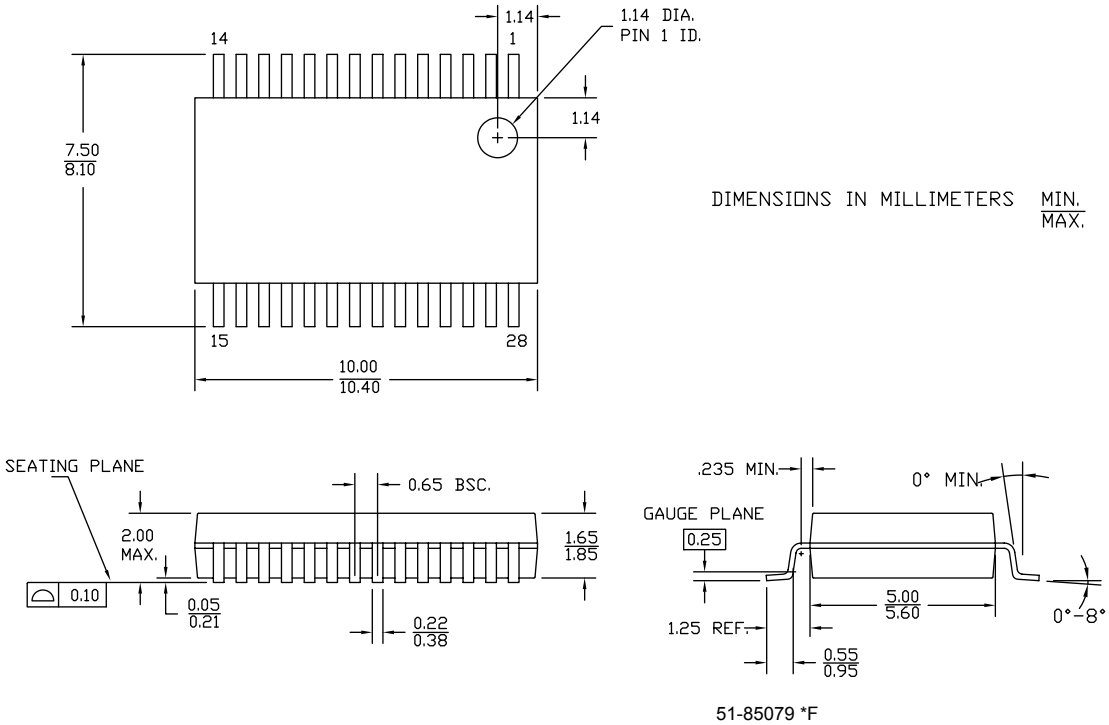


NOTES:

1. HATCH AREA IS SOLDERABLE EXPOSED PAD
2. BASED ON REF JEDEC # MO-248
3. PACKAGE WEIGHT: 38mg ± 4 mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

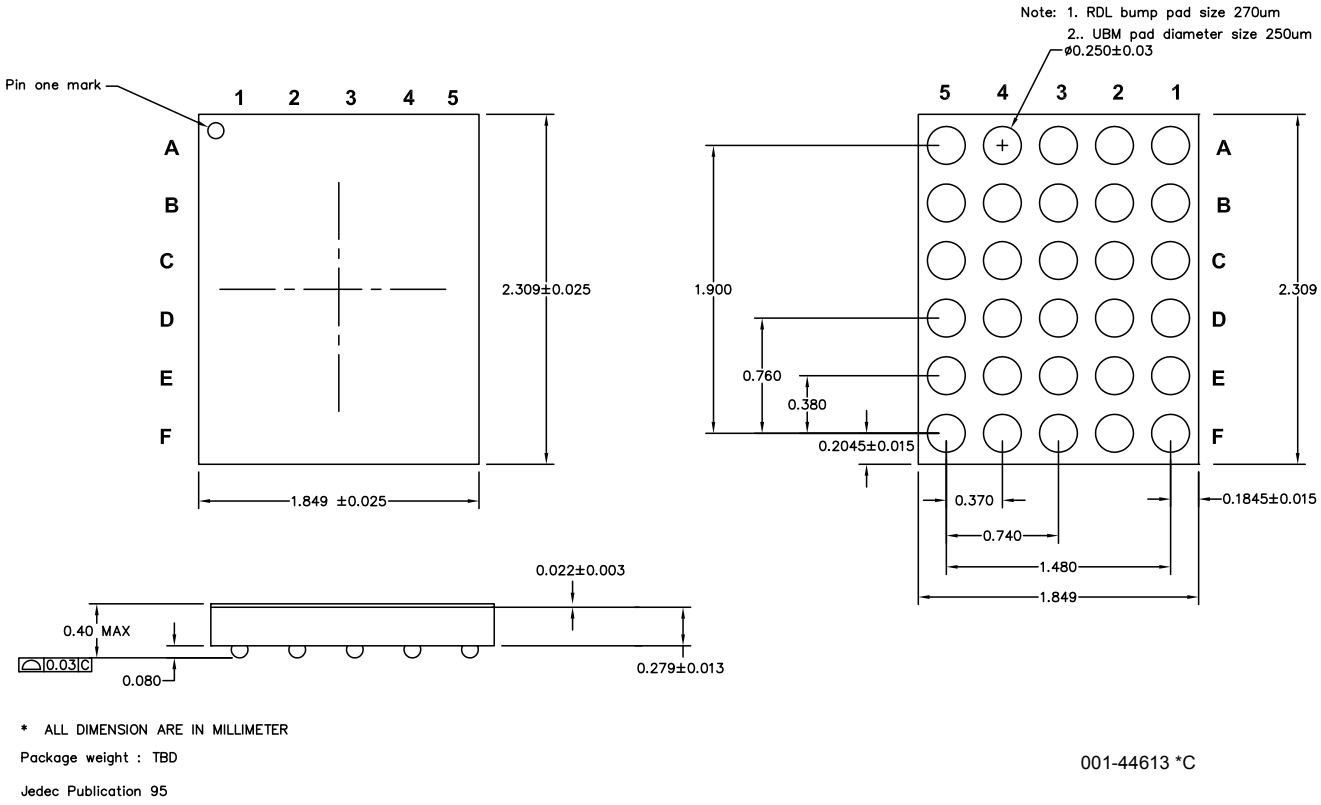
001-48913 *D

Figure 20. 28-pin SSOP (210 Mils)



51-85079 *F

Figure 21. 30-Ball (1.85 × 2.31 × 0.40 mm) WLCSP



Important Note For information on the preferred dimensions for mounting the QFN packages, see the application note *Design Guidelines for Cypress Quad Flat No Extended Lead (QFN) Packaged Devices – AN72845* available at http://www.cypress.com.

It is important to note that pinned vias for thermal conduction are not required for the low power 24, 32, and 48-pin QFN PSoC devices.

Thermal Impedances

Table 33 illustrates the minimum solder reflow peak temperature to achieve good solderability.

Table 33. Thermal Impedances Per Package

Package	Typical θ_{JA} [28]
8 SOIC	127 °C/W
16 SOIC	80 °C/W
16 QFN	46 °C/W
24 QFN[29]	25 °C/W
28 SSOP	96 °C/W
30 WLCSP	54 °C/W
32 QFN[29]	27 °C/W
48 QFN[29]	28 °C/W

Solder Reflow Specifications

Table 34 shows the solder reflow temperature limits that must not be exceeded.

Table 34. Solder Reflow Specifications

Package	Maximum Peak Temperature (T_C)	Maximum Time above T_C – 5 °C
8-Pin SOIC	260 °C	30 seconds
16-Pin SOIC	260 °C	30 seconds
16-Pin QFN	260 °C	30 seconds
24-Pin QFN	260 °C	30 seconds
28-Pin SSOP	260 °C	30 seconds
30-Pin WLCSP	260 °C	30 seconds
32-Pin QFN	260 °C	30 seconds
48-Pin QFN	260 °C	30 seconds

Notes
28. $T_J = T_A$ + Power × θ_{JA}.
29. To achieve the thermal impedance specified for the QFN package, refer to application note *Design Guidelines for Cypress Quad Flat No Extended Lead (QFN) Packaged Devices – AN72845* available at http://www.cypress.com.
30. Higher temperatures is required based on the solder melting point. Typical temperatures for solder are 220 ±5 °C with Sn-Pb or 245 ± 5 °C with Sn-Ag-Cu paste. Refer to the solder manufacturer specifications.

Ordering Information

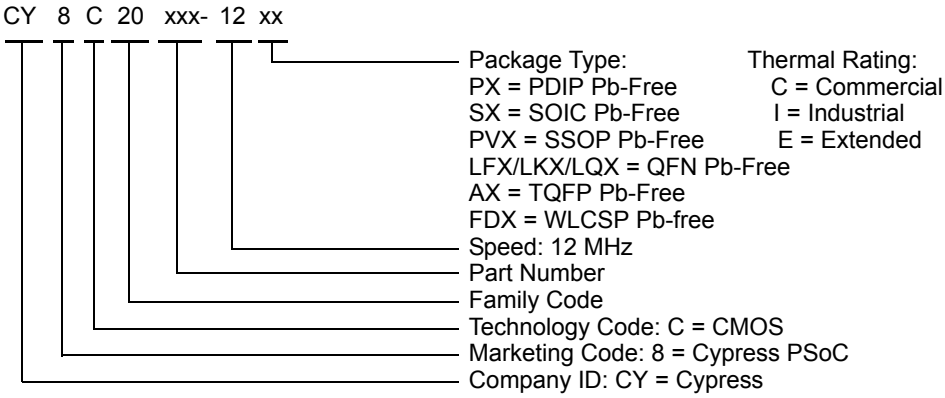
Table 36 lists the CY8C20234, CY8C20334, CY8C20434, CY8C20534, and CY8C20634 PSoC device's key package features and ordering codes.

Table 36. PSoC Device Key Features and Ordering Information

Ordering Code	Package	Flash (Bytes)	SRAM (Bytes)	Digital Blocks	CapSense-Blocks	Digital I/O Pins	Analog Inputs	Analog Outputs	XRES Pin
CY8C20134-12SXI	8-Pin SOIC	8 K	512	0	1	6	6	0	No
CY8C20234-12SXI	16-Pin SOIC	8 K	512	0	1	13	13	0	Yes
CY8C20234-12SXIT	16-pin SOIC	8 K	512	0	1	13	13	0	Yes
CY8C20534-12PVXI	28-Pin SSOP	8 K	512	0	1	24	24[31]	0	Yes
CY8C20534-12PVXIT	28-Pin SSOP	8 K	512	0	1	24	24[31]	0	Yes
CY8C20000-12LFXI	48-Pin OCD QFN[16]	8 K	512	0	1	28	28[31]	0	Yes
CY8C20234-12LKXI	16-Pin (3 × 3 mm 0.60 Max) Sawn QFN	8 K	512	0	1	13	13[31]	0	Yes
CY8C20234-12LKXIT	16-Pin (3 × 3 mm 0.60 Max) Sawn QFN (Tape and Reel)	8 K	512	0	1	13	13[31]	0	Yes
CY8C20334-12LQXI	24-Pin (4 × 4 mm 0.60 Max) Sawn QFN	8 K	512	0	1	20	20[31]	0	Yes
CY8C20334-12LQXIT	24-Pin (4 × 4 mm 0.60 Max) Sawn QFN (Tape and Reel)	8 K	512	0	1	20	20[31]	0	Yes
CY8C20434-12LQXI	32-Pin (5 × 5 mm 0.60 Max) Thin Sawn QFN	8 K	512	0	1	28	28	0	Yes
CY8C20434-12LQXIT	32-Pin (5 × 5 mm 0.60 Max) Thin Sawn QFN (Tape and Reel)	8 K	512	0	1	28	28	0	Yes
CY8C20634-12FDXI	30-Ball WLCSP	8 K	512	0	1	27	27	0	Yes
CY8C20634-12FDXIT	30-Ball WLCSP (Tape and Reel)	8 K	512	0	1	27	27	0	Yes

Note For Die sales information, contact a local Cypress sales office or Field Applications Engineer (FAE).

Ordering Code Definitions



Document Conventions

Units of Measure

Table 38 lists the unit sof measures.

Table 38. Units of Measure

Symbol	Unit of Measure	Symbol	Unit of Measure
°C	degree Celsius	ms	millisecond
pF	picofarad	ns	nanosecond
kHz	kilohertz	ps	picosecond
MHz	megahertz	µV	microvolts
kΩ	kilohm	mV	millivolts
Ω	ohm	V	volts
µA	microampere	W	watt
mA	milliampere	mm	millimeter
nA	nanoampere	%	percent
µs	microsecond		

Numeric Conventions

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase ‘h’ (for example, ‘14h’ or ‘3Ah’). Hexadecimal numbers may also be represented by a ‘0x’ prefix, the C coding convention. Binary numbers have an appended lowercase ‘b’ (for example, 01010100b’ or ‘01000011b’). Numbers not indicated by an ‘h’ or ‘b’ are decimals.

Glossary

active high	1. A logic signal having its asserted state as the logic 1 state. 2. A logic signal having the logic 1 state as the higher voltage of the two states.
analog blocks	The basic programmable opamp circuits. These are SC (switched capacitor) and CT (continuous time) blocks. These blocks can be interconnected to provide ADCs, DACs, multi-pole filters, gain stages, and much more.
analog-to-digital (ADC)	A device that changes an analog signal to a digital signal of corresponding magnitude. Typically, an ADC converts a voltage to a digital number. The digital-to-analog (DAC) converter performs the reverse operation.
Application programming interface (API)	A series of software routines that comprise an interface between a computer application and lower level services and functions (for example, user modules and libraries). APIs serve as building blocks for programmers that create software applications.
asynchronous	A signal whose data is acknowledged or acted upon immediately, irrespective of any clock signal.
Bandgap reference	A stable voltage reference design that matches the positive temperature coefficient of VT with the negative temperature coefficient of VBE, to produce a zero temperature coefficient (ideally) reference.
bandwidth	1. The frequency range of a message or information processing system measured in hertz. 2. The width of the spectral region over which an amplifier (or absorber) has substantial gain (or loss); it is sometimes represented more specifically as, for example, full width at half maximum.
bias	1. A systematic deviation of a value from a reference value. 2. The amount by which the average of a set of values departs from a reference value. 3. The electrical, mechanical, magnetic, or other force (field) applied to a device to establish a reference level to operate the device.

Glossary

External Reset (XRES)	An active high signal that is driven into the PSoC device. It causes all operation of the CPU and blocks to stop and return to a pre-defined state.
Flash	An electrically programmable and erasable, non-volatile technology that provides you the programmability and data storage of EPROMs, plus in-system erasability. Non-volatile means that the data is retained when power is OFF.
Flash block	The smallest amount of Flash ROM space that may be programmed at one time and the smallest amount of Flash space that may be protected. A Flash block holds 64 bytes.
frequency	The number of cycles or events per unit of time, for a periodic function.
gain	The ratio of output current, voltage, or power to input current, voltage, or power, respectively. Gain is usually expressed in dB.
I^2C	A two-wire serial computer bus by Philips Semiconductors (now NXP Semiconductors). I2C is an Inter-Integrated Circuit. It is used to connect low-speed peripherals in an embedded system. The original system was created in the early 1980s as a battery control interface, but it was later used as a simple internal bus system for building control electronics. I2C uses only two bi-directional pins, clock and data, both running at +5V and pulled high with resistors. The bus operates at 100 kbits/second in standard mode and 400 kbits/second in fast mode.
ICE	The in-circuit emulator that allows you to test the project in a hardware environment, while viewing the debugging device activity in a software environment (PSoC Designer).
input/output (I/O)	A device that introduces data into or extracts data from a system.
interrupt	A suspension of a process, such as the execution of a computer program, caused by an event external to that process, and performed in such a way that the process can be resumed.
interrupt service routine (ISR)	A block of code that normal code execution is diverted to when the M8C receives a hardware interrupt. Many interrupt sources may each exist with its own priority and individual ISR code block. Each ISR code block ends with the RETI instruction, returning the device to the point in the program where it left normal program execution.
jitter	1. A misplacement of the timing of a transition from its ideal position. A typical form of corruption that occurs on serial data streams. 2. The abrupt and unwanted variations of one or more signal characteristics, such as the interval between successive pulses, the amplitude of successive cycles, or the frequency or phase of successive cycles.
low-voltage detect (LVD)	A circuit that senses V_{DD} and provides an interrupt to the system when V_{DD} falls lower than a selected threshold.
M8C	An 8-bit Harvard-architecture microprocessor. The microprocessor coordinates all activity inside a PSoC by interfacing to the Flash, SRAM, and register space.
master device	A device that controls the timing for data exchanges between two devices. Or when devices are cascaded in width, the master device is the one that controls the timing for data exchanges between the cascaded devices and an external interface. The controlled device is called the ***slave device.***
microcontroller	An integrated circuit chip that is designed primarily for control systems and products. In addition to a CPU, a microcontroller typically includes memory, timing circuits, and IO circuitry. The reason for this is to permit the realization of a controller with a minimal quantity of chips, thus achieving maximal possible miniaturization. This in turn, reduces the volume and the cost of the controller. The microcontroller is normally not used for general-purpose computation as is a microprocessor.
mixed-signal	The reference to a circuit containing both analog and digital techniques and components.

Glossary

modulator	A device that imposes a signal on a carrier.
noise	1. A disturbance that affects a signal and that may distort the information carried by the signal. 2. The random variations of one or more characteristics of any entity such as voltage, current, or data.
oscillator	A circuit that may be crystal controlled and is used to generate a clock frequency.
parity	A technique for testing transmitting data. Typically, a binary digit is added to the data to make the sum of all the digits of the binary data either always even (even parity) or always odd (odd parity).
Phase-locked loop (PLL)	An electronic circuit that controls an ***oscillator*** so that it maintains a constant phase angle relative to a reference signal.
pinouts	The pin number assignment: the relation between the logical inputs and outputs of the PSoC device and their physical counterparts in the printed circuit board (PCB) package. Pinouts involve pin numbers as a link between schematic and PCB design (both being computer generated files) and may also involve pin names.
port	A group of pins, usually eight.
Power on reset (POR)	A circuit that forces the PSoC device to reset when the voltage is lower than a pre-set level. This is a type of hardware reset.
PSoC®	Cypress Semiconductor's PSoC® is a registered trademark and Programmable System-on-Chip™ is a trademark of Cypress.
PSoC Designer™	The software for Cypress' Programmable System-on-Chip technology.
pulse width modulator (PWM)	An output in the form of duty cycle which varies as a function of the applied measurand
RAM	An acronym for random access memory. A data-storage device from which data can be read out and new data can be written in.
register	A storage device with a specific capacity, such as a bit or byte.
reset	A means of bringing a system back to a know state. See hardware reset and software reset.
ROM	An acronym for read only memory. A data-storage device from which data can be read out, but new data cannot be written in.
serial	1. Pertaining to a process in which all events occur one after the other. 2. Pertaining to the sequential or consecutive occurrence of two or more related activities in a single device or channel.
settling time	The time it takes for an output signal or value to stabilize after the input has changed from one value to another.
shift register	A memory storage device that sequentially shifts a word either left or right to output a stream of serial data.
slave device	A device that allows another device to control the timing for data exchanges between two devices. Or when devices are cascaded in width, the slave device is the one that allows another device to control the timing of data exchanges between the cascaded devices and an external interface. The controlling device is called the master device.

Document History Page

Document Title: CY8C20134/CY8C20234/CY8C20334/CY8C20434/CY8C20534/CY8C20634, PSoC® Programmable System-on-Chip™ Document Number: 001-05356				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*Q	3638597	BVI	06/06/2012	Updated F_{SCLK} parameter in the Table 32, “SPI Slave AC Specifications,” on page 31. Changed t_{OUT_HIGH} to t_{OUT_H} in Table 31, “SPI Master AC Specifications,” on page 31 Updated package diagrams: 001-13937 to *D 001-44613 to *B Removed obsolete specs 001-17397 and 001-14503 referenced in page 40
*R	4306760	PRKU	03/26/2014	Added note to connect all V_{SS} pins to one common GND plane. Updated 16-pin COL (Sawn) package drawing.
*S	4455557	DIMA	08/13/2014	Replaced references of “Application Notes for Surface Mount Assembly of Amkor’s MicroLeadFrame (MLF) Packages” with “Design Guidelines for Cypress Quad Flat No Extended Lead (QFN) Packaged Devices – AN72845” in all instances across the document. Added CapSense Design Resources. Updated Ordering Information: Updated Table 36: Added CY8C20234-12SXIT and its corresponding details.
*T	4748586	DIMA	05/14/2015	Removed “CapSense Design Resources”. Added More Information. Updated Packaging Dimensions: spec 51-85066 – Changed revision from *F to *G. spec 001-13937 – Changed revision from *E to *F. spec 51-85079 – Changed revision from *E to *F. Updated to new template. Completing Sunset Review.

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