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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	40MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, POR, PWM, WDT
Number of I/O	54
Program Memory Size	48KB (24K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	3.8K x 8
Voltage - Supply (Vcc/Vdd)	4.2V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18f6527-i-pt

PIC18F8722 FAMILY

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If the IRCF bits and the INTSRC bit are all clear, the INTOSC output is not enabled and the IOFS bit will remain clear; there will be no indication of the current clock source. The INTRC source is providing the device clocks.

If the IRCF bits are changed from all clear (thus, enabling the INTOSC output) or if INTSRC is set, the IOFS bit becomes set after the INTOSC output becomes stable. Clocks to the device continue while the INTOSC source stabilizes after an interval of TIOBST (parameter 39, Table 28-12).

If the IRCF bits were previously at a non-zero value, or if INTSRC was set before setting SCS1 and the INTOSC source was already stable, the IOFS bit will remain set.

On transitions from RC_RUN mode to PRI_RUN mode, the device continues to be clocked from the INTOSC multiplexer while the primary clock is started. When the primary clock becomes ready, a clock switch to the primary clock occurs (see Figure 3-4). When the clock switch is complete, the IOFS bit is cleared, the OST bit is set and the primary clock is providing the device clock. The IDLEN and SCS bits are not affected by the switch. The INTRC source will continue to run if either the WDT or the Fail-Safe Clock Monitor is enabled.

FIGURE 3-3: TRANSITION TIMING TO RC_RUN MODE

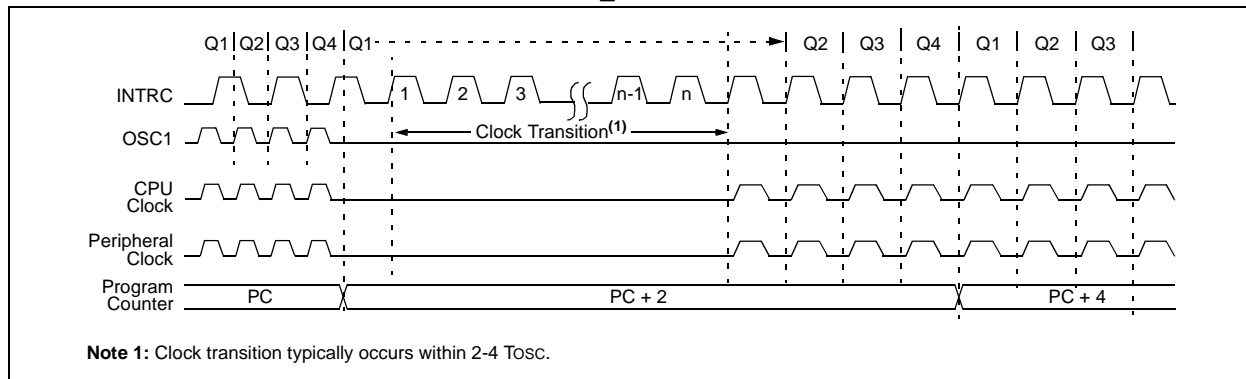
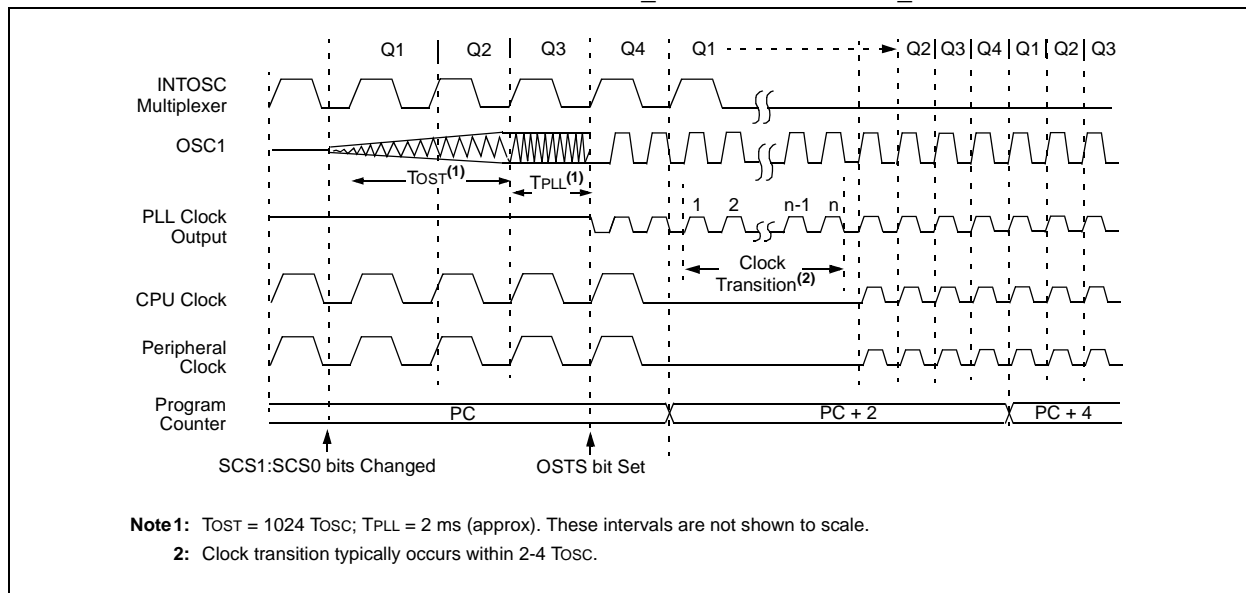


FIGURE 3-4: TRANSITION TIMING FROM RC_RUN MODE TO PRI_RUN MODE



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TABLE 4-4: INITIALIZATION CONDITIONS FOR ALL REGISTERS (CONTINUED)

Register	Applicable Devices				Power-on Reset, Brown-out Reset	MCLR Resets, WDT Reset, RESET Instruction, Stack Resets	Wake-up via WDT or Interrupt
FSR1H	6X27	6X22	8X27	8X22	---- 0000	---- 0000	---- uuuu
FSR1L	6X27	6X22	8X27	8X22	xxxx xxxx	uuuu uuuu	uuuu uuuu
BSR	6X27	6X22	8X27	8X22	---- 0000	---- 0000	---- uuuu
INDF2	6X27	6X22	8X27	8X22	N/A	N/A	N/A
POSTINC2	6X27	6X22	8X27	8X22	N/A	N/A	N/A
POSTDEC2	6X27	6X22	8X27	8X22	N/A	N/A	N/A
PREINC2	6X27	6X22	8X27	8X22	N/A	N/A	N/A
PLUSW2	6X27	6X22	8X27	8X22	N/A	N/A	N/A
FSR2H	6X27	6X22	8X27	8X22	---- 0000	---- 0000	---- uuuu
FSR2L	6X27	6X22	8X27	8X22	xxxx xxxx	uuuu uuuu	uuuu uuuu
STATUS	6X27	6X22	8X27	8X22	---x xxxx	---u uuuu	---u uuuu
TMR0H	6X27	6X22	8X27	8X22	0000 0000	0000 0000	uuuu uuuu
TMR0L	6X27	6X22	8X27	8X22	xxxx xxxx	uuuu uuuu	uuuu uuuu
T0CON	6X27	6X22	8X27	8X22	1111 1111	1111 1111	uuuu uuuu
OSCCON	6X27	6X22	8X27	8X22	0100 q000	0100 q000	uuuu uuqu
HLVDCON	6X27	6X22	8X27	8X22	0-00 0101	0-00 0101	u-uu uuuu
WDTCON	6X27	6X22	8X27	8X22	---- ---0	---- ---0	---- ---u
RCON ⁽⁴⁾	6X27	6X22	8X27	8X22	0q-1 11q0	0q-q qquu	uq-u qquu
TMR1H	6X27	6X22	8X27	8X22	xxxx xxxx	uuuu uuuu	uuuu uuuu
TMR1L	6X27	6X22	8X27	8X22	xxxx xxxx	uuuu uuuu	uuuu uuuu
T1CON	6X27	6X22	8X27	8X22	0000 0000	u0uu uuuu	uuuu uuuu
TMR2	6X27	6X22	8X27	8X22	0000 0000	0000 0000	uuuu uuuu
PR2	6X27	6X22	8X27	8X22	1111 1111	uuuu uuuu	uuuu uuuu
T2CON	6X27	6X22	8X27	8X22	-000 0000	-000 0000	-uuu uuuu
SSP1BUF	6X27	6X22	8X27	8X22	xxxx xxxx	uuuu uuuu	uuuu uuuu
SSP1ADD	6X27	6X22	8X27	8X22	0000 0000	0000 0000	uuuu uuuu
SSP1STAT	6X27	6X22	8X27	8X22	0000 0000	0000 0000	uuuu uuuu
SSP1CON1	6X27	6X22	8X27	8X22	0000 0000	0000 0000	uuuu uuuu
SSP1CON2	6X27	6X22	8X27	8X22	0000 0000	0000 0000	uuuu uuuu

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as '0', q = value depends on condition.

Shaded cells indicate conditions do not apply for the designated device.

- Note**
- 1: One or more bits in the INTCONx or PIRx registers will be affected (to cause wake-up).
 - 2: When the wake-up is due to an interrupt and the GIEL or GIEH bit is set, the PC is loaded with the interrupt vector (0008h or 0018h).
 - 3: When the wake-up is due to an interrupt and the GIEL or GIEH bit is set, the TOSU, TOSH and TOSL are updated with the current value of the PC. The STKPTR is modified to point to the next location in the hardware stack.
 - 4: See Table 4-3 for Reset value for specific condition.
 - 5: Bits 6 and 7 of PORTA, LATA and TRISA are enabled, depending on the oscillator mode selected. When not enabled as PORTA pins, they are disabled and read '0'.

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TABLE 5-3: REGISTER FILE SUMMARY (CONTINUED)

File Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Details on page:
PORTJ ⁽²⁾	RJ7	RJ6	RJ5	RJ4	RJ3	RJ2	RJ1	RJ0	xxxx xxxx	60, 156
PORTH ⁽²⁾	RH7	RH6	RH5	RH4	RH3	RH2	RH1	RH0	0000 xxxx	60, 154
PORTG	—	—	RG5 ⁽⁵⁾	RG4	RG3	RG2	RG1	RG0	--xx xxxx	60, 151
PORTF	RF7	RF6	RF5	RF4	RF3	RF2	RF1	RF0	x000 0000	60, 149
PORTE	RE7	RE6	RE5	RE4	RE3	RE2	RE1	RE0	xxxx xxxx	60, 146
PORTD	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	xxxx xxxx	60, 143
PORTC	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	xxxx xxxx	60, 140
PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx xxxx	60, 137
PORTA	RA7 ⁽⁴⁾	RA6 ⁽⁴⁾	RA5	RA4	RA3	RA2	RA1	RA0	xx0x 0000	61, 135
SPBRGH1	EUSART1 Baud Rate Generator Register High Byte								0000 0000	61, 252
BAUDCON1	ABDOVF	RCIDL	—	SCKP	BRG16	—	WUE	ABDEN	01-0 0-00	61, 250
SPBRGH2	EUSART2 Baud Rate Generator Register High Byte								0000 0000	61, 252
BAUDCON2	ABDOVF	RCIDL	—	SCKP	BRG16	—	WUE	ABDEN	01-0 0-00	61, 250
ECCP1DEL	P1RSEN	P1DC6	P1DC5	P1DC4	P1DC3	P1DC2	P1DC1	P1DC0	0000 0000	61, 200
TMR4	Timer4 Register								0000 0000	61, 178
PR4	Timer4 Period Register								1111 1111	61, 178
T4CON	—	T4OUTPS3	T4OUTPS2	T4OUTPS1	T4OUTPS0	TMR4ON	T4CKPS1	T4CKPS0	-000 0000	61, 178
CCPR4H	Capture/Compare/PWM Register 4 High Byte								xxxx xxxx	61, 180
CCPR4L	Capture/Compare/PWM Register 4 Low Byte								xxxx xxxx	61, 180
CCP4CON	—	—	DC4B1	DC4B0	CCP4M3	CCP4M2	CCP4M1	CCP4M0	--00 0000	61, 179
CCPR5H	Capture/Compare/PWM Register 5 High Byte								xxxx xxxx	61, 180
CCPR5L	Capture/Compare/PWM Register 5 Low Byte								xxxx xxxx	61, 180
CCP5CON	—	—	DC5B1	DC5B0	CCP5M3	CCP5M2	CCP5M1	CCP5M0	--00 0000	61, 179
SPBRG2	EUSART2 Baud Rate Generator Register Low Byte								0000 0000	61, 252
RCREG2	EUSART2 Receive Register								0000 0000	61, 260
TXREG2	EUSART2 Transmit Register								0000 0000	61, 257
TXSTA2	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	0000 0010	61, 248
RCSTA2	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000x	61, 249
ECCP3AS	ECCP3ASE	ECCP3AS2	ECCP3AS1	ECCP3AS0	PSS3AC1	PSS3AC0	PSS3BD1	PSS3BD0	0000 0000	61, 201
ECCP3DEL	P3RSEN	P3DC6	P3DC5	P3DC4	P3DC3	P3DC2	P3DC1	P3DC0	0000 0000	61, 200
ECCP2AS	ECCP2ASE	ECCP2AS2	ECCP2AS1	ECCP2AS0	PSS2AC1	PSS2AC0	PSS2BD1	PSS2BD0	0000 0000	61, 201
ECCP2DEL	P2RSEN	P2DC6	P2DC5	P2DC4	P2DC3	P2DC2	P2DC1	P2DC0	0000 0000	61, 200
SSP2BUF	MSSP2 Receive Buffer/Transmit Register								xxxx xxxx	61, 170
SSP2ADD	MSSP2 Address Register in I ² C™ Slave mode. MSSP2 Baud Rate Reload Register in I ² C Master mode.								0000 0000	61, 170
SSP2STAT	SMP	CKE	D/A	P	S	R/W	UA	BF	0000 0000	61, 216
SSP2CON1	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	61, 217
SSP2CON2	GCEN	ACKSTAT	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	0000 0000	61, 218

Legend: x = unknown, u = unchanged, - = unimplemented, q = value depends on condition

- Note**
- 1: The SBOREN bit is only available when the BOREN<1:0> Configuration bits = 01; otherwise, this bit reads as '0'.
 - 2: These registers and/or bits are not implemented on 64-pin devices and are read as '0'. Reset values are shown for 80-pin devices; individual unimplemented bits should be interpreted as '-'.
3: The PLEN bit is only available in specific oscillator configuration; otherwise, it is disabled and reads as '0'. See **Section 2.6.4 “PLL in INTOSC Modes”**.
 - 4: RA6/RA7 and their associated latch and direction bits are individually configured as port pins based on various primary oscillator modes. When disabled, these bits read as '0'.
 - 5: RG5 and LATG5 are only available when Master Clear is disabled (MCLRE Configuration bit = 0); otherwise, RG5 and LATG5 read as '0'.
 - 6: Bit 7 and Bit 6 are cleared by user software or by a POR.
 - 7: Bit 21 of TBLPTRU allows access to the device Configuration bits.

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5.3.5 STATUS REGISTER

The STATUS register, shown in Register 5-2, contains the arithmetic status of the ALU. As with any other SFR, it can be the operand for any instruction.

If the STATUS register is the destination for an instruction that affects the Z, DC, C, OV or N bits, the results of the instruction are not written; instead, the STATUS register is updated according to the instruction performed. Therefore, the result of an instruction with the STATUS register as its destination may be different than intended. As an example, `CLRF STATUS` will set the Z bit and leave the remaining Status bits unchanged ('000u u1uu').

It is recommended that only `BCF`, `BSF`, `SWAPF`, `MOVFF` and `MOVWF` instructions are used to alter the STATUS register, because these instructions do not affect the Z, C, DC, OV or N bits in the STATUS register.

For other instructions that do not affect Status bits, see the instruction set summaries in Table 26-2 and Table 26-3.

Note: The C and DC bits operate as the borrow and digit borrow bits, respectively, in subtraction.

REGISTER 5-2: STATUS: ARITHMETIC STATUS REGISTER

U-0		U-0		U-0		R/W-x		R/W-x		R/W-x		R/W-x		R/W-x	
—		—		—		N		OV		Z		DC ⁽¹⁾		C ⁽²⁾	
bit 7														bit 0	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7-5 **Unimplemented:** Read as '0'

bit 4 **N:** Negative bit

This bit is used for signed arithmetic (2's complement). It indicates whether the result was negative (ALU MSB = 1).

1 = Result was negative

0 = Result was positive

bit 3 **OV:** Overflow bit

This bit is used for signed arithmetic (2's complement). It indicates an overflow of the 7-bit magnitude which causes the sign bit (bit 7 of the result) to change state.

1 = Overflow occurred for signed arithmetic (in this arithmetic operation)

0 = No overflow occurred

bit 2 **Z:** Zero bit

1 = The result of an arithmetic or logic operation is zero

0 = The result of an arithmetic or logic operation is not zero

bit 1 **DC:** Digit Carry/borrow bit⁽¹⁾

For `ADDWF`, `ADDLW`, `SUBLW` and `SUBWF` instructions:

1 = A carry-out from the 4th low-order bit of the result occurred

0 = No carry-out from the 4th low-order bit of the result

bit 0 **C:** Carry/borrow bit⁽²⁾

For `ADDWF`, `ADDLW`, `SUBLW` and `SUBWF` instructions:

1 = A carry-out from the Most Significant bit of the result occurred

0 = No carry-out from the Most Significant bit of the result occurred

Note 1: For borrow, the polarity is reversed. A subtraction is executed by adding the 2's complement of the second operand. For rotate (`RRF`, `RLF`) instructions, this bit is loaded with either bit 4 or bit 3 of the source register.

2: For borrow, the polarity is reversed. A subtraction is executed by adding the 2's complement of the second operand. For rotate (`RRF`, `RLF`) instructions, this bit is loaded with either the high or low-order bit of the source register.

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7.1 External Memory Bus Control

The operation of the interface is controlled by the MEMCON register (Register 7-1). This register is available in all program memory operating modes except Microcontroller mode. In this mode, the register is disabled and cannot be written to.

The EBDIS bit (MEMCON<7>) controls the operation of the bus and related port functions. Clearing EBDIS enables the interface and disables the I/O functions of the ports, as well as any other functions multiplexed to those pins. Setting the bit enables the I/O ports and other functions but allows the interface to override everything else on the pins when an external memory operation is required. By default, the external bus is always enabled and disables all other I/O.

The operation of the EBDIS bit is also influenced by the program memory mode being used. This is discussed in more detail in **Section 7.4 “Program Memory Modes and the External Memory Bus”**.

The WAIT bits allow for the addition of wait states to external memory operations. The use of these bits is discussed in **Section 7.3 “Wait States”**.

The WM bits select the particular operating mode used when the bus is operating in 16-bit Data Width mode. These are discussed in more detail in **Section 7.5 “16-Bit Data Width Modes”**. These bits have no effect when an 8-bit Data Width mode is selected.

WM<1:0>: TBLWT Operation with 16-Bit Data Bus Width Select bits

- 1x = Word Write mode: TABLAT0 and TABLAT1 word output, WRH active when TABLAT1 written
- 01 = Byte Select mode: TABLAT data copied on both MSB and LSB; WRH and (UB or LB) will activate

REGISTER 7-1: MEMCON: EXTERNAL MEMORY BUS CONTROL REGISTER

R/W-0	U-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0
EBDIS	—	WAIT1	WAIT0	—	—	WM1	WM0
bit 7							bit 0

Legend:

R = Readable bit
-n = Value at POR

W = Writable bit
'1' = Bit is set

U = Unimplemented bit, read as '0'
'0' = Bit is cleared
x = Bit is unknown

- bit 7 **EBDIS:** External Bus Disable bit
 - 1 = External bus enabled when microcontroller accesses external memory; otherwise, all external bus drivers are mapped as I/O ports
 - 0 = External bus always enabled, I/O ports are disabled
- bit 6 **Unimplemented:** Read as '0'
- bit 5-4 **WAIT<1:0>:** Table Reads and Writes Bus Cycle Wait Count bits
 - 11 = Table reads and writes will wait 0 Tcy
 - 10 = Table reads and writes will wait 1 Tcy
 - 01 = Table reads and writes will wait 2 Tcy
 - 00 = Table reads and writes will wait 3 Tcy
- bit 3-2 **Unimplemented:** Read as '0'
- bit 1-0 **WM<1:0>:** TBLWT Operation with 16-Bit Data Bus Width Select bits
 - 1 = Result was negative
 - 0 = Result was positive

7.6.1 8-BIT MODE TIMING

The presentation of control signals on the External Memory Bus is different for the various operating modes. Typical signal timing diagrams are shown in Figure 7-8 through Figure 7-11.

FIGURE 7-8: EXTERNAL BUS TIMING FOR TBLRD (MICROPROCESSOR MODE)

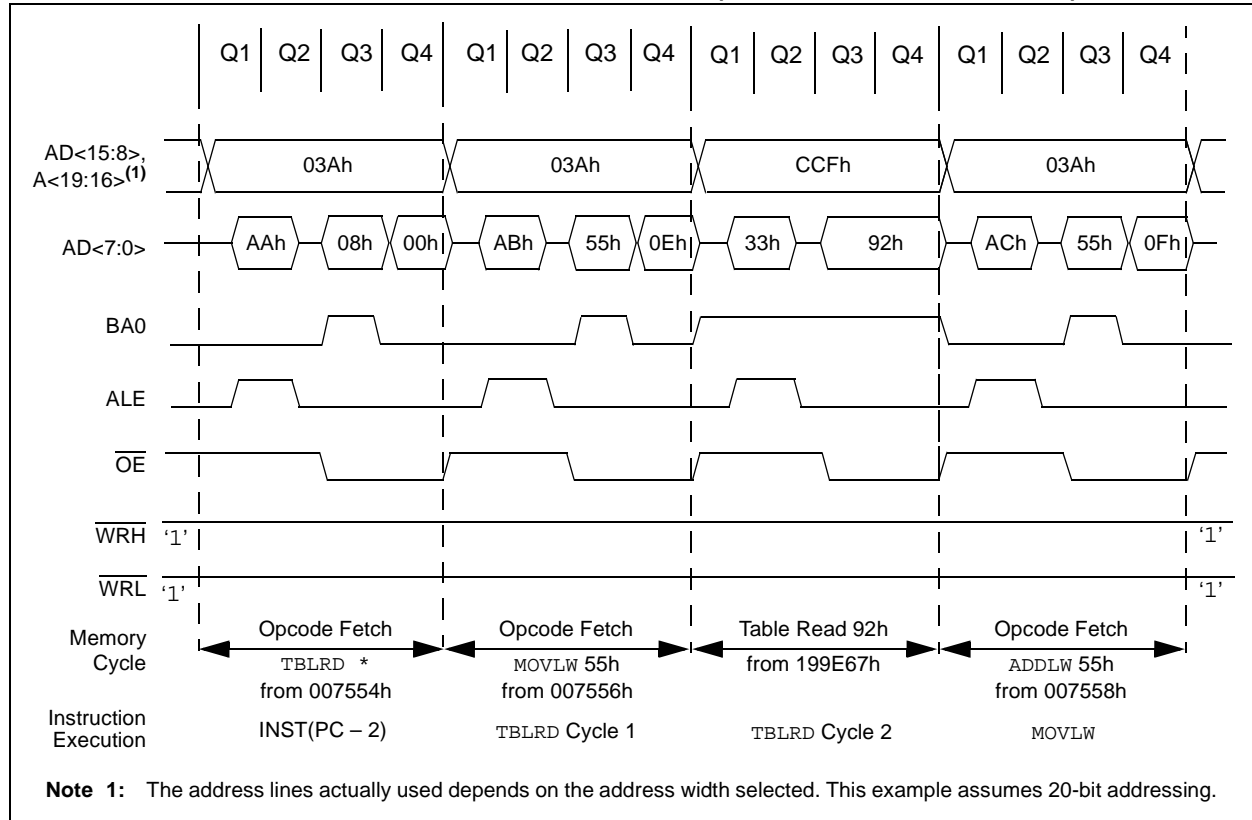
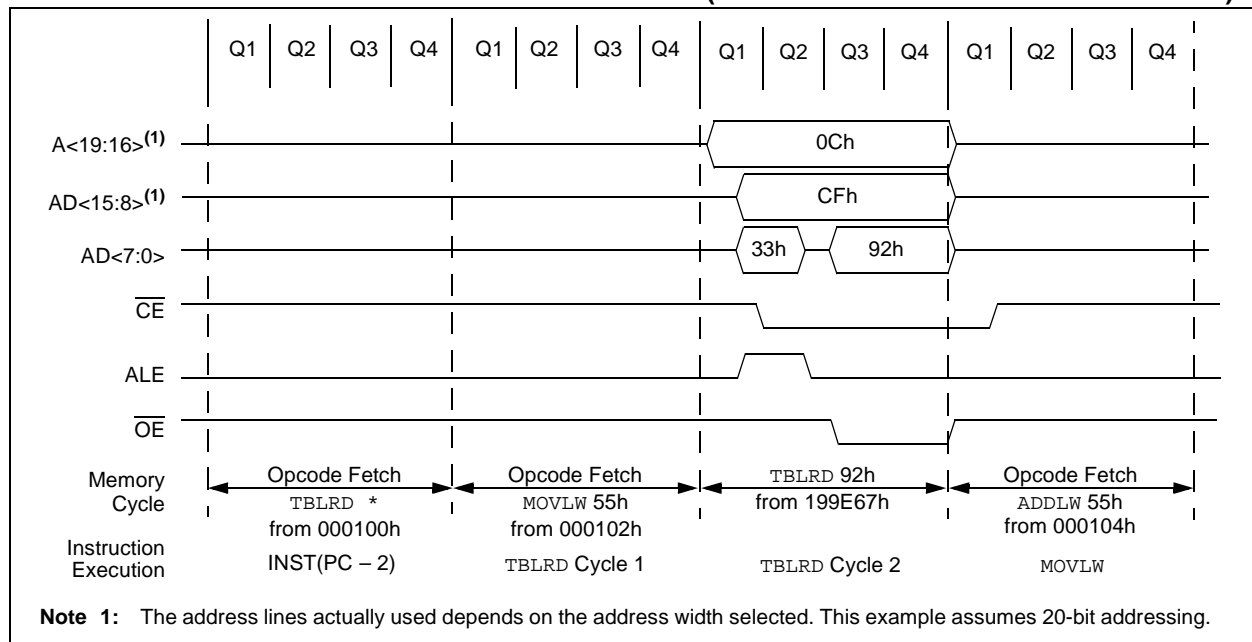


FIGURE 7-9: EXTERNAL BUS TIMING FOR TBLRD (EXTENDED MICROCONTROLLER MODE)



11.2 PORTB, TRISB and LATB Registers

PORTB is an 8-bit wide, bidirectional port. The corresponding Data Direction register is TRISB. Setting a TRISB bit (= 1) will make the corresponding PORTB pin an input (i.e., put the corresponding output driver in a high-impedance mode). Clearing a TRISB bit (= 0) will make the corresponding PORTB pin an output (i.e., put the contents of the output latch on the selected pin).

The Data Latch register (LATB) is also memory mapped. Read-modify-write operations on the LATB register read and write the latched output value for PORTB.

EXAMPLE 11-2: INITIALIZING PORTB

```
CLRF    PORTB    ; Initialize PORTB by
                  ; clearing output
                  ; data latches
CLRF    LATB     ; Alternate method
                  ; to clear output
                  ; data latches
MOVLW   0CFh     ; Value used to
                  ; initialize data
                  ; direction
MOVWF   TRISB    ; Set RB<3:0> as inputs
                  ; RB<5:4> as outputs
                  ; RB<7:6> as inputs
```

Each of the PORTB pins has a weak internal pull-up. A single control bit can turn on all the pull-ups. This is performed by clearing bit $\overline{\text{RBPU}}$ (INTCON2<7>). The weak pull-up is automatically turned off when the port pin is configured as an output. The pull-ups are disabled on a Power-on Reset.

Four of the PORTB pins (RB<7:4>) have an interrupt-on-change feature. Only pins configured as inputs can cause this interrupt to occur (i.e., any RB7:RB4 pin configured as an output is excluded from the interrupt-on-change comparison). The input pins (of RB7:RB4) are compared with the old value latched on the last read of PORTB. The “mismatch” outputs of RB7:RB4 are ORed together to generate the RB Port Change Interrupt with Flag bit, RBIF (INTCON<0>).

This interrupt can wake the device from power-managed modes. The user, in the Interrupt Service Routine, can clear the interrupt in the following manner:

- Any read or write of PORTB (except with the MOVSF, MOVSS, MOVFF (ANY), PORTB instruction). This will end the mismatch condition.
- Clear flag bit, RBIF.

A mismatch condition will continue to set flag bit, RBIF. Reading PORTB will end the mismatch condition and allow flag bit, RBIF, to be cleared.

The interrupt-on-change feature is recommended for wake-up on key depression operation and operations where PORTB is only used for the interrupt-on-change feature. Polling of PORTB is not recommended while using the interrupt-on-change feature.

For 80-pin devices, RB3 can be configured as the alternate peripheral pin for the ECCP2 module by clearing the CCP2MX Configuration bit. This applies only when the device is in one of the operating modes other than the default Microcontroller mode. If the device is in Microcontroller mode, the alternate assignment for ECCP2 is RE7. As with other ECCP2 configurations, the user must ensure that the TRISB<3> bit is set appropriately for the intended operation.

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TABLE 17-2: REGISTERS ASSOCIATED WITH CAPTURE, COMPARE, TIMER1 AND TIMER3

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on page
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	57
RCON	IPEN	SBOREN	—	\overline{RI}	\overline{TO}	\overline{PD}	\overline{POR}	BOR	56
PIR1	PSPIF	ADIF	RC1IF	TX1IF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	60
PIE1	PSPIE	ADIE	RC1IE	TX1IE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	60
IPR1	PSPIP	ADIP	RC1IP	TX1IP	SSP1IP	CCP1IP	TMR2IP	TMR1IP	60
PIR2	OSCFIF	CMIF	—	EEIF	BCL1IF	HLVDIF	TMR3IF	CCP2IF	60
PIE2	OSCFIE	CMIE	—	EEIE	BCL1IE	HLVDIE	TMR3IE	CCP2IE	60
IPR2	OSCFIP	CMIP	—	EEIP	BCL1IP	HLVDIP	TMR3IP	CCP2IP	60
PIR3	SSP2IF	BCL2IF	RC2IF	TX2IF	TMR4IF	CCP5IF	CCP4IF	CCP3IF	60
PIE3	SSP2IE	BCL2IE	RC2IE	TX2IE	TMR4IE	CCP5IE	CCP4IE	CCP3IE	60
IPR3	SSP2IP	BCL2IP	RC2IP	TX2IP	TMR4IP	CCP5IP	CCP4IP	CCP3IP	60
TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	60
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	60
TRISE	TRISE7	TRISE6	TRISE5	TRISE4	TRISE3	TRISE2	TRISE1	TRISE0	60
TRISG	—	—	—	TRISG4	TRISG3	TRISG2	TRISG1	TRISG0	60
TRISH ⁽¹⁾	TRISH7	TRISH6	TRISH5	TRISH4	TRISH3	TRISH2	TRISH1	TRISH0	60
TMR1L	Timer1 Register Low Byte								58
TMR1H	Timer1 Register High Byte								58
T1CON	RD16	T1RUN	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{T1SYN\overline{C}}$	TMR1CS	TMR1ON	58
TMR3H	Timer3 Register High Byte								59
TMR3L	Timer3 Register Low Byte								59
T3CON	RD16	T3CCP2	T3CKPS1	T3CKPS0	T3CCP1	$\overline{T3SYN\overline{C}}$	TMR3CS	TMR3ON	59
CCPR1L	Enhanced Capture/Compare/PWM Register 1 Low Byte								59
CCPR1H	Enhanced Capture/Compare/PWM Register 1 High Byte								59
CCP1CON	P1M1	P1M0	DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0	59
CCPR2L	Enhanced Capture/Compare/PWM Register 2 Low Byte								59
CCPR2H	Enhanced Capture/Compare/PWM Register 2 High Byte								59
CCP2CON	P2M1	P2M0	DC2B1	DC2B0	CCP2M3	CCP2M2	CCP2M1	CCP2M0	59
CCP3CON	P3M1	P3M0	DC3B1	DC3B0	CCP3M3	CCP3M2	CCP3M1	CCP3M0	59
CCP4CON	—	—	DC4B1	DC4B0	CCP4M3	CCP4M2	CCP4M1	CCP4M0	61
CCP5CON	—	—	DC5B1	DC5B0	CCP5M3	CCP5M2	CCP5M1	CCP5M0	61

Legend: — = unimplemented, read as '0'. Shaded cells are not used by Capture/Compare, Timer1 or Timer3.

Note 1: Implemented on 80-pin devices only.

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TABLE 18-3: PIN CONFIGURATIONS FOR ECCP3

ECCP Mode	CCP3CON Configuration	RG0	RE4	RE3	RG3	RH5	RH4
PIC18F6527/6622/6627/6722 Devices:							
Compatible CCP	00xx 11xx	ECCP3	RE4	RE3	RG3/CCP4	N/A	N/A
Dual PWM	10xx 11xx	P3A	P3B	RE3	RG3/CCP4	N/A	N/A
Quad PWM	x1xx 11xx	P3A	P3B	P3C	CCP4/P3D ⁽¹⁾	N/A	N/A
PIC18F8527/8622/8627/8722 Devices, ECCPMX = 1, Microcontroller mode:							
Compatible CCP	00xx 11xx	ECCP3	RE4	RE3	RG3/CCP4	RH5/AN13	RH4/AN12
Dual PWM	10xx 11xx	P3A	P3B	RE3	RG3/CCP4	RH5/AN13	RH4/AN12
Quad PWM	x1xx 11xx	P3A	P3B	P3C	CCP4/P3D ⁽¹⁾	RH5/AN13	RH4/AN12
PIC18F8527/8622/8627/8722 Devices, ECCPMX = 0, Microcontroller mode:							
Compatible CCP	00xx 11xx	ECCP3	RE4	RE3	RG3/CCP4	RH5/AN13	RH4/AN12
Dual PWM	10xx 11xx	P3A	RE4	RE3	RG3/CCP4	P3B	RH4/AN12
Quad PWM	x1xx 11xx	P3A	RE4	RE3	CCP4/P3D ⁽¹⁾	P3B	P3C
PIC18F8527/8622/8627/8722 Devices, ECCPMX = 1, all other Program Memory modes:							
Compatible CCP	00xx 11xx	ECCP3	AD12 ⁽²⁾	AD10 ⁽²⁾	RG3/CCP4	RH5/AN13	RH4/AN12
Dual PWM	10xx 11xx	P3A	AD12/P3B ⁽²⁾	AD10 ⁽²⁾	RG3/CCP4	RH5/AN13	RH4/AN12
Quad PWM	x1xx 11xx	P3A	AD12/P3B ⁽²⁾	P3C/AD10 ⁽¹⁾	CCP4/P3D ⁽¹⁾	RH5/AN13	RH4/AN12
PIC18F8527/8622/8627/8722 Devices, ECCPMX = 0, all other Program Memory modes:							
Compatible CCP	00xx 11xx	ECCP3	AD12 ⁽²⁾	AD10 ⁽²⁾	RG3/CCP4	RH5/AN13	RH4/AN12
Dual PWM	10xx 11xx	P3A	AD12 ⁽²⁾	AD10 ⁽²⁾	RG3/CCP4	P3B	RH4/AN12
Quad PWM	x1xx 11xx	P3A	AD12 ⁽²⁾	AD10 ⁽²⁾	CCP4/P3D ⁽¹⁾	P3B	P3C

Legend: x = Don't care, N/A = Not available. Shaded cells indicate pin assignments not used by ECCP3 in a given mode.

Note 1: With ECCP3 in Quad PWM mode, the CCP4 module's output overrides P3D.

2: The EMB address bus width will determine whether the pin will perform an EMB or port/peripheral function.

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18.4.7.1 Auto-Shutdown and Automatic Restart

The Auto-Shutdown feature can be configured to allow automatic restarts of the module following a shutdown event. This is enabled by setting the P1RSEN bit of the ECCP1DEL register (ECCP1DEL<7>).

In Shutdown mode with P1RSEN = 1 (Figure 18-10), the ECCP1ASE bit will remain set for as long as the cause of the shutdown continues. When the shutdown condition clears, the ECCP1ASE bit is cleared. If P1RSEN = 0 (Figure 18-11), once a shutdown condition occurs, the ECCP1ASE bit will remain set until it is cleared by firmware. Once ECCP1ASE is cleared, the Enhanced PWM will resume at the beginning of the next PWM period.

Note: Writing to the ECCP1ASE bit is disabled while a shutdown condition is active.

Independent of the P1RSEN bit setting, if the auto-shutdown source is one of the comparators, the shutdown condition is a level. The ECCP1ASE bit cannot be cleared as long as the cause of the shutdown persists.

The Auto-Shutdown mode can be forced by writing a '1' to the ECCP1ASE bit.

18.4.8 START-UP CONSIDERATIONS

When the ECCP module is used in the PWM mode, the application hardware must use the proper external pull-up and/or pull-down resistors on the PWM output pins. When the microcontroller is released from Reset, all of the I/O pins are in the high-impedance state. The external circuits must keep the power switch devices in the OFF state until the microcontroller drives the I/O pins with the proper signal levels or activates the PWM output(s).

The CCP1M<1:0> bits (CCP1CON<1:0>) allow the user to choose whether the PWM output signals are active-high or active-low for each pair of PWM output pins (P1A/P1C and P1B/P1D). The PWM output polarities must be selected before the PWM pins are configured as outputs. Changing the polarity configuration while the PWM pins are configured as outputs is not recommended since it may result in damage to the application circuits.

The P1A, P1B, P1C and P1D output latches may not be in the proper states when the PWM module is initialized. Enabling the PWM pins for output at the same time as the ECCP1 module may cause damage to the application circuit. The ECCP1 module must be enabled in the proper output mode and complete a full PWM cycle before configuring the PWM pins as outputs. The completion of a full PWM cycle is indicated by the TMR2IF bit being set as the second PWM period begins.

FIGURE 18-10: PWM AUTO-SHUTDOWN (P1RSEN = 1, AUTO-RESTART ENABLED)

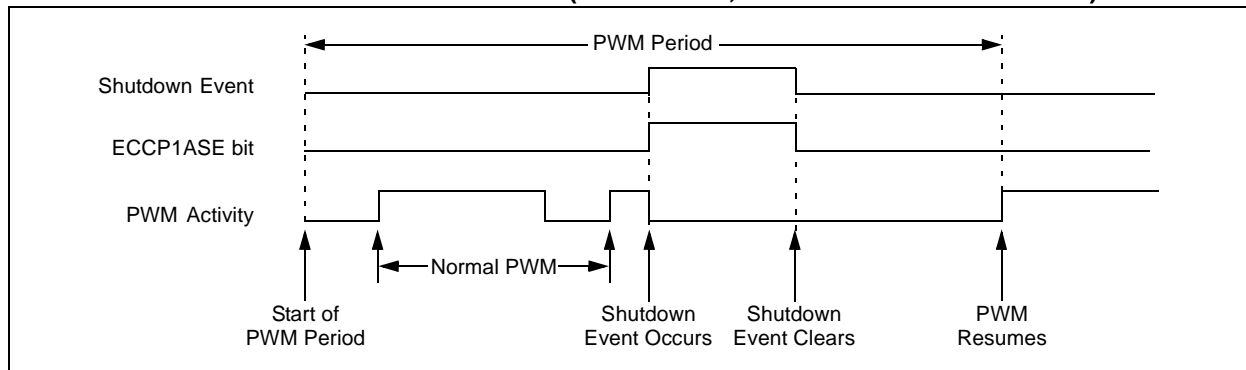
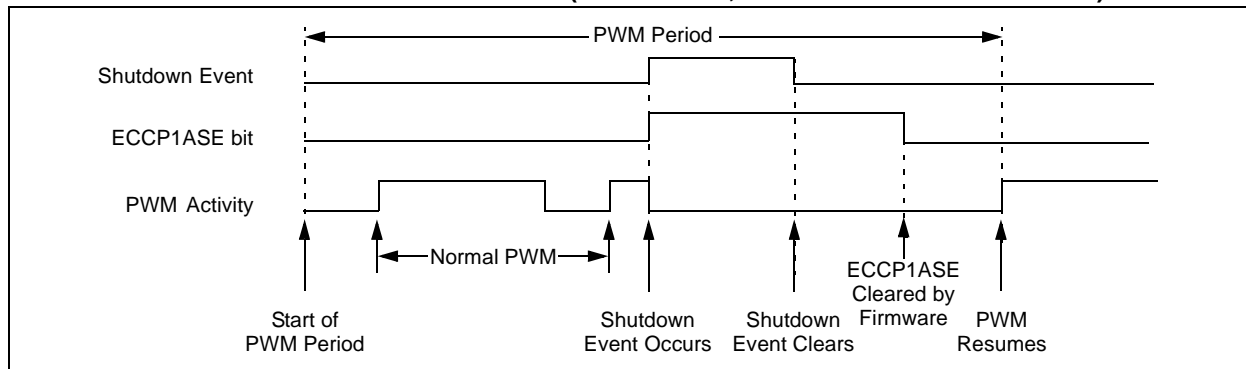


FIGURE 18-11: PWM AUTO-SHUTDOWN (P1RSEN = 0, AUTO-RESTART DISABLED)



Master mode is enabled by setting and clearing the appropriate SSPM bits in SSPxCON1 and by setting the SSPEN bit. In Master mode, the SCLx and SDAx lines are manipulated by the MSSP hardware if the TRIS bits are set.

In Firmware Controlled Master mode, user code conducts all I²C bus operations based on Start and Stop bit conditions.

1. Assert a Start condition on SDAx and SCLx.
2. Assert a Repeated Start condition on SDAx and SCLx.
3. Write to the SSPxBUF register initiating transmission of data/address.
4. Configure the I²C port to receive data.
5. Generate an Acknowledge condition at the end of a received byte of data.
6. Generate a Stop condition on SDAx and SCLx.

The following events will cause the SSP Interrupt Flag bit, SSPxIF, to be set (and SSP interrupt, if enabled):

- FIGURE 19-16: MSSP BLOCK DIAGRAM (I²C™ MASTER MODE)**



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20.4 EUSART Synchronous Slave Mode

Synchronous Slave mode is entered by clearing bit, CSRC (TXSTAx<7>). This mode differs from the Synchronous Master mode in that the shift clock is supplied externally at the CKx pin (instead of being supplied internally in Master mode). This allows the device to transfer or receive data while in any low-power mode.

20.4.1 EUSART SYNCHRONOUS SLAVE TRANSMISSION

The operation of the Synchronous Master and Slave modes is identical, except in the case of Sleep mode.

If two words are written to the TXREGx and then the SLEEP instruction is executed, the following will occur:

- The first word will immediately transfer to the TSRx register and transmit.
- The second word will remain in the TXREGx register.
- Flag bit, TXxIF, will not be set.
- When the first word has been shifted out of TSRx, the TXREGx register will transfer the second word to the TSRx and flag bit, TXxIF, will now be set.
- If enable bit, TXxIE, is set, the interrupt will wake the chip from Sleep. If the global interrupt is enabled, the program will branch to the interrupt vector.

To set up a Synchronous Slave Transmission:

- Enable the synchronous slave serial port by setting bits, SYNC and SPEN, and clearing bit, CSRC.
- Clear bits, CREN and SREN.
- If interrupts are desired, set enable bit, TXxIE.
- If 9-bit transmission is desired, set bit, TX9.
- Enable the transmission by setting enable bit, TXEN.
- If 9-bit transmission is selected, the ninth bit should be loaded in bit, TX9D.
- Start transmission by loading data to the TXREGx register.
- If using interrupts, ensure that the GIE and PEIE bits in the INTCON register (INTCON<7:6>) are set.

TABLE 20-9: REGISTERS ASSOCIATED WITH SYNCHRONOUS SLAVE TRANSMISSION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on page
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	57
PIR1	PSPIF	ADIF	RC1IF	TX1IF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	60
PIE1	PSPIE	ADIE	RC1IE	TX1IE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	60
IPR1	PSPIP	ADIP	RC1IP	TX1IP	SSP1IP	CCP1IP	TMR2IP	TMR1IP	60
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	60
TRISG	—	—	—	TRISG4	TRISG3	TRISG2	TRISG1	TRISG0	60
RCSTAx	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	59
TXREGx	EUSARTx Transmit Register								59
TXSTAx	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	59
BAUDCONx	ABDOVF	RCIDL	—	SCKP	BRG16	—	WUE	ABDEN	61
SPBRGHx	EUSARTx Baud Rate Generator Register High Byte								61
SPBRGx	EUSARTx Baud Rate Generator Register Low Byte								59

Legend: — = unimplemented, read as '0'. Shaded cells are not used for synchronous slave transmission.

The value in the ADRESH:ADRESL registers is not modified for a Power-on Reset. The ADRESH:ADRESL registers will contain unknown data after a Power-on Reset.

After the A/D module has been configured as desired, the selected channel must be acquired before the conversion is started. The analog input channels must have their corresponding TRIS bits selected as an input. To determine acquisition time, see **Section 21.1 “A/D Acquisition Requirements”**. After this acquisition time has elapsed, the A/D conversion can be started. An acquisition time can be programmed to occur between setting the GO/DONE bit and the actual start of the conversion.

The following steps should be followed to perform an A/D conversion:

1. Configure the A/D module:
 - Configure analog pins, voltage reference and digital I/O (ADCON1)
 - Select A/D input channel (ADCON0)
 - Select A/D acquisition time (ADCON2)
 - Select A/D conversion clock (ADCON2)
 - Turn on A/D module (ADCON0)
2. Configure A/D interrupt (if desired):
 - Clear ADIF bit
 - Set ADIE bit
 - Set GIE bit
3. Wait the required acquisition time (if required).
4. Start conversion:
 - Set GO/DONE bit (ADCON0 register)

5. Wait for A/D conversion to complete, by either:
 - Polling for the GO/DONE bit to be cleared
 OR
 - Waiting for the A/D interrupt
6. Read A/D Result registers (ADRESH:ADRESL); clear bit ADIF, if required.
7. For next conversion, go to step 1 or step 2, as required. The A/D conversion time per bit is defined as T_{AD}. A minimum wait of 2 T_{AD} is required before the next acquisition starts.

FIGURE 21-2: A/D TRANSFER FUNCTION

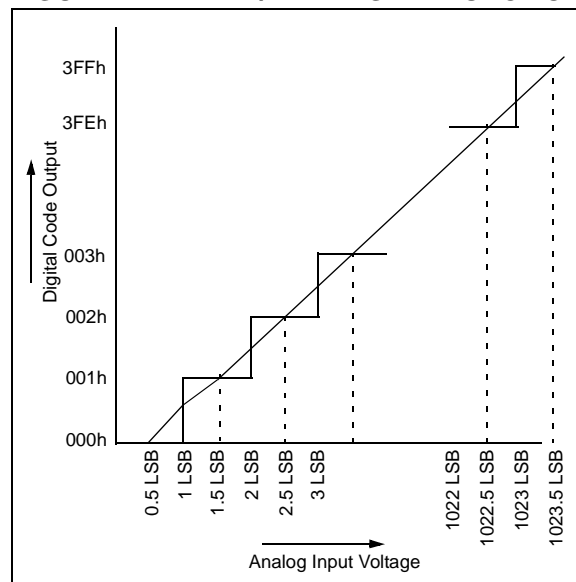
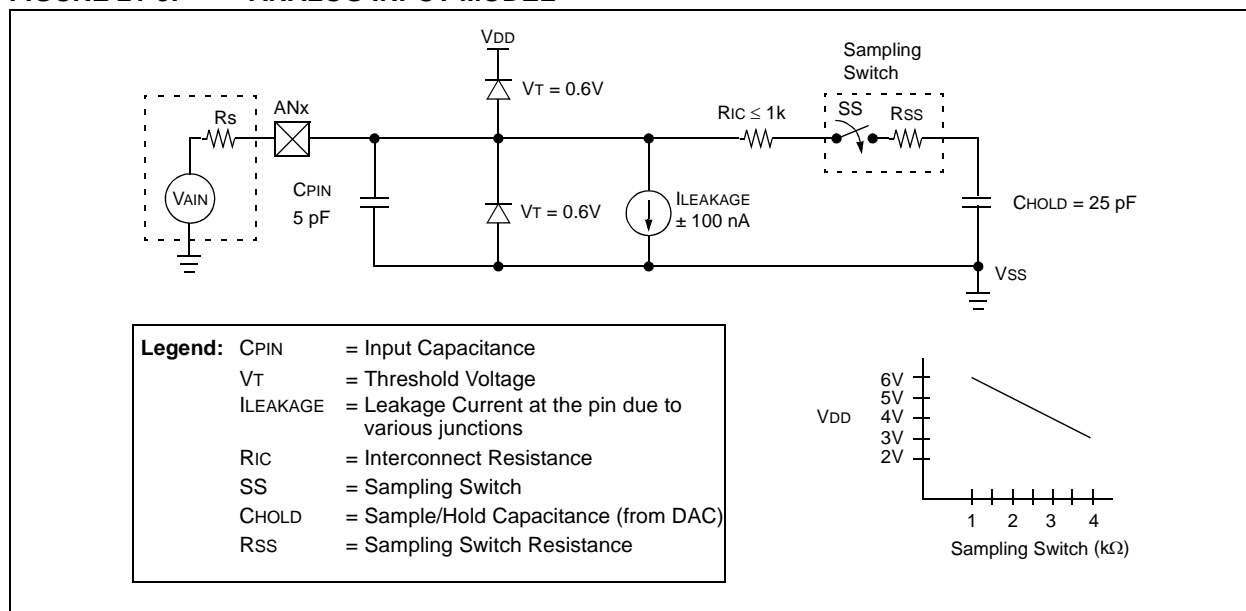
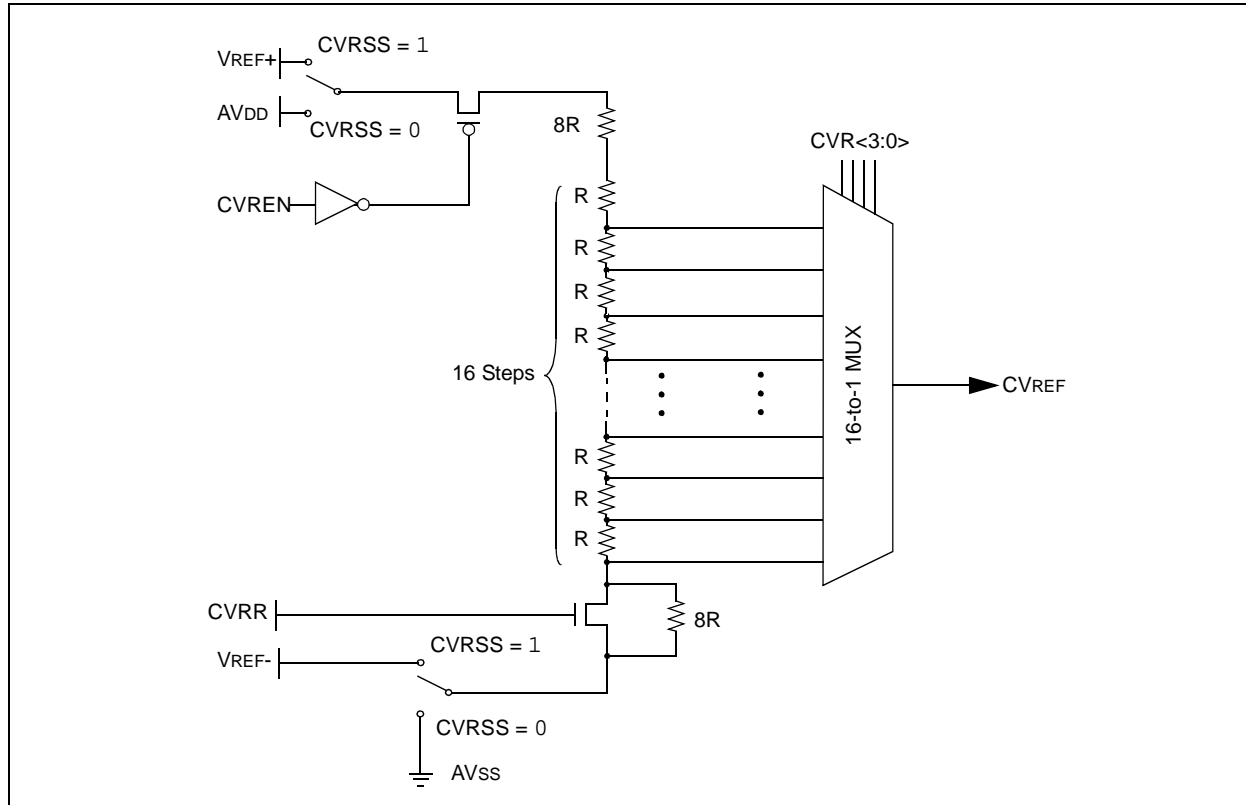


FIGURE 21-3: ANALOG INPUT MODEL



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FIGURE 23-1: COMPARATOR VOLTAGE REFERENCE BLOCK DIAGRAM



23.2 Voltage Reference Accuracy/Error

The full range of voltage reference cannot be realized due to the construction of the module. The transistors on the top and bottom of the resistor ladder network (Figure 23-1) keep CVREF from approaching the reference source rails. The voltage reference is derived from the reference source; therefore, the CVREF output changes with fluctuations in that source. The tested absolute accuracy of the voltage reference can be found in **Section 28.0 “Electrical Characteristics”**.

23.3 Operation During Sleep

When the device wakes up from Sleep through an interrupt or a Watchdog Timer time-out, the contents of the CVRCON register are not affected. To minimize current consumption in Sleep mode, the voltage reference should be disabled.

23.4 Effects of a Reset

A device Reset disables the voltage reference by clearing bit, CVREN (CVRCON<7>). This Reset also disconnects the reference from the RF5 pin by clearing bit, CVROE (CVRCON<6>), and selects the high-voltage range by clearing bit, CVRR (CVRCON<5>). The CVR value select bits are also cleared.

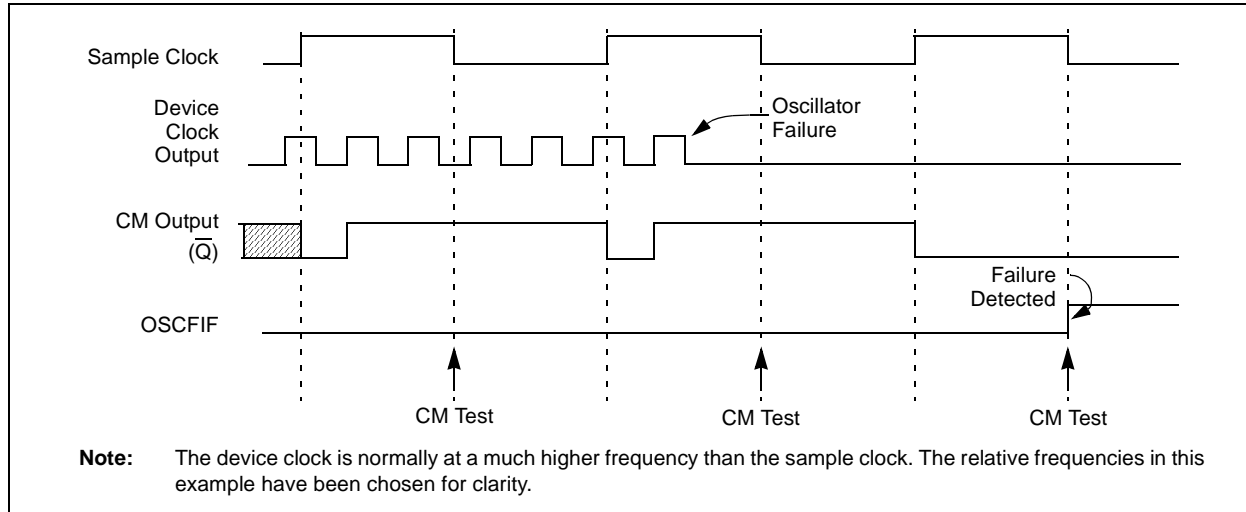
23.5 Connection Considerations

The voltage reference module operates independently of the comparator module. The output of the reference generator may be connected to the RF5 pin if the CVROE bit is set. Enabling the voltage reference output onto RF5 when it is configured as a digital input will increase current consumption. Connecting RF5 as a digital output with CVRSS enabled will also increase current consumption.

The RF5 pin can be used as a simple D/A output with limited drive capability. Due to the limited current drive capability, a buffer must be used on the voltage reference output for external connections to VREF. Figure 23-2 shows an example buffering technique.

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FIGURE 25-4: FSCM TIMING DIAGRAM



25.4.3 FSCM INTERRUPTS IN POWER-MANAGED MODES

By entering a power-managed mode, the clock multiplexor selects the clock source selected by the OSCCON register. Fail-Safe Monitoring of the power-managed clock source resumes in the power-managed mode.

If an oscillator failure occurs during power-managed operation, the subsequent events depend on whether or not the oscillator failure interrupt is enabled. If enabled (OSCFIF = 1), code execution will be clocked by the INTOSC multiplexer. An automatic transition back to the failed clock source will not occur.

If the interrupt is disabled, subsequent interrupts while in Idle mode will cause the CPU to begin executing instructions while being clocked by the INTOSC source.

25.4.4 POR OR WAKE FROM SLEEP

The FSCM is designed to detect oscillator failure at any point after the device has exited Power-on Reset (POR) or low-power Sleep mode. When the primary device clock is EC, RC or INTRC modes, monitoring can begin immediately following these events.

For oscillator modes involving a crystal or resonator (HS, HSPLL, LP or XT), the situation is somewhat different. Since the oscillator may require a start-up time considerably longer than the FSCM sample clock time, a false clock failure may be detected. To prevent this, the internal oscillator block is automatically configured as the device clock and functions until the primary clock is stable (the OST and PLL timers have timed out). This is identical to Two-Speed Start-up mode. Once the primary clock is stable, the INTRC returns to its role as the FSCM source.

Note: The same logic that prevents false oscillator failure interrupts on POR, or wake from Sleep, will also prevent the detection of the oscillator's failure to start at all following these events. This can be avoided by monitoring the OSTS bit and using a timing routine to determine if the oscillator is taking too long to start. Even so, no oscillator failure interrupt will be flagged.

As noted in **Section 25.3.1 "Special Considerations for Using Two-Speed Start-up"**, it is also possible to select another clock configuration and enter an alternate power-managed mode while waiting for the primary clock to become stable. When the new power-managed mode is selected, the primary clock is disabled.

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27.2 MPASM Assembler

The MPASM Assembler is a full-featured, universal macro assembler for all PIC MCUs.

The MPASM Assembler generates relocatable object files for the MPLINK Object Linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code and COFF files for debugging.

The MPASM Assembler features include:

- Integration into MPLAB IDE projects
- User-defined macros to streamline assembly code
- Conditional assembly for multi-purpose source files
- Directives that allow complete control over the assembly process

27.3 MPLAB C18 and MPLAB C30 C Compilers

The MPLAB C18 and MPLAB C30 Code Development Systems are complete ANSI C compilers for Microchip's PIC18 and PIC24 families of microcontrollers and the dsPIC30 and dsPIC33 family of digital signal controllers. These compilers provide powerful integration capabilities, superior code optimization and ease of use not found with other compilers.

For easy source level debugging, the compilers provide symbol information that is optimized to the MPLAB IDE debugger.

27.4 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK Object Linker combines relocatable objects created by the MPASM Assembler and the MPLAB C18 C Compiler. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB Object Librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/library features include:

- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

27.5 MPLAB ASM30 Assembler, Linker and Librarian

MPLAB ASM30 Assembler produces relocatable machine code from symbolic assembly language for dsPIC30F devices. MPLAB C30 C Compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

- Support for the entire dsPIC30F instruction set
- Support for fixed-point and floating-point data
- Command line interface
- Rich directive set
- Flexible macro language
- MPLAB IDE compatibility

27.6 MPLAB SIM Software Simulator

The MPLAB SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC MCUs and dsPIC® DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.

The MPLAB SIM Software Simulator fully supports symbolic debugging using the MPLAB C18 and MPLAB C30 C Compilers, and the MPASM and MPLAB ASM30 Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.

28.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings^(†)

Ambient temperature under bias	-40°C to +125°C
Storage temperature	-65°C to +150°C
Voltage on any pin with respect to VSS (except VDD and $\overline{\text{MCLR}}$)	-0.3V to (VDD + 0.3V)
Voltage on VDD with respect to VSS	-0.3V to +7.5V
Voltage on $\overline{\text{MCLR}}$ with respect to VSS (Note 2)	0V to +13.25V
Total power dissipation (Note 1)	1.0W
Maximum current out of VSS pin	300 mA
Maximum current into VDD pin	250 mA
Input clamp current, I _{IK} (V _I < 0 or V _I > VDD)	±20 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > VDD)	±20 mA
Maximum output current sunk by any I/O pin	25 mA
Maximum output current sourced by any I/O pin	25 mA
Maximum current sunk by all ports	200 mA
Maximum current sourced by all ports	200 mA

Note 1: Power dissipation is calculated as follows:

$$P_{dis} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum (V_{OL} \times I_{OL})$$

- 2:** Voltage spikes below VSS at the RG5/ $\overline{\text{MCLR}}$ /VPP pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50-100Ω should be used when applying a “low” level to the RG5/ $\overline{\text{MCLR}}$ /VPP pin, rather than pulling this pin directly to VSS.

† **NOTICE:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

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FIGURE 28-9: PROGRAM MEMORY WRITE TIMING DIAGRAM

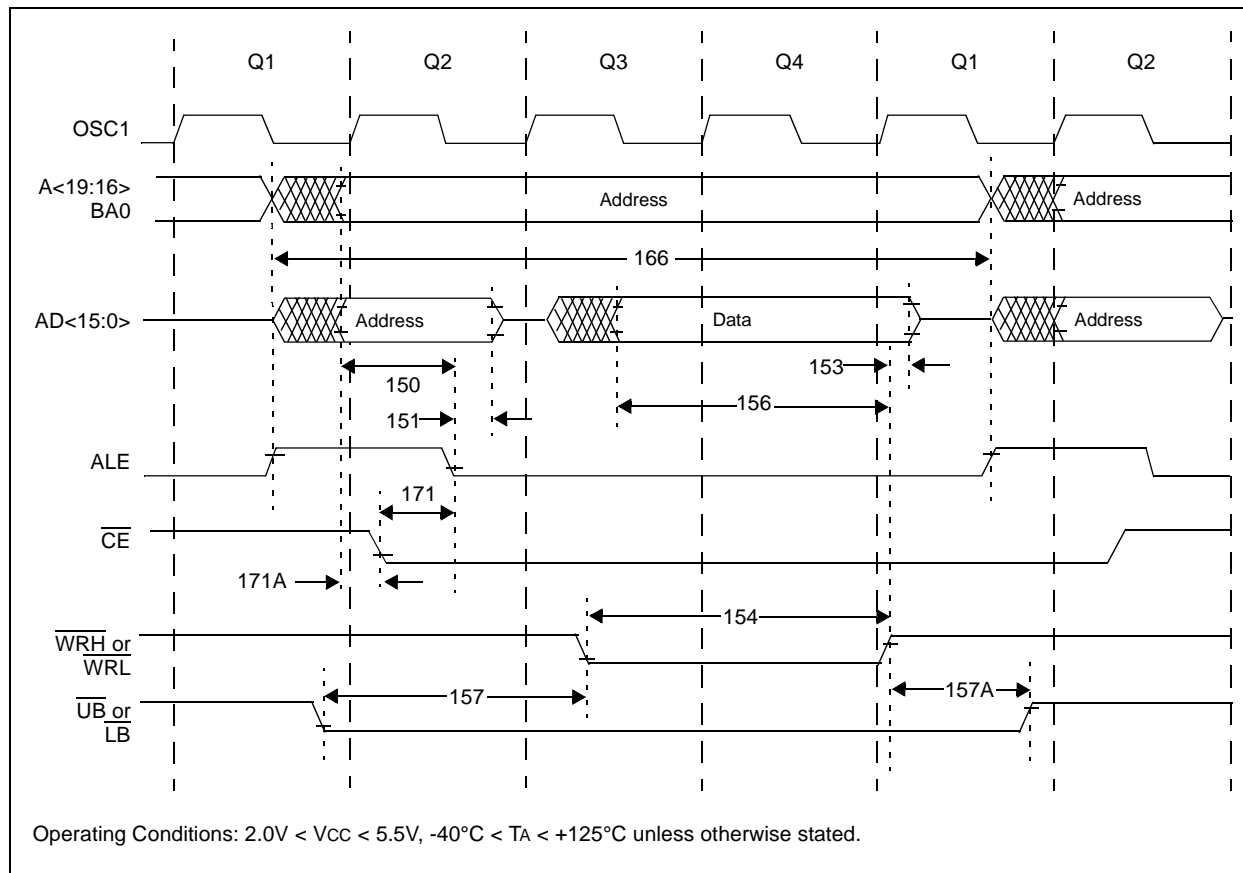


TABLE 28-11: PROGRAM MEMORY WRITE TIMING REQUIREMENTS

Param. No	Symbol	Characteristics	Min	Typ	Max	Units
150	TadV2aL	Address Out Valid to ALE ↓ (address setup time)	0.25 T _{CY} – 10	—	—	ns
151	TaIL2adL	ALE ↓ to Address Out Invalid (address hold time)	5	—	—	ns
153	TwrH2adL	WR _n ↑ to Data Out Invalid (data hold time)	5	—	—	ns
154	TwrL	WR _n Pulse Width	0.5 T _{CY} – 5	0.5 T _{CY}	—	ns
156	TadV2wrH	Data Valid before WR _n ↑ (data setup time)	0.5 T _{CY} – 10	—	—	ns
157	TbsV2wrL	Byte Select Valid before WR _n ↓ (byte select setup time)	0.25 T _{CY}	—	—	ns
157A	TwrH2bsL	WR _n ↑ to Byte Select Invalid (byte select hold time)	0.125 T _{CY} – 5	—	—	ns
166	TaIH2aLH	ALE ↑ to ALE ↑ (cycle time)	—	0.25 T _{CY}	—	ns
171	TaIH2csL	Chip Enable Active to ALE ↓	0.25 T _{CY} – 20	—	—	ns
171A	TubL2oeH	AD Valid to Chip Enable Active	—	—	10	ns

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