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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	40MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, POR, PWM, WDT
Number of I/O	54
Program Memory Size	128KB (64K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	3.8K x 8
Voltage - Supply (Vcc/Vdd)	4.2V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18f6722t-i-pt

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2.4 RC Oscillator

For timing insensitive applications, the RC and RCIO Oscillator modes offer additional cost savings. The actual oscillator frequency is a function of several factors:

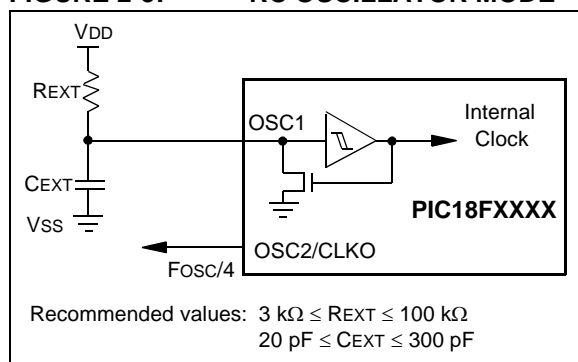
- supply voltage
- values of the external resistor (REXT) and capacitor (CEXT)
- operating temperature

Given the same device, operating voltage and temperature and component values, there will also be unit-to-unit frequency variations. These are due to factors such as:

- normal manufacturing variation
- difference in lead frame capacitance between package types (especially for low CEXT values)
- variations within the tolerance of limits of REXT and CEXT

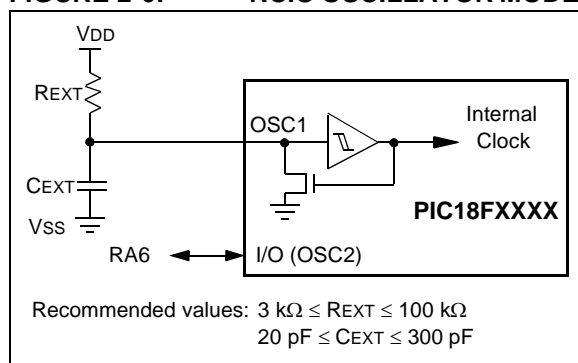
In the RC Oscillator mode, the oscillator frequency divided by 4 is available on the OSC2 pin. This signal may be used for test purposes or to synchronize other logic. Figure 2-5 shows how the R/C combination is connected.

FIGURE 2-5: RC OSCILLATOR MODE



The RCIO Oscillator mode (Figure 2-6) functions like the RC mode, except that the OSC2 pin becomes an additional general purpose I/O pin. The I/O pin becomes bit 6 of PORTA (RA6).

FIGURE 2-6: RCIO OSCILLATOR MODE



2.5 PLL Frequency Multiplier

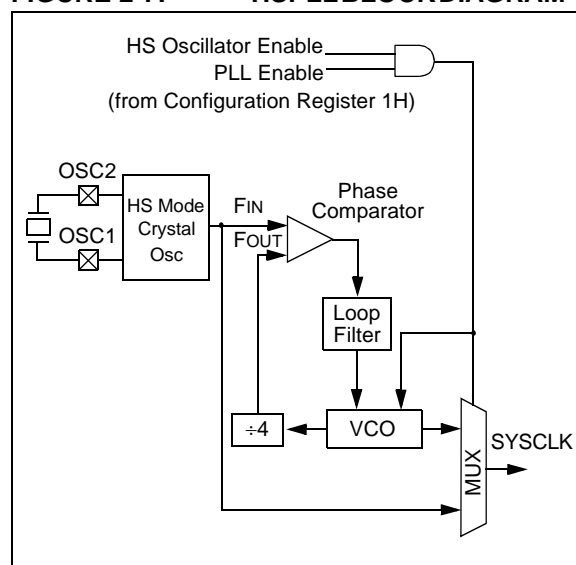
A Phase Locked Loop (PLL) circuit is provided as an option for users who wish to use a lower frequency oscillator circuit or to clock the device up to its highest rated frequency from a crystal oscillator. This may be useful for customers who are concerned with EMI due to high-frequency crystals or users who require higher clock speeds from an internal oscillator.

2.5.1 HSPLL OSCILLATOR MODE

The HSPLL mode makes use of the HS mode oscillator for frequencies up to 10 MHz. A PLL then multiplies the oscillator output frequency by 4 to produce an internal clock frequency up to 40 MHz. The PLEN bit is not available when this mode is configured as the primary clock source.

The PLL is only available to the crystal oscillator when the FOSC<3:0> Configuration bits are programmed for HSPLL mode (= 0110).

FIGURE 2-7: HSPLL BLOCK DIAGRAM



2.5.2 PLL AND INTOSC

The PLL is also available to the internal oscillator block when the internal oscillator block is configured as the primary clock source. In this configuration, the PLL is enabled in software and generates a clock output of up to 32 MHz. The operation of INTOSC with the PLL is described in **Section 2.6.4 "PLL in INTOSC Modes"**.

3.4.3 RC_IDLE MODE

In RC_IDLE mode, the CPU is disabled but the peripherals continue to be clocked from the internal oscillator block using the INTOSC multiplexer. This mode allows for controllable power conservation during Idle periods.

From RC_RUN, this mode is entered by setting the IDLEN bit and executing a *SLEEP* instruction. If the device is in another Run mode, first set IDLEN, then set the SCS1 bit and execute *SLEEP*. Although its value is ignored, it is recommended that SCS0 also be cleared; this is to maintain software compatibility with future devices. The INTOSC multiplexer may be used to select a higher clock frequency by modifying the IRCF bits before executing the *SLEEP* instruction. When the clock source is switched to the INTOSC multiplexer, the primary oscillator is shut down and the OSTS bit is cleared.

If the IRCF bits are set to any non-zero value, or the INTSRC bit is set, the INTOSC output is enabled. The IOFS bit becomes set, after the INTOSC output becomes stable, after an interval of TIOBST (parameter 39, Table 28-12). Clocks to the peripherals continue while the INTOSC source stabilizes. If the IRCF bits were previously at a non-zero value, or INTSRC was set before the *SLEEP* instruction was executed and the INTOSC source was already stable, the IOFS bit will remain set. If the IRCF bits and INTSRC are all clear, the INTOSC output will not be enabled, the IOFS bit will remain clear and there will be no indication of the current clock source.

When a wake event occurs, the peripherals continue to be clocked from the INTOSC multiplexer. After a delay of TcSD (parameter 38, Table 28-12) following the wake event, the CPU begins executing code being clocked by the INTOSC multiplexer. The IDLEN and SCS bits are not affected by the wake-up. The INTRC source will continue to run if either the WDT or the Fail-Safe Clock Monitor is enabled.

3.5 Exiting Idle and Sleep Modes

An exit from Sleep mode or any of the Idle modes is triggered by an interrupt, a Reset or a WDT time-out. This section discusses the triggers that cause exits from power-managed modes. The clocking subsystem actions are discussed in each of the power-managed modes (see **Section 3.2 “Run Modes”**, **Section 3.3 “Sleep Mode”** and **Section 3.4 “Idle Modes”**).

3.5.1 EXIT BY INTERRUPT

Any of the available interrupt sources can cause the device to exit from an Idle mode or the Sleep mode to a Run mode. To enable this functionality, an interrupt source must be enabled by setting its enable bit in one of the INTCON or PIE registers. The exit sequence is initiated when the corresponding interrupt flag bit is set.

On all exits from Idle or Sleep modes by interrupt, code execution branches to the interrupt vector if the GIE/GIEH bit (INTCON<7>) is set. Otherwise, code execution continues or resumes without branching (see **Section 10.0 “Interrupts”**).

A fixed delay of interval TcSD following the wake event is required when leaving Sleep and Idle modes. This delay is required for the CPU to prepare for execution. Instruction execution resumes on the first clock cycle following this delay.

3.5.2 EXIT BY WDT TIME-OUT

A WDT time-out will cause different actions depending on which power-managed mode the device is in when the time-out occurs.

If the device is not executing code (all Idle modes and Sleep mode), the time-out will result in an exit from the power-managed mode (see **Section 3.2 “Run Modes”** and **Section 3.3 “Sleep Mode”**). If the device is executing code (all Run modes), the time-out will result in a WDT Reset (see **Section 25.2 “Watchdog Timer (WDT)”**).

The WDT timer and postscaler are cleared by executing a *SLEEP* or *CLRWDT* instruction, the loss of a currently selected clock source (if the Fail-Safe Clock Monitor is enabled) and modifying the IRCF bits in the OSCCON register if the internal oscillator block is the device clock source.

3.5.3 EXIT BY RESET

Normally, the device is held in Reset by the Oscillator Start-up Timer (OST) until the primary clock becomes ready. At that time, the OSTS bit is set and the device begins executing code. If the internal oscillator block is the new clock source, the IOFS bit is set instead.

The exit delay time from Reset to the start of code execution depends on both the clock sources before and after the wake-up and the type of oscillator if the new clock source is the primary clock. Exit delays are summarized in Table 3-2.

Code execution can begin before the primary clock becomes ready. If either the Two-Speed Start-up (see **Section 25.3 “Two-Speed Start-up”**) or Fail-Safe Clock Monitor (see **Section 25.4 “Fail-Safe Clock Monitor”**) is enabled, the device may begin execution as soon as the Reset source has cleared. Execution is clocked by the INTOSC multiplexer driven by the internal oscillator block. Execution is clocked by the internal oscillator block until either the primary clock becomes ready or a power-managed mode is entered before the primary clock becomes ready; the primary clock is then shut down.

5.0 MEMORY ORGANIZATION

There are three types of memory in PIC18 Enhanced microcontroller devices:

- Program Memory
- Data RAM
- Data EEPROM

As Harvard architecture devices, the data and program memories use separate busses; this allows for concurrent access of the two memory spaces. The data EEPROM, for practical purposes, can be regarded as a peripheral device, since it is addressed and accessed through a set of control registers.

Additional detailed information on the operation of the Flash program memory is provided in **Section 6.0 “Flash Program Memory”**. Data EEPROM is discussed separately in **Section 8.0 “Data EEPROM Memory”**.

5.1 Program Memory Organization

PIC18 microcontrollers implement a 21-bit program counter, which is capable of addressing a 2-Mbyte program memory space. Accessing a location between the upper boundary of the physically implemented memory and the 2-Mbyte address will return all '0's (a NOP instruction).

The PIC18F6527 and PIC18F8527 each have 48 Kbytes of Flash memory and can store up to 24,576 single-word instructions.

The PIC18F6622 and PIC18F8622 each have 64 Kbytes of Flash memory and can store up to 32,768 single-word instructions.

The PIC18F6627 and PIC18F8627 each have 96 Kbytes of Flash memory and can store up to 49,152 single-word instructions.

The PIC18F6722 and PIC18F8722 each have 128 Kbytes of Flash memory and can store up to 65,536 single-word instructions.

PIC18 devices have two interrupt vectors. The Reset vector address is at 0000h and the interrupt vector addresses are at 0008h and 0018h.

The program memory map for the PIC18F8722 family of devices is shown in Figure 5-1.

5.1.1 PIC18F8527/8622/8627/8722 PROGRAM MEMORY MODES

PIC18F8527/8622/8627/8722 devices differ significantly from their PIC18 predecessors in their utilization of program memory. In addition to available on-chip Flash program memory, these controllers can also address up to 2 Mbytes of external program memory through the external memory interface. There are four distinct operating modes available to the controllers:

- Microprocessor (MP)
- Microprocessor with Boot Block (MPBB)
- Extended Microcontroller (EMC)
- Microcontroller (MC)

The program memory mode is determined by setting the two Least Significant bits of the Configuration Register 3L (CONFIG3L) as shown in Register 25-4 (see **Section 25.1 “Configuration Bits”** for additional details on the device Configuration bits).

The program memory modes operate as follows:

- The **Microprocessor Mode** permits access only to external program memory; the contents of the on-chip Flash memory are ignored. The 21-bit program counter permits access to a 2-Mbyte linear program memory space.
- The **Microprocessor with Boot Block Mode** accesses on-chip Flash memory from the boot block. Above this, external program memory is accessed all the way up to the 2-Mbyte limit. Program execution automatically switches between the two memories as required. The boot block is configurable to 1, 2 or 4 Kbytes.
- The **Microcontroller Mode** accesses only on-chip Flash memory. Attempts to read above the physical limit of the on-chip Flash (0BFFFh for the PIC18F8527, 0FFFFh for the PIC18F8622, 17FFFh for the PIC18F8627, 1FFFFh for the PIC18F8722) causes a read of all '0's (a NOP instruction).
The Microcontroller mode is also the only operating mode available to PIC18F6527/6622/6627/6722 devices.
- The **Extended Microcontroller Mode** allows access to both internal and external program memories as a single block. The device can access its entire on-chip Flash memory; above this, the device accesses external program memory up to the 2-Mbyte program space limit. As with Boot Block mode, execution automatically switches between the two memories as required.

In all modes, the microcontroller has complete access to data RAM and EEPROM.

Figure 5-2 compares the memory maps of the different program memory modes. The differences between on-chip and external memory access limitations are more fully explained in Table 5-1.

7.6.1 8-BIT MODE TIMING

The presentation of control signals on the External Memory Bus is different for the various operating modes. Typical signal timing diagrams are shown in Figure 7-8 through Figure 7-11.

FIGURE 7-8: EXTERNAL BUS TIMING FOR TBLRD (MICROPROCESSOR MODE)

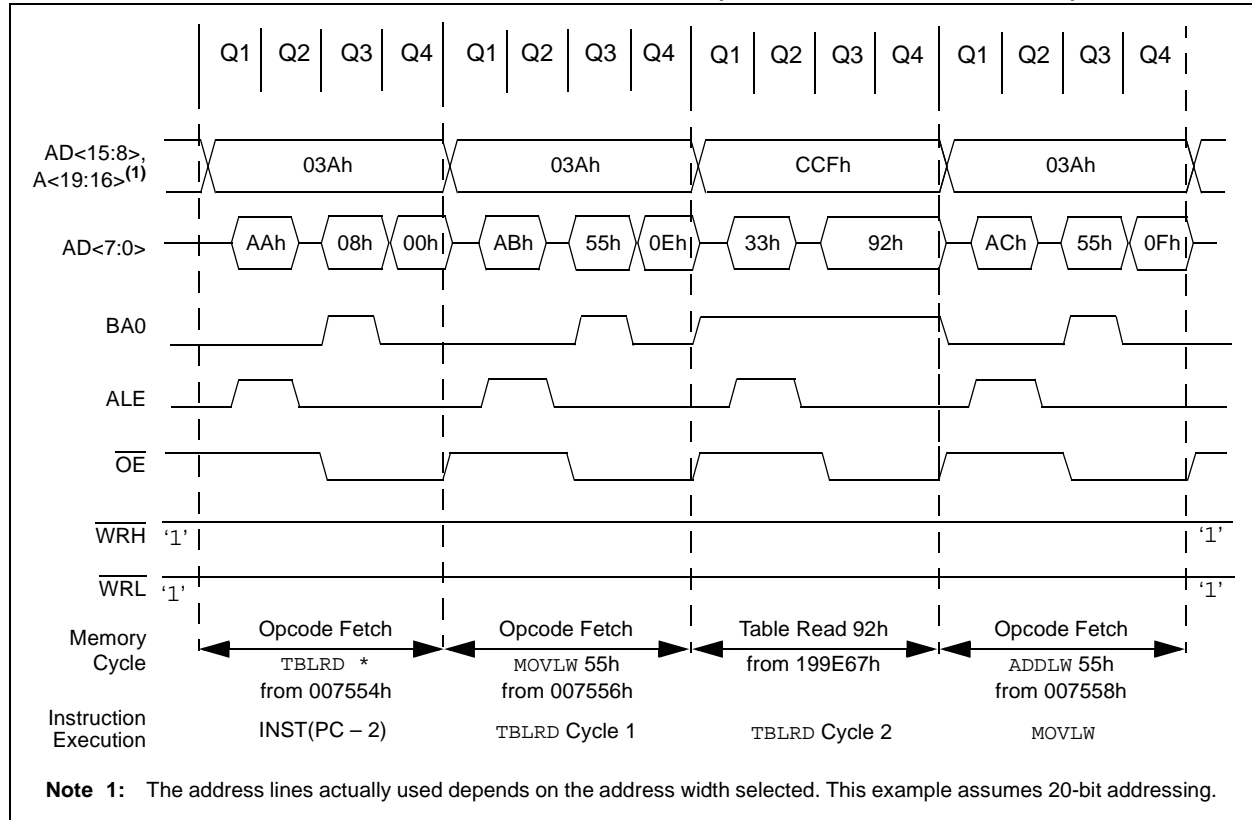
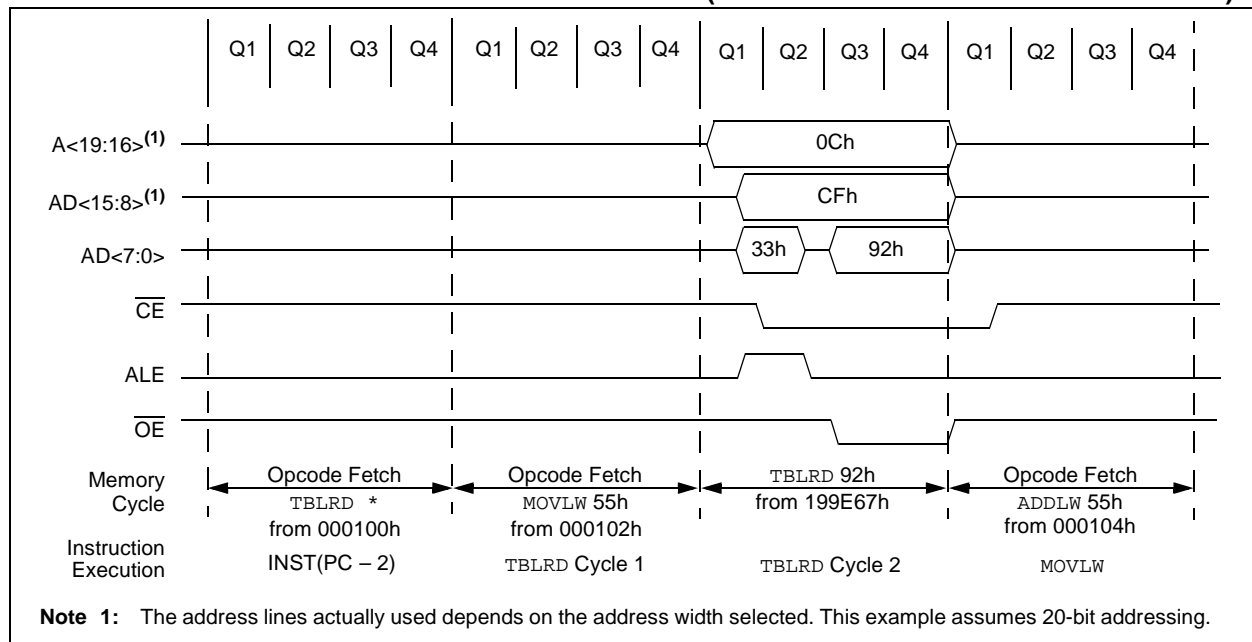


FIGURE 7-9: EXTERNAL BUS TIMING FOR TBLRD (EXTENDED MICROCONTROLLER MODE)



PIC18F8722 FAMILY

FIGURE 7-10: EXTERNAL MEMORY BUS TIMING FOR SLEEP (MICROPROCESSOR MODE)

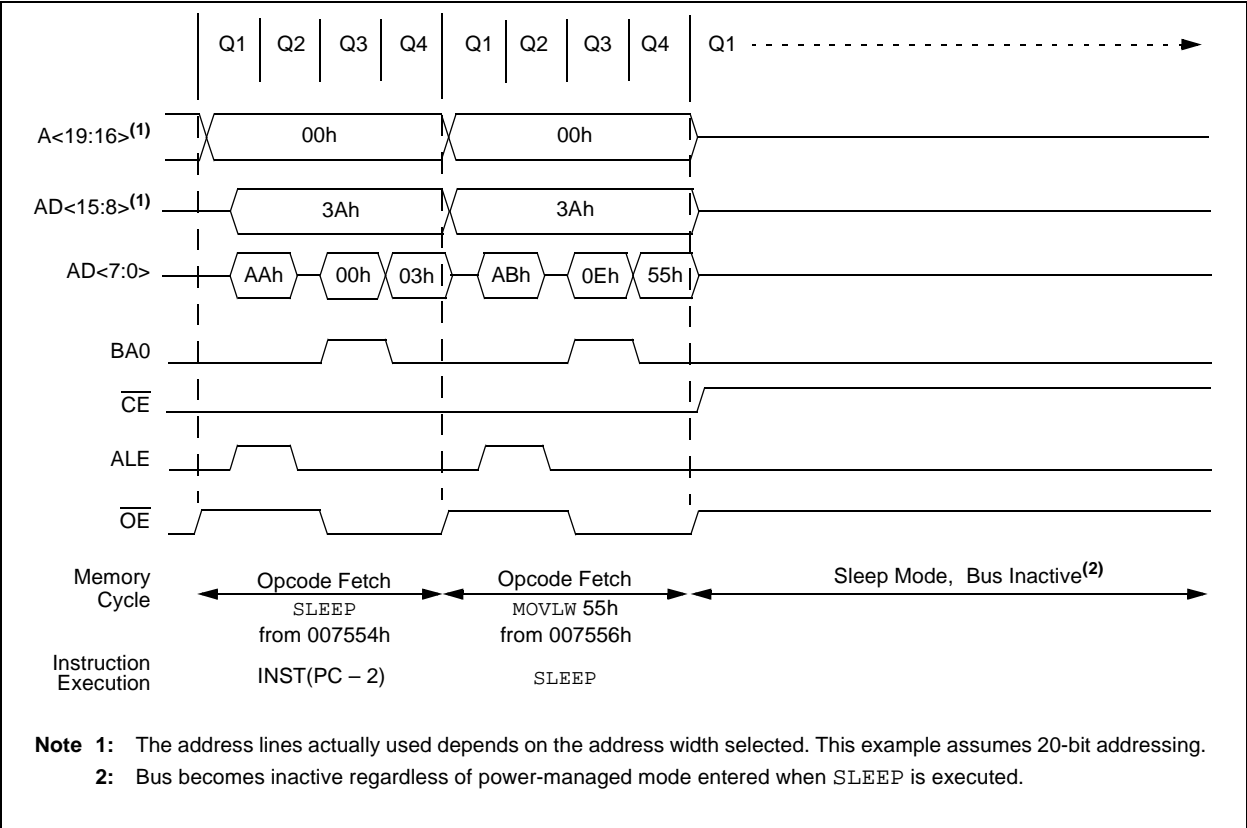
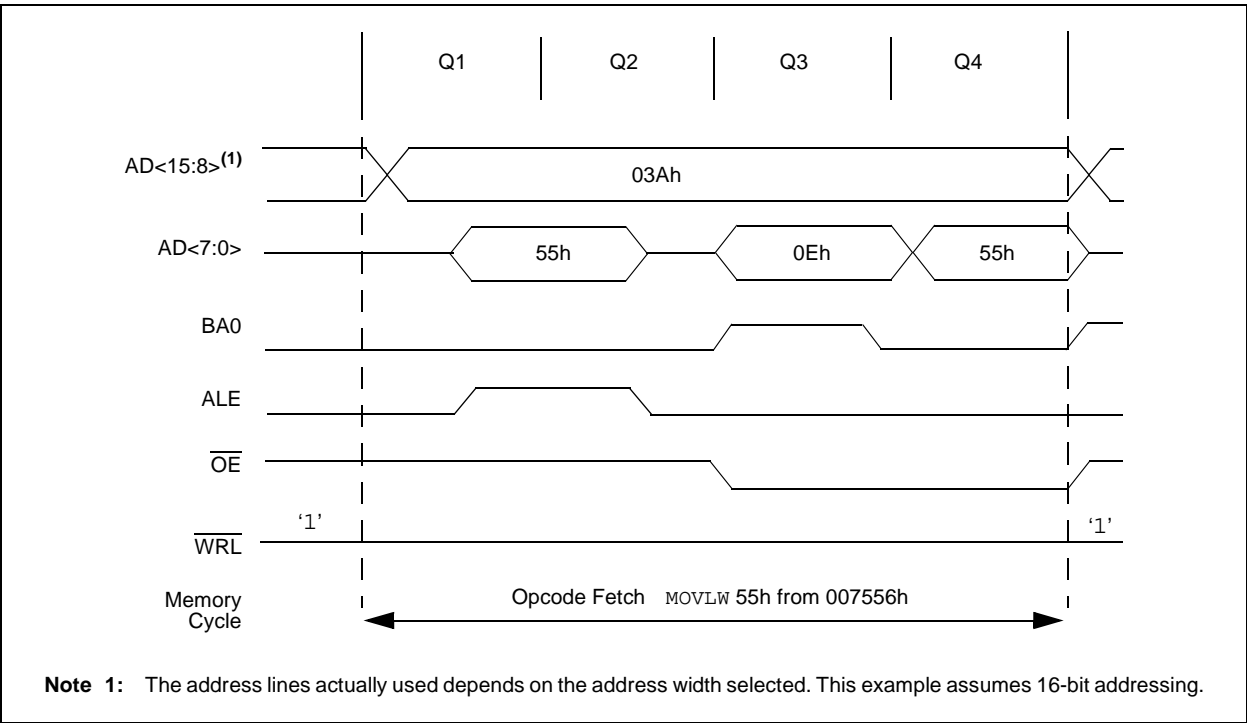


FIGURE 7-11: TYPICAL OPCODE FETCH, 8-BIT MODE



8.0 DATA EEPROM MEMORY

The data EEPROM is a nonvolatile memory array, separate from the data RAM and program memory, that is used for long-term storage of program data. It is not directly mapped in either the register file or program memory space, but is indirectly addressed through the Special Function Registers (SFRs). The EEPROM is readable and writable during normal operation over the entire VDD range.

Five SFRs are used to read and write to the data EEPROM, as well as the program memory. They are:

- EECON1
- EECON2
- EEDATA
- EEADR
- EEADRH

The data EEPROM allows byte read and write. When interfacing to the data memory block, EEDATA holds the 8-bit data for read/write and the EEADRH:EEADR register pair holds the address of the EEPROM location being accessed.

The EEPROM data memory is rated for high erase/write cycle endurance. A byte write automatically erases the location and writes the new data (erase-before-write). The write time is controlled by an on-chip timer; it will vary with voltage and temperature, as well as from chip-to-chip. Please refer to parameter D122 (Table 28-1 in **Section 28.0 “Electrical Characteristics”**) for exact limits.

8.1 EEADR and EEADRH Registers

The EEADRH:EEADR register pair is used to address the data EEPROM for read and write operations. EEADRH holds the two MSBs of the address; the upper 6 bits are ignored. The 10-bit range of the pair can address a memory range of 1024 bytes (00h to 3FFh).

8.2 EECON1 and EECON2 Registers

Access to the data EEPROM is controlled by two registers: EECON1 and EECON2. These are the same registers which control access to the program memory and are used in a similar manner for the data EEPROM.

The EECON1 register (Register) is the control register for data and program memory access. Control bit EEPGD determines if the access will be to program or data EEPROM memory. When clear, operations will access the data EEPROM memory. When set, program memory is accessed.

Control bit CFGS determines if the access will be to the Configuration registers or to program memory/data EEPROM memory. When set, subsequent operations access Configuration registers. When CFGS is clear, the EEPGD bit selects either program Flash or data EEPROM memory.

The WREN bit, when set, will allow a write operation. On power-up, the WREN bit is clear. The WRERR bit is set in hardware when the WREN bit is set and cleared when the internal programming timer expires and the write operation is complete.

Note: During normal operation, the WRERR is read as '1'. This can indicate that a write operation was prematurely terminated by a Reset, or a write operation was attempted improperly.

The WR control bit initiates write operations. The bit cannot be cleared, only set, in software; it is cleared in hardware at the completion of the write operation.

Note: The EEIF interrupt flag bit (PIR2<4>) is set when the write is complete. It must be cleared in software.

Control bits, RD and WR, start read and erase/write operations, respectively. These bits are set by firmware and cleared by hardware at the completion of the operation.

The RD bit cannot be set when accessing program memory (EEPGD = 1). Program memory is read using table read instructions. See **Section 6.1 “Table Reads and Table Writes”** regarding table reads.

The EECON2 register is not a physical register. It is used exclusively in the memory write and erase sequences. Reading EECON2 will read all '0's.

10.0 INTERRUPTS

The PIC18F8722 family of devices have multiple interrupt sources and an interrupt priority feature that allows most interrupt sources to be assigned a high-priority level or a low-priority level. The high-priority interrupt vector is at 0008h and the low-priority interrupt vector is at 0018h. High-priority interrupt events will interrupt any low-priority interrupts that may be in progress.

There are ten registers which are used to control interrupt operation. These registers are:

- RCON
- INTCON
- INTCON2
- INTCON3
- PIR1, PIR2, PIR3
- PIE1, PIE2, PIE3
- IPR1, IPR2, IPR3

It is recommended that the Microchip header files supplied with MPLAB® IDE be used for the symbolic bit names in these registers. This allows the assembler/compiler to automatically take care of the placement of these bits within the specified register.

In general, interrupt sources have three bits to control their operation. They are:

- **Flag bit** to indicate that an interrupt event occurred
- **Enable bit** that allows program execution to branch to the interrupt vector address when the flag bit is set
- **Priority bit** to select high priority or low priority

The interrupt priority feature is enabled by setting the IPEN bit (RCON<7>). When interrupt priority is enabled, there are two bits which enable interrupts globally. Setting the GIEH bit (INTCON<7>) enables all interrupts that have the priority bit set (high priority). Setting the GIEL bit (INTCON<6>) enables all interrupts that have the priority bit cleared (low priority). When the interrupt flag, enable bit and appropriate global interrupt enable bit are set, the interrupt will vector immediately to address 0008h or 0018h, depending on the priority bit setting. Individual interrupts can be disabled through their corresponding enable bits.

When the IPEN bit is cleared (default state), the interrupt priority feature is disabled and interrupts are compatible with PIC® mid-range devices. In Compatibility mode, the interrupt priority bits for each source have no effect. INTCON<6> is the PEIE bit, which enables/disables all peripheral interrupt sources. INTCON<7> is the GIE bit, which enables/disables all interrupt sources. All interrupts branch to address 0008h in Compatibility mode.

When an interrupt is responded to, the global interrupt enable bit is cleared to disable further interrupts. If the IPEN bit is cleared, this is the GIE bit. If interrupt priority levels are used, this will be either the GIEH or GIEL bit. High-priority interrupt sources can interrupt a low-priority interrupt. Low-priority interrupts are not processed while high-priority interrupts are in progress.

The return address is pushed onto the stack and the PC is loaded with the interrupt vector address (0008h or 0018h). Once in the Interrupt Service Routine, the source(s) of the interrupt can be determined by polling the interrupt flag bits. The interrupt flag bits must be cleared in software before re-enabling interrupts to avoid recursive interrupts.

The “return from interrupt” instruction, RETFIE, exits the interrupt routine and sets the GIE bit (GIEH or GIEL if priority levels are used), which re-enables interrupts.

For external interrupt events, such as the INTx pins or the PORTB input change interrupt, the interrupt latency will be three to four instruction cycles. The exact latency is the same for one or two-cycle instructions. Individual interrupt flag bits are set, regardless of the status of their corresponding enable bit or the GIE bit.

Note: Do not use the MOVFF instruction to modify any of the interrupt control registers while any interrupt is enabled. Doing so may cause erratic microcontroller behavior.
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PIC18F8722 FAMILY

TABLE 11-5: PORTC FUNCTIONS (CONTINUED)

Pin Name	Function	TRIS Setting	I/O	I/O Type	Description
RC6/TX1/CK1	RC6	0	O	DIG	LATC<6> data output.
		1	I	ST	PORTC<6> data input.
	TX1	0	O	DIG	Asynchronous serial transmit data output (EUSART1 module). Takes priority over port data.
		0	O	DIG	Synchronous serial clock output (EUSART1 module). Takes priority over port data.
	CK1	0	O	DIG	Synchronous serial clock output (EUSART1 module). Takes priority over port data.
		1	I	ST	Synchronous serial clock input (EUSART1 module).
RC7/RX1/DT1	RC7	0	O	DIG	LATC<7> data output.
		1	I	ST	PORTC<7> data input.
	RX1	1	I	ST	Asynchronous serial receive data input (EUSART1 module)
		1	O	DIG	Synchronous serial data output (EUSART1 module). Takes priority over port data. User must configure as input.
	DT1	1	O	DIG	Synchronous serial data output (EUSART1 module). Takes priority over port data. User must configure as input.
		1	I	ST	Synchronous serial data input (EUSART1 module). User must configure as an input.

Legend: DIG = Digital level output; TTL = TTL input buffer; ST = Schmitt Trigger input buffer; ANA = Analog level input/output; I²C/SMB = I²C/SMBus input buffer; x = Don't care (TRIS bit does not affect port direction or is overridden for this option).

Note 1: Default assignment for ECCP2 when CCP2MX Configuration bit is set.

TABLE 11-6: SUMMARY OF REGISTERS ASSOCIATED WITH PORTC

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on page
PORTC	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	60
LATC	LATC7	LATC6	LATC5	LATC4	LATC3	LATC2	LATC1	LATC0	60
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	60

PIC18F8722 FAMILY

TABLE 11-13: PORTG FUNCTIONS

Pin Name	Function	TRIS Setting	I/O	I/O Type	Description
RG0/ECCP3/P3A	RG0	0	O	DIG	LATG<0> data output.
		1	I	ST	PORTG<0> data input.
	ECCP3	0	O	DIG	ECCP3 compare and ECCP3 PWM output. Takes priority over port data.
		1	I	ST	ECCP3 capture input.
	P3A	0	O	DIG	ECCP3 Enhanced PWM output, channel B. May be configured for tri-state during Enhanced PWM shutdown events. Takes priority over port data.
RG1/TX2/CK2	RG1	0	O	DIG	LATG<1> data output.
		1	I	ST	PORTG<1> data input.
	TX2	0	O	DIG	Asynchronous serial transmit data output (EUSART2 module). Takes priority over port data.
		0	O	DIG	Synchronous serial clock output (EUSART2 module). Takes priority over port data.
		1	I	ST	Synchronous serial clock input (EUSART2 module).
RG2/RX2/DT2	RG2	0	O	DIG	LATG<2> data output.
		1	I	ST	PORTG<2> data input.
	RX2	1	I	ST	Asynchronous serial receive data input (EUSART2 module).
		1	O	DIG	Synchronous serial data output (EUSART2 module). Takes priority over port data. User must configure as an input.
		1	I	ST	Synchronous serial data input (EUSART2 module). User must configure as an input.
RG3/CCP4/P3D	RG3	0	O	DIG	LATG<3> data output.
		1	I	ST	PORTG<3> data input.
	CCP4	0	O	DIG	CCP4 compare and PWM output; takes priority over port data and P3D function.
		1	I	ST	CCP4 capture input.
	P3D	0	O	DIG	ECCP3 Enhanced PWM output, channel D. May be configured for tri-state during Enhanced PWM shutdown events. Takes priority over port data.
RG4/CCP5/P1D	RG4	0	O	DIG	LATG<4> data output.
		1	I	ST	PORTG<4> data input.
	CCP5	0	O	DIG	CCP5 compare and PWM output. Takes priority over port data and P1D function.
		1	I	ST	CCP5 capture input.
	P1D	0	O	DIG	ECCP1 Enhanced PWM output, channel B. May be configured for tri-state during Enhanced PWM shutdown events. Takes priority over port data.
RG5/MCLR/VPP	RG5	— ⁽¹⁾	I	ST	PORTG<5> data input; enabled when MCLRE Configuration bit is clear.
	MCLR	—	I	ST	External Master Clear input; enabled when MCLRE Configuration bit is set.
	VPP	—	I	ANA	High-voltage detection; used for ICSP™ mode entry detection. Always available regardless of pin mode.

Legend: PWR = Power Supply, O = Output, I = Input, ANA = Analog Signal, DIG = Digital Output, ST = Schmitt Buffer Input, TTL = TTL Buffer Input, x = Don't care (TRIS bit does not affect port direction or is overridden for this option).

Note 1: RG5 does not have a corresponding TRISG bit.

PIC18F8722 FAMILY

11.8 PORTH, LATH and TRISH Registers

Note: PORTH is available only on PIC18F8527/8622/8627/8722 devices.

PORTH is an 8-bit wide, bidirectional I/O port. The corresponding Data Direction register is TRISH. Setting a TRISH bit (= 1) will make the corresponding PORTH pin an input (i.e., put the corresponding output driver in a high-impedance mode). Clearing a TRISH bit (= 0) will make the corresponding PORTH pin an output (i.e., put the contents of the output latch on the selected pin).

The Data Latch register (LATH) is also memory mapped. Read-modify-write operations on the LATH register, read and write the latched output value for PORTH.

All pins on PORTH are implemented with Schmitt Trigger input buffers. Each pin is individually configurable as an input or output.

Note: On a Power-on Reset, these pins are configured as digital inputs.

When the external memory interface is enabled, four of the PORTH pins function as the high-order address lines for the interface. The address output from the interface takes priority over other digital I/O. The corresponding TRISH bits are also overridden.

EXAMPLE 11-8: INITIALIZING PORTH

```
CLRF    PORTH    ; Initialize PORTH by
                  ; clearing output
                  ; data latches
CLRF    LATH      ; Alternate method
                  ; to clear output
                  ; data latches
MOVLW   0CFh     ; Value used to
                  ; initialize data
                  ; direction
MOVWF   TRISH     ; Set RH3:RH0 as inputs
                  ; RH5:RH4 as outputs
                  ; RH7:RH6 as inputs
```

PIC18F8722 FAMILY

17.1 CCP Module Configuration

Each Capture/Compare/PWM module is associated with a control register (generically, CCPxCON) and a data register (CCPRx). The data register, in turn, is comprised of two 8-bit registers: CCPRxL (low byte) and CCPRxH (high byte). All registers are both readable and writable.

17.1.1 CCP MODULES AND TIMER RESOURCES

The CCP/ECCP modules utilize Timers 1, 2, 3 or 4, depending on the mode selected. Timer1 and Timer3 are available to modules in Capture or Compare modes, while Timer2 and Timer4 are available for modules in PWM mode.

TABLE 17-1: CCP MODE – TIMER RESOURCE

CCP Mode	Timer Resource
Capture	Timer1 or Timer3
Compare	Timer1 or Timer3
PWM	Timer2 or Timer4

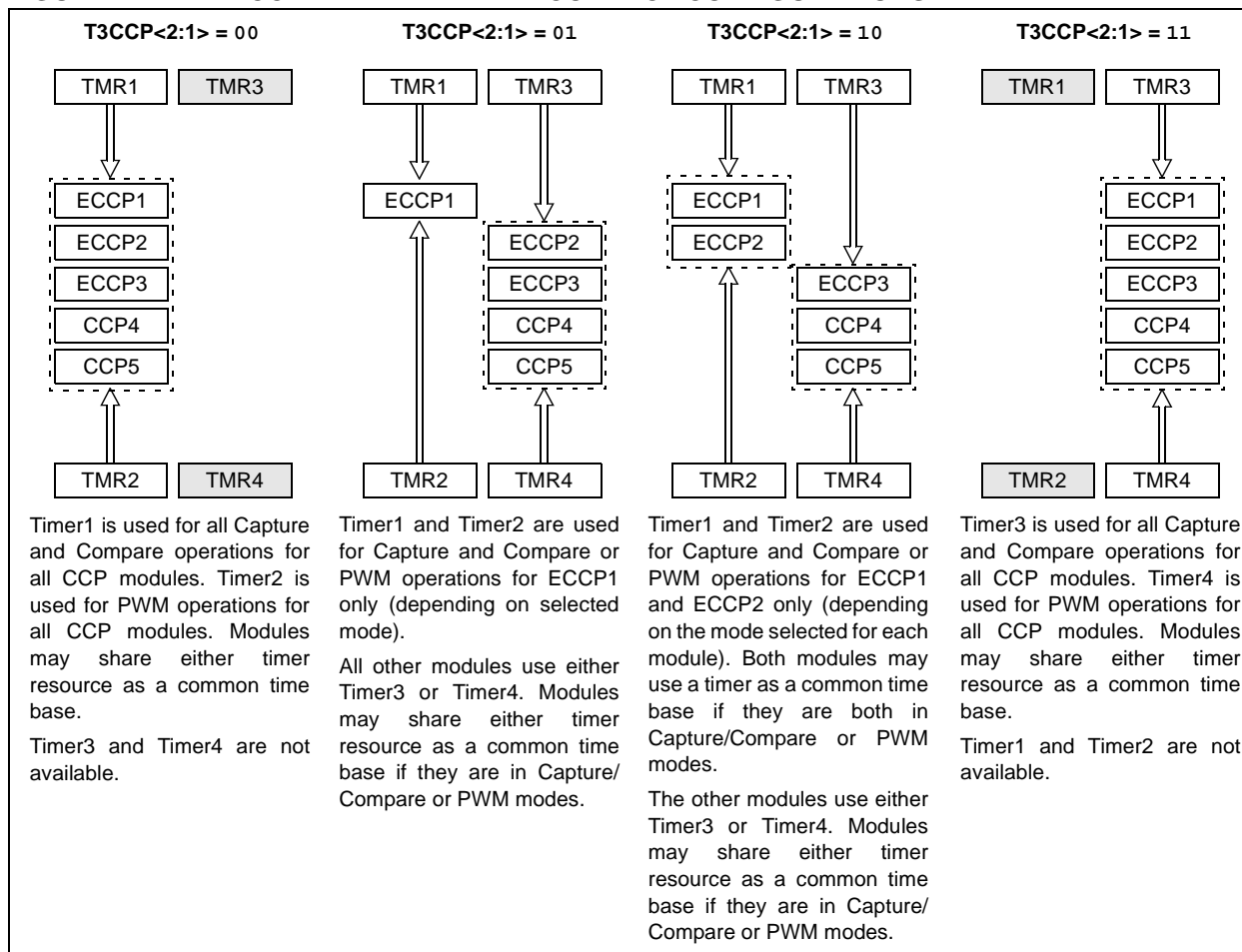
The assignment of a particular timer to a module is determined by the Timer to CCP enable bits in the T3CON register (Register 15-1). Depending on the configuration selected, up to four timers may be active at once, with modules in the same configuration (Capture/Compare or PWM) sharing timer resources. The possible configurations are shown in Figure 17-1.

17.1.2 ECCP2 PIN ASSIGNMENT

The pin assignment for ECCP2 (Capture input, Compare and PWM output) can change, based on device configuration. The CCP2MX Configuration bit determines which pin ECCP2 is multiplexed to. By default, it is assigned to RC1 (CCP2MX = 1). If the Configuration bit is cleared, ECCP2 is multiplexed with RE7 in Microcontroller mode, or RE3 in all other modes.

Changing the pin assignment of ECCP2 does not automatically change any requirements for configuring the port pin. Users must always verify that the appropriate TRIS register is configured correctly for ECCP2 operation regardless of where it is located.

FIGURE 17-1: CCP AND TIMER INTERCONNECT CONFIGURATIONS



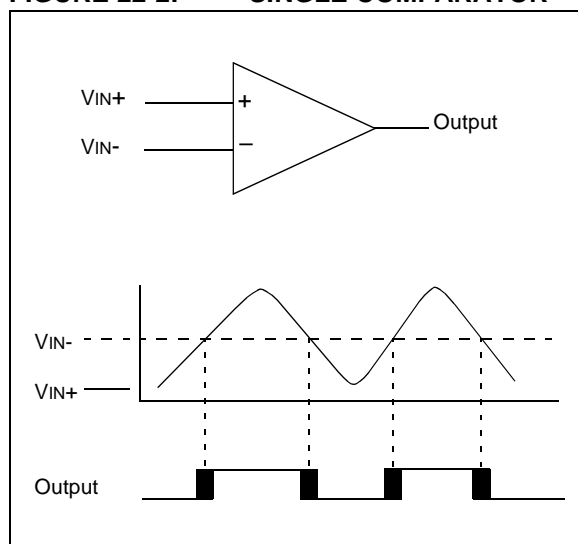
22.2 Comparator Operation

A single comparator is shown in Figure 22-2, along with the relationship between the analog input levels and the digital output. When the analog input at V_{IN+} is less than the analog input V_{IN-} , the output of the comparator is a digital low level. When the analog input at V_{IN+} is greater than the analog input V_{IN-} , the output of the comparator is a digital high level. The shaded areas of the output of the comparator in Figure 22-2 represent the uncertainty, due to input offsets and response time.

22.3 Comparator Reference

Depending on the comparator operating mode, either an external or internal voltage reference may be used. The analog signal present at V_{IN-} is compared to the signal at V_{IN+} and the digital output of the comparator is adjusted accordingly (Figure 22-2).

FIGURE 22-2: SINGLE COMPARATOR



22.3.1 EXTERNAL REFERENCE SIGNAL

When external voltage references are used, the comparator module can be configured to have the comparators operate from the same or different reference sources. However, threshold detector applications may require the same reference. The reference signal must be between V_{SS} and V_{DD} and can be applied to either pin of the comparator(s).

22.3.2 INTERNAL REFERENCE SIGNAL

The comparator module also allows the selection of an internally generated voltage reference from the comparator voltage reference module. This module is described in more detail in **Section 23.0 “Comparator Voltage Reference Module”**.

The internal reference is only available in the mode where four inputs are multiplexed to two comparators ($CM<2:0> = 110$). In this mode, the internal voltage reference is applied to the V_{IN+} pin of both comparators.

22.4 Comparator Response Time

Response time is the minimum time, after selecting a new reference voltage or input source, before the comparator output has a valid level. If the internal reference is changed, the maximum delay of the internal voltage reference must be considered when using the comparator outputs. Otherwise, the maximum delay of the comparators should be used (see **Section 28.0 “Electrical Characteristics”**).

22.5 Comparator Outputs

The comparator outputs are read through the CMCON register. These bits are read-only. The comparator outputs may also be directly output to the RF1 and RF2 I/O pins. When enabled, multiplexors in the output path of the RF1 and RF2 pins will switch and the output of each pin will be the unsynchronized output of the comparator. The uncertainty of each of the comparators is related to the input offset voltage and the response time given in the specifications. Figure 22-3 shows the comparator output block diagram.

The TRISF bits will still function as an output enable/disable for the RF1 and RF2 pins while in this mode.

The polarity of the comparator outputs can be changed using the C2INV and C1INV bits ($CMCON<5:4>$).

- Note 1:** When reading the PORT register, all pins configured as analog inputs will read as a '0'. Pins configured as digital inputs will convert an analog input according to the Schmitt Trigger input specification.

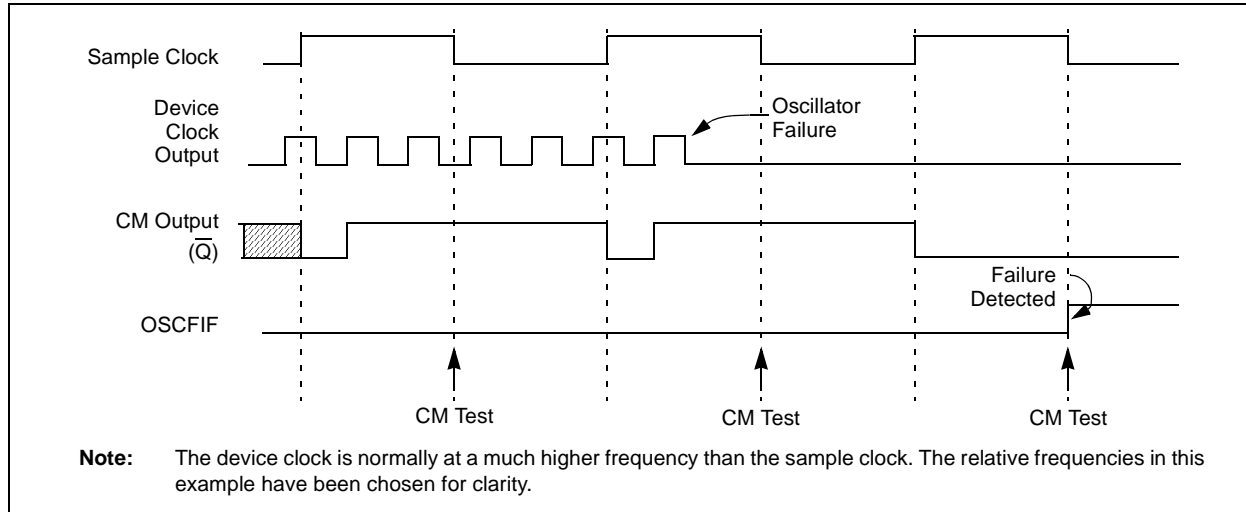
2: Analog levels on any pin defined as a digital input may cause the input buffer to consume more current than is specified.

PIC18F8722 FAMILY

NOTES:

PIC18F8722 FAMILY

FIGURE 25-4: FSCM TIMING DIAGRAM



25.4.3 FSCM INTERRUPTS IN POWER-MANAGED MODES

By entering a power-managed mode, the clock multiplexor selects the clock source selected by the OSCCON register. Fail-Safe Monitoring of the power-managed clock source resumes in the power-managed mode.

If an oscillator failure occurs during power-managed operation, the subsequent events depend on whether or not the oscillator failure interrupt is enabled. If enabled (OSCFIF = 1), code execution will be clocked by the INTOSC multiplexer. An automatic transition back to the failed clock source will not occur.

If the interrupt is disabled, subsequent interrupts while in Idle mode will cause the CPU to begin executing instructions while being clocked by the INTOSC source.

25.4.4 POR OR WAKE FROM SLEEP

The FSCM is designed to detect oscillator failure at any point after the device has exited Power-on Reset (POR) or low-power Sleep mode. When the primary device clock is EC, RC or INTRC modes, monitoring can begin immediately following these events.

For oscillator modes involving a crystal or resonator (HS, HSPLL, LP or XT), the situation is somewhat different. Since the oscillator may require a start-up time considerably longer than the FSCM sample clock time, a false clock failure may be detected. To prevent this, the internal oscillator block is automatically configured as the device clock and functions until the primary clock is stable (the OST and PLL timers have timed out). This is identical to Two-Speed Start-up mode. Once the primary clock is stable, the INTRC returns to its role as the FSCM source.

Note: The same logic that prevents false oscillator failure interrupts on POR, or wake from Sleep, will also prevent the detection of the oscillator's failure to start at all following these events. This can be avoided by monitoring the OSTS bit and using a timing routine to determine if the oscillator is taking too long to start. Even so, no oscillator failure interrupt will be flagged.

As noted in **Section 25.3.1 "Special Considerations for Using Two-Speed Start-up"**, it is also possible to select another clock configuration and enter an alternate power-managed mode while waiting for the primary clock to become stable. When the new power-managed mode is selected, the primary clock is disabled.

FIGURE 26-1: GENERAL FORMAT FOR INSTRUCTIONS

Byte-oriented file register operations		Example Instruction					
<div><div>15109870</div><table><tr><td>OPCODE</td><td>d</td><td>a</td><td>f (FILE #)</td></tr></table></div> <div>d = 0 for result destination to be WREG register d = 1 for result destination to be file register (f) a = 0 to force Access Bank a = 1 for BSR to select bank f = 8-bit file register address</div>	OPCODE	d	a	f (FILE #)		ADDWF MYREG, W, B	
OPCODE	d	a	f (FILE #)				
Byte to Byte move operations (2-word)							
<div><div>1512110</div><table><tr><td>OPCODE</td><td>f (Source FILE #)</td></tr></table></div> <div><div>1512110</div><table><tr><td>1111</td><td>f (Destination FILE #)</td></tr></table></div> <div>f = 12-bit file register address</div>	OPCODE	f (Source FILE #)	1111	f (Destination FILE #)		MOVFF MYREG1, MYREG2	
OPCODE	f (Source FILE #)						
1111	f (Destination FILE #)						
Bit-oriented file register operations							
<div><div>1512119870</div><table><tr><td>OPCODE</td><td>b (BIT #)</td><td>a</td><td>f (FILE #)</td></tr></table></div> <div>b = 3-bit position of bit in file register (f) a = 0 to force Access Bank a = 1 for BSR to select bank f = 8-bit file register address</div>	OPCODE	b (BIT #)	a	f (FILE #)		BSF MYREG, bit, B	
OPCODE	b (BIT #)	a	f (FILE #)				
Literal operations							
<div><div>15870</div><table><tr><td>OPCODE</td><td>k (literal)</td></tr></table></div> <div>k = 8-bit immediate value</div>	OPCODE	k (literal)		MOVLW 7Fh			
OPCODE	k (literal)						
Control operations							
CALL, GOTO and Branch operations							
<div><div>15870</div><table><tr><td>OPCODE</td><td>n<7:0> (literal)</td></tr></table></div> <div><div>1512110</div><table><tr><td>1111</td><td>n<19:8> (literal)</td></tr></table></div> <div>n = 20-bit immediate value</div>	OPCODE	n<7:0> (literal)	1111	n<19:8> (literal)		GOTO Label	
OPCODE	n<7:0> (literal)						
1111	n<19:8> (literal)						
<div><div>15870</div><table><tr><td>OPCODE</td><td>S</td><td>n<7:0> (literal)</td></tr></table></div> <div><div>1512110</div><table><tr><td>1111</td><td>n<19:8> (literal)</td></tr></table></div> <div>S = Fast bit</div>	OPCODE	S	n<7:0> (literal)	1111	n<19:8> (literal)		CALL MYFUNC
OPCODE	S	n<7:0> (literal)					
1111	n<19:8> (literal)						
<div><div>1511100</div><table><tr><td>OPCODE</td><td>n<10:0> (literal)</td></tr></table></div>	OPCODE	n<10:0> (literal)		BRA MYFUNC			
OPCODE	n<10:0> (literal)						
<div><div>15870</div><table><tr><td>OPCODE</td><td>n<7:0> (literal)</td></tr></table></div>	OPCODE	n<7:0> (literal)		BC MYFUNC			
OPCODE	n<7:0> (literal)						

PIC18F8722 FAMILY

TBLWT	Table Write			
Syntax:	TBLWT (*,*; *-, +*)			
Operands:	None			
Operation:	if TBLWT*, (TABLAT) → Holding Register; TBLPTR – No Change if TBLWT*+, (TABLAT) → Holding Register; (TBLPTR) + 1 → TBLPTR if TBLWT*-, (TABLAT) → Holding Register; (TBLPTR) – 1 → TBLPTR if TBLWT+*, (TBLPTR) + 1 → TBLPTR; (TABLAT) → Holding Register			
Status Affected:	None			
Encoding:	0000	0000	0000	11nn nn=0 * =1 *+ =2 *- =3 +*
Description:	<p>This instruction uses the 3 LSBs of TBLPTR to determine which of the 8 holding registers the TABLAT is written to. The holding registers are used to program the contents of Program Memory (P.M.). (Refer to Section 5.0 “Memory Organization” for additional details on programming Flash memory.)</p> <p>The TBLPTR (a 21-bit pointer) points to each byte in the program memory. TBLPTR has a 2-Mbyte address range. The LSB of the TBLPTR selects which byte of the program memory location to access.</p> <p>TBLPTR<0> = 0:Least Significant Byte of Program Memory Word</p> <p>TBLPTR<0> = 1:Most Significant Byte of Program Memory Word</p> <p>The TBLWT instruction can modify the value of TBLPTR as follows:</p> <ul style="list-style-type: none">• no change• post-increment• post-decrement• pre-increment			
Words:	1			
Cycles:	2			
Q Cycle Activity:				

	Q1	Q2	Q3	Q4
Decode	No operation	No operation	No operation	No operation
No operation	No operation (Read TABLAT)	No operation	No operation	No operation (Write to Holding Register)

TBLWT	Table Write (Continued)
<u>Example 1:</u>	TBLWT *+;
Before Instruction	
TABLAT	= 55h
TBLPTR	= 00A356h
HOLDING REGISTER (00A356h)	= FFh
After Instructions (table write completion)	
TABLAT	= 55h
TBLPTR	= 00A357h
HOLDING REGISTER (00A356h)	= 55h
<u>Example 2:</u>	TBLWT *-;
Before Instruction	
TABLAT	= 34h
TBLPTR	= 01389Ah
HOLDING REGISTER (01389Ah)	= FFh
HOLDING REGISTER (01389Bh)	= FFh
After Instruction (table write completion)	
TABLAT	= 34h
TBLPTR	= 01389Bh
HOLDING REGISTER (01389Ah)	= FFh
HOLDING REGISTER (01389Bh)	= 34h

PIC18F8722 FAMILY

28.2 DC Characteristics: Power-Down and Supply Current PIC18F6X27/6X22/8X27/8X22 (Industrial, Extended) PIC18LF6X27/6X22/8X27/8X22 (Industrial) (Continued)

PIC18LF6X27/6X22/8X27/8X22 (Industrial)		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial					
PIC18F6X27/6X22/8X27/8X22 (Industrial, Extended)		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended					
Param No.	Device	Typ	Max	Units	Conditions		
	Supply Current (IDD) ⁽²⁾						
	All devices	9.0	13	mA	-40°C	VDD = 4.2V	Fosc = 4 MHz, 16 MHz internal (PRI_RUN HS+PLL)
		9.0	13	mA	+25°C		
		9.0	13	mA	+85°C		
	Extended devices only	9.6	15	mA	+125°C		
	All devices	12	15	mA	-40°C	VDD = 5.0V	Fosc = 4 MHz, 16 MHz internal (PRI_RUN HS+PLL)
		12	15	mA	+25°C		
		12	15	mA	+85°C		
	Extended devices only	12	17	mA	+125°C		
	All devices	18	23.5	mA	-40°C	VDD = 4.2V	Fosc = 10 MHz, 40 MHz internal (PRI_RUN HS+PLL)
		19	23.5	mA	+25°C		
		19	23.5	mA	+85°C		
	All devices	25	29	mA	-40°C	VDD = 5.0V	Fosc = 10 MHz, 40 MHz internal (PRI_RUN HS+PLL)
		25	29	mA	+25°C		
25		29	mA	+85°C			

Legend: Shading of rows is to assist in readability of the table.

- Note 1:** The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to V_{DD} or V_{SS} and all features that add delta current disabled (such as WDT, Timer1 Oscillator, BOR, etc.).
- 2:** The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption.
The test conditions for all I_{DD} measurements in active operation mode are:
 OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to V_{DD} OR V_{SS} ;
 MCLR = V_{DD} ; WDT enabled/disabled as specified.
- 3:** When operation below -10°C is expected, use T1OSC High-Power mode, where LPT1OSC (CONFIG3H<2>) = 0. When operation will always be above -10°C , then the low-power Timer1 oscillator may be selected.
- 4:** BOR and HLVD enable internal band gap reference. With both modules enabled, current consumption will be less than the sum of both specifications.

PIC18F8722 FAMILY

28.4.3 TIMING DIAGRAMS AND SPECIFICATIONS

FIGURE 28-6: EXTERNAL CLOCK TIMING (ALL MODES EXCEPT PLL)

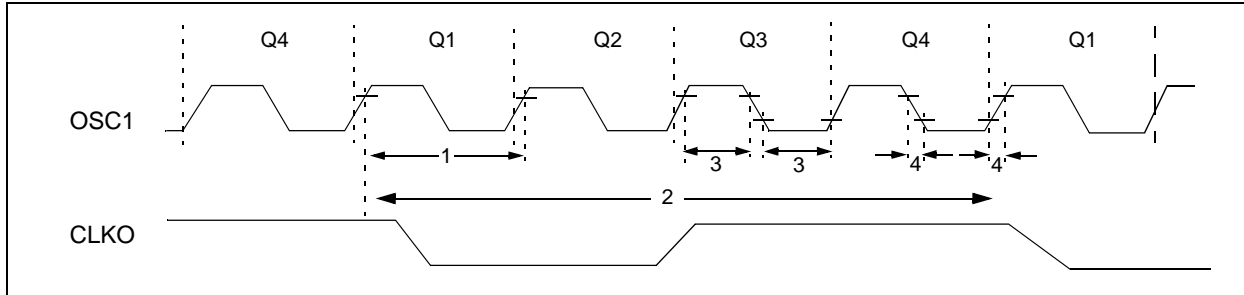


TABLE 28-6: EXTERNAL CLOCK TIMING REQUIREMENTS

Param. No.	Symbol	Characteristic	Min	Max	Units	Conditions
1A	Fosc	External CLKI Frequency ⁽¹⁾	DC	1	MHz	XT, RC Oscillator mode
			DC	25	MHz	HS Oscillator mode
			DC	31.25	kHz	LP Oscillator mode
		Oscillator Frequency ⁽¹⁾	DC	40	MHz	EC Oscillator mode
			DC	4	MHz	RC Oscillator mode
			0.1	4	MHz	XT Oscillator mode
			4	25	MHz	HS Oscillator mode
			4	10	MHz	HS + PLL Oscillator mode
			5	200	kHz	LP Oscillator mode
1	Tosc	External CLKI Period ⁽¹⁾	1000	—	ns	XT, RC Oscillator mode
			40	—	ns	HS Oscillator mode
			32	—	μs	LP Oscillator mode
		Oscillator Period ⁽¹⁾	25	—	ns	EC Oscillator mode
			250	—	ns	RC Oscillator mode
			250	1	μs	XT Oscillator mode
			40	250	ns	HS Oscillator mode
			100	250	ns	HS + PLL Oscillator mode
			5	200	μs	LP Oscillator mode
2	Tcy	Instruction Cycle Time ⁽¹⁾	100	—	ns	Tcy = 4/Fosc, Industrial
			160	—	ns	Tcy = 4/Fosc, Extended
3	TosL, TosH	External Clock in (OSC1) High or Low Time	30	—	ns	XT Oscillator mode
			2.5	—	μs	LP Oscillator mode
			10	—	ns	HS Oscillator mode
4	TosR, TosF	External Clock in (OSC1) Rise or Fall Time	—	20	ns	XT Oscillator mode
			—	50	ns	LP Oscillator mode
			—	7.5	ns	HS Oscillator mode

Note 1: Instruction cycle period (Tcy) equals four times the input oscillator time base period for all configurations except PLL. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at “min.” values with an external clock applied to the OSC1/CLKI pin. When an external clock input is used, the “max.” cycle time limit is “DC” (no clock) for all devices.

PIC18F8722 FAMILY

RCALL	351
RESET	351
RETFIE	352
RETLW	352
RETURN	353
RLCF	353
RLNCF	354
RRCF	354
RRNCF	355
SETF	355
SETF (Indexed Literal Offset Mode)	369
SLEEP	356
Standard Instructions	321
SUBFWB	356
SUBLW	357
SUBWF	357
SUBWFB	358
SWAPF	358
TBLRD	359
TBLWT	360
TSTFSZ	361
XORLW	361
XORWF	362
INTCON Register	
RBIF Bit	137
INTCON Registers	121
Inter-Integrated Circuit. <i>See</i> I ² C.	
Internal Oscillator Block	34
Adjustment	34
INTIO Modes	34
INTOSC Frequency Drift	35
INTOSC Output Frequency	34
OSCTUNE Register	34
PLL in INTOSC Modes	35
Internal RC Oscillator	
Use with WDT	312
Internet Address	439
Interrupt Sources	297
A/D Conversion Complete	275
Capture Complete (CCP)	181
Compare Complete (CCP)	182
Interrupt-on-Change (RB7:RB4)	137
INTx Pin	134
PORTB, Interrupt-on-Change	134
TMR0	134
TMR0 Overflow	163
TMR1 Overflow	165
TMR2 to PR2 Match (PWM)	184, 192
TMR3 Overflow	173, 175
TMR4 to PR4 Match	178
TMR4 to PR4 Match (PWM)	177
Interrupts	119
Interrupts, Flag Bits	
Interrupt-on-Change (RB7:RB4) Flag	
(RBIF Bit)	137
INTOSC, INTRC. <i>See</i> Internal Oscillator Block.	
IORLW	344
IORWF	344
IPR Registers	130
K	
Key Features	
Easy Migration	8
Expanded Memory	7
External Memory Interface	8

L

LFSR	345
Low-Voltage ICSP Programming. <i>See</i> Single-Supply ICSP Programming	

M

Master Clear ($\overline{\text{MCLR}}$)	51
Master Synchronous Serial Port (MSSP). <i>See</i> MSSP.	
Memory	
Mode Memory Access	64
Memory Maps for PIC18F8722 Family	
Program Memory Modes	65
Memory Organization	63
Data Memory	72
Program Memory	63
Modes	63
Memory Programming Requirements	393
Microchip Internet Web Site	439
Microcontroller Mode	100
Microprocessor Mode	100
Microprocessor with Boot Block Mode	100
Migration from Baseline to Enhanced Devices	426
Migration from High-End to Enhanced Devices	427
Migration from Mid-Range to Enhanced Devices	427
MOVF	345
MOVFF	346
MOVLB	346
MOVLW	347
MOVSF	365
MOVSS	366
MOVWF	347
MPLAB ASM30 Assembler, Linker, Librarian	372
MPLAB ICD 2 In-Circuit Debugger	373
MPLAB ICE 2000 High-Performance	
Universal In-Circuit Emulator	373
MPLAB Integrated Development	
Environment Software	371
MPLAB PM3 Device Programmer	373
MPLAB REAL ICE In-Circuit Emulator System	373
MPLINK Object Linker/MPLIB Object Librarian	372
MSSP	
$\overline{\text{ACK}}$ Pulse	219, 220
Control Registers (general)	205
I ² C Mode. <i>See</i> I ² C Mode.	
Module Overview	205
SPI Master/Slave Connection	209
TMR4 Output for Clock Shift	178
MULLW	348
MULWF	348

N

NEGF	349
NOP	349

O

Opcode Field Descriptions	322
Oscillator Configuration	31
EC	31
ECIO	31
HS	31
HSPLL	31
Internal Oscillator Block	34
INTIO1	31
INTIO2	31
LP	31