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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	40MHz
Connectivity	EBI/EMI, I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, POR, PWM, WDT
Number of I/O	70
Program Memory Size	64KB (32K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	3.8K x 8
Voltage - Supply (Vcc/Vdd)	4.2V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-TQFP
Supplier Device Package	80-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18f8622-i-pt

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Din Nome	Pin Number	Pin	Buffer	Description
	TQFP	Туре	Туре	Description
				PORTD is a bidirectional I/O port.
RD0/PSP0 RD0 PSP0	58	I/O I/O	ST TTL	Digital I/O. Parallel Slave Port data.
RD1/PSP1 RD1 PSP1	55	I/O I/O	ST TTL	Digital I/O. Parallel Slave Port data.
RD2/PSP2 RD2 PSP2	54	I/O I/O	ST TTL	Digital I/O. Parallel Slave Port data.
RD3/PSP3 RD3 PSP3	53	I/O I/O	ST TTL	Digital I/O. Parallel Slave Port data.
RD4/PSP4/SDO2 RD4 PSP4 SDO2	52	I/O I/O O	ST TTL	Digital I/O. Parallel Slave Port data. SPI data out.
RD5/PSP5/SDI2/SDA2 RD5 PSP5 SDI2 SDA2	51	I/O I/O I I/O	ST TTL ST I ² C/SMB	Digital I/O. Parallel Slave Port data. SPI data in. I ² C™ data I/O.
RD6/PSP6/SCK2/SCL2 RD6 PSP6 SCK2 SCL2	50	I/O I/O I/O I/O	ST TTL ST I ² C/SMB	Digital I/O. Parallel Slave Port data. Synchronous serial clock input/output for SPI mode. Synchronous serial clock input/output for I ² C mode.
RD7/PSP7/SS2 RD7 PSP7 SS2	49	I/O I/O I	ST TTL TTL	Digital I/O. Parallel Slave Port data. SPI slave select input.
Legend: TTL = TTL co ST = Schmi I = Input P = Power	ompatible input tt Trigger input	CMO with CM O I ² C™	S OS levels	 CMOS compatible input or output Analog = Analog input Output I²C/SMBus input buffer

TABLE 1-3: PIC18F6527/6622/6627/6722 PINOUT I/O DESCRIPTIONS (CONTINUED)

Note 1: Default assignment for ECCP2 when Configuration bit, CCP2MX, is set.

2: Alternate assignment for ECCP2 when Configuration bit, CCP2MX, is cleared.



CALL, RCAL	21				
KEIFIE, KE	Stack	evel 1		٦Ć	
	Stack L	evel 31			
	Reset	Vector			
	High-Priority I	nterrunt Vector		00086	
	Tigh-Thomy T			000611	
	Low-Priority I	nterrupt Vector		0018h	
On-Chip Program Memory	On-Chip Program Memory	On-Chip Program Memory	On-Chip Program Memory		
PIC18FX527	PIC18FX622	PIC18FX627	PIC18FX722		
0C000h	0FFFh 10000h			I Isar Memory Space	
		017FFFh 018000h			
Read '0'	Read '0'	Read '0'			
				01EEEb	

TABLE 5-1: MEMORY ACCESS FOR PIC18F8527/8622/8627/8722 PROGRAM MEMORY MODES

	Inte	rnal Program Men	nory	External Program Memory			
Operating Mode	Execution From	Table Read From	Table Write To	Execution From	Table Read From	Table Write To	
Microprocessor	No Access	No Access	No Access	Yes	Yes	Yes	
Microprocessor w/ Boot Block	Yes	Yes	Yes	Yes	Yes	Yes	
Microcontroller	Yes	Yes	Yes	No Access	No Access	No Access	
Extended Microcontroller	Yes	Yes	Yes	Yes	Yes	Yes	

5.3.5 STATUS REGISTER

The STATUS register, shown in Register 5-2, contains the arithmetic status of the ALU. As with any other SFR, it can be the operand for any instruction.

If the STATUS register is the destination for an instruction that affects the Z, DC, C, OV or N bits, the results of the instruction are not written; instead, the STATUS register is updated according to the instruction performed. Therefore, the result of an instruction with the STATUS register as its destination may be different than intended. As an example, CLRF STATUS will set the Z bit and leave the remaining Status bits unchanged ('000u uluu'). It is recommended that only BCF, BSF, SWAPF, MOVFF and MOVWF instructions are used to alter the STATUS register, because these instructions do not affect the Z, C, DC, OV or N bits in the STATUS register.

For other instructions that do not affect Status bits, see the instruction set summaries in Table 26-2 and Table 26-3.

Note: The C and DC bits operate as the borrow and digit borrow bits, respectively, in subtraction.

REGISTER 5-2: STATUS: ARITHMETIC STATUS REGISTER

U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
		—	N	OV	Z	DC ⁽¹⁾	C ⁽²⁾
bit 7							bit 0
Legend:							
R = Read	lable bit	W = Writable	bit	U = Unimplei	mented bit, read	d as '0'	
-n = Value	e at POR	'1' = Bit is se	t	'0' = Bit is cle	ared	x = Bit is unkr	nown
bit 7-5	Unimplemen	ted: Read as	0'				
bit 4	N: Negative b	bit					
	This bit is use negative (ALI 1 = Result wa 0 = Result wa	ed for signed a U MSB = 1). as negative as positive	rithmetic (2's d	complement). I	t indicates whe	ther the result w	vas
bit 3	OV: Overflow This bit is use magnitude wl 1 = Overflow 0 = No overfl	bit bit for signed a hich causes the occurred for si ow occurred	rithmetic (2's o e sign bit (bit 7 gned arithmet	complement). I 7 of the result) tic (in this arithi	t indicates an o to change state netic operation	verflow of the 7)	-bit
bit 2	Z: Zero bit						
	1 = The resul 0 = The resul	t of an arithme t of an arithme	tic or logic op tic or logic op	eration is zero eration is not z	ero		
bit 1	DC: Digit Car	ry/borrow bit(1))				
	For addwf, a	DDLW, SUBLW a	and SUBWF ins	structions:			
	1 = A carry-o 0 = No carry-	ut from the 4th out from the 41	low-order bit h low-order bi	of the result oc t of the result	curred		
bit 0	C: Carry/borr For ADDWF, A 1 = A carry-o 0 = No carry-	ow bit ⁽²⁾ DDLW, SUBLW a ut from the Mo out from the M	and SUBWF ins st Significant I ost Significan	structions: bit of the result t bit of the resu	occurred It occurred		
Note 1: 2:	For borrow, the po operand. For rotat For borrow, the po	larity is reverse e (RRF, RLF) in larity is reverse e (RRF, RLF) in	ed. A subtractions this structions, this ed. A subtractions this	on is executed s bit is loaded v on is executed s bit is loaded v	by adding the 2 with either bit 4 by adding the 2 with either the 1	's complement or bit 3 of the so 's complement high or low-orde	of the second ource register. of the second er bit of the

source register.







REGISTER 10-5: PIR2: PERIPHERAL INTERRUPT REQUEST (FLAG) REGISTER 2

R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
OSCFIF	CMIF	_	EEIF	BCL1IF	HLVDIF	TMR3IF	CCP2IF
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, rea	d as '0'	
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown
bit 7	OSCFIF: Osc	illator Fail Inte	rrupt Flag bit				
	1 = Device of	scillator failed,	clock input ha	as changed to I	NTOSC (must	be cleared in so	oftware)
hit C		ock operating	Flog bit				
DILO		arator interrupt	Flag bit	the cleared in	coftwara)		
	1 = Compara0 = Compara	itor input has c	ot changed	t be cleared in a	soliwale)		
bit 5	Unimplemen	ted: Read as '	0'				
bit 4	EEIF: EEPRO	DM or Flash W	rite Operation	Interrupt Flag	bit		
	1 = The write	operation is c	omplete (mus	t be cleared in	software)		
	0 = The write	operation is n	ot complete o	r has not been	started		
bit 3	BCL1IF: MSS	SP1 Bus Collisi	ion Interrupt F	lag bit			
	1 = A bus c	ollision occurr	ed while the	MSSP1 modu	ule configured	in l ² C™ Mast	er mode was
	0 – No bus c	ing (must be ci ollision occurre	eared in softw	/are)			
hit 2		/I ow-Voltage	Detect Interru	nt Flag bit			
5112	1 = A low-vol	tage condition	occurred (mu	ist be cleared in	n software)		
	0 = The devie	ce voltage is al	bove the Low-	-Voltage Detect	t trip point		
bit 1	TMR3IF: TMF	R3 Overflow In	terrupt Flag b	it			
	1 = TMR3 re	gister overflow	ed (must be c	leared in softw	are)		
	0 = TMR3 re	gister did not o	verflow				
bit 0	CCP2IF: ECC	CP2 Interrupt F	lag bit				
	<u>Capture mode</u>	<u>ə:</u> TMP3 register	conturo occu	rrod (must bo c	loared in coffw	(ara)	
	0 = No TMR1	1/TMR3 register	er capture occu	urred		ale)	
	Compare mod	de:	·				
	1 = A TMR1/	TMR3 register	compare mat	ch occurred (m	nust be cleared	in software)	
	0 = No TMR1	1/TMR3 registe	er compare ma	atch occurred			
	<u>PWM mode:</u>	s mode					
	Unused in this	s moue.					

R/W-0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
SSP2IP	BCL2IP	RC2IP	TX2IP	TMR4IP	CCP5IP	CCP4IP	CCP3IP
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, read	d as '0'	
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown
bit 7	SSP2IP: MS	SP2 Interrupt P	riority bit				
	1 = High price	ority					
bit 6	BCI 2IP: MS	SP2 Bus Collisi	ion Interrupt F	Priority bit			
Site	1 = High price	ority		nonty sit			
	0 = Low prior	ority					
bit 5	RC2IP: EUS	ART2 Receive	Interrupt Prior	rity bit			
	1 = High price	ority					
L:1 4	0 = Low prio	ority					
DIT 4	1 High price		Interrupt Prio	rity bit			
	$1 = \operatorname{High} \operatorname{pric}$ $0 = \operatorname{Low} \operatorname{pric}$	brity					
bit 3	TMR4IP: TM	R4 to PR4 Mat	ch Interrupt P	riority bit			
	1 = High pric	ority		2			
	0 = Low prior	ority					
bit 2	CCP5IP: CC	P5 Interrupt Pri	ority bit				
	1 = High price	ority					
hit 1		DA Intorrunt Dri	ority bit				
DICT	1 – High pric	r4 interrupt r ii arity					
	0 = Low prior	ority					
bit 0	CCP3IP: EC	CP3 Interrupt P	Priority bit				
	1 = High pric	ority					
	0 = Low prio	ority					

REGISTER 10-12: IPR3: PERIPHERAL INTERRUPT PRIORITY REGISTER 3

Pin Name	Function	TRIS Setting	I/O	l/O Type	Description
RH0/A16	RH0	0	0	DIG	LATH<0> data output.
		1	Ι	ST	PORTH<0> data input.
	A16	x	0	DIG	External memory interface, address line 16. Takes priority over port data.
RH1/A17	RH1	0	0	DIG	LATH<1> data output.
		1	Ι	ST	PORTH<1> data input.
	A17	x	0	DIG	External memory interface, address line 17. Takes priority over port data.
RH2/A18	RH2	0	0	DIG	LATH<2> data output.
		1	Ι	ST	PORTH<2> data input.
	A18	x	0	DIG	External memory interface, address line 18. Takes priority over port data.
RH3/A19	RH3	0	0	DIG	LATH<3> data output.
		1	Ι	ST	PORTH<3> data input.
	A19	x	0	DIG	External memory interface, address line 19. Takes priority over port data.
RH4/AN12/	RH4	0	0	DIG	LATH<4> data output.
P3C		1	Ι	ST	PORTH<4> data input.
	AN12	1	Ι	ANA	A/D input channel 12. Default configuration on POR.
	P3C ⁽¹⁾	0	0	DIG	ECCP3 Enhanced PWM output, channel C. May be configured for tri-state during Enhanced PWM shutdown events. Takes priority over port data.
RH5/AN13/	RH5	0	0	DIG	LATH<5> data output.
P3B		1	Ι	ST	PORTH<5> data input.
	AN13	1	Ι	ANA	A/D input channel 13. Default configuration on POR.
	P3B ⁽¹⁾	0	0	DIG	ECCP3 Enhanced PWM output, channel B. May be configured for tri-state during Enhanced PWM shutdown events. Takes priority over port data.
RH6/AN14/	RH6	0	0	DIG	LATH<6> data output.
P1C		1	Ι	ST	PORTH<6> data input.
	AN14	1	Ι	ANA	A/D input channel 14. Default configuration on POR.
	P1C ⁽¹⁾	0	0	DIG	ECCP1 Enhanced PWM output, channel C. May be configured for tri-state during Enhanced PWM shutdown events. Takes priority over port data.
RH7/AN15/	RH7	0	0	DIG	LATH<7> data output.
P1B		1	Ι	ST	PORTH<7> data input.
	AN15	1	Ι	ANA	A/D input channel 15. Default configuration on POR.
	P1B ⁽¹⁾	0	0	DIG	ECCP1 Enhanced PWM output, channel B. May be configured for tri-state during Enhanced PWM shutdown events. Takes priority over port data.

TABLE 11-15: PORTH FUNCTIONS

Legend: PWR = Power Supply, O = Output, I = Input, ANA = Analog Signal, DIG = Digital Output, ST = Schmitt Buffer Input, TTL = TTL Buffer Input, x = Don't care (TRIS bit does not affect port direction or is overridden for this option).

Note 1: Alternate assignment for P1B/P1C/P3B/P3C (ECCPMX is clear).

TABLE 11-16:	SUMMARY C	OF REGISTERS	ASSOCIATED	WITH PORTH

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on page
TRISH	TRISH7	TRISH6	TRISH5	TRISH4	TRISH3	TRISH2	TRISH1	TRISH0	60
PORTH	RH7	RH6	RH5	RH4	RH3	RH2	RH1	RH0	60
LATH	LATH7	LATH6	LATH5	LATH4	LATH3	LATH2	LATH1	LATH0	60
ADCON1	—	—	VCFG1	VCFG0	PCFG3	PCFG2	PCFG1	PCFG0	59

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15.0 TIMER3 MODULE

The Timer3 timer/counter module incorporates these features:

- Software selectable operation as a 16-bit timer or counter
- Readable and writable 8-bit registers (TMR3H and TMR3L)
- Selectable clock source (internal or external) with device clock or Timer1 oscillator internal options
- Interrupt-on-overflow
- Module Reset on CCP Special Event Trigger

A simplified block diagram of the Timer3 module is shown in Figure 15-1. A block diagram of the module's operation in Read/Write mode is shown in Figure 15-2.

The Timer3 module is controlled through the T3CON register (Register 15-1). It also selects the clock source options for the CCP modules (see **Section 17.1.1** "**CCP Modules and Timer Resources**" for more information).

REGISTER 15-1: T3CON: TIMER3 CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
RD16	T3CCP2	T3CKPS1	T3CKPS0	T3CCP1	T3SYNC	TMR3CS	TMR3ON
bit 7							bit 0

Legend:				
R = Readable b	oit	W = Writable bit	U = Unimplemented bit,	, read as '0'
-n = Value at P	OR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown
bit 7	RD16: 16-Bit	Read/Write Mode Enable	e bit	
	1 = Enables re 0 = Enables re	egister read/write of Time egister read/write of Time	er3 in one 16-bit operation er3 in two 8-bit operations	
bit 6, 3	T3CCP<2:1>:	Timer3 and Timer1 to C	CPx Enable bits	
	11 = Timer3 10 = Timer3 Timer1	and Timer4 are the clock and Timer4 are the clock and Timer2 are the clock	sources for ECCP1, ECCP3 sources for ECCP3, CCP4	2, ECCP3, CCP4 and CCP5 and CCP5;
	01 = Timer3 Timer1	and Timer2 are the clock and Timer2 are the clock and Timer2 are the clock	sources for ECCP2, ECCP3	3, CCP4 and CCP5;
	00 = Timer1	and Timer2 are the clock	sources for ECCP1, ECCP2	2, ECCP3, CCP4 and CCP5
bit 5-4	T3CKPS<1:0:	: Timer3 Input Clock Pre	escale Select bits	
	11 = 1:8 Pres	cale value		
	10 = 1.4 Pres	cale value		
	00 = 1:1 Pres	cale value		
bit 2	T3SYNC: Tim (Not usable if	er3 External Clock Input the device clock comes	Synchronization Control bit from Timer1/Timer3.)	
	When TMR3C	<u>CS = 1:</u>		
	1 = Do not syn	nchronize external clock	input	
	When TMR3C	S = 0		
	This bit is igno	ored. Timer3 uses the int	ernal clock when TMR3CS =	: 0.
bit 1	TMR3CS: Tim	ner3 Clock Source Select	t bit	
	1 = External c 0 = Internal c	clock input from Timer1 o lock (Fosc/4)	scillator or T13CKI (on the ris	ing edge after the first falling edge)
bit 0	TMR3ON: Tim	ner3 On bit		
	1 = Enables T 0 = Stops Tim	ïmer3 er3		

17.2 Capture Mode

In Capture mode, the CCPRxH:CCPRxL register pair captures the 16-bit value of the TMR1 or TMR3 registers when an event occurs on the corresponding CCPx pin. An event is defined as one of the following:

- every falling edge
- every rising edge
- every 4th rising edge
- every 16th rising edge

The event is selected by the mode select bits, CCPxM<3:0> (CCPxCON<3:0>). When a capture is made, the interrupt request flag bit, CCPxIF, is set; it must be cleared in software. If another capture occurs before the value in the CCPRx registers is read, the old captured value is overwritten by the new captured value.

17.2.1 CCPx PIN CONFIGURATION

In Capture mode, the appropriate CCPx pin should be configured as an input by setting the corresponding TRIS direction bit.

Note:	If a CCPx pin is configured as an output, a					
	write to the port can cause a capture					
	condition.					

17.2.2 TIMER1/TIMER3 MODE SELECTION

The timers that are to be used with the capture feature (Timer1 and/or Timer3) must be running in Timer mode or Synchronized Counter mode. In Asynchronous Counter mode, the capture operation will not work. The timer to be used with each CCP module is selected in the T3CON register (see Section 17.1.1 "CCP Modules and Timer Resources").

17.2.3 SOFTWARE INTERRUPT

When the Capture mode is changed, a false capture interrupt may be generated. The user should keep the CCPxIE interrupt enable bit clear to avoid false interrupts. The interrupt flag bit, CCPxIF, should also be cleared following any such change in operating mode.

17.2.4 CCP PRESCALER

There are four prescaler settings in Capture mode; they are specified as part of the operating mode selected by the mode select bits (CCPxM<3:0>). Whenever the CCP module is turned off, or Capture mode is disabled, the prescaler counter is cleared. This means that any Reset will clear the prescaler counter.

Switching from one capture prescaler to another may generate an interrupt. Also, the prescaler counter will not be cleared; therefore, the first capture may be from a non-zero prescaler. Example 17-1 shows the recommended method for switching between capture prescalers. This example also clears the prescaler counter and will not generate the "false" interrupt.

EXAMPLE 17-1: CHANGING BETWEEN CAPTURE PRESCALERS (CCP5 SHOWN)

CLRF MOVLW	CCP5CON NEW_CAPT_PS	; ;	Turn CCP module off Load WREG with the
		;	new prescaler mode
		;	value and CCP ON
MOVWF	CCP5CON	;	Load CCP5CON with
		;	this value

FIGURE 17-2: CAPTURE MODE OPERATION BLOCK DIAGRAM



The CCPRxH register and a 2-bit internal latch are used to double-buffer the PWM duty cycle. This double-buffering is essential for glitchless PWM operation.

When the CCPRxH and 2-bit latch match TMR2 (TMR4), concatenated with an internal 2-bit Q clock or 2 bits of the TMR2 (TMR4) prescaler, the CCPx pin is cleared.

The maximum PWM resolution (bits) for a given PWM frequency is given by the equation:

EQUATION 17-3:

PWM Resolution (max) =
$$\frac{\log(\frac{Fosc}{FPWM})}{\log(2)}$$
 bits

Note: If the PWM duty cycle value is longer than the PWM period, the CCPx pin will not be cleared.

17.4.3 SETUP FOR PWM OPERATION

The following steps should be taken when configuring the CCP module for PWM operation:

- 1. Set the PWM period by writing to the PR2 (PR4) register.
- Set the PWM duty cycle by writing to the CCPRxL register and CCPxCON<5:4> bits.
- 3. Make the CCPx pin an output by clearing the appropriate TRIS bit.
- 4. Set the TMR2 (TMR4) prescale value, then enable Timer2 (Timer4) by writing to T2CON (T4CON).
- 5. Configure the CCPx module for PWM operation.

TABLE 17-3: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS AT 40 MHz

PWM Frequency	2.44 kHz	9.77 kHz	39.06 kHz	156.25 kHz	312.50 kHz	416.67 kHz
Timer Prescaler (1, 4, 16)	16	4	1	1	1	1
PR2 Value	FFh	FFh	FFh	3Fh	1Fh	17h
Maximum Resolution (bits)	10	10	10	8	7	6.58

19.4.9 I²C MASTER MODE REPEATED START CONDITION TIMING

A Repeated Start condition occurs when the RSEN bit (SSPxCON2<1>) is programmed high and the I²C logic module is in the Idle state. When the RSEN bit is set, the SCLx pin is asserted low. When the SCLx pin is sampled low, the Baud Rate Generator is loaded with the contents of SSPxADD<5:0> and begins counting. The SDAx pin is released (brought high) for one Baud Rate Generator count (TBRG). When the Baud Rate Generator times out, if SDAx is sampled high, the SCLx pin will be deasserted (brought high). When SCLx is sampled high, the Baud Rate Generator is reloaded with the contents of SSPxADD<6:0> and begins counting. SDAx and SCLx must be sampled high for one TBRG. This action is then followed by assertion of the SDAx pin (SDAx = 0) for one TBRG while SCLx is high. Following this, the RSEN bit (SSPxCON2<1>) will be automatically cleared and the Baud Rate Generator will not be reloaded, leaving the SDAx pin held low. As soon as a Start condition is detected on the SDAx and SCLx pins, the S bit (SSPxSTAT<3>) will be set. The SSPxIF bit will not be set until the Baud Rate Generator has timed out.

- **Note 1:** If RSEN is programmed while any other event is in progress, it will not take effect.
 - **2:** A bus collision during the Repeated Start condition occurs if:
 - SDAx is sampled low when SCLx goes from low-to-high.
 - SCLx goes low before SDAx is asserted low. This may indicate that another master is attempting to transmit a data '1'.

Immediately following the SSPxIF bit getting set, the user may write the SSPxBUF with the 7-bit address in 7-bit mode or the default first address in 10-bit mode. After the first eight bits are transmitted and an ACK is received, the user may then transmit an additional eight bits of address (10-bit mode) or eight bits of data (7-bit mode).

19.4.9.1 WCOL Status Flag

If the user writes the SSPxBUF when a Repeated Start sequence is in progress, the WCOL is set and the contents of the buffer are unchanged (the write doesn't occur).

Note: Because queueing of events is not allowed, writing of the lower 5 bits of SSPxCON2 is disabled until the Repeated Start condition is complete.

FIGURE 19-20: REPEATED START CONDITION WAVEFORM



22.2 Comparator Operation

A single comparator is shown in Figure 22-2, along with the relationship between the analog input levels and the digital output. When the analog input at VIN+ is less than the analog input VIN-, the output of the comparator is a digital low level. When the analog input at VIN+ is greater than the analog input VIN-, the output of the comparator is a digital high level. The shaded areas of the output of the comparator in Figure 22-2 represent the uncertainty, due to input offsets and response time.

22.3 Comparator Reference

Depending on the comparator operating mode, either an external or internal voltage reference may be used. The analog signal present at VIN- is compared to the signal at VIN+ and the digital output of the comparator is adjusted accordingly (Figure 22-2).



22.3.1 EXTERNAL REFERENCE SIGNAL

When external voltage references are used, the comparator module can be configured to have the comparators operate from the same or different reference sources. However, threshold detector applications may require the same reference. The reference signal must be between Vss and VDD and can be applied to either pin of the comparator(s).

22.3.2 INTERNAL REFERENCE SIGNAL

The comparator module also allows the selection of an internally generated voltage reference from the comparator voltage reference module. This module is described in more detail in **Section 23.0 "Comparator Voltage Reference Module"**.

The internal reference is only available in the mode where four inputs are multiplexed to two comparators (CM<2:0> = 110). In this mode, the internal voltage reference is applied to the VIN+ pin of both comparators.

22.4 Comparator Response Time

Response time is the minimum time, after selecting a new reference voltage or input source, before the comparator output has a valid level. If the internal reference is changed, the maximum delay of the internal voltage reference must be considered when using the comparator outputs. Otherwise, the maximum delay of the comparators should be used (see Section 28.0 "Electrical Characteristics").

22.5 Comparator Outputs

The comparator outputs are read through the CMCON register. These bits are read-only. The comparator outputs may also be directly output to the RF1 and RF2 I/O pins. When enabled, multiplexors in the output path of the RF1 and RF2 pins will switch and the output of each pin will be the unsynchronized output of the comparator. The uncertainty of each of the comparators is related to the input offset voltage and the response time given in the specifications. Figure 22-3 shows the comparator output block diagram.

The TRISF bits will still function as an output enable/ disable for the RF1 and RF2 pins while in this mode.

The polarity of the comparator outputs can be changed using the C2INV and C1INV bits (CMCON<5:4>).

- Note 1: When reading the PORT register, all pins configured as analog inputs will read as a '0'. Pins configured as digital inputs will convert an analog input according to the Schmitt Trigger input specification.
 - 2: Analog levels on any pin defined as a digital input may cause the input buffer to consume more current than is specified.

24.2 HLVD Setup

The following steps are needed to set up the HLVD module:

- 1. Write the value to the HLVDL<3:0> bits that selects the desired HLVD trip point.
- Set the VDIRMAG bit to detect high voltage (VDIRMAG = 1) or low voltage (VDIRMAG = 0).
- 3. Enable the HLVD module by setting the HLVDEN bit.
- 4. Clear the HLVD interrupt flag (PIR2<2>), which may have been set from a previous interrupt.
- Enable the HLVD interrupt if interrupts are desired by setting the HLVDIE and GIE bits (PIE2<2> and INTCON<7>). An interrupt will not be generated until the IRVST bit is set.

24.3 Current Consumption

When the module is enabled, the HLVD comparator and voltage divider are enabled and will consume static current. The total current consumption, when enabled, is specified in electrical specification parameter D022B (Section 28.2 "DC Characteristics"). Depending on the application, the HLVD module does not need to be operating constantly. To decrease the current requirements, the HLVD circuitry may only need to be enabled for short periods where the voltage is checked. After doing the check, the HLVD module may be disabled.

24.4 HLVD Start-up Time

The internal reference voltage of the HLVD module, specified in electrical specification parameter D420 (**Section 28.2 "DC Characteristics**"), may be used by other internal circuitry, such as the Programmable Brown-out Reset. If the HLVD or other circuits using the voltage reference are disabled to lower the device's current consumption, the reference voltage circuit will require time to become stable before a low or high-voltage condition can be reliably detected. This start-up time, TIRVST, is an interval that is independent of device clock speed. It is specified in electrical specification parameter 36 (Table 28-12).

The HLVD interrupt flag is not enabled until TIRVST has expired and a stable reference voltage is reached. For this reason, brief excursions beyond the set point may not be detected during this interval. Refer to Figure 24-2 or Figure 24-3.





MUL	LW	Multiply L	iteral with	w				
Synta	ax:	MULLW	k					
Oper	ands:	$0 \le k \le 25$	$0 \le k \le 255$					
Oper	ation:	(W) x k \rightarrow	PRODH:PF	RODL				
Statu	is Affected:	None						
Enco	oding:	0000	1101	kkkk	kkkk			
Desc	cription:	An unsign out betwee 8-bit literal placed in F PRODH co	An unsigned multiplication is carried out between the contents of W and the 8-bit literal 'k'. The 16-bit result is placed in PRODH:PRODL register pair. PRODH contains the high byte.					
		W is uncha	anged.					
		None of th	e status fla	gs are a	iffected.			
		Note that r possible in is possible	Note that neither Overflow nor Carry is possible in this operation. A Zero result is possible but not detected.					
Word	ds:	1	1					
Cycle	es:	1						
QC	ycle Activity:							
	Q1	Q2	Q3		Q4			
	Decode	Read literal 'k'	Process Data	re Pl P	Write gisters RODH: RODL			
Exan	nple:	MULLW	0C4h					
	Before Instruc W PRODH PRODL After Instructio W	tion = E: = ? = ? on = E:	2h 2h					

MULWF	Multiply W	with f					
Syntax:	MULWF	f {,a}					
Operands:	$\begin{array}{l} 0 \leq f \leq 255 \\ a \in [0,1] \end{array}$	$\begin{array}{l} 0 \leq f \leq 255 \\ a \in [0,1] \end{array}$					
Operation:	(W) x (f) \rightarrow PRODH:PRODL						
Status Affected:	None	None					
Encoding:	0000	0000 001a ffff ffff					
Description:	An unsigned multiplication is carried out between the contents of W and the register file location 'f'. The 16-bit result is stored in the PRODH:PRODL register pair. PRODH contains the high byte. Both W and 'f' are unchanged.						
	None of the status flags are affected.						
	Note that neither Overflow nor Carry is possible in this operation. A Zero result is possible but not detected.						
	If 'a' is '0', t 'a' is '1', the GPR bank	he Acces e BSR is ι (default).	s Bank is ised to se	selected. If elect the			
	If 'a' is '0' and the extended instruction so is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever f ≤ 95 (5Fh). See Section 26.2.3 "Byte-Oriented and Bit-Oriented Instructions in Indexed						
Words:	1						
Cycles:	1						
Q Cycle Activity:							
Q1	Q2	C	3	Q4			
Decode	Read register 'f	Proc Da	ess ta	Write registers PRODH: PRODL			
Example:	MULWF	REG,	1				
Before Instruction W = C4h REG = B5h PRODH = ?							

= = =

C4h B5h 8Ah 94h

After Instruction

W REG PRODH PRODL

RETI	RETURN Return from Subroutine							
Synta	ax:	RETURN	{s}					
Oper	ands:	$s \in \left[0,1\right]$	s ∈ [0,1]					
Oper	ation:	$(TOS) \rightarrow F$ if s = 1 $(WS) \rightarrow W$ (STATUSS) $(BSRS) \rightarrow$ PCLATU, F	$(TOS) \rightarrow PC,$ if s = 1 $(WS) \rightarrow W,$ $(STATUSS) \rightarrow STATUS,$ $(BSRS) \rightarrow BSR,$ PCLATU, PCLATH are unchanged					
Statu	s Affected:	None						
Enco	ding:	0000	0000	0001	001s			
Desc	ription:	Return from popped an is loaded in 's'= 1, the registers W loaded into registers W 's' = 0, no occurs (de	popped and the top of the stack (TOS) is loaded into the program counter. If 's'= 1, the contents of the shadow registers WS, STATUSS and BSRS are loaded into their corresponding registers W, STATUS and BSR. If 's' = 0, no update of these registers occurs (default)					
Word	ls:	1	1					
Cycle	es:	2						
QC	ycle Activity:							
	Q1	Q2	Q	3	Q4			
	Decode	No operation	Proce Dat	ess F a fro	POP PC			
	No operation	No operation	No operat	tion o	No peration			
Exam	nple:	RETURN						

After Inst	ruction:
PC	= TOS

Rotate Left	f through Car	ry				
RLCF f {	,d {,a}}					
$0 \leq f \leq 255$						
d ∈ [0,1] a ∈ [0,1]						
$a \in [0, 1]$	$(f_{a}, p_{a}) \rightarrow doot an + 1$					
$(1<1>) \rightarrow de$ $(f<7>) \rightarrow C,$ $(C) \rightarrow dest<$	$(f<7>) \rightarrow C,$ (C) \rightarrow dest<0>					
C, N, Z						
0011	01da fff	f ffff				
The contents of register 'f' are rotated one bit to the left through the Carry flag. If 'd' is '0', the result is placed in W. If 'd' is '1', the result is stored back in register 'f' (default).						
If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the GPR bank (default).						
set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever f ≤ 95 (5Fh). See Section 26.2.3 "Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode" for details						
C	 registe 	rf <mark>≁</mark>				
1						
1						
·						
02	03	04				
Read	Process	Write to				
register 'f'	Data	destination				
RLCF	REG, 0,	0				
tion						
	0110					
= 1110 = 0	0110					
= 1110 = 0	0110					
	0110					
	0110 1100					
	Rotate Left RLCF f { $0 \le f \le 255$ $d \in [0,1]$ $a \in [0,1]$ $a \in [0,1]$ (f <n>) $\rightarrow de$ (f<7>) $\rightarrow C$, (C) $\rightarrow destechtor C, N, Z 0011 The content one bit to th If 'd' is '0', tt is '1', the ref 'f' (default). If 'a' is '0', tt If 'a' is '0' at set is enabl in Indexed I mode when Section 26 Bit-Oriente Literal Offs 1 1 Q2 Read register 'f' RLCF$</n>	Rotate Left f through CarRLCFf {,d {,a}} $0 \le f \le 255$ $d \in [0,1]$ $a \in [0,1]$ $a \in [0,1]$ $a \in [0,1]$ (f(-r>) \rightarrow dest(-n + 1>,(f(-7>) \rightarrow C,(C) \rightarrow dest(-0>C, N, Z 0011 $011a$ $01da$ fff The contents of register 'f'one bit to the left through tIf 'd' is '0', the result is placeis '1', the result is stored bar'f' (default).If 'a' is '0', the Access BanIf 'a' is '0' and the extendeset is enabled, this instructin Indexed Literal Offset Acmode whenever $f \le 95$ (5FSection 26.2.3 "Byte-OriesBit-Oriented InstructionsLiteral Offset Mode" for cols11Q2Q3ReadProcessregister 'f'DataRLCFREG, 0,				

RLNCF	Rotate Lef	it f (no carry)		RRCF	Rotate Rig	ht f through	Carry	
Syntax:	RLNCF	f {,d {,a}}		Syntax:	RRCF f{	,d {,a}}		
Operands:	0 ≤ f ≤ 255 d ∈ [0,1] a ∈ [0,1]			Operands:	$\begin{array}{l} 0 \leq f \leq 255 \\ d \in [0,1] \\ a \in [0,1] \end{array}$			
Operation:	$(f < n >) \rightarrow d$ $(f < 7 >) \rightarrow d$	est <n +="" 1="">, est<0></n>		Operation:	$(f < n >) \rightarrow de$ $(f < 0 >) \rightarrow C$	est <n 1="" –="">, ,</n>		
Status Affected:	N, Z				$(C) \rightarrow dest$			
Encoding:	0100	01da ff	ff ffff	Encoding:	0, N, Z	00do ff	ff fff	
Description:	The conter one bit to t is placed ir stored bac If 'a' is '0', t	hts of register ' he left. If 'd' is n W. If 'd' is '1' k in register 'f' the Access Ba	f' are rotated '0', the result , the result is (default). nk is selected.	Description:	0011 00da ffff ffff The contents of register 'f' are rotated one bit to the right through the Carry flag. If 'd' is '0', the result is placed in W If 'd' is '1', the result is placed back in			
	If 'a' is '1', t GPR bank If 'a' is '0' a set is enab	the BSR is use (default). and the extend	d to select the led instruction		If 'a' is '0', the Access Bank is selecte If 'a' is '1', the BSR is used to select th GPR bank (default).			
	in Indexed mode when Section 26 Bit-Oriente Literal Off	Literal Offset never f ≤ 95 (5 5.2.3 "Byte-Or ed Instruction set Mode" for register f	Addressing iFh). See riented and ns in Indexed details.		If 'a' is '0' a set is enab in Indexed mode wher Section 26 Bit-Oriente Literal Offs	nd the extend led, this instru Literal Offset J never f \leq 95 (5 .2.3 "Byte-Or ed Instruction set Mode" for	ed instruction ction operates Addressing Fh). See riented and in Indexed details.	
Words:	1				→ C	→ registe	er f 🔶	
Cycles:	1							
Q Cycle Activity:				words:	1			
Q1	Q2	Q3	Q4		1			
Decode	Read register 'f'	Process Data	Write to destination	Q Cycle Activity:	Q2	Q3	Q4	
	i oglotor i	2 414	dootmation	Decode	Read	Process	Write to	
Example:	RLNCF	REG, 1,	0		register 'f'	Data	destination	
Before Instruction REG = 1010 1011 After Instruction REG = 0101 0111		Example: Before Instruct REG C After Instructi	RRCF ction = 1110 (= 0 on = 1110 (REG, 0,	0			
				W C	= 011100 = 0)011		

SUBWFB Subtract W from f with Borrow				
Syntax:	SL	JBWFB	f {,d {,a}}	
Operands:	0 ≤	≤ f ≤ 255		
	d e	≡ [0,1] - [0,1]		
Operation:	a e (f)	= [0,1] _ (\\/)	$(\overline{C}) \rightarrow dest$	
Status Affected:	(I) N		$(C) \rightarrow uesi$	
Encoding:	IN,	0101	10do ff	f fff
Description:		btract W	and the Carry	flag (borrow)
Description.	fro	m regist	er 'f' (2's comp	lement
	me	ethod). If	'd' is '0', the re	sult is stored
	in \ in I	W. If 'd' i register '	s '1', the result f' (default).	is stored back
	lf 'a	a' is '0', f	the Access Bar	nk is selected.
	lf 'a GF	a' is '1', t PR bank	he BSR is use (default).	d to select the
	lf 'a	a' is '0' a	ind the extende	ed instruction
	se in	t is enab Indexed	Literal Offset A	ddressing
	mc	de wher	hever $f \le 95$ (5F	Fh). See
	Se	ction 26	.2.3 "Byte-Ori	ented and
	Bit	eral Off	ed Instruction set Mode" for	s in Indexed
Words:	1			dotano.
Cycles:	1			
Q Cycle Activity:				
Q1		Q2	Q3	Q4
Decode	F	Read	Process	Write to
	reg	jister 'f'	Data	destination
Example 1:		UBWFB	REG, 1, 0	
Before Instruc REG	tion =	19h	(0001 10	01)
W	=	0Dh	(0000 11	01)
After Instructio	= on	1		
REG	=	0Ch	(0000 10	11)
W C	=	0Dh 1	(0000 11	01)
Z	=	0	, requit is n	
IN Example 2:	=			USILIVE
Before Instruc	tion	JODWID	NHO, 0, 0	
REG	=	1Bh	(0001 10	11)
W C	=	1Ah 0	(0001 10)	10)
After Instruction	on	-		
REG	=	1Bh 00b	(0001 10	11)
Č	=	1		
Z N	=	1 0	; result is ze	ero
Example 3:	S	UBWFB	REG, 1, 0	
Before Instruc	ction			
REG	=	03h	(0000 00)	11)
C	=	0En 1	(0000 11	UI)
After Instruction	on			
REG	=	⊦5h	(1111 01 ; [2's com p	υυ) Ι
W	=	0Eh	(0000 11	01)
Z	=	0		
N	=	1	; result is n	egative

SWAPF	Swap f				
Syntax:	SWAPF f	{,d {,a}}			
Operands:	$0 \leq f \leq 255$				
	d ∈ [0,1] a ∈ [0,1]				
Operation:	(f<3:0>) → (f<7:4>) →	dest<7:4>, dest<3:0>			
Status Affected:	None				
Encoding:	0011	10da ff:	ff ffff		
Description:	The upper and lower nibbles of register 'f' are exchanged. If 'd' is '0', the result is placed in W. If 'd' is '1', the result is placed in register 'f' (default).				
If 'a' is '0', the Access Bank is sele If 'a' is '1', the BSR is used to sele GPR bank (default).					
If 'a' is '0' and the extended instru- set is enabled, this instruction op- in Indexed Literal Offset Addressi mode whenever f ≤ 95 (5Fh). See Section 26.2.3 "Byte-Oriented a Bit-Oriented Instructions in Ind Literal Offset Mode" for details					
Words:	1				
Cycles:	1				
Q Cycle Activity:					
Q1	Q2	Q3	Q4		
Decode	Read register 'f'	Process Data	Write to destination		
Example: SWAPF REG, 1, 0 Before Instruction REG = 53h After Instruction					
REG	= 3011				



TABLE 28-18: EXAMPLE SPI MODE REQUIREMENTS (SLAVE MODE TIMING, CKE = 0)

Param No.	Symbol	Characteristic		Min	Max	Units	Conditions
70	TssL2scH, TssL2scL	$\overline{SSx} \downarrow$ to SCKx \downarrow or SCKx \uparrow Input		3 Тсү		ns	
71	TscH	SCKx Input High Time	Continuous	1.25 Tcy + 30	—	ns	
71A		(Slave mode)	Single Byte	40		ns	(Note 1)
72	TscL	SCKx Input Low Time	Continuous	1.25 Tcy + 30	—	ns	
72A		(Slave mode)	Single Byte	40	—	ns	(Note 1)
73	TDIV2scH, TDIV2scL	Setup Time of SDIx Data Input to SCKx	Edge	20		ns	
73A	Тв2в	Last Clock Edge of Byte 1 to the First Cloc	ck Edge of Byte 2	1.5 Tcy + 40	—	ns	(Note 2)
74	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx E	Edge	40		ns	
75	TDOR	SDOx Data Output Rise Time	PIC18FXXXX	—	25	ns	
			PIC18LFXXXX	—	45	ns	VDD = 2.0V
76	TDOF	SDOx Data Output Fall Time		_	25	ns	
77	TssH2doZ	SSx ↑ to SDOx Output High-Impedance)	10	50	ns	
78	TscR	SCKx Output Rise Time (Master mode)	PIC18FXXXX	—	25	ns	
			PIC18LFXXXX	—	45	ns	VDD = 2.0V
79	TscF	SCKx Output Fall Time (Master mode)		—	25	ns	
80	TscH2doV,	SDOx Data Output Valid after SCKx	PIC18FXXXX	—	50	ns	
	TscL2doV	Edge	PIC18LFXXXX	—	100	ns	VDD = 2.0V
83	TscH2ssH, TscL2ssH	SSx ↑ after SCKx Edge		1.5 TCY + 40		ns	

Note 1: Requires the use of Parameter #73A.

2: Only if Parameter #71A and #72A are used.

APPENDIX C: CONVERSION CONSIDERATIONS

This appendix discusses the considerations for converting from previous versions of a device to the ones listed in this data sheet. Typically, these changes are due to the differences in the process technology used. An example of this type of conversion is from a PIC16C74A to a PIC16C74B.

Not Applicable

APPENDIX D: MIGRATION FROM BASELINE TO ENHANCED DEVICES

This section discusses how to migrate from a Baseline device (i.e., PIC16C5X) to an Enhanced MCU device (i.e., PIC18FXXX).

The following are the list of modifications over the PIC16C5X microcontroller family:

Not Currently Available

0	-	-	
_	0	0	r
	•	۰.	L

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Timi	TMR4 Register TMR4 to PR4 Match Interrupt ing Diagrams A/D Conversion Asynchronous Reception Asynchronous Transmission (Back to Back) . Automatic Baud Rate Calculation Auto-Wake-up Bit (WUE) During Normal Operation	177,	177 177 178 416 261 258 258 256 262
Timi	TMR4 Register TMR4 to PR4 Match Interrupt ing Diagrams A/D Conversion Asynchronous Reception Asynchronous Transmission (Back to Back) . Aynchronous Transmission (Back to Back) . Automatic Baud Rate Calculation Auto-Wake-up Bit (WUE) During Normal Operation Auto-Wake-up Bit (WUE) During Sleep	177,	177 177 178 416 261 258 258 258 256 262 262
Timi	TMR4 Register TMR4 to PR4 Match Interrupt ing Diagrams A/D Conversion Asynchronous Reception Asynchronous Transmission (Back to Back) . Asynchronous Transmission (Back to Back) . Automatic Baud Rate Calculation Auto-Wake-up Bit (WUE) During Normal Operation Auto-Wake-up Bit (WUE) During Sleep Baud Rate Generator with Clock Arbitration	177,	177 177 178 416 261 258 258 258 256 262 262 262 233
Timi	TMR4 Register TMR4 Register TMR4 to PR4 Match Interrupt A/D Conversion Asynchronous Reception Asynchronous Transmission Asynchronous Transmission (Back to Back) . Automatic Baud Rate Calculation Auto-Wake-up Bit (WUE) During Normal Operation Auto-Wake-up Bit (WUE) During Sleep Normal Operation Baud Rate Generator with Clock Arbitration . BRG Overflow Sequence	177,	177 177 178 416 261 258 258 256 262 262 233 256
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Timi	TMR4 Register TMR4 to PR4 Match Interrupt ing Diagrams A/D Conversion Asynchronous Reception Asynchronous Transmission (Back to Back) . Asynchronous Transmission (Back to Back) . Automatic Baud Rate Calculation Auto-Wake-up Bit (WUE) During Normal Operation Auto-Wake-up Bit (WUE) During Sleep Baud Rate Generator with Clock Arbitration BRG Overflow Sequence BRG Reset Due to SDAx Arbitration	177,	177 177 178 261 258 258 256 262 262 233 256
Timi	TMR4 Register TMR4 to PR4 Match Interrupt ing Diagrams A/D Conversion Asynchronous Reception Asynchronous Transmission (Back to Back) . Asynchronous Transmission (Back to Back) . Automatic Baud Rate Calculation Auto-Wake-up Bit (WUE) During Normal Operation Auto-Wake-up Bit (WUE) During Sleep Baud Rate Generator with Clock Arbitration BRG Overflow Sequence BRG Reset Due to SDAx Arbitration During Start Condition	177,	1777 1778 416 261 258 258 256 262 262 233 256 242 242
Timi	TMR4 Register TMR4 to PR4 Match Interrupt A/D Conversion Asynchronous Reception Asynchronous Transmission Asynchronous Transmission (Back to Back) . Automatic Baud Rate Calculation Auto-Wake-up Bit (WUE) During Normal Operation Auto-Wake-up Bit (WUE) During Sleep Normal Operation Baud Rate Generator with Clock Arbitration BRG Overflow Sequence BRG Reset Due to SDAx Arbitration During Start Condition Brown-out Reset (BOR)		1777 1778 416 261 258 258 256 262 262 233 256 242 403
Timi	TMR4 Register TMR4 to PR4 Match Interrupt ing Diagrams A/D Conversion Asynchronous Reception Asynchronous Transmission (Back to Back) . Asynchronous Transmission (Back to Back) . Automatic Baud Rate Calculation Auto-Wake-up Bit (WUE) During Normal Operation Auto-Wake-up Bit (WUE) During Sleep Baud Rate Generator with Clock Arbitration BRG Overflow Sequence BRG Reset Due to SDAx Arbitration During Start Condition Brown-out Reset (BOR) Bus Collision During a Repeated Start	177,	177 177 178 416 261 258 258 258 258 262 262 233 256 242 403
Timi	TMR4 Register TMR4 Register TMR4 to PR4 Match Interrupt ing Diagrams A/D Conversion Asynchronous Reception Asynchronous Transmission Asynchronous Transmission (Back to Back) Automatic Baud Rate Calculation Auto-Wake-up Bit (WUE) During Normal Operation Auto-Wake-up Bit (WUE) During Sleep Baud Rate Generator with Clock Arbitration BRG Overflow Sequence BRG Reset Due to SDAx Arbitration During Start Condition Brown-out Reset (BOR) Bus Collision During a Repeated Start Condition (Case 1)	177,	177 177 178 416 261 258 258 258 258 258 258 258 258 258 258
Timi	TMR4 Register TMR4 to PR4 Match Interrupt ng Diagrams A/D Conversion Asynchronous Reception Asynchronous Transmission (Back to Back) . Asynchronous Transmission (Back to Back) . Automatic Baud Rate Calculation Auto-Wake-up Bit (WUE) During Normal Operation Auto-Wake-up Bit (WUE) During Sleep Baud Rate Generator with Clock Arbitration BRG Overflow Sequence BRG Reset Due to SDAx Arbitration During Start Condition Bus Collision During a Repeated Start Condition (Case 1)		177 177 416 261 258 258 256 262 233 256 242 403 242
Timi	TMR4 Register TMR4 to PR4 Match Interrupt A/D Conversion Asynchronous Reception Asynchronous Transmission Asynchronous Transmission (Back to Back) . Asynchronous Transmission (Back to Back) . Automatic Baud Rate Calculation Auto-Wake-up Bit (WUE) During Normal Operation Auto-Wake-up Bit (WUE) During Sleep Normal Operation Auto-Wake-up Bit (WUE) During Sleep Baud Rate Generator with Clock Arbitration BRG Overflow Sequence BRG Reset Due to SDAx Arbitration During Start Condition Brown-out Reset (BOR) Bus Collision During a Repeated Start Condition (Case 1) Bus Collision During a Repeated Start		177 177 178 261 258 258 256 262 233 256 242 403 242
Timi	TMR4 Register TMR4 Register TMR4 to PR4 Match Interrupt A/D Conversion Asynchronous Reception Asynchronous Transmission Asynchronous Transmission (Back to Back) . Automatic Baud Rate Calculation Auto-Wake-up Bit (WUE) During Normal Operation Auto-Wake-up Bit (WUE) During Sleep Baud Rate Generator with Clock Arbitration . BRG Overflow Sequence BRG Reset Due to SDAx Arbitration During Start Condition Brown-out Reset (BOR) Bus Collision During a Repeated Start Condition (Case 1) Bus Collision During a Repeated Start Condition (Case 2)	177,	1777 1778 4166 261 2588 2568 262 262 233 2566 2422 403 2423 2433 243
Timi	 TMR4 Register TMR4 to PR4 Match Interrupt Ing Diagrams A/D Conversion Asynchronous Reception Asynchronous Transmission (Back to Back) Asynchronous Transmission (Back to Back) Automatic Baud Rate Calculation Auto-Wake-up Bit (WUE) During Normal Operation Auto-Wake-up Bit (WUE) During Sleep Baud Rate Generator with Clock Arbitration BRG Overflow Sequence BRG Reset Due to SDAx Arbitration During Start Condition Brown-out Reset (BOR) Bus Collision During a Repeated Start Condition (Case 1) Bus Collision During a Repeated Start Condition (Case 2) 	177,	177 177 178 261 258 258 256 262 233 256 262 233 256 242 403 243
Timi	 TMR4 Register TMR4 to PR4 Match Interrupt mg Diagrams A/D Conversion Asynchronous Reception Asynchronous Transmission Asynchronous Transmission (Back to Back) Automatic Baud Rate Calculation Auto-Wake-up Bit (WUE) During Normal Operation Auto-Wake-up Bit (WUE) During Sleep Baud Rate Generator with Clock Arbitration BRG Overflow Sequence BRG Reset Due to SDAx Arbitration During Start Condition Brown-out Reset (BOR) Bus Collision During a Repeated Start Condition (Case 2) Bus Collision During a Start Ocondition Column (Column 20) 		177 177 178 416 261 258 258 258 258 262 262 233 256 242 403 243 243
Timi	 TMR4 Register TMR4 to PR4 Match Interrupt mg Diagrams A/D Conversion Asynchronous Reception Asynchronous Transmission Asynchronous Transmission (Back to Back) Automatic Baud Rate Calculation Auto-Wake-up Bit (WUE) During Normal Operation Auto-Wake-up Bit (WUE) During Sleep Baud Rate Generator with Clock Arbitration BRG Overflow Sequence BRG Reset Due to SDAx Arbitration During Start Condition Brown-out Reset (BOR) Bus Collision During a Repeated Start Condition (Case 1) Bus Collision During a Start Condition During a Start Condition (SCLx = 0) 		177 177 178 416 261 258 258 258 262 262 233 256 242 403 243 243 243
Timi	TMR4 Register	177,	177 177 178 416 261 258 258 256 262 233 256 242 403 243 243 243 243
Timi	 TMR4 Register TMR4 Register TMR4 to PR4 Match Interrupt Ing Diagrams A/D Conversion Asynchronous Reception Asynchronous Transmission (Back to Back) Automatic Baud Rate Calculation Auto-Wake-up Bit (WUE) During Normal Operation Auto-Wake-up Bit (WUE) During Sleep Baud Rate Generator with Clock Arbitration BRG Overflow Sequence BRG Reset Due to SDAx Arbitration During Start Condition Brown-out Reset (BOR) Bus Collision During a Repeated Start Condition (Case 1) Bus Collision During a Start Condition (SCLx = 0) Bus Collision During a Stop Condition (Case 1) 		177 177 178 416 261 258 258 256 262 233 256 242 403 243 243 243 243 242 242
Timi	 TMR4 Register TMR4 to PR4 Match Interrupt mg Diagrams A/D Conversion Asynchronous Reception Asynchronous Transmission Asynchronous Transmission (Back to Back) Automatic Baud Rate Calculation Auto-Wake-up Bit (WUE) During Normal Operation Auto-Wake-up Bit (WUE) During Sleep Baud Rate Generator with Clock Arbitration BRG Overflow Sequence BRG Reset Due to SDAx Arbitration During Start Condition Brown-out Reset (BOR) Bus Collision During a Repeated Start Condition (Case 1) Bus Collision During a Start Condition (SCLx = 0) Bus Collision During a Stop Condition (Case 1) 		177 177 416 261 258 258 256 262 233 256 242 403 243 243 243 243 243
Timi	 TMR4 Register TMR4 to PR4 Match Interrupt mg Diagrams A/D Conversion Asynchronous Reception Asynchronous Transmission Asynchronous Transmission (Back to Back) Automatic Baud Rate Calculation Auto-Wake-up Bit (WUE) During Normal Operation Auto-Wake-up Bit (WUE) During Sleep Baud Rate Generator with Clock Arbitration BRG Overflow Sequence BRG Reset Due to SDAx Arbitration During Start Condition Brown-out Reset (BOR) Bus Collision During a Repeated Start Condition (Case 1) Bus Collision During a Start Condition (SCLx = 0) Bus Collision During a Stop Condition (Case 1) Bus Collision During a Stop Condition Uring a Stop 		1777 1778 4166 261 2588 2588 2566 2622 2333 2566 2422 403 2432 2433 2433 2432 2433